From Defect Analysis to Gate-Level Fault Modeling of Controllable-Polarity Silicon Nanowires

Hassan Ghasemzadeh Mohammadi, Pierre-Emmanuel Gaillardon, *Member, IEEE*, and Giovanni De Micheli, *Fellow, IEEE*

***Abstract*—*Controllable-polarity silicon nanowire transistors* (CP-SiNWFETs) are among the promising candidates to complement or even replace the current CMOS technology in the near future. Polarity control is a desirable property that allows the online configuration of the device polarity. CP-SiNWFETs result in smaller and faster logic gates unachievable with conventional CMOS implementations. From a circuit testing point of view, it is unclear if the current CMOS and FinFET fault models are comprehensive enough to model all the defects of CP-SiNWFETs. In this paper, we explore the possible manufacturing defects of this technology through analyzing the fabrication steps and the layout structure of logic gates. Using the obtained defects, we then evaluate their impacts on the performance and the functionality of CP-SiNWFET logic gates. Out of the results, we extend the current fault model to a new a hybrid model, including stuck at p-type and stuck-at n-type, which can be efficiently used to test the logic circuits in this technology. The newly introduced fault model can be utilized to adequately capture the malfunction behavior of CP logic gates in the presence of nanowire break, bridge, and float defects. Moreover, the simulations revealed that the current CMOS test methods are insufficient to cover all faults, i.e., stuck-Open. We proposed an appropriate test method to capture such faults as well.**

***Index Terms*—Controllable-polarity silicon nanowires, defect, fault model, gate oxide short, nanotechnology.**

I. Introduction

THE continued feature-size scaling trend for extending Moore's law has been faced with the significant challenges of short-channel effect and leakage power. To discover possibilities for further performance and functionality, an important research effort has been devoted to innovative device structures. FinFET [1] and FDSOI [2] transistors are successfully replacing bulk CMOS transistors beyond the 22-nm technology node. Following the trend towards one-dimensional structures, *Silicon nanowires* (SiNWs) with *gate-all-around* structures [3] provide an even better electrostatic control over the channel and reduce leakage current.

Beyond 45 nm, many devices exhibit Schottky characteristic at source and drain contacts such as SiNWs [4], carbon nanotubes [5], and graphene [6]. These devices have ambipolar behavior, i.e., they support the flow of both n-type and p-type carriers. While ambipolarity is usually suppressed by fabrication process to provide unipolar devices [7], it can be used to enhance the logic functionality, i.e., the capability of implementing more complex functions using smaller number of transistors [8]. *Controllable-polarity silicon nanowire FETs* (CP-SiNWFETs), such as *double-gate* (DG) [9] and *Three-independent-gate* (TIG) [10] are among the fabricated examples of *controllable-polarity* (CP) devices. These devices have been successfully used for the fabrication of CP logic gates that provide compact hardware realization with remarkable circuit design flexibility.

To reveal fabrication defects and circuits malfunctioning, a number of structural fault models for planar single-gate CMOS and FinFET technologies have been proposed and proved to be efficient. For instance, stuck-at [11], delay [12], stuck-Open [13], and bridging fault [14] are among the most commonly-used models for CMOS technology. For FinFETs, a few number of studies have been conducted in modeling defects such as floating gates and shorts [15], [16], stuck-Open/stuck-On [17], [18], and *gate oxide short* (GOS) [19]. These studies revealed the deficiency of current CMOS fault models for detecting all the defects in FinFET circuits, and required the introduction of new fault models for test generation purpose.

In this paper, we perform an inductive fault analysis to investigate the specific malfunctions of CP-SiNWFETs. We used *three-independent-gate silicon nanowire FETs* (TIG-SiNWFETs), which have been fabricated and reported as potential candidates for CP devices. A preliminary version of this study appeared in [20]. For a new technology such as CP-SiNWFET, which has different geometrical structure and physics of operation rather than CMOS technology, it is not *a priori* known that how the manufacturing defects will impact the device and logic circuits. Considering the technology process, the possible defects that can change the functionality of the CP-SiNWFETs and occur during fabrication process are modeled. Using the obtained defect model, we investigate the functionality and the performance of various logic gates in the presence of defects. Out of the obtained results for CP-SiNWFET technology, we extend the current CMOS fault model that contains stuck-at p-type and n-type. The results also confirm that the inefficiency of the traditional test methods for covering the defects, such as Open defects on polarity terminals of the device, in CP-SiNWFET technology.

The remainder of the paper is organized as follows. The background on fault modeling is presented in Section II. In Section III, the CP devices are briefly reviewed and the

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The authors are with the Integrated Systems Laboratory, Ecole Polytechnique Federale de Lausanne, Lausanne 1015, Switzerland (e-mail: hassan.ghasemzadeh@epfl.ch; pierre-emmanuel.gaillardon@epfl.ch; giovanni.demicheli@epfl.ch).

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structure of logic gates designed in this technology are detailed by introducing the static/dynamic polarity concept. The detail of the defect modeling for CP-SiNWFETs is demonstrated in Section IV. The fault modeling for CP logic gates is investigated in Section V and the paper is concluded in Section VI.

II. Background and Motivation

Moving towards nano-scaled technologies, process variation negatively affects the driving current of transistors and consequently results in delay faults. Moreover, undetected design rules violations increase the chance of bridge faults as unintended resistive connections between two or more conductive parts. Bridge faults could be efficiently diagnosed by supply current monitoring through IDDQ test [21] for bulk planar CMOS, but the test is becoming less effective for the deeply nanoscaled technologies [22]. *Line edge roughness* (LER) is an inevitable limitation of etching process and leads to non-homogeneous deposition of dielectrics when the dielectric thickness goes beyond 5 nm. This may result into the GOS [23]. Last but not least, twin boundaries during forming the nanowires may strongly influence the *On* current of the device that finally causes to channel break [24], [25].

Proper fault modeling for testing manufacturing defects plays a significant role for quality of circuits and their correct functionality. Currently, few researches have been carried out on fault modeling of the FinFET. Simsir *et al.*, in [15] and [16] investigated open and short faults on FinFETs, and they showed that *stuck-Open faults* (SOFs) on the back gate of FinFET have a unique effect on the leakage and delay. In [19], the GOS defect on the FinFET dielectric has been studied. The amount of *saturation drain current* ($I_{D(SAT)}$) vastly increases with GOS at the front gate dielectric. However, GOS occurrence in the back-gate dielectric causes much lower carrier density in the device channel. The SOF, Stuck-On and GOS on different number of Fins in a FinFET have been examined by Liu and Xu [17] and Harutyunyan *et al.* [18]. The results manifested that when the number of faults is large enough, the defect can be captured by SOF or delay fault tests. Champac *et al.* [13] presented the problem of SOF detection for small nanometer technologies. They proposed a new multiple test vector mechanism to enhance the probability of SOF detection.

While stuck-at, SOF, bridge, and delay faults efficiently model the defects in CMOS, FinFET, and CNT devices, the particular structure of devices with CP necessitates further study to see whether these fault models can properly capture the manufacturing defects. There is no available comprehensive fault model for circuits designed with these devices. In the following, we analyze the possible manufacturing defects of CP transistors, and then investigate their impact of the functionality of the various types of CP logic gates.

III. CP: From Device to Logic Gates

In this section, we describe the transistors with CP. We present the realization of the logic gates in this technology and discuss how CP devices help the compact implementation of logic gates. We briefly review the main steps of manufacturing process which is necessary for our defect modeling.

A. Transistors With CP

Ambipolar conduction of the nanoscaled devices can be controlled by adjusting the device polarity online. Such transistors with CP have been successfully implemented in SiNWs [9], [10], carbon nanotube [26], graphene [27], and FinFET [28]. In such transistors, one electrode gate, the *control gate* (CG), works like conventional MOSFETS, and provides the conduction by controlling potential barriers. At least one another electrode gate, the *polarity gate* (PG), is needed to control the n-type or p-type characteristics of the device. Indeed, the type of carriers that flow in the device channel is adjustable through the applied voltage on PG.

Among various technologies of CP transistors, SiNWs have a CMOS compatible fabrication process. Different architectures have been proposed for their implementations [9], [10], [29], [30]. As an example, Fig. 1 represents a TIG-SiNWFET with a CG and two PGs (PG_S and PG_D). Here, the side regions (PG_S and PG_D) determine the majority (MAJ) carriers through adjusting the Schottky barrier height at the source/drain junctions. Thus, the device can exhibit controllable n-type and p-type characteristics. DG-SiNWFETs [9] exploit a similar structure than TIG-SiNWFETs where the two PGs are connected together. Reconfigurable SiNW [29] is another example in which only one PG is utilized for configuration of transistor to desired polarity. In this paper, we use the TIG-SiNWFET as the target device. Nevertheless, the fault modeling for other CP devices can be obtained straightforward following the same methodology. Accordingly, without loss of generality, we provide our discussion based on this device.

B. Fabrication Process

As shown in [9], the TIG-SiNWFET devices are fabricated in a top-down approach. Table I summarizes the fabrications process of the device along with the outcome of each step. The Bosch etching process [31] is utilized to form the nanowire stack. An high-κ gate dielectric is then deposited over each patterned nanowire and provides a thin oxide layer (≤ 5 nm) around the channel. Oxidation process is followed by a conformal metal deposition to shape the PGs around the nanowires. Finally, the CG structure is self-aligned to PGs. Thus, a three-gate device is obtained in which PGs are electrically isolated by the controlled deposition of the gate oxide.

C. Logic Gate Realization of CP Circuits

The CP transistors as configurable structures can be efficiently utilized to implement logic gates. The polarity terminals are used to select the device polarity. According to the different configuration of PGs, the CP logic gates are divided into two categories.

The first group, called *static polarity* (SP), is characterized by the PG gates directly connected to either power supply (V_{dd}) or ground (GND) rails to provide the desired polarity. In SP logic

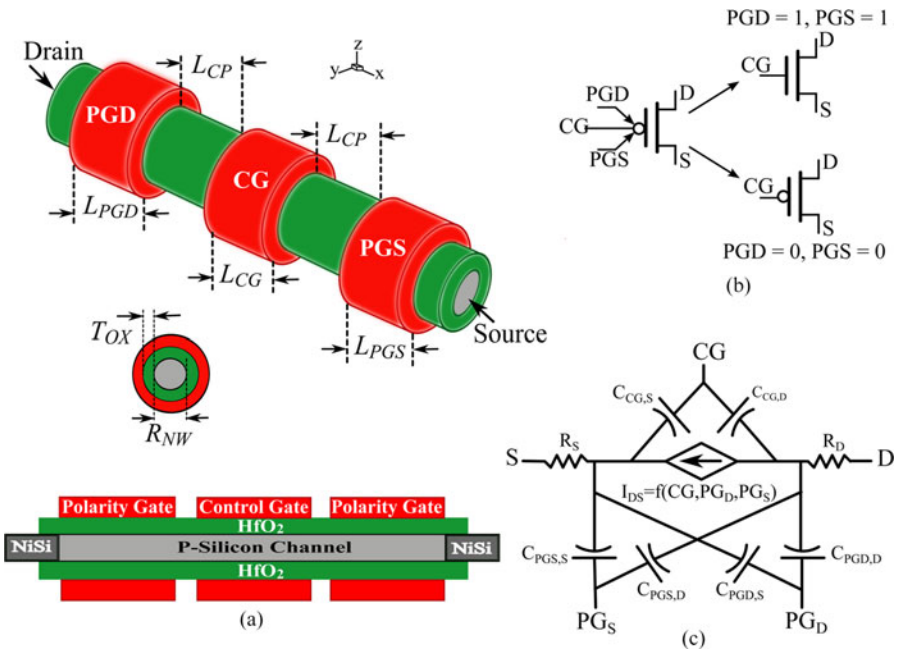

Fig. 1. TIG-SiNWFET. (a) The 3-D structure as used for TCAD simulation, (b) TIG-SiNWFET circuit symbol, and (c) the lumped model of the device.

TABLE I
TIG-SiNWFET FABRICATION PROCESS STEPS AND RELATED DEFECT MODEL

TIG-SiNWFET fabrication process		
Process	Outcome	Possible defects
(1) HSQ-based nanowire patterning	Initial pattern of nanowires	Nanowire break
(2) Bosch process	Nanowire formation	Nanowire break
(3) Oxide deposition	Dielectric formation	GOS
(4) Metal-gate stack deposition	Polarity and control gates	Bridge between two or more terminals
(5) Metal layer(s) deposition	Interconnections	Bridge among interconnects, Floating gates

gates, the polarity of all devices remains the same during the whole device life-time. Fig. 2(a) illustrates the three examples of SP logic gates (INV, NAND, and NOR gates) realized in TIG-SiNWFET technology.

The second group, called *dynamic polarity* (DP), consists of logic gates in which the PGs are treated as an extra logic variable. Indeed, the polarity of transistors is dynamically configured by a logic signal during the logic gate operation. Since the conductivity of CP transistors can be controlled by control and PGs, this property provides more flexibility for compact realization of binate logic gates. The conductivity of a CP transistor is possible when CG, PG_s, and PG_d have the same values ($'1'$ for the n-type and $'0'$ for the p-type as shown in Fig. 2). Similarly the transistor has no conductivity when $CG \oplus (PG_S \cdot PG_D) = 1$. This property notifies the intrinsic XOR characteristics of the CP transistors, which has been used for the compact realization of the binate logics such as XOR gate [8]. Fig. 2(b) represents the implementation of three DP logic gates (XOR, XOR-3, and MAJ) in TIG-SiNWFET technology. The complementary pull-up and pull-down with parallel transistors leads to static full-swing logic gates and prevents threshold drops in the output.

D. Simulation Setup

In order to first model the possible defects of this technology, and then to investigate their impact on the performance and the functionality of logic gates, we need to setup a simulation framework that brings together device and circuit simulators. Consequently, a two-step simulation environment, that integrates the Sentaurus TCAD [32] and HSPICE [33] simulators into a single framework, is used to facilitate high-level simulations. First, we build a TCAD model of the TIG-SiNWFET, for which the *I–V* curves are calibrated with those of our fabricated devices. The typical parameters of the TIG-SiNWFET shown in the Fig. 1 are listed in Table II. The supply voltage used in the simulations is 1.2 V.

In the next phase, circuit level simulations are realized by a simple compact model in Verilog-A (see Fig. 1(c)). The result of the TCAD simulations from the previous step, makes a look-up table that characterizes the channel conductivity as a function of the V_{CG}, V_{PGS}, and V_{PGD}. Moreover, it provides the value of the parasitic capacitance among various terminals and the access resistance corresponding to the source and drain. This model is used in our simulations to efficiently implement the functional behavior of the TIG-SiNWFET.

IV. MANUFACTURING DEFECTS OF TIG-SiNWFETs: FROM DEVICE TO LOGIC CELLS

In this section, the possible defects of TIG-SiNWFETs are analyzed by considering major manufacturing steps. The defect model then is used for inductive fault analysis. We follow the

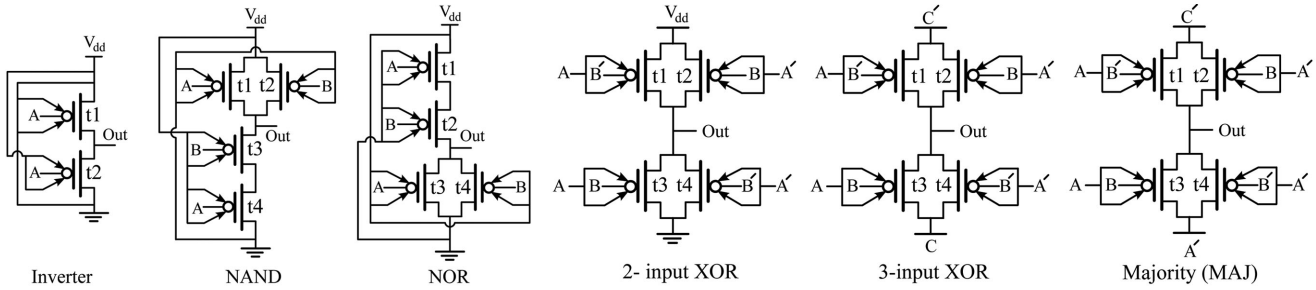

Fig. 2. Logic gate realization in TIG-SiNWFET. Inverter, NAND, and NOR gates are the examples of the SP logic gates. Accordingly, 2-input XOR, 3-input XOR and MAJ logic gates are those of DP logic structures.

TABLE II
TIG-SiNWFET STRUCTURAL AND PHYSICAL PARAMETERS

Device Parameter	Value
Length of CG (L_{CG})	22 nm
Length of PGs (L_{PGS}, L_{PGD})	22 nm
Length of Spacer (L_{CP})	18 nm
Channel Dopping Concentaration	10^{15} cm^{-3}
Schottky Barrier Height	0.41 eV
Oxide Thickness (T_{Ox})	5.1 nm
Radius of NanoWire (R_{NW})	7.5 nm

device fabrication process and consider the layout structure of logic cells to provide the opportunity of finding the most probable possible defects. This defect model helps us to find a realistic fault model for non-classical CMOS devices.

A. Device Manufacturing Defects

During the nanowire patterning and etching, variations along with LER contribute to lowering the pattern sharpness that may lead to nanowire break. The defect can drastically limit the driving current of the device or lead to a SOF. When the dielectric thickness is scaled beyond the 5 nm, the control for conformal oxide formation is reduced, and this eventually leads to poor insulator coverage. Consequently, GOS defects may happen. GOS may degrade the performance of the device or even malfunctioning according to the defect size. Finally, the similar mechanism may result in bridge defect between the CG and each adjacent PG. These are the most possible defects during TIG-SiNWFETs fabrication, which are also summarized in Table I.

B. Logic Cell Defects

Different sources of defects such as under/over polishing, poorly planarized surfaces, and scratches contribute to a combination of open and bridge defects in logic cells during polysilicon and metal deposition [34]. Open defects form floating regions that are very challenging for test in emerging technologies since they may affect either the performance or the functionality of logic cells. Bridge defects cause unwanted cell-internal connections between a logic cell input and the power rails (V_{dd}/GND) or any other adjacent inputs. Bridge defects similarly may have local impact (logic cell performance degradation) or global impact (deteriorate the functionality of several

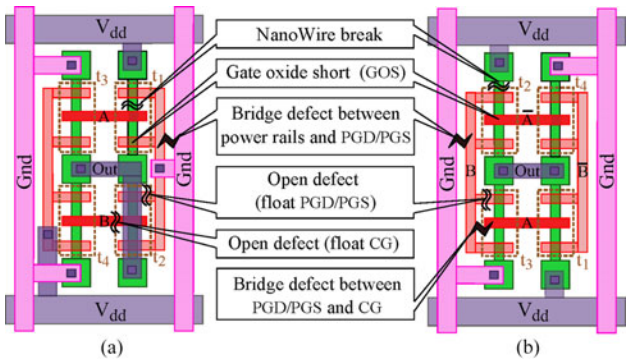

Fig. 3. Layouts of the NOR (a) and 2-input XOR (b) based on the SoT method [35], [36] with several possible defects.

logic cell) and become very challenging for emerging technologies. The bridge defects are extracted by considering the proximity of interconnects in the layout of the logic cells. The logic cell defects then are added to the device manufacturing defects to form our defect model for TIG-SiNWFET technology. Fig. 3 represents the layouts of two TIG-based logic cells ((a) NOR gate and (b) 2-input XOR) with some highlighted possible defects. Note that the presented layouts rely on the *sea-of-tile* (SoT) physical design methodology presented in [35] and [36].

V. FAULT-MODELING IN CP-SiNW CIRCUITS

In this section, we study the behavior of SP and DP TIG-SiNWFET logic gates in the presence of fabrication defects, discussed in the previous section.

A. GOS in CP-SiNWFETs

We report the effect of GOS occurrence in TIG-SiNWFETs. Then, we propose a new model for GOS which enables us to inject circuit level faults, and finally we study the effect of GOS on SP and DP dynamic logic circuits.

1) GOS in TIG-SiNWFETs: A GOS is a manufacturing defect happening in the oxide around the nanowire. The impact of a GOS mainly depends on its size. The defect may considerably decrease the impedance between the gate and the channel, and entirely change the electrical behavior of the transistor for a big enough GOS. For the TIG-SiNWFET, three gates (PG_S, CG, and PG_D) contribute to the functionality of the device. Therefore, three locations are possible for the GOS defect. The

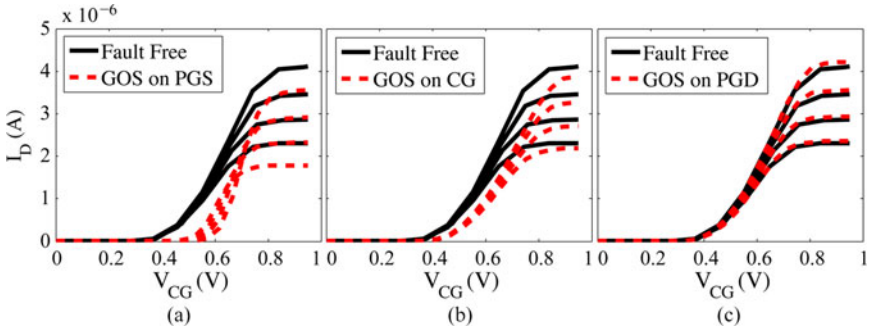

Fig. 4. Behavior of defective n-type TIG-SiNWFETs in the presence of GOS: (a) GOS under PG_S, (b) GOS under CG, and (c) GOS under PG_D.

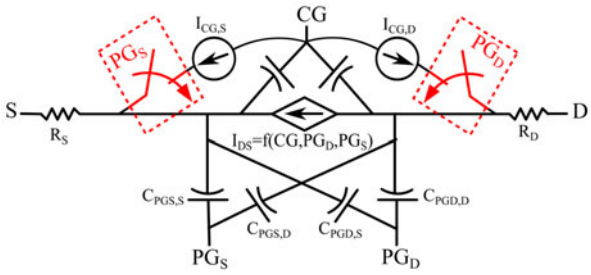

Fig. 5. Nonlinear piecewise model of GOS under CG for n-type TIG-SiNWFETs. The switches are necessary to realize the impact of the PGs on the leakage of defective device in DP logics.

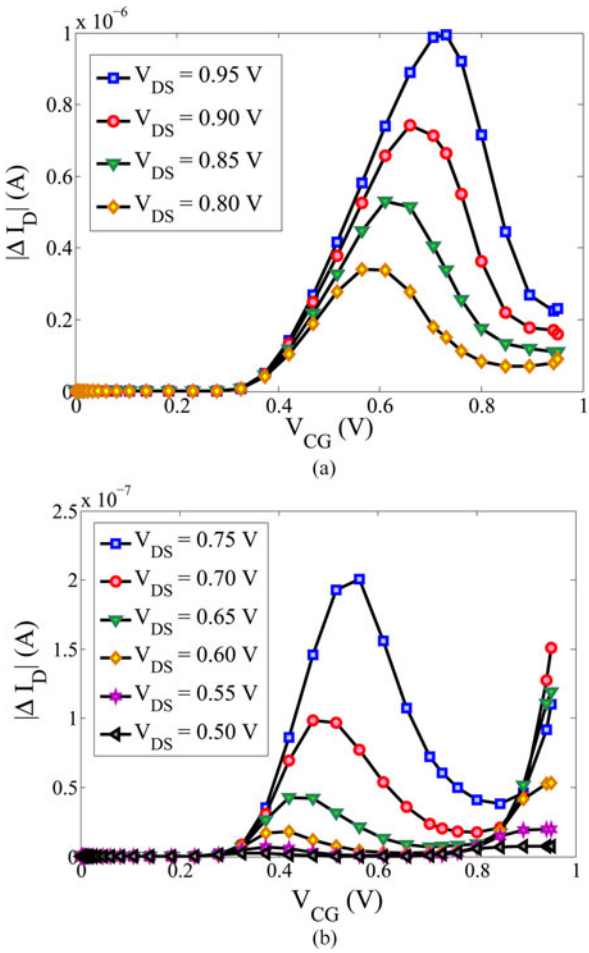

Fig. 6. Difference of I_D with and without GOS under CG versus V_{CG}. (a) Samples of $|\Delta I_D| - V_{CG}$ for $V_{DS} \geq 0.8$. The curves can be modeled by a degree-2 polynomial above the threshold. (b) Samples of $|\Delta I_D| - V_{CG}$ for $V_{DS} \leq 0.8$. The curves can be modeled by a degree-3 polynomial above the threshold.

defect injection on TCAD model of the device is accomplished through replacing a tiny cuboid (10 nm $\times$ 10 nm) of the dielectric layer with the channel material. Thus, a conductive path is created between the defective gate and the channel. The effects of GOS on the performance of the TIG-SiNWFETs are fully investigated in [20], and can be summarized as: 1) the parasitic current from the defective gate to the drain/source, which is proportional to the gate-drain/gate-source voltage; 2) the degradation of transistor driving current ($I_{D(SAT)}$) and the increase of *threshold voltage* (V_{Th}); 3) a sharp rise in the leakage current of the defective gate, which is proportional to the gate voltage. Fig. 4(a)–(c) depict the behavior of n-type TIG-SiNWFETs in the presence of GOS under PG_S, CG, and PG_D, respectively. Here, GOS occurrence in PG_S and CG results in a significant reduction of $I_{D(SAT)}$ similar to bulk CMOS. Moreover, the defect causes a weak inversion and tightens the channel for carriers, that leads to a slight increase of V_{Th} ($\Delta V_{Th} = 170$ mV and $\Delta V_{Th} = 140$ mV for defective PG_S and CG, respectively). However, GOS effect in PG_D is negligible (see Fig. 4(c)). In the following, we propose an equivalent lumped model for GOS defect.

2) GOS Modeling in TIG-SiNWFET: The proposed GOS model for TIG-SiNWFETs consists of two nonlinear piecewise *voltage controlled current sources* VCCSs (I_{GD}, and I_{GS}) that connect the faulty gate to the drain and source respectively (see Fig. 5). These VCCSs might be followed by extra switches that show the effect of other gates on the current flow. For example, the GOS in CG is modeled by two extra switches that are controlled by the PG_S and PG_D (red blocks of Fig. 5). These switches highlight that the leakage current between CG and source/drain depends on the PG voltages. Here, we explain how the model is extracted for a GOS in CG. The same procedure is then used for the modeling of the GOS in PG_S and PG_D, respectively.

In the proposed model, the variation of $I_{\rm DS}$ for a TIG-SiNWFET with and without GOS under CG is used to model the current loss (see Fig. 6). Here, $|\Delta(I_D)|$ represents the

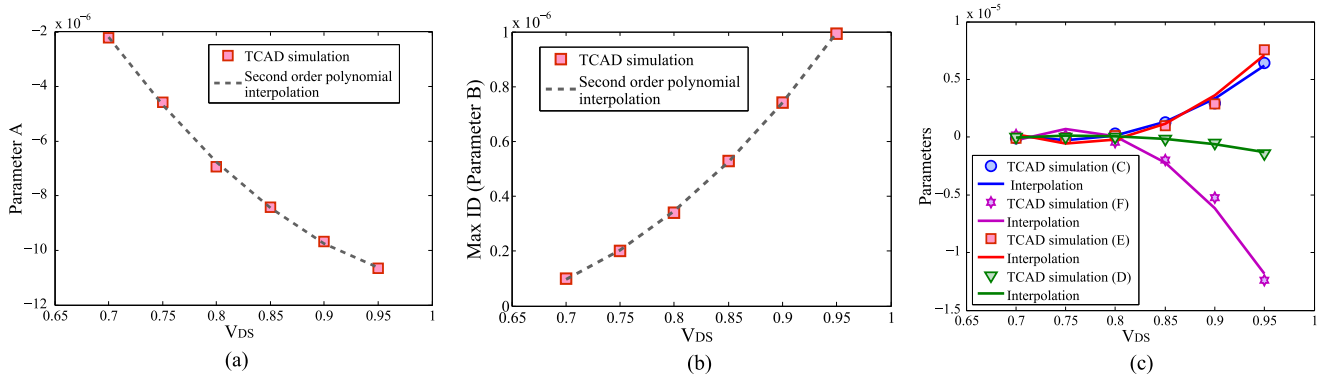

Fig. 7. Parameters of the GOS model estimator as a function of V_{DS}. All the parameters can be interpolated with second order polynomials. (a) Interpolation of parameter A as a function of V_{DS}. (b) Interpolation of parameter B as a function of V_{DS}. (c) Second order interpolation for parameters of the third order polynomial as a function of V_{DS}.

difference of $I_{\rm DS}$ for a faulty (GOS under CG) and non-faulty device, in which $I_{\rm DS}$ depends on both $V_{\rm CG}$ and $V_{\rm DS}$ values ($|\Delta(I_D)| = |I_{D\,(\text{faulty})} - I_{D\,(\text{non-faulty})}|$). In the proposed model, $|\Delta(I_D)|$ determines the amount of $I_{CG,D}$. For $V_{\rm DS} >= 0.80$ (see Fig. 6(a)), $|\Delta(I_D)|$ is $V_{\rm CG}$ controlled and we use a second-order polynomial of $V_{\rm CG}$ to represent $I_{CG,D}$ as shown in Eq. (1). For $V_{\rm DS} < 0.80$ (see Fig. 6(b)), $|\Delta(I_D)|$ shows a rapid increase when $V_{\rm CG}$ is approaching V_{dd}. This behavior is related to the negative $I_{D(sat)}$ when $V_{\rm DS}$ decreases. Thus, $|\Delta(I_D)|$ is modeled by a third-order polynomial of $V_{\rm CG}$ to represent $I_{CG,D}$ as shown in Eq. (1). In both cases, the impact of GOS on the current loss is above V_{Th}. For $V_{\rm CG} < V_{Th}$, $I_{CG,D}$ current is limited to the device leakage as well as the drain-to-gate leakage when V_{dd} is high. Therefore, the $I_{CG,D}$ is obtained by the following equation:

$$I_{CG,D} = \begin{cases} A(V_{\rm CG} - B)^2 & : V_{\rm DS} \geq 0.8 \\ C(V_{\rm CG})^3 + D(V_{\rm CG})^2 & : V_{\rm DS} < 0.8 \\ +E(V_{\rm CG}) + F & \end{cases} \quad (1)$$

where A, B, C, D, E, and F are the fitting parameters, which are all shown in Fig. 7. All the parameters in both equations are a function of $V_{\rm DS}$. Fig. 7(a)–(c) represents the relation of these parameters with $V_{\rm DS}$. All the parameters can be estimated by a second order polynomial of $V_{\rm DS}$ (the curves show the interpolation of the parameters with corresponding second order polynomial). The same procedure is utilized to find the $I_{\rm CG,S}$ model. We built this model in Verilog-A and we used it for circuit simulations.

3) GOS in SP and DP Logic Circuits: Here, we present a case study for circuit level GOS injection. We performed the circuit level GOS simulations for SP (INV) and DP (2-input XOR) logic gates. Here, the defect is injected under the CG gate. Fig. 8 represents the transient simulation of an inverter with a defect on the pull-down transistor. Note that we only depict the inverter response when its input changes from 0 to 1, since the faulty n-type transistor affects the inverter response more significantly during this transition. The result demonstrates a significant reduction of noise margin (NM_L). A similar experiment is done on the pull-down transistor (t4) of a 2-input XOR. The result is shown in Fig. 9. Here, the GOS-impacted defect result in degraded logic levels that can cause logic gate functionality failure during output low-to-high transition ($AB = (00 \rightarrow 01)$) and noise margin reduction during output high-to-low transition ($AB = (10 \rightarrow 11)$).

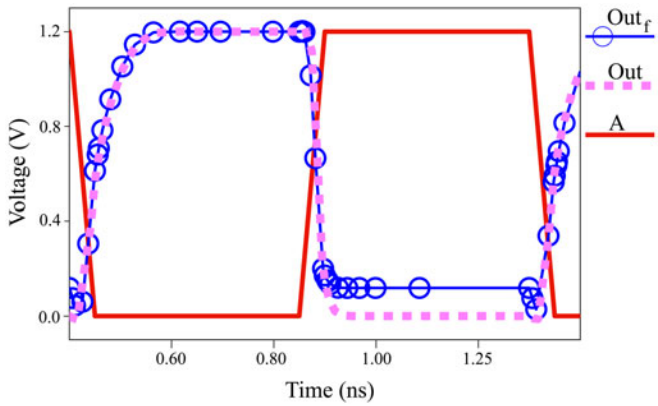

Fig. 8. GOS occurrence in CG of the pull-down transistor of an Inverter.

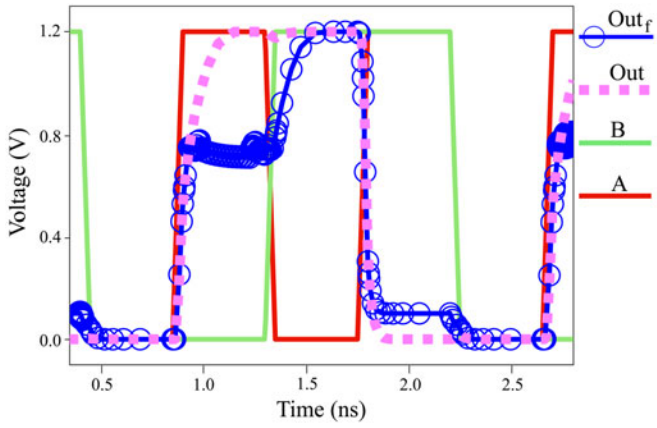

Fig. 9. GOS occurrence in CG of a pull-down transistor (t3) of an XOR.

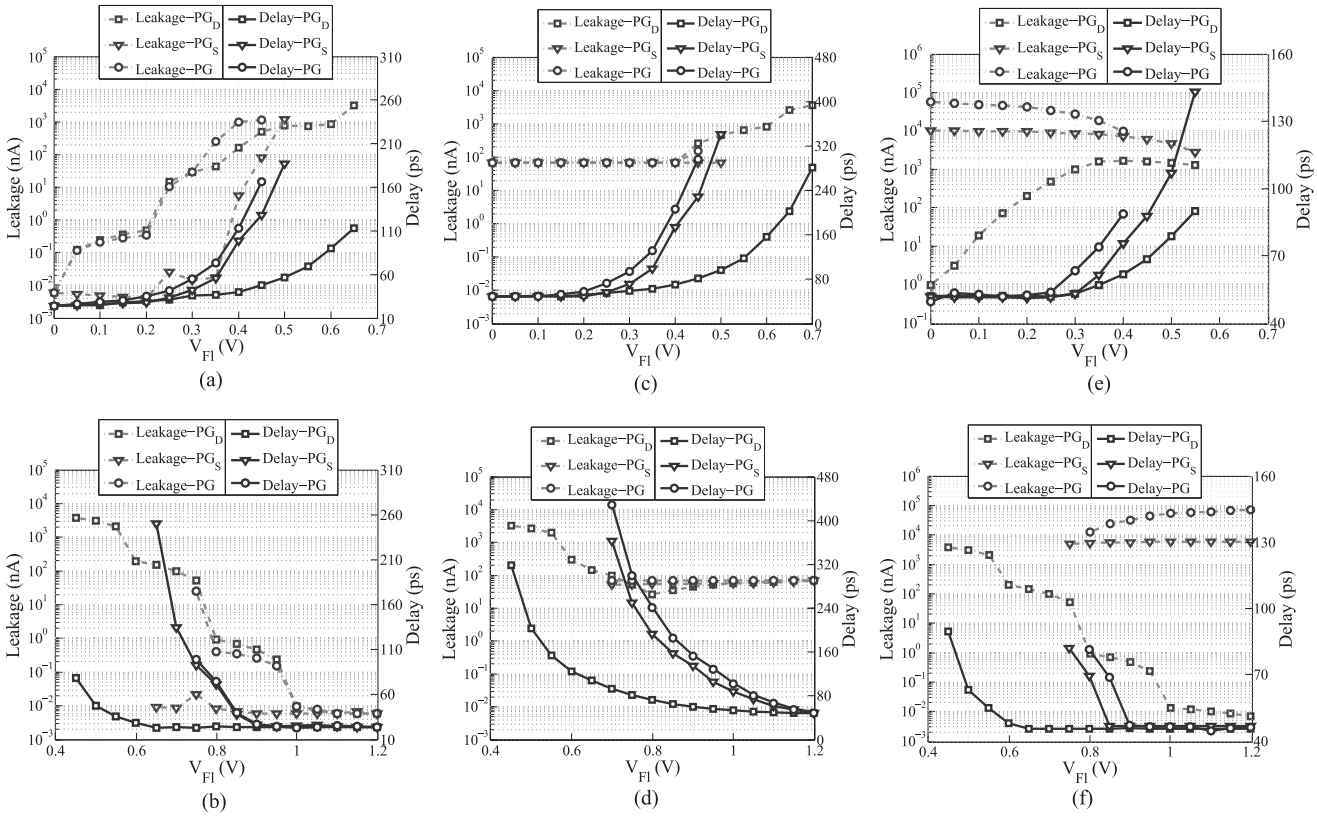

Fig. 10. Leakage-delay variation with different biases on PG_S and PG_D of the TIG-SiNWFET transistors in the SP and DP logic gates. (a) INV (transistor t1). (b) INV (transistor t3). (c) NAND (transistor t1). (d) NAND (transistor t3). (e) XOR (transistor t1). (f) XOR (transistor t3).

B. Open CGs and PGs on the SP and DP Logic Gates

In this section, we investigate the impact of open defects on the functionality and the performance of CP logic gates. When an open defect happens on a node, that should be treated as a floating node. According to the capacitances that couple to the float node, and transitions that occur across the coupling capacitances, the float node may acquire the intended original value, or vary dynamically. Due to the coupling effects, it is necessary to analyze the logic gates for a range of possible voltages which may be exhibited on the floating node. The voltage value for a float node, V_{Fl}, is varied from V_{Lo} to V_{Hi}. (V_{Lo}, V_{Hi}) is a subset of (GND, V_{dd}) in which the functionality of the logic gate under test is correct. We simulated SP (INV and NAND) and DP (2-input XOR, 3-input XOR, and MAJ) logic gates with open faults on the PGs of the pull-up and pull-down transistors. The defect-free PG biases are set to their nominal values (for SP logic gates $PG_S = PG_D = '0'$ and $PG_S = PG_D = '1'$ for pull-up and pull-down devices, respectively, and for the DP gates $PG_S = PG_D =$*appropriate input signals*).

Fig. 10(a) and (b) illustrates the leakage-delay variation with respect to V_{Fl} for the PGs of the pull-up and pull-down transistors in an inverter (INV) gate. Here, float on PG_D, float on PG_S, and float on both PGs are denoted by PG_D, PG_D, and PG_D, respectively. In Fig. 10(a), the delays of PG_D and PG_S stay relatively constant up to $V_{Fl} = 0.3$ V. When V_{Fl} further increases to $0.50\,V$, the delay of output low-to-high transition for float PG_S rises exponentially (7×). However, the delay of PG_D increases slightly, since PG_D plays a less important role in control of carrier concentrations. The leakage shows a drastical increase for both cases (5×). This is due to the fact that, here, the leakage is dominated by the p-type transistor. Finally, beyond $V_{Fl} = 0.50$, the p-type is always *Off*. Fig. 10(b) also shows a similar trend to pull-up transistor as discussed. Consequently, open defects on the TIG-SiNWFETs in INV logic gates get along with several fault models, corresponding to the voltage of V_{Fl}. For V_{Fl} below 0.50 V, the pull-down transistor (t3) is polarized to n-type. Here, the float defect impacts the timing of the INV gate but does not change the functionality. Beyond this threshold, the INV gate exhibits an incorrect functionality that can be captured by the common SOF model.

In Fig. 10(c) and (d), the variation in leakage and delay of the pull-up (t1) and pull-down (t3) transistors of the TIG-SiNWFET NAND are shown. A drastic increase in delay occurs as V_{Fl} changes from its intended bias similar to what observed for the INV gate. For t3, the leakage represents a relatively small variation . This is due to the fact that leakage of n-type device (t3) is dominated by the other transistor (t4) of the pull-down in NAND gate. Therefore, the open defect in TIG-SiNWFET NAND can be detected using the combination of delay fault and SOF.

The leakage-delay characteristics of the 2-input XOR are illustrated in Fig. 10(e) and (f). Against the SP gates, here only the leakage represents a considerable variation (five orders of magnitude) for the various V_{Fl} (see Fig. 10(e)). Thus, the defect

can be tested only with stuck-On fault model. Fig. 10(f) also represents the behavior of XOR when the open fault happens in the pull-down transistor (t3). Here, the leakage variation (six orders of magnitude) contributes to detect the faulty device, while the delay represents a slight variation. Therefore, the test of open defect for TIG-SiNWFET XOR requires a combination of SOF, and stuck-On fault models. For the 3-input XOR and MAJ logic gates, there exists at least an input pattern that can reveal the defective device. Thus, the SOF is enough for these logic gates.

C. Bridge Characterization in the SP and DP Logic Gates

Among various types of bridge defects, short between polarity terminals and supply voltage is exclusive to CP logic gates. In SP logic gates, the bridge connection between polarity controls and V_{DD} in pull-up network changes the desired polarity of the device from p to n. Similarly, bridge defect between polarity controls and GND in pull-down network leads to the polarity change from n-type to p-type. This defect in SP logic gates represents similar behavior to channel break which can be easily covered by SOF. For the DP logic circuit, this defect can be masked depending on the location of the faulty transistor in the circuit. As PGs come from input signals, and polarity terminals are accessible from circuit inputs, it is possible to define a logic level fault model for this defect to facilitate the test process. We define the stuck-at n-type fault to represent the bridge defect in the pull-up network. The stuck-at n-type defect can be applied on the circuits using $V_{\text{stuck-at}\,n} = [PG_D : '1'\, PG_S : '1']$. Similarly, the stuck-at p-type defect is defined by $V_{\text{stuck-at}\,p} = [\text{PG}_D : '0'\, \text{PG}_S : '0']$.

In order to evaluate the performance of this model, we analyzed the TIG-SiNWFETs XOR by exhaustive fault injection. If the faulty device is located in pull-down network, the wrong output of the logic gate reveals the fault. For the pull-up network, the fault detection is only possible by leakage observation. Here, the leakage variation is more than $\times 10^6$. This variation is high enough to be sensible by the I_{DDQ} test.

D. Channel Break in the SP and DP Logic Gates

Channel break demonstrates a similar behavior like SOFs in SP logic gates. The detection of this defect requires to employ a two-pattern test. The first vector initializes the gate output and the second one evaluates the wrong output value in the presence of a fault. For example, a NAND gate as a SP logic contains three vectors of two-pattern tests ($v1 = (11 \rightarrow 01), v2 = (11 \rightarrow 10), v3 = (00 \rightarrow 11)$), by which all the channel break defects for the TIG-SiNWFET NAND can be detected. Although it is possible to detect all faults related to the SP logic gates such as FinFET NAND gates, detection of open faults in DP logic gates is nontrivial. When a channel break happens on a transistor of a DP TIG-SiNWFET gate, the redundant structure of the transistors masks the impact of faulty transistor. Here, the fault masking depends on the capacitances that couple to the output node and the polarity of the fault free transistor. In order to simulate this situation, we performed fault injection using vectors $V_{P_{\text{Off}}} = [\text{CG: } '1'\ \text{PG} : '0']$ (p-type off transistor) and $V_{N_{\text{Off}}} = [\text{CG: } '0'\ \text{PG} : '1']$ (n-type off transistor). When the negated value of the CG signal is applied to PGs, the transistor goes to the turn off mode. The vectors have been applied on the 2-input TIG-SiNWFET XOR (FO4) to evaluate the channel break on the DP logic gates. Here, all the injected faults are masked by the transistors in the pull-up and pull-down networks. Indeed, the channel break defect does not change the logic gate functionality. The defect only affects the performance parameters of the gate such as delay and leakage. Our simulation results on 2-input XOR revealed that the variation of performance parameters are too low for the purpose of fault detection ($\Delta\ leakage \leq 100\%$, and Δ delay $\leq 58\%$). The challenging part to reveal this defect is limited access to the polarity terminals in DP logic gates, since they are utilized as logic gate inputs. In the following, we propose a procedure which can be efficiently used for channel break detection of DP logic gates.

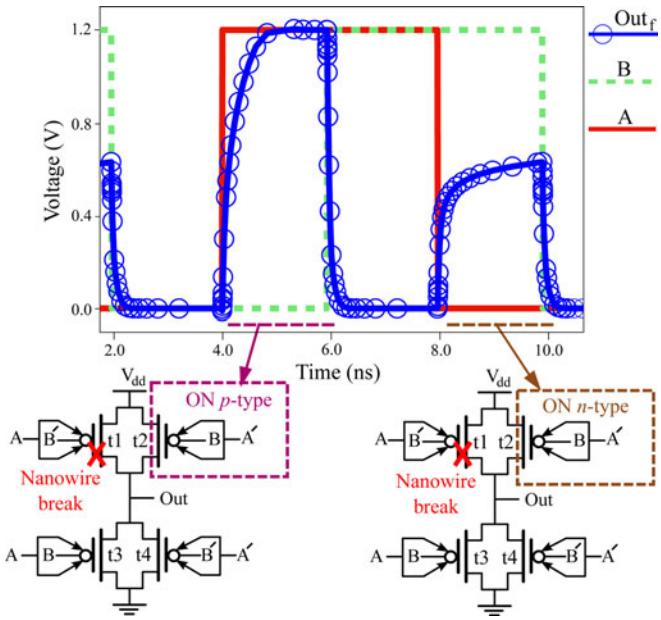

Fig. 11. Nanowire break defect detection using a pair of two-pattern test.

Unlike the SP logic gates, the detection of channel break defects in DP logic gates requires a pair of two-pattern test vectors. Suppose that we have a channel break defect in a pull-up transistor (t1) of an 2-input XOR gate. In this case, the transmission gate structure that connects the output to V_{dd} is degraded to a pass transistor (t2). The first vector, ($v1 = (00 \rightarrow 10)$), initializes the gate output to $'0'$ and then connects the gate output to V_{dd} by polarizing the fault-free device (t2) to a ON p-type transistor (see Fig. 11). The second vector, ($v2 = (11 \rightarrow 01)$), initializes the gate output to $'0'$ again and then connect the gate output to V_{dd} by oppositely polarizing the fault-free device (t2) to a ON n-type transistor (see Fig. 11). The n-type transistor, in pull-up, passes a weak $'1'$ that leads to a large delay penalty in the XOR output to switch from $'0'$ to V_{IH} (The V_{IH} value for this technology is 0.60 V). Here, we observe a delay up to $10\times$ for the XOR gate. In case of no channel break, an *ON* transmission gate in pull-up network passes a strong $'1'$ to the gate output for both test vectors without introducing any extra delay. The same scenario can be utilized for channel break detection in

pull-down network as well. Therefore, the delay can be used a criteria for the detection of channel break.

VI. Conclusion

Further scaling of the planar CMOS technology has been confronted with serious challenges such as increased leakage and process variation. Among the alternative technologies, CP-SINWs such as TIG-SiNWFETs are promising owing to their lower leakage and great electrostatic control. Moreover, their reconfigurable structures provide the opportunity of implementing logic gates with enhanced functionality, i.e., implementing logic gates with fewer number of devices than that of the current technology. As one of the necessary design steps, fault modeling is needed for this new technology. In this paper, we performed an inductive fault analysis on the TIG-SiNWFETs. According to the fabrication process steps, a defect model was extracted. This model contains channel break, GOS, bridge and float defects. We simulated the effect of these defects on various categories of CP circuits. Then, we extended the current CMOS fault model to a new hybrid model, including stuck-at n-type and stuck-at p-type, which can be efficiently used for the detection of defects in CP logic gates. The experimental results revealed that the GOS and floats on the PGs are detectable by analyzing the performance parameters like delay and leakage. We also illustrated that the current CMOS test methods are not able to capture all faults in CP logic gates, i.e., stuck-Open. Finally, we proposed an appropriate test method to cover such faults.

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Hassan Ghasemzadeh Mohammadi received the B.Sc. degree in computer engineering from the Iran University of Science and Technology, Tehran, Iran, in 2005, and the M.Sc. degree in computer engineering from the Sharif University of Technology, Tehran, in 2008. In 2011, he joined the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where he is currently working toward the Ph.D. degree in computer science. His research interests include interesting problems in fault-tolerant design, circuit testing, and reliability.

Pierre-Emmanuel Gaillardon (S'10–M'11) received the Degree in electrical engineer degree from CPE-Lyon, Lyon, France, in 2008, the M.Sc. degree in electrical engineering from INSA Lyon, Lyon, in 2008, and the Ph.D. degree in electrical engineering from CEA-LETI, Grenoble, France, and the University of Lyon, Lyon, in 2011. In starting January 2016, he will become an Assistant Professor at the Electrical and Computer Engineering Department, University of Utah, Salt Lake City, UT, USA. Previously, he was a Research Assistant with CEA-LETI, Grenoble, and a Visiting Research Associate with Stanford University, Palo Alto, CA, USA. His research activities and interests include the development of reconfigurable logic architectures and circuits exploiting emerging device technologies and novel EDA techniques. He received the C-Innov 2011 Best Thesis Award and the Nanoarch 2012 Best Paper Award. He is an Associate Editor of the IEEE TRANSACTIONS ON NANOTECHNOLOGY. He has been serving as a TPC Member for many conferences, including DATE'15–16, VLSI-SoC'15, CMOS-ETR'13–15, Nanoarch'12–15, ISVLSI'14–15 conferences and is a Reviewer for several journals and funding agencies.

Giovanni De Micheli (S'79–M'79–SM'80–F'94) received the Degree in nuclear engineering from the Politecnico di Milano, Milan, Italy, in 1979, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of California at Berkeley, Berkeley, CA, USA, in 1980 and 1983, respectively.

He was a Professor of electrical engineering with Stanford University, Stanford, CA. He is currently a Professor and the Director of the Institute of Electrical Engineering at the Integrated Systems Centre, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where he is also the Program Leader of the Nano-Tera.ch Program. He has authored or coauthored more than 600 papers in journals and conferences, and a book entitled *Synthesis and Optimization of Digital Circuits* (New York, NY, USA: McGraw-Hill, 1994), and coauthored and coedited eight other books. His citation H-index is 84 according to Google Scholar. His current research interests include design technologies for integrated circuits and systems, such as synthesis for emerging technologies, networks on chips, 3-D integration, and heterogeneous platform design, including electrical components and biosensors, and data processing of biomedical information.

Prof. De Micheli is a Fellow of the Association for Computing Machinery and a Member of the Academia Europaea and Scientific Advisory Board of imec and STMicroelectronics. He has been with the IEEE in several capacities, including as the Division 1 Director from 2008 to 2009, the Cofounder and President Elect of the IEEE Council on Electronic Design Automation from 2005 to 2007, the President of the IEEE Circuits and Systems Society in 2003, and the Editor-in-Chief of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (CAD) and the IEEE TRANSACTIONS ON INTEGRATED CIRCUITS AND SYSTEMS (ICAS) from 1987 to 2001. He has been the Chair of several conferences, including DATE since 2010, pHealth since 2006, the International Conference on Very Large Scale Integration since 2006, the Design Automation Conference (DAC) since 2000, and the International Conference on Computer Design since 1989. He received the 2012 IEEE/Circuits and Systems Society (CAS) Mac Van Valkenburg Award for contributions to theory, practice, and experimentation in design methods and tools, the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems, the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000, and the D. Pederson Award for the best paper in the IEEE CAD and ICAS in 1987, and several best paper awards, including the DAC in 1983 and 1993, the DATE in 2005, and the NANOARCH in 2010 and 2012.