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On Temperature Dependency of Steep Subthreshold Slope in Dual-Independent-Gate FinFET

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ABSTRACT Dual-independent-gate silicon FinFET has demonstrated a steep subthreshold slope (SS) when a positive feedback induced by weak impact ionization is triggered. In this paper, we study the temperature dependency of the steep SS by characterizing the fabricated device from 100 to 380 K. The measured characteristics of SS show a reduced sensitivity to temperature as compared to conventional MOSFETs. Based on the temperature-dependent characterization, we further analyze the steep-SS characteristics and propose feasible improvements for optimizing the device performance.

INDEX TERMS FinFET, Schottky barrier, steep subthreshold slope, impact ionization, feedback.

I. INTRODUCTION

Lowering the supply voltage is considered as an efficient way to reduce the power consumption of integrated circuits. In this context, transistors with a steep Subthreshold Slope (SS) are expected to maintain good switching properties at very low operation voltage.

In order to break the fundamental limit of the SS in conventional MOSFETs, devices based on different mechanisms are proposed, such as Tunnel FET, IMOS, and NEMFET [1]–[3]. In addition, a class of devices also achieves a super-steep SS ($<$10 mV/dec) by introducing a positive feedback induced by weak impact ionization. This steep-SS behavior has been demonstrated with various device structures, including partially-depleted SOI MOSFET [4], fully-depleted SOI MOSFET [5], [6], junctionless transistor [7] and Dual-Independent-Gate (DIG) FinFET [8]. We refer to such a class of devices with Super-Steep Subthreshold Slope, as S4-FETs. The S4-FETs demonstrate greatly improved SS over the subthreshold region with good reliability, as well as low leakage and high I_{on}/I_{off} ratio, showing their potential for low-power applications.

In this paper, we study the subthreshold characteristics of the S4-FETs, by performing temperature-dependent characterization on DIG FinFET from 100 K to 380 K. It is observed that the SS shows less sensitivity to temperature than conventional MOSFETs. We also perform an analysis on the SS based on the temperature-dependent characterization. According to the analysis, we suggest that, in addition to enhancing the impact ionization, a better control of the Schottky-barrier bias region and the leakage reduction can further optimize the SS and reduce the required drain bias.

II. DEVICE OVERVIEW

Fig. 1(a) shows the structure of a DIG FinFET. The device exploits a fin-shaped channel with metallic source and drain contacts. The channel electrostatics is controlled by two electrodes: The Schottky-Barrier Bias (SBB) electrostatically modulates the Schottky barriers at source and drain; The Gate (G) controls the potential barrier in the channel to turn the device *on* or *off*. Note that, thanks to its control on the Schottky-barrier injection, the SBB has the capability to

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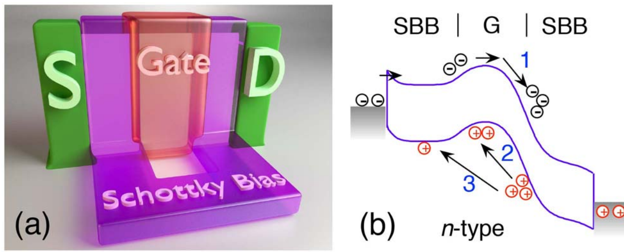

FIGURE 1. (a) Conceptual sketch of a DIG FinFET with steep SS. (b) Mechanism of the impact ionization induced positive feedback during transition in *n*-type configuration [8].

determine the polarity of the device by favoring either the conduction of electrons or holes [9].

The DIG FinFET is fabricated with a dopant-free process on a lightly *p*-type doped ($\sim 10^{15}/cm^3$) SOI wafer [8]. The height and the thickness of the fin are 340 nm and 40 nm, respectively. Thus, the fin-shaped channel is fully depleted considering the low doping concentration and the thin thickness. The length of the gate and each SBB region are 200 nm with 15 nm SiO_2 as gate dielectric. Nickel silicide is used to form near-midgap Schottky barriers at source and drain. The large dimensions of the device are used in order to increase the yield in our academic cleanroom environment. However, no physical limitations preclude the use of more aggressive dimensions. In the meantime, the thick gate oxide can also enhance the steep SS as discussed in Section IV.

The steep-SS operation in *n*-type configuration is illustrated in Fig. 1(b). When $V_{SBB} > 0$, electrons are selected to tunnel through the Schottky barrier into the channel. When acquiring enough energy, the electrons can cause weak impact ionization, and electron/hole pairs are generated (step 1). The generated holes accumulate in the potential well under the gate (step 2). This lowers the barrier and provides more electrons for impact ionization, thus forming a positive feedback [5]. In addition to the FinFET structure enhancing carrier multiplication [2], a dynamic modulation of the Schottky barrier also contributes to the steep SS. During the transition, the energy band in the SBB region is lowered by the increased quasi-Fermi potential and the generated holes (step 3). This helps to maintain the potential well for the accumulation, thus improving the average SS over the subthreshold region. The operation of *p*-type configuration is similar but with $V_{SBB} < 0$. Note that, the weak impact ionization only occurs during the transition and vanishes when the device completely turns *on*, leading to a good reliability of the S4-FETs [5], [8].

III. TEMPERATURE-DEPENDENT CHARACTERIZATION

In this section, we present the temperature-dependent characterization of the DIG FinFET.

The device characteristics at room temperature are shown in [8]. It demonstrates an average SS of 6 mV/dec over 5 decades of drain current, as well as I_{on}/I_{off} ratio of 10^7.

The *n*-type characteristics at different temperatures are shown in Fig. 2(a). The steep SS is observed from 100 K to 380 K without significant degradation. The minimal SS values obtained for different V_{DS} and temperature conditions are reported in Fig. 2(b). The results show that the SS can be significantly improved by increasing V_{DS}. When $V_{DS} \geq 3V$, the device shows a SS well below thermal limit from 300 K to 380 K. In contrast to the normal-SS operation ($V_{DS} = 2V$), the lines with $V_{DS} \geq 3V$ in Fig. 2(b) shows smaller slope, which indicates a reduced sensitivity to temperature.

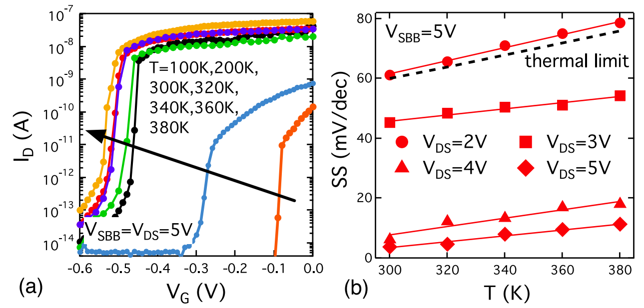

FIGURE 2. (a) *n*-type characteristics with steep SS at different temperatures, (b) Minimal SS at different temperatures and V_{DS}.

Compared to the steep SS in *n*-type characteristics, the *p*-type behavior of the device at room temperature is similar to normal MOSFETs [8]. The weaker impact ionization in *p*-type characteristics than in *n*-type operation is considered as due to the lower impact ionization rate of holes than electrons, which is caused by a much larger phonon scattering rate of holes than electrons [10], [11]. Since the ionization rate decreases with higher temperature, the high-temperature *p*-type characteristics are also similar to normal MOSFETs. In contrast, the low-temperature results of *p*-type operation are in the most concerned and physical relevant regime. Therefore, we try to also observe the impact ionization induced SS improvement in *p*-type configuration by lowering the temperature. As shown in Fig. 3(a), there is nearly

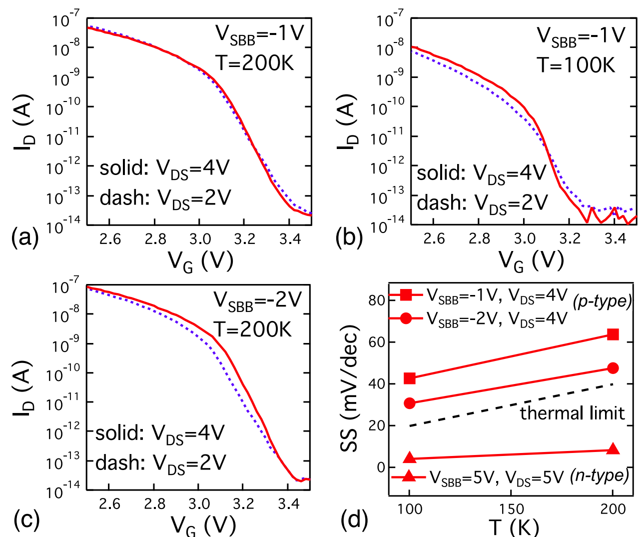

FIGURE 3. (a)–(c) *p*-type characteristics with different V_{SBB} and V_{DS} at 100 K and 200 K. (d) SS of *n*-type and *p*-type configurations at low temperatures.

no improvement of SS by increasing V_{DS} with $V_{SBB}=-1V$ at 200 K. However, by further lowering the temperature to 100 K [Fig. 3(b)] or increasing V_{SBB} to $-2V$ [Fig. 3(c)], the V_{DS}-dependent SS becomes evident, according to the enhancement of ionization with lower temperature and/or higher electric field. Fig. 3(d) summarizes the SS under low temperatures and different V_{SBB} conditions for both n-type and p-type operations. The steep SS in n-type behavior at low temperatures keeps the reduced sensitivity to temperature similar to the high-temperature range. For p-type operation, although still above the thermal limit, the SS becomes less sensitive to temperature when $V_{SBB}=-2V$, similarly to the n-type behavior.

IV. DISCUSSIONS ON THE STEEP-SUBTHRESHOLD-SLOPE CHARACTERISTICS

In this section, we analyze the steep-SS behavior and formulate its expressions. Our study builds on the results obtained for SOI-based S4-FET [4]. Similarly to the SOI-based device, the expression of SS in DIG FinFET is derived as:

$$SS = \frac{kT}{q}\ln 10 \cdot n \tag{1}$$

where

$$n = \frac{1+r}{1+r\frac{dV_{BS}}{dV_{GS}}} \quad \text{and} \quad r = \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}$$

In the DIG FinFET, V_B is the potential at the middle point between the two sidewalls of the fin in the gate-controlled region, and V_{BS} is the difference between V_B and the voltage at source. In contrast, V_B in the SOI-based device stands for the potential at the bottom of the silicon channel [4]. Although the position of V_B used in this work is different than in [4], they both represent the locations where the accumulated charges are stored, thus having similar effects on the steep-SS operation. The DIG FinFET structure also excludes the influence on the SS from a back bias applied through the SOI wafer. It has been validated on the device by varying the back bias from -4V to +4V. As a result, a consistent subthreshold behavior, i.e., the same SS and V_T, is observed under different back biases (data no shown).

Eq. (1) shows that when $dV_{BS}/dV_{GS} < 1$, a small r will lead to a SS approaching the thermal limit. This explains why scaling conventional MOSFET efforts tend to thin the gate oxide. However, when the carriers generated by impact ionization charge the body, it is possible to have $dV_{BS}/dV_{GS} > 1$. In this case, a large r (i.e., thick oxide) can magnify the feedback and further reduce the SS. Therefore, in this kind of steep-SS devices, the scaling down of t_{ox} can be relaxed.

In the presented n-type characteristics of the DIG FinFET, the SS below thermal limit indicates that $dV_{BS}/dV_{GS} > 1$. In contrast, the SS of the p-type characteristics is beyond the thermal limit with $dV_{BS}/dV_{GS} < 1$. Nevertheless, the improvement of SS with increased V_{SBB} and V_{DS} implies that a SS below thermal limit may be also achieved in p-type operation by further optimizing dV_{BS}/dV_{GS}.

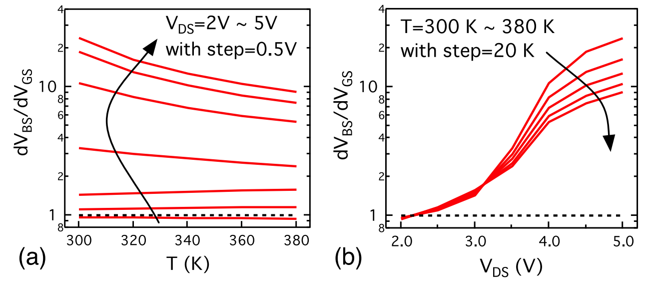

FIGURE 4. Extracted dV_{BS}/dV_{GS} from the n-type characteristics at different temperatures and V_{DS}.

To better understand the operation, Fig. 4 shows dV_{BS}/dV_{GS} extracted from the n-type characteristics according to (1). When $V_{DS} \geq 2.5V$, dV_{BS}/dV_{GS} starts to be larger than one. When $V_{DS} \geq 3.5V$, it is observed that dV_{BS}/dV_{GS} significantly decreases with higher temperature. In addition, dV_{BS}/dV_{GS} also increases with larger V_{DS}.

An expression is then derived to describe the temperature-dependent behavior of dV_{BS}/dV_{GS}. By extending the analysis on SOI-based device to DIG FinFET [4], we obtain the expression for n-type operation as:

$$\begin{aligned}\frac{dV_{BS}}{dV_{GS}} &\simeq \frac{m}{n}\cdot\frac{1}{1+I_{gt}/I_{gi}} \\ &\propto \frac{m}{n}\exp\left[\frac{q}{kT}\left(\frac{V_{GS}}{n}-\frac{V_B-V_{B,SBBs}}{m}\right)\right] \\ &\quad\cdot\exp\left(-\frac{\beta_i l}{V_{DS}}\right)\end{aligned} \tag{2}$$

where I_{gt} is the *off*-state leakage current and I_{gi} is the impact-ionization current [4]. β_i is a constant and l is a structural parameter. m is the ideality factor of the junction between the gated region and the region controlled by the SBB at source (SBBs). Eq. (2) well captures the dependency of dV_{BS}/dV_{GS} on temperature and drain bias in Fig. 4.

We also notice a significant difference in (2) compared to the SOI-based devices: the centric potential at the SBBs region ($V_{B,SBBs}$) replaces the V_S in [4]. Compared to the fixed V_S, $V_{B,SBBs}$ continuously increases during the transition thanks to the increase of quasi-Fermi potential and the effects of the holes generated by the impact ionization. Thus, the improved dV_{BS}/dV_{GS} during the transition can support a better SS over the subthreshold region. As experimentally demonstrated in [8], the DIG FinFET has much better SS compared to the similar device but without the SBB region at source. This proves the importance of the Gate-SBBs junction in the feedback operation. A better control on the SBB region, such as tuning the oxide thickness and the fin width at the SBB region, can thus further optimize the device performance.

Eq. (2) also suggests that lower leakage current I_{gt} helps to improve the SS. With a very small I_{gt}, $dV_{BS}/dV_{GS} > 1$ may be triggered by a very small impact-ionization current I_{gi}, and hence, by a low V_{DS}. Therefore, a gate-all-around nanowire structure may be applicable for future improvements.

Through the study on the temperature dependency of the steep SS, the operation of the device is better understood, and we suggest feasible improvements on the device performance based on the study.

First, the device performance can be improved by applying an optimized process with scaled dimensions and technology boosters, such as strain technology for enhancing the carrier mobility and tuning ionization rates. As a Schottky-barrier device, the drive current is limited by the Schottky-Barrier Height (SBH). Thus, a reduced SBH for electrons improves the drive current of *n*-type configuration. Furthermore, a channel material with smaller bandgap can be used to form lower SBH for both electrons and holes, thus improving the drive currents for both *n*-type and *p*-type configurations [12].

Towards low-power applications, the steep-SS devices are desired to operate with a sufficiently low V_{DS}. The strategy to reduce V_{DS} for DIG FinFETs is consequently discussed as follows.

First, as demonstrated in [5], a similar steep-SS operation is achieved in a 25 nm SOI device with $V_{DS} = 1.2V$. With the additional aid of the DIG structure, the dynamic modulation of Schottky barriers can further improve the steep SS. Therefore, the DIG FinFET with deeply scaled dimensions and optimized source/drain resistance may require a $V_{DS} \leq 1.2V$, which is close to the threshold energy to trigger impact ionization in silicon as the bandgap of silicon is ~1.12 eV at 300 K.

On the other hand, as discussed above, the steep SS indeed depends on the ratio between the impact-ionization generation and the recombination. Although with fewer generation, the impact ionization can still occur with a sub-bandgap drain bias [13]. Thus, a steep SS below thermal limit is still conceivable with a sub-bandgap drain bias if the feedback is optimized with the improvements for leakage reduction, such as applying a nanowire structure.

In addition, the threshold energy to trigger impact ionization decreases with the decreasing bandgap of the material [10]. Thus, the required V_{DS} can also be reduced by replacing silicon with other materials with smaller bandgap or higher impact ionization rate, which is consistent with the suggestion for improving the drive current. For instance, the bandgap of germanium is ~0.66 eV at 300 K, giving enhanced ionization rates for both electrons and holes [10]. In this respect, the inherent suppression of *off*-currents in the DIG-FET approach allows to keep I_{gt} sufficiently low as a further requirement for obtaining steep slopes in (2). Thus, the steep SS can be expected in germanium-based devices with a V_{DS} below 1 V for both *n*-type and *p*-type conductions.

V. CONCLUSION

We investigated the temperature dependency of the subthreshold slope in the DIG FinFET through characterization of *n*-type and *p*-type operation from 100 K to 380 K. The steep subthreshold slope shows reduced sensitivity to temperature as compared to conventional MOSFETs. Based on the characterization, we analyzed the epitomized subthreshold slope in the formula and suggested that an improved control on the Schottky-barrier bias region and a reduction of the leakage current can further optimize the device performance.

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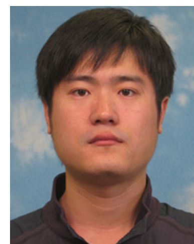

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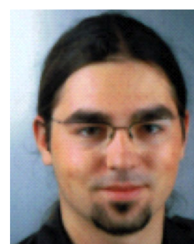

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