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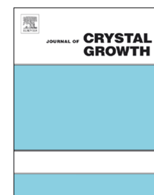

Bottom-up engineering of InAs at the nanoscale: From V-shaped nanomembranes to nanowires

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ABSTRACT

The ability to rationally tune the morphology of nanostructures is a fundamental milestone in nanoscale engineering. In particular, the possibility to switch between different shapes within the same material system represents a further step in the development of complex nanoscale devices and it increases the potential of nanostructures in practical applications. We recently reported a new form of InAs nanostructures growing epitaxially on Si substrates as vertical V-shaped membranes. Here we demonstrate the possibility of modifying the shape of these nanomembranes and turning them into nanowires by modulating the surface roughness of the substrate by varying the surface treatment. We show that the growth of nanomembranes is favored on smooth surfaces. Conversely rough surfaces enhance the growth of nanowires. We also show that the V/III ratio plays a key role in determining the absolute yield, i.e. how many nanostructures form during growth. These results envisage a new degree of freedom in the engineering of bottom-up nanostructures and contribute to the achievement of nanostructure networks.

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1. Introduction

Nanoscale structures with controlled size and morphology have attracted extensive interest over the past years. The miniaturization of integrated circuits down to sub-micrometric scales has been key in the developments of increasingly more advanced microelectronic devices which are ubiquitous in our daily life [1]. In recent years, however, the pace of miniaturization has considerably slowed down as the customary "top-down" fabrication methods are reaching the limit of their capability [2]. Two issues in particular are hindering the development of even smaller electronic components: the failure of semiconductor physics in nanometer-scale devices and the fundamental limitations of conventional photolithography, which constitutes a key step in the top-down approach. An alternative methodology, called "bottom-up", has shown promising results in overcoming these limits. Nanostructures created "bottom-up", i.e. built from their smallest possible components, atoms and molecules, are regarded as the fundamental building blocks of future electronic devices. Examples of non-planar nanostructures can be as simple as nanowires [3,4] or more complex structures such as nanomembranes [5–9], nanowalls [10], nanoplates [11], nanosheets [12,13], nanotrees [14], tripods and tetrapods [15–18]. Besides electronics, non-planar nanostructures have also found many novel applications in research areas such as energy storage [19], energy generation [20,21], lasers [22,23] and non-linear optics [8,24]. Here what makes the "bottom-up" approaches particularly interesting is that they offer a way to synthesize nanocrystals with controlled size and shape.

The last few years have also seen an increased interest in III–V materials and in the integration of III–Vs on silicon which is facilitated by nanowires [25–31]. Nanoscale electronics, optoelectronics, photonics and photovoltaics would benefit from this integration because nanoscale structures could be eventually engineered on silicon, a mature and less expensive platform and with complementary functionality. III–V nanostructures are promising as they offer an efficient elastic relaxation of the strain thanks to their small footprint and free-standing nature [32–34].

In order to bring the integration of III–V materials and silicon closer to the existing technological platforms, the nanostructures should be obtained in an ordered manner on (001) substrates. Silicon (001) is the platform in use across the microelectronics industry, as CMOS fabrication on [110] or [111] surfaces have inferior gate oxide reliability. One should also note that nanowire growth along (001) results in a

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reduction of structural defects and suppression of polytypism [35,36]. The ordered growth of III–V nanostructures has been intensively studied very recently in different material systems [26,35,37–44]. Different techniques such as electron beam, nanosphere, nanoimprint or phase-shift lithography have been used for the definition of the patterns [45–50]. Only a few groups report on ordered growth of nanostructures on silicon (001) [35,51,52].

An important milestone in nanoscale engineering is the understanding of the underlying mechanisms that allow for the fabrication of different shapes. Several groups have shown the ability to rationally change the shape of the structures for example by inducing new branches [14,53–55] or by directly crystallizing the material in different configurations [56,57]. In these cases the different shapes are achieved by simply changing the growth conditions. Utama et al. have recently suggested the possibility to manipulate the shape of the non-planar nanostructures in van der Waals epitaxy by changing the surface treatments prior to growth, although they did not fully unravel the underlying mechanism [18,58].

We recently reported on a new form of InAs nanostructures, vertical wing-shaped membranes [8]. A microscopic model for the formation of the membranes and a detailed study on the effect of the growth conditions on their morphology were also reported [8,9]. In this work we demonstrate that it is possible to modify the shape of InAs nanostructures simply by modulating the surface roughness of the substrate. We examine the role of the V/III ratio, etching and cleaning steps in the relative occurrence of nanomembranes and nanowires. We show that, among these factors, fine sample preparation can be used to favor the presence of one or the other type of nanostructure which relies on two different growth mechanisms. We also show that the V/III ratio plays a key role in determining the absolute yield, i.e. how many nanostructures form during the growth. The ability to manipulate the shape of nanostructures is a further step in the fabrication of advanced nanodevices and nanosystems as it gives a new degree of freedom in the engineering of bottom-up nanostructures.

2. Experiments

The InAs nanostructures were grown by MBE in a DCA P600 system. The growths were performed on (001) p-doped silicon wafers with a resistivity of 0.1–0.5 Ω cm. To achieve precise positioning of the nanostructures, we defined regular arrays of nanoscale holes on a thermally oxidized Si(001) wafer, with diameters ranging from 30 to 350 nm and pitches (the inter-hole distances) ranging from 200 to 2000 nm. The thermal oxide layer was grown in a Centrotherm furnace at 900 °C; before loading into the furnace, the wafers have been cleaned with a RCA process to remove organic and metallic contaminants. The pattern was predefined in a ZEP resist with electron-beam lithography and had been transferred to the 20 nm thick oxide layer using a 12 s 7:1 buffered HF (BHF) wet etch or by a He/CHF_3 reactive ion etch. Prior to the introduction in the MBE chamber, a further dip in a wet etching solution was performed in order to guarantee a pristine surface. The samples with patterns defined in the 7:1 BHF solution were dipped in the same wet etching solution for a further 1 s before loading. The patterns prepared with the He/CHF_3 dry etch were dipped in three wet etch solutions: a 7:1 BHF; a customized, highly diluted BHF wet etch for a more controlled etching rate; a typical isotropic polysilicon etch in nitric and hydrofluoridric acid. The reason for using different etching solutions was to deliberately change the surface roughness of the silicon substrate. After the last dip it was observed that the oxide thickness is reduced to 10 nm. The different sample preparations are summarized in Table 1.

Table 1
Summary of the different sample preparations.

Sample prep.	Main etch	Final dip (wet)	Dilution
N.1	BHF (wet)	NH_4F (40%):HF (49%)	7:1
N.2	CHF_3/He (dry)	NH_4F (40%):HF (49%)	7:1
N.3	CHF_3/He (dry)	NH_4F (40%):HF (49%)	500:1
N.4	CHF_3/He (dry)	HNO_3 (70%):HF(49%):H_2O	50:3:20

The substrates were subsequently degassed at 600 °C for 2 h in UHV and transferred to the growth chamber. There, they were again heated to 770 °C for 30 min to further remove possible surface contaminants. After this steps, the HF treated silicon surfaces are hydrogen free as the hydrogen desorbs already at 510 °C [59]. The growth was carried out at a nominal In growth rate of 0.2 Å/s, As_4 partial pressure ranging between 0.1×10^5 and 1.4×10^5 Torr (V/III beam equivalent pressure – BEP – ratios from 6 to 90), temperature 520 °C, and with 7 rpm rotation. In a previous work [9] we showed that at this temperature there is optimal growth selectivity: the nanostructures preferentially nucleate in the openings where the silicon surface is exposed, rather than on the SiO_2 of the growth mask [41]. Once the growth temperature had been reached, both sources (As and In) were opened at the same time and then switched off simultaneously at the end of the growth. The samples were then cooled down to 200 °C and removed from the reactor. The morphology of the samples was characterized by scanning electron microscopy (SEM) and by transmission electron microscopy (TEM) in a TECNAI F20 operated at 200 kV from the Institut Català de Nanociència i Nanotecnologia (ICN2) at UAB Campus, Bellaterra, Barcelona; in a Phillips CM300 operated at 300 kV and a FEI Tecnai OSIRIS operated at 200 kV from the Centre de Microscopie Electronique (CIME) at EPFL Lausanne. TEM cross-sections were prepared by using a Focus Ion Beam (FIB).

3. Results

In this section we analyze the influence of the substrate preparation on the relative occurrence of nanomembranes and nanowires. The first subsection is dedicated to the description of the effects of a full wet chemical etch. Then we move to analyze the growth on patterns defined through dry etching. The results obtained by varying the final dip are presented in a further subsection.

3.1. *Analysis of sample prep. N.1: wet etch + BHF dip*

As an initial step in the analysis of the experimental results we examine the growth of InAs nanostructures on a first substrate obtained by defining the pattern with a main etch and dip in a 7:1 BHF etch (sample preparation N.1). Fig. 1 shows scanning electron microscopy (SEM) planar and tilted images of the samples grown under an As_4 partial pressure of 1.15×10^5 (V/III BEP ratio = 60) for 2 h. It is worthwhile to note that the sample had been prepared and grown in the same experimental conditions employed in the previously reported works on V-shaped nanomembranes [8,9]. Interestingly, as we show in Fig. 1(a), it can be seen that in addition to the V-shaped nanomembranes (Fig. 1(b) and (c)), nanowires (Fig. 1(c) and (d)) and tripods (Fig. 1(e)) are also present. Under these particular growth conditions the nanomembranes represent 90% of the structures grown while the nanowires are typically 9%. Only a small occurrence of tripods ($<0.5\%$) is detected.

We now proceed to determine if the V/III BEP ratio can influence the occurrence of any of these nanostructures. To this

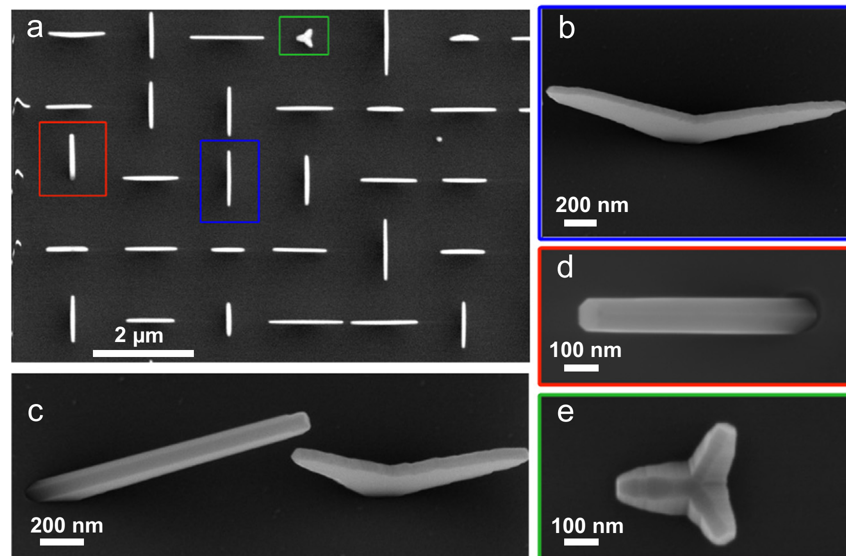

Fig. 1. Scanning electron microscopy (SEM) images of InAs nanostructures grown at 520 °C under an As_4 partial pressure of 1.15×10^5 Torr. (a) A low magnification planar view image illustrates the outcome of the growth: V-shaped nanomembranes, nanowires and tripods. (b) A tilted view (20°) of an InAs nanomembrane showing arms branching towards two ⟨111⟩ B directions. (c) A tilted view (20°) of a nanowire with a nanomembrane. (d) A planar view of an InAs nanowire. (e) A planar view of an InAs tripod.

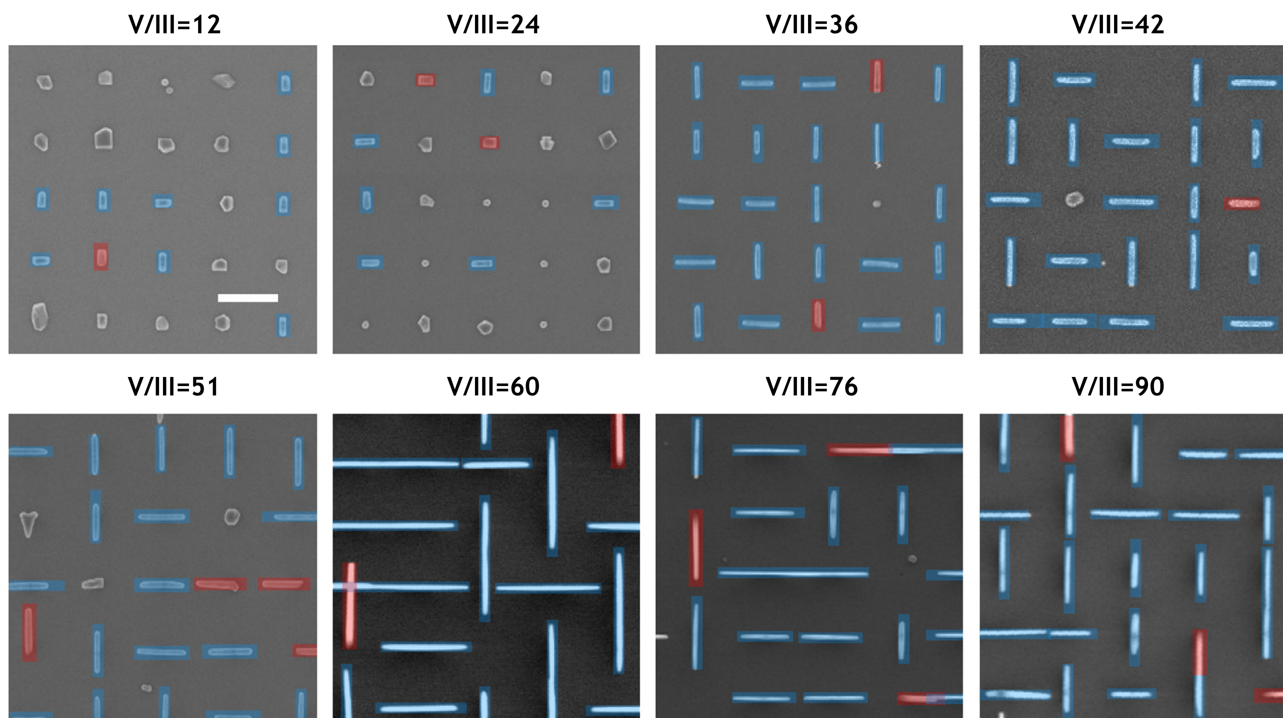

Fig. 2. Planar view SEM images of InAs nanomembranes and nanowires grown at 520 °C and under different V/III beam equivalent pressure ratios, from 12 to 90. In the images, the hole diameter is 90 nm and the inter-hole distance is 1 μm. The V-shaped nanomembranes are highlighted in blue while the nanowires in red. The picture illustrates how the yield of the nanostructures depends on the V/III ratio and improves as the V/III ratio increases. The scale bar is 1 μm and is the same for all images. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

purpose we performed another set of growths using the sample preparation N.1 and varying the V/III BEP ratios from 6 to 90. For simplicity we will write V/III ratio instead of V/III BEP ratio. Representative planar view SEM images are displayed in Fig. 2.

Here the inter-hole distance is 1000 nm and the opening size is 90 nm. At very low V/III ratio (V/III=6, shown elsewhere [9] and not shown here) we find only indium droplets. This is in agreement with the observation that the formation of indium terminated Si(001) surfaces inhibits the formation of InAs islands [60]. By increasing the V/III ratio up to 12, the nanostructures start to form. At this V/III ratio we have many islands but by increasing the V/III ratio, islands progressively give way to nanomembranes and nanowires. We conclude then that the yield of the nanostructures depends strongly on the V/III ratio. Another observation stemming from the SEM images in Fig. 2 is that the length of the nanowires and nanomembranes increases with the V/III ratio. Indeed, similar to nanowires, the length of the arms of the nanomembranes depends on the V/III ratio, consistent with a group V-limited growth regime [9]. In Fig. 3 we summarize the statistical analysis of the yield of the nanomembranes (Fig. 3(a)) and of the nanowires (Fig. 3(b)) as a function of the V/III ratio for different hole diameters. In agreement with Fig. 2, the yield is low for small V/III ratios and increases with the V/III ratio. The yield

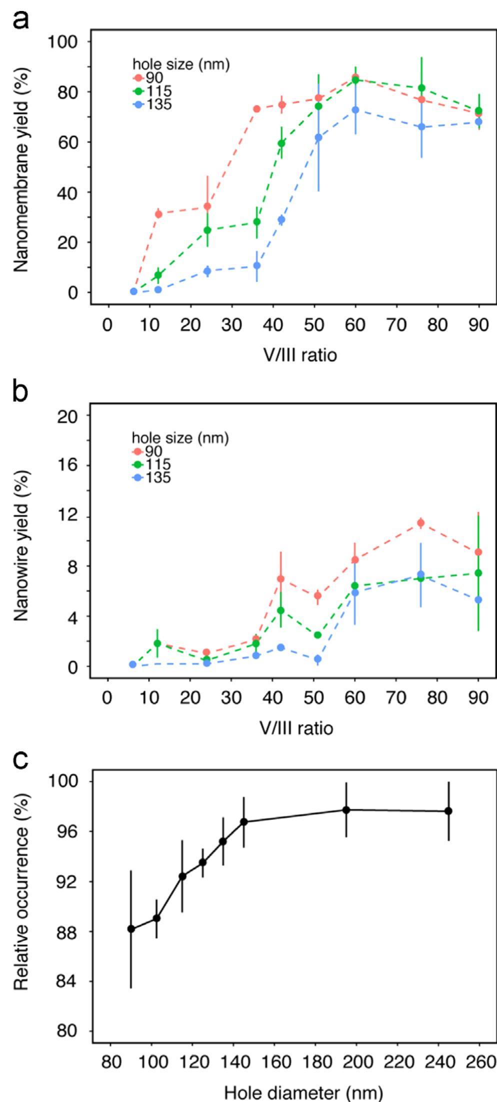

Fig. 3. The yields of InAs nanomembranes (a) and nanowires (b) are plotted as a function of the V/III BEP ratio, for opening size 90, 115 and 135 nm. The yields of both nanostructures increase by increasing the V/III ratio until they reach a plateau. The results do not depend on the inter-hole distances. (c) Relative yield of nanomembranes at V/III ratio=60 as a function of the opening size: a small decrease is observed for smaller hole diameters.

depends inversely on the hole diameter (i.e. it decreases with larger holes). Conversely, the results do not show a dependence of yield on the inter-hole distance (see Supporting Information for further details).

Having looked at the yield of nanostructures in the different patterns, we turn our attention to the relative occurrence of nanomembranes against nanowires (Fig. 3(c)). Across all patterns with different V/III ratios we observe a general an increased occurrence of nanomembranes, between 90% and 98%. This shows that, while the V/III ratio has a role in determining the overall yield of the nanostructures, it does not significantly impact the relative occurrence of nanomembranes. Conversely we see that the relative occurrence of nanomembranes seems to show a dependence on the hole diameter and it decreases as the hole size decreases (Fig. 3(c)).

3.2. Analysis of sample prep. N.2: dry etch + BHF dip

In order to determine if the hole size really limits the yield of nanostructures and if it could potentially increase the nanowire formation, we fabricated arrays with smaller holes. In order to reach smaller diameters, we replaced the standard wet etch (isotropic, inevitably enlarges the diameter) with a dry etch (anisotropic). A 7 s He/CHF_3 reactive ion etch (RIE) and a fast dip in a BHF solution (sample prep. N.2) allowed us to obtain holes as small as 30 nm in diameter, three times smaller than the smallest we could achieve in the previous sample preparation N.1. We then performed a new growth keeping the same growth conditions ($T=520\,^{\circ}$C, BEP V/III=60 and a nominal In growth rate of 0.2 Å/s) of our first sample with preparation N.1. As shown here below, the novel sample preparation drastically changes the outcome of the growth. The first difference we observe with the new preparation is that the absolute yield (defined as the sum of yield of nanomembranes and yield of nanowires) is reduced. For a hole diameter of 90 nm, with the previous sample preparation in a wet chemical etch, a yield of 95% was achieved. With the new preparation, the yield at the same hole diameters decreases to 45%. Even at smaller hole diameters (which did not exist in the previous sample) the yield increases but only up to 70% for the smallest hole size of 30 nm. We look now at the relative occurrence of nanomembranes against nanowires as a function of the hole diameters. These results are reported in Fig. 4(a). We observe a significant drop in the nucleation of the nanomembranes especially at small holes. In line with the previous sample preparation, the relative occurrence decreases by decreasing the opening size. Interestingly, for hole diameters below 175 nm the relative occurrence of nanomembranes is less than 50% while for sample preparation N.1 it was in a range between 88% and 96%.

In summary, we can confirm that small holes favor the growth of nanowires rather than nanomembranes. In addition, for the same hole size the occurrence of nanowires is enhanced by the use of a dry etch. This different behavior suggests that the two etching procedures produce holes with different features.

3.3. Analysis of sample prep. N.3 (dry etch + highly diluted BHF dip) and sample prep. N.4 (dry etch + polySi dip). The role of surface roughness

To further investigate the effect of the etching procedures on the characteristics of the holes, we grew another set of samples on patterned substrates prepared by dry etching followed by different etching solutions. Our hypothesis here is that surface roughness might be key in the initial stages of growth, thereby allowing one growth mode or the other. We chose etching solutions having a strong influence on the silicon surface roughness. There is extensive literature on the effect of etching solutions on the surface roughness of silicon. Higashi et al. found that the microscopic roughness of the silicon surface can be altered by varying the pH of the HF solutions [61]. In particular, a high pH HF solution shows a smoothening effect on Si(111) surfaces. On other silicon surface orientations such as (001) the solution develops (111) facets, thereby increasing the surface roughness [62]. One way to increase the pH is to add NH_4F [63,64]. In this case, etching Si(001) with NH_4F starts with the formation of small (100) terraces and pyramids with (111) facets and continues with the uncorrelated etch of the terraces. This process leads to a continuous increase in surface roughness during the etching process [62]. Conversely, in microelectronics, a widely used process to reduce surface roughness is a wet chemical etching of silicon in HNO_3:HF solutions with high concentrations of HNO_3 (solution called polysilicon etch) [65]. This etch consists of a two-step chemical process: (1) oxidation of Si to form SiO_2 by the acid HNO_3 and (2) dissolution of SiO_2 by HF and release of a new silicon surface. This is conceptually similar to the sacrificial oxidation performed in microelectronics to remove the RIE damaged silicon [66].

In order to create a rougher surface, we modified the final dip we had used in sample preparations N.1 and N.2 (a common buffered HF composition of 7:1 NH_4F (40%)–HF (49%), with a pH of 5 [67]) by adding NH_4F. We prepared a highly diluted solution:

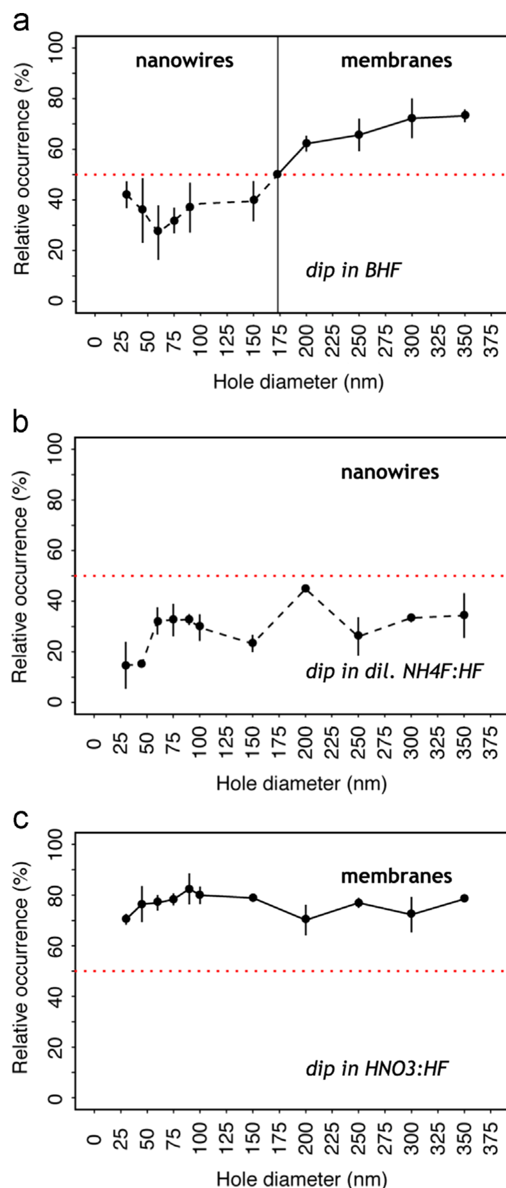

Fig. 4. The relative occurrence of nanomembranes against nanowires for different sample preparations: (a) dry etch followed by a standard BHF; (b) dry etch followed by a dip in a highly diluted NH_4F:HF solution; and (c) dry etch followed by a dip in a HNO_3:HF solution. Different sample preparations can lead to a similar occurrence of nanomembranes and nanowires as in (a), favor nanowires as in (b) where the relative occurrence of nanomembranes drops to 20–30% or favor the nanomembranes as in (c) where their relative occurrence is as high as 70–80%.

500:1 NH_4F (40%)–HF (49%) which we found to have a pH 8. Dry etching followed by this solution is referred to as sample preparation N.3 listed in the table in Section 2. In order to perform a complementary test on a smoother surface, we substituted the BHF dip with a HNO_3:HF etch. Dry etching followed by a dip in HNO_3:HF:H_2O 50:3:20 solution is referred to as sample preparation N.4.

Fig. 4(b) and (c) shows the relative occurrence of nanomembranes against nanowires obtained with these solutions. Data are plotted as a function of the hole diameter, in analogy with Fig. 4(a). Examining the results of the growth on the rough surface (sample prep. N.3) we found that the occurrence of nanowires is larger not only for small holes but also for large holes, where we had seen a majority of nanomembranes with the sample preparation N.2. As we can see in Fig. 4(b) the relative occurrence of nanomembranes against nanowires is always below 50%, even for holes larger than 200 nm. This strongly suggests that the increased roughness of the sample promotes the growth of nanowires. On the other hand, growth on the smoother surface (sample prep. N.4) gave a complementary result and indicated that a smooth surface promotes the occurrence of nanomembranes. The occurrence of nanomembranes has indeed increased to above 70% for all the hole diameters investigated (Fig. 4(c)), similar to what was obtained with the wet etch in sample preparation N.1. As a result, the occurrence of nanowires is reduced accordingly. We note that we obtained a high occurrence of nanomembranes also with another surface treatment consisting of oxidation and of dissolution of oxide and as such yielding smooth surfaces. In this case, after the reactive ion etch in He/CHF_3, the silicon surface has been oxidized in water in a clean room environment. Then, the thin layer of SiO_2 has been dissolved by a dip in buffered HF. This result (not shown) would support our hypothesis that by changing the roughness of the silicon surface it is possible to tune the type of nanostructure to be grown.

Fig. 5 shows a column chart with the absolute yield of nanomembranes as a function of the sample preparation (top). The same Fig. shows top view SEM micrographs of the different sample preparations where nanomembranes are highlighted in blue and the nanowires in red. The absolute yield of nanostructures obtained on the rough surface (sample prep. N.3) is similar to the what was obtained with sample preparation N.2. Interestingly, the absolute yield is much higher on the smoother surface and it is very close to the values obtained with a full wet etching preparation (sample prep. N.1).

4. Discussion

We turn now to the analysis on the role of the substrate preparation in the yield of nanowire and nanomembrane growth. We start by discussing the dependence of the relative occurrence on the hole diameter observed on the samples prepared with a full BHF etch and with the dry etch followed by a dip in BHF (sample prep. N.1 and N.2). To answer the question as to why the growth of nanowires is favored at the expenses of the nanomembranes for smaller hole sizes and rougher Si surfaces, we looked in more detail at the initial stages of growth for the two types of nanostructures.

In a previous publication [8] we showed that the InAs V-shaped nanomembranes stem from the two opposite facets of a nanoscale nucleus with a rectangular pyramidal shape. In the early stages of growth a Stranski–Krastanov (SK) type of quantum dot (QD) with {111} facets nucleates as a consequence of the high lattice mismatch between InAs and Si (11.6%). Subsequently, the growth proceeds selectively on the two (111)B facets of the QD forming the arms of the nanomembranes. The lateral growth of the arms, that consist of (0–11) and (01–1) surfaces, proceeds via step-flow in the ⟨011⟩ directions, slowly compared to ⟨111⟩ B. The width of the nanomembrane is thus given by the distance between the two opposite {110} planes and as such it is mainly determined by the width of the initial quantum dot [9]. An example of this is shown in Fig. 6(a). Here, a cross sectional high-resolution TEM image taken at the interface between the InAs V-shaped nanomembrane and the Si substrate reveals the characteristic nucleus.

In Fig. 6(b) we show a representative TEM image of the bottom part of a nanowire. In this case, we could never find a pyramidal nucleus from which the nanowire should originate. This result is in agreement with the extensive existing literature. The area where the initial stage of the growth takes place exhibits zinc-blende crystalline structure, as we can see in the associated fast Fourier transform in Fig. 6(c). The absence of this pyramidal nucleus at the base of nanowires suggests that the SK growth of QDs is being suppressed in the holes. Moreover, the more frequent appearance of nanowires at smaller hole sizes indicates that the suppression of SK is more

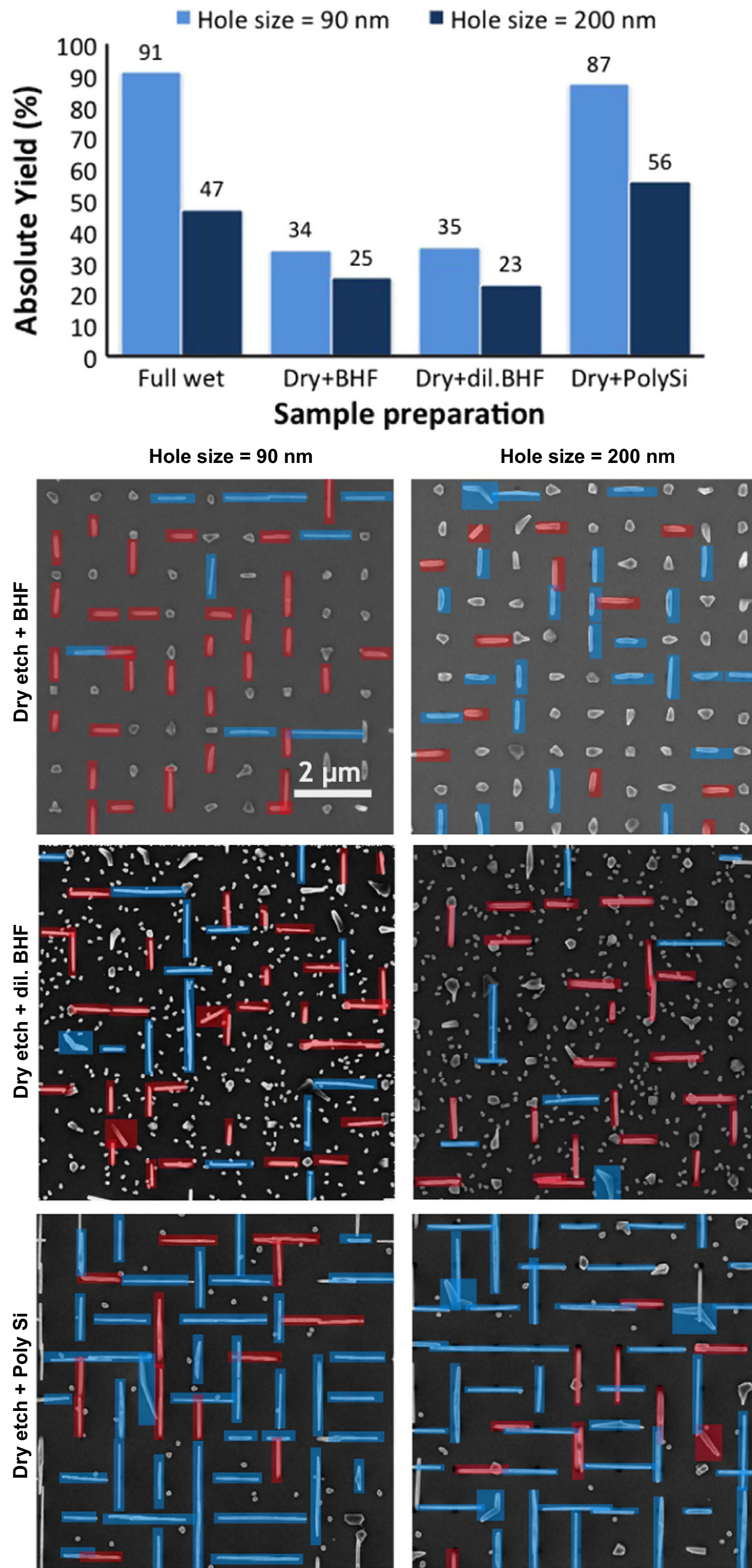

Fig. 5. Top. Column chart reporting the absolute yield of nanomembranes as a function of the sample preparation. Hole sizes 90 nm and 200 nm have been chosen for representing the growth outcome in small and large holes. Bottom. Top view SEM micrographs of samples prepared with a dry etching in He/CHF_3 followed by different dips in wet etching solutions: in standard BHF, in a highly diluted NH_4F:HF, and in a HNO_3:HF solution. The inter-hole distance is 1000 nm and the hole diameters are 90 nm and 200 nm. The V-shaped nanomembranes are highlighted in blue while the nanowires are highlighted in red. The relative occurrence of nanomembranes with respect to nanowires changes with the sample preparation. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

likely for smaller holes. It is worth noting that the SK growth mode on a confined area (like the apertures of the mask oxide) is different from that on a large unpatterned surface. As SK growth is a mechanism to release mismatch strain, there is a critical size for the hole below which the SK mechanism is suppressed [68]. This can explain why smaller holes tend to favor the growth of nanowires.

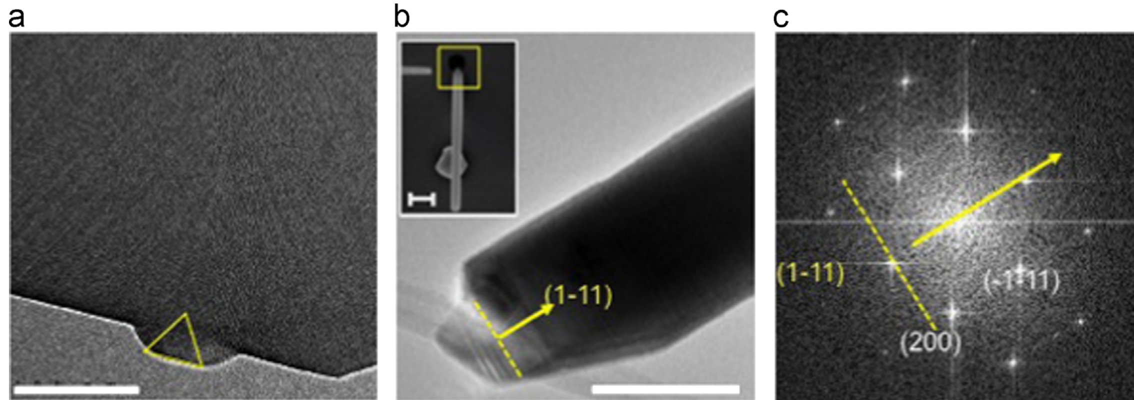

Fig. 6. (a) High-resolution TEM image of the bottom part of a nanomembrane exhibiting the characteristic nucleus, which could be formed by a Stranski Krastanov growth. The scale bar is 100 nm. (b) Low magnification TEM image showing the bottom part of a representative nanowire. Inset: SEM top view micrograph of the nanowire with the bottom part marked in the yellow square. The scale bars of the TEM and SEM images are respectively 100 nm and 200 nm. (c) Associated fast Fourier transform (power spectrum) showing that the crystalline structure of the nanowire at the initial stages of growth is zinc-blende. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

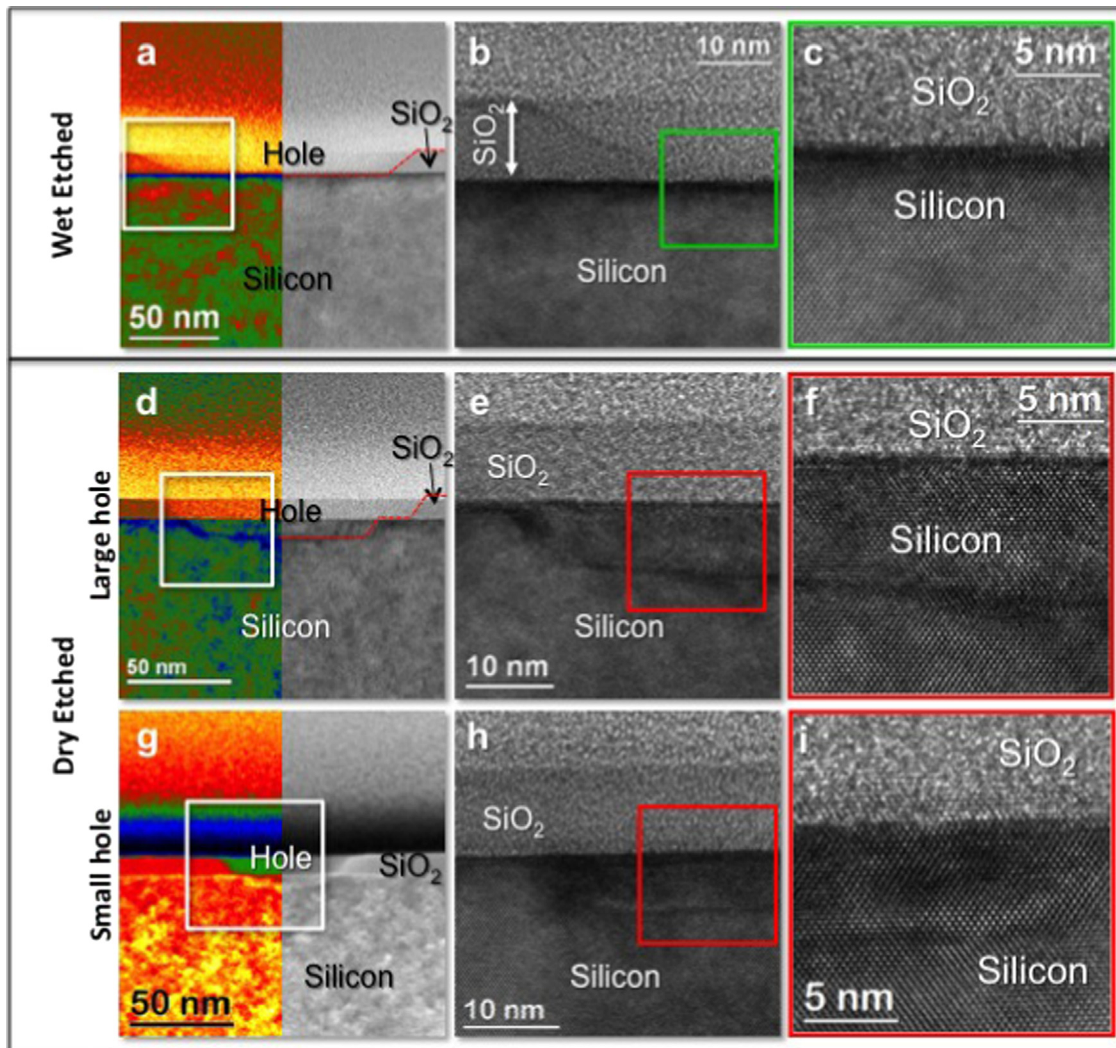

Fig. 7. (a, d, g) Low magnification HRTEM/HAADF images of the patterned silicon substrate under wet/dry etched conditions. The left side of the images is false colored to enhance the hole morphology. (b, e, h) HRTEM images of one corner of the holes. (c/f/i) Magnified details of the squared regions in (b/e/h) evidencing the silicon damage under the hole from the dry etching treatment (with the presence of crystal defects and recrystallization). (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

We now turn our attention to the role of the surface treatment (roughness) on the relative occurrence of nanomembranes/nanowires. An enhancement of the nanowire growth was obtained by substituting the wet etch in BHF with the dry etch in CHF_3/He (from sample prep. N.1. to sample prep. 2). For a given hole diameter, the percentage of nanowires obtained with dry etching is higher than that obtained with wet etching.

Atomic force microscopy (AFM) measurements of the silicon oxide under the different treatments showed that its roughness does not vary. This prompted us to perform TEM analysis in order to study the morphologies of the holes obtained with the two etching procedures.

Cross-sectional low magnification HRTEM images of the nanoscale holes obtained by dry and wet etching followed by a dip in BHF are reported in Fig. 7. Fig. 7(a), (d) and (g) are false color images showing the different morphologies of the holes defined with wet etching (a) and dry etching ((d) large size hole and (g) small size hole). Fig. 7 (b), (c); (e), (f); and (h), (i) show the profile of the holes at different magnifications. In the case of dry etching the hole shows a deep dig in the crystalline silicon as the etching does not land selectively on the silicon substrate. The dig in silicon is reduced by decreasing the hole size due to the aspect ratio dependent etching (ARDE) phenomenon [69]. In Fig. 7 it can also be seen that, on the other hand, the silicon dioxide is selectively removed in the hole defined with a full BHF wet etch. We believe that the surface at the bottom of the holes for sample prep. N.2 (dry etching) is rougher than that obtained with the sample prep. N.1 (wet etching). CHF_3-based dry etching is known to modify the silicon surface, in part due to the ion bombardment of the RIE process, which can even sputter material off the surface. As a consequence, the silicon exposed to plasma is generally damaged [70], while concentrated and buffered HF wet etching does not affect the crystal order of the Si(001) surface [71,72].

We have also tried to characterize the roughness of the silicon surface after the four sample preparations with AFM analysis. Unlike the TEM analysis reported above, in the AFM measurements the roughness of the silicon surface has been measured on large areas of the sample and not in the nanoscale holes: indeed, measuring roughness inside nanoscale holes is not within reach of the existing state-of-the-art AFM techniques. The AFM measurements proved inconclusive as we could not detect any difference in roughness on the large areas within the experimental error: this however does not disprove the TEM analysis conducted within the holes and is compatible with ARDE, the effect where the etch rate depends on the aspect ratio (depth/width) of the features to be etched [69].

In conclusion, we believe that the main driver favoring the formation of nanowires or nanomembranes is not as much the hole size *per se* but the roughness of the substrate: a small hole size simply increases the probability of having only a small area available for the SK transition which in turn favors the growth of nanowires since – as we have explained above – it is not relying on SK unlike in the growth of nanomembranes. An equal or better level of control can be achieved by directly acting on the roughness of the substrate: by increasing the roughness we can reach the critical size below which SK is suppressed. This gives us a way to control the relative occurrence of nanomembranes independently from the hole size in the array, effectively providing a new extra degree of freedom. Removing the constraint on the size of the array is an important step in obtaining more control on the design of nanosystems and in determining the size of the nanostructures.

5. Conclusions

In summary, we have investigated the role of the growth conditions and sample preparation parameters for the growth of InAs nanowires and nanomembranes. In particular we showed for the first time the role of the sample preparation (etching and cleaning steps) in favoring the occurrence of nanomembranes or nanowires. We showed that the formation of InAs V-shaped nanomembranes is quenched by increasing the roughness of the substrate since the formation of Stranski Krastanov quantum dots from which the nanomembranes' stem is suppressed under these conditions. This quenching of the nanomembranes in turn favors the growth of nanowires. Conversely, the preparation of a smooth surface enhances the growth of nanomembranes at the expenses of nanowires' growth. This work is a further step towards fabrication of nanostructure networks and the achievement of high complexity on the same substrate.

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Appendix A. Supplementary data

Supplementary data associated with this paper can be found in the online version at http://dx.doi.org/10.1016/j.jcrysgro.2015.01.040.

References

[1] S.E. Thompson, S. Parthasarathy, Moore's law: the future of Si microelectronics, Mater. Today 9 (6) (2006) 20–25. http://dx.doi.org/10.1016/S1369-7021(06)71539-5.
[2] H. Iwai, Roadmap for 22 nm and beyond (invited paper), Microelectron. Eng. 86 (7–9) (2009) 1520–1528.
[3] E.P.A.M. Bakkers, J.A. van Dam, S. De Franceschi, L.P. Kouwenhoven, M. Kaiser, M. Verheijen, H. Wondergem, P. van der Sluis, Epitaxial growth of InP nanowires on germanium, Nat. Mater. 3 (11) (2004) 769–773. http://dx.doi.org/10.1038/nmat1235.
[4] T. Martensson, C.P.T. Svensson, B.A. Wacaser, M.W. Larsson, W. Seifert, K. Deppert, A. Gustafsson, L.R. Wallenberg, L. Samuelson, Epitaxial III–V nanowires on silicon, Nano Lett. 4 (10) (2004) 1987–1990. http://dx.doi.org/10.1021/nl0487267 http://arxiv:hepth/10.1021/nl0487267.
[5] W. Cheng, M.J. Campolongo, S.J. Tan, D. Luo, Freestanding ultrathin nanomembranes via self-assembly, Nano Today 4 (6) (2009) 482–493. http://dx.doi.org/10.1016/j.nantod.2009.10.005, URL 〈http://www.sciencedirect.com/science/article/pii/S1748013209001169〉.
[6] R. Vendamme, S.-Y. Onoue, A. Nakao, T. Kunitake, Robust free-standing nanomembranes of organic/inorganic interpenetrating networks, Nat. Mater. 5 (6) (2006) 494–501. http://dx.doi.org/10.1038/nmat1655.
[7] Y. Yang, Y. Zhuang, Y. He, B. Bai, X. Wang, Fine tuning of the dimensionality of zinc silicate nanostructures and their application as highly efficient absorbents for toxic metal ions, Nano Res. 3 (8) (2010) 581–593. http://dx.doi.org/10.1007/s12274-010-0019-3.
[8] S. Conesa-Boj, E. Russo-Averchi, A. Dalmau-Mallorqui, J. Trevino, E.F. Pecora, C. Forestiere, A. Handin, M. Ek, L. Zweifel, L.R. Wallenberg, D. Rüffer, M. Heiss, D. Troadec, L. Dal Negro, P. Caroff, A. Fontcuberta i Morral, Vertical III–V V-shaped nanomembranes epitaxially grown on a patterned Si[001] substrate and their enhanced light scattering, ACS Nano 6 (12) (2012) 10982–10991. http://dx.doi.org/10.1021/nn304526k http://arxiv:hepth/10.1021/nn304526k.
[9] E. Russo-Averchi, A. Dalmau-Mallorquí, I. Canales-Mundet, G. Tütüncüoğlu, E. Alarcon-Llado, M. Heiss, D. Rüffer, S. Conesa-Boj, P. Caroff, A. Fontcuberta i Morral, Growth mechanisms and process window for InAs V-shaped nanoscale membranes on Si[001], Nanotechnology 24 (43) (2013) 435603, URL 〈http://stacks.iop.org/0957-4484/24/i=43/a=435603〉.
[10] M. Hiramatsu, K. Shiji, H. Amano, M. Hori, Fabrication of vertically aligned carbon nanowalls using capacitively coupled plasma-enhanced chemical vapor deposition assisted by hydrogen radical injection, Appl. Phys. Lett. 84 (23) (2004) 4708–4710.

[11] M. Aagesen, E. Johnson, C.B. Sorensen, S.O. Mariager, R. Feidenhans'l, E. Spiecker, J. Nygard, P.E. Lindelof, Molecular beam epitaxy growth of free-standing plane-parallel InAs nanoplates, Nat. Nano 2 (12) (2007) 761–764. http://dx.doi.org/10.1038/nnano.2007.378.

[12] J. Liu, X. Huang, Y. Li, K.M. Sulieman, X. He, F. Sun, Hierarchical nanostructures of cupric oxide on a copper substrate: controllable morphology and wettability, J. Mater. Chem. 16 (2006) 4427–4434. http://dx.doi.org/10.1039/B611691D.

[13] C.-Y. Chi, C.-C. Chang, S. Hu, T.-W. Yeh, S.B. Cronin, P.D. Dapkus, Twin-free GaAs nanosheets by selective area growth: implications for defect-free nanostructures, Nano Lett. 13 (6) (2013) 2506–2515. http://dx.doi.org/10.1021/nl400561j ; URL ⟨http://pubs.acs.org/doi/abs/10.1021/nl400561j⟩.

[14] K.A. Dick, K. Deppert, M.W. Larsson, T. Martensson, W. Seifert, L.R. Wallenberg, L. Samuelson, Synthesis of branched 'nanotrees' by controlled seeding of multiple branching events, Nat. Mater. 3 (6) (2004) 380–384. http://dx.doi.org/10.1038/nmat1133.

[15] M.I.B. Utama, Q. Zhang, S. Jia, D. Li, J. Wang, Q. Xiong, Epitaxial II–VI tripod nanocrystals: a generalization of van der Waals epitaxy for nonplanar polytypic nanoarchitectures, ACS Nano 6 (3) (2012) 2281–2288. http://dx.doi.org/10.1021/nn204344z http://arxiv:hepth/10.1021/nn204344z.

[16] B.-B. Wang, J.-J. Xie, Q. Yuan, Y.-P. Zhao, Growth mechanism and joint structure of ZnO tetrapods, J. Phys. D: Appl. Phys. 41 (10) (2008) 102005, URL ⟨http://stacks.iop.org/0022-3727/41/i=10/a=102005⟩.

[17] L. Zhao, Q. Pang, W. Ge, J. Wang, Investigating the growth mechanism of CdSe nano-tetrapods, Integr. Ferroelectr. 137 (1) (2012) 98–104. http://dx.doi.org/10.1080/10584587.2012.687283 http://arxiv:hepth/10.1080/10584587.2012.687283.

[18] M.I.B. Utama, M. de la Mata, C. Magen, J. Arbiol, Q. Xiong, Twinning-, polytypism-, and polarity-induced morphological modulation in nonplanar nanostructures with van der Waals epitaxy, Adv. Funct. Mater. 23 (13) (2013) 1636–1646. http://dx.doi.org/10.1002/adfm.201202027.

[19] C.K. Chan, H. Peng, G. Liu, K. McIlwrath, X.F. Zhang, R.A. Huggins, Y. Cui, High-performance lithium battery anodes using silicon nanowires, Nat. Nano 3 (1) (2008) 31–35. http://dx.doi.org/10.1038/nnano.2007.411.

[20] J. Wallentin, N. Anttu, D. Asoli, M. Huffman, I. Åberg, M.H. Magnusson, G. Siefer, P. Fuss-Kailuweit, F. Dimroth, B. Witzigmann, H.Q. Xu, L. Samuelson, M.T. Borgström, InP nanowire array solar cells achieving 13.8 limit, Science 339 (6123) (2013) 1057–1060. http://dx.doi.org/10.1126/science.1230969 ; URL ⟨http://www.sciencemag.org/content/339/6123/1057.abstract⟩.

[21] J.V. Holm, H.I. Jørgensen, P. Krogstrup, J. Nygård, H. Liu, M. Aagesen, Surface-passivated GaAsP single-nanowire solar cells exceeding 10% efficiency grown on silicon, Nat. Commun. 4 (2013) 1498. http://dx.doi.org/10.1038/ncomms2510.

[22] D. Saxena, S. Mokkapati, P. Parkinson, N. Jiang, Q. Gao, H.H. Tan, C. Jagadish, Optically pumped room-temperature GaAs nanowire lasers, Nat. Photon. 7 (12) (2013) 963–968. http://dx.doi.org/10.1038/nphoton.2013.303.

[23] M.H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, P. Yang, Room-temperature ultraviolet nanowire nanolasers, Science 292 (5523) (2001) 1897–1899. http://dx.doi.org/10.1126/science.1060367, URL ⟨http://www.sciencemag.org/content/292/5523/1897.abstract⟩.

[24] E.F. Pecora, G.F. Walsh, C. Forestiere, A. Handin, E. Russo-Averchi, A. Dalmau-Mallorqui, I. Canales-Mundet, A. Fontcuberta i Morral, L.D. Negro, Enhanced second harmonic generation from InAs nano-wing structures on silicon, Nanoscale 5 (2013) 10163–10170. http://dx.doi.org/10.1039/C3NR03083K.

[25] R. Chen, T.-T.D. Tran, K.W. Ng, W.S. Ko, L.C. Chuang, F.G. Sedgwick, C. Chang-Hasnain, Nanolasers grown on silicon, Nat. Photon. 5 (3) (2011) 170–175. http://dx.doi.org/10.1038/nphoton.2010.315.

[26] M.T. Björk, H. Schmid, C.D. Bessire, K.E. Moselund, H. Ghoneim, S. Karg, E. Lörtscher, H. Riel, Si-InAs heterojunction Esaki tunnel diodes with high current densities, Appl. Phys. Lett. 97 (16) (2010), http://dx.doi.org/10.1063/1.3499365.

[27] W. Wei, X.-Y. Bao, C. Soci, Y. Ding, Z.-L. Wang, D. Wang, Direct heteroepitaxy of vertical InAs nanowires on Si substrates for broad band photovoltaics and photodetection, Nano Lett. 9 (8) (2009) 2926–2934. http://dx.doi.org/10.1021/nl901270n, pMID: 19624100; http://arxiv:hepth/10.1021/nl901270n.

[28] E. Russo-Averchi, M. Heiss, L. Michelet, P. Krogstrup, J. Nygard, C. Magen, J. R. Morante, E. Uccelli, J. Arbiol, A. Fontcuberta i Morral, Suppression of three dimensional twinning for a 100% yield of vertical GaAs nanowires on silicon, Nanoscale 4 (2012) 1486–1490. http://dx.doi.org/10.1039/C2NR11799A.

[29] G.E. Cirlin, V.G. Dubrovskii, I.P. Soshnikov, N.V. Sibirev, Y.B. Samsonenko, A. D. Bouravleuv, J.C. Harmand, F. Glas, Critical diameters and temperature domains for MBE growth of III–V nanowires on lattice mismatched substrates, Phys. Status Solidi RRL—Rapid Res. Lett. 3 (4) (2009) 112–114. http://dx.doi.org/10.1002/pssr.200903057.

[30] P. Krogstrup, R. Popovitz-Biro, E. Johnson, M.H. Madsen, J. Nygaard, H. Shtrikman, Structural phase control in self-catalyzed growth of GaAs nanowires on silicon (111), Nano Lett. 10 (11) (2010) 4475–4482. http://dx.doi.org/10.1021/nl102308k http://arxiv:hepth/10.1021/nl102308k.

[31] E. Uccelli, J. Arbiol, C. Magen, P. Krogstrup, E. Russo-Averchi, M. Heiss, G. Mugny, F. Morier-Genoud, J. NygÅrd, J.R. Morante, A. Fontcuberta i Morral, Three-dimensional multiple-order twinning of self-catalyzed GaAs nanowires on Si substrates, Nano Lett. 11 (9) (2011) 3827–3832. http://dx.doi.org/10.1021/nl201902w, pMID: 21823613; http://arxiv:hepth/10.1021/nl201902w.

[32] K. Tomioka, Y. Kobayashi, J. Motohisa, S. Hara, T. Fukui, Selective-area growth of vertically aligned GaAs and GaAs/AlGaAs core-shell nanowires on Si(111) substrate, Nanotechnology 20 (14) (2009) 145302, URL ⟨http://stacks.iop.org/0957-4484/20/i=14/a=145302⟩.

[33] G. Balakrishnan, S. Huang, L.R. Dawson, Y.-C. Xin, P. Conlin, D.L. Huffaker, Growth mechanisms of highly mismatched AlSb on a Si substrate, Appl. Phys. Lett. 86 (3) (2005), http://dx.doi.org/10.1063/1.1850611.

[34] C.D. Bessire, M.T. Bjork, H. Schmid, A. Schenk, K.B. Reuter, H. Riel, Trap-assisted tunneling in Si-InAs nanowire heterojunction tunnel diodes, Nano Lett. 11 (10) (2011) 4195–4199. http://dx.doi.org/10.1021/nl202103a 21875101.

[35] J. Wang, S. Plissard, M. Hocevar, T.T.T. Vu, T. Zehender, G.G.W. Immink, M. A. Verheijen, J. Haverkort, E.P.A.M. Bakkers, Position-controlled [100] InP nanowire arrays, Appl. Phys. Lett. 100 (5) (2012), http://dx.doi.org/10.1063/1.3679136.

[36] S. Conesa-Boj, I. Zardo, S. Estrade, L. Wei, P. Jean Alet, P. Roca i Cabarrocas, J. R. Morante, F. Peiro, A.R.i. Morral, J. Arbiol, Defect formation in Ga-catalyzed silicon nanowires, Cryst. Growth Des. 10 (4) (2010) 1534–1543. http://dx.doi.org/10.1021/cg900741y.

[37] M.T. Borgstrom, G. Immink, B. Ketelaars, R. Algra, E.P.A.M. Bakkers, Synergetic nanowire growth, Nat. Nano 2 (9) (2007) 541–544. http://dx.doi.org/10.1038/nnano.2007.263.

[38] S. Hertenberger, D. Rudolph, M. Bichler, J.J. Finley, G. Abstreiter, G. Koblmüller, Growth kinetics in position-controlled and catalyst-free InAs nanowire arrays on Si(111) grown by selective area molecular beam epitaxy, J. Appl. Phys. 108 (11) (2010), http://dx.doi.org/10.1063/1.3525610.

[39] S. Plissard, K.A. Dick, G. Larrieu, S. Godey, A. Addad, X. Wallart, P. Caroff, Gold-free growth of GaAs nanowires on silicon: arrays and polytypism, Nanotechnology 21 (38) (2010) 385602, URL ⟨http://stacks.iop.org/0957-4484/21/i=38/a=385602⟩.

[40] S. Gibson, R. LaPierre, Study of radial growth in patterned self-catalyzed GaAs nanowire arrays by gas source molecular beam epitaxy, Phys. Status Solidi RRL —Rapid Res. Lett. 7 (10) (2013) 845–849. http://dx.doi.org/10.1002/pssr.201307142.

[41] S. Plissard, G. Larrieu, X. Wallart, P. Caroff, High yield of self-catalyzed GaAs nanowire arrays grown on silicon via gallium droplet positioning, Nanotechnology 22 (27) (2011) 275602, URL ⟨http://stacks.iop.org/0957-4484/22/i=27/a=275602⟩.

[42] B. Bauer, A. Rudolph, M. Soda, A.F.i. Morral, J. Zweck, D. Schuh, E. Reiger, Position controlled self-catalyzed growth of GaAs nanowires by molecular beam epitaxy, Nanotechnology 21 (43) (2010) 435601, URL ⟨http://stacks.iop.org/0957-4484/21/i=43/a=435601⟩.

[43] S.J. Gibson, J.P. Boulanger, R.R. LaPierre, Opportunities and pitfalls in patterned self-catalyzed GaAs nanowire growth on silicon, Semicond. Sci. Technol. 28 (10) (2013) 105025, URL ⟨http://stacks.iop.org/0268-1242/28/i=10/a=105025⟩.

[44] M. Heiss, E. Russo-Averchi, A. Dalmau-Mallorquí, G. Tütüncüoğlu, F. Matteini, D. Rüffer, S. Conesa-Boj, O. Demichel, E. Alarcon-Lladó, A.F.i. Morral, III–V nanowire arrays: growth and light interaction, Nanotechnology 25 (1) (2014) 014015, URL ⟨http://stacks.iop.org/0957-4484/25/i=1/a=014015⟩.

[45] H.J. Fan, P. Werner, M. Zacharias, Semiconductor nanowires: from self-organization to patterned growth, Small 2 (6) (2006) 700–717. http://dx.doi.org/10.1002/smll.200500495.

[46] D. Lerose, M. Bechelany, L. Philippe, J. Michler, S. Christiansen, Ordered arrays of epitaxial silicon nanowires produced by nanosphere lithography and chemical vapor deposition, J. Cryst. Growth 312 (20) (2010) 2887–2891. http://dx.doi.org/10.1016/j.jcrysgro.2010.07.023, URL ⟨http://www.sciencedirect.com/science/article/pii/S0022024810004732⟩.

[47] K.A. Dick, K. Deppert, L.S. Karlsson, W. Seifert, L.R. Wallenberg, L. Samuelson, Position controlled interconnected InAs nanowire networks, Nano Lett. 6 (12) (2006) 2842–2847. http://dx.doi.org/10.1021/nl062035o 17163716; arxiv:hepth/10.1021/nl062035o.

[48] A. Pierret, M. Hocevar, S.L. Diedenhofen, R.E. Algra, E. Vlieg, E.C. Timmering, M. A. Verschuuren, G.W.G. Immink, M.A. Verheijen, E.P.A.M. Bakkers, Generic nano-imprint process for fabrication of nanowire arrays, Nanotechnology 21 (6) (2010) 065305, URL ⟨http://stacks.iop.org/0957-4484/21/i=6/a=065305⟩.

[49] A.M. Munshi, D.L. Dheeraj, V.T. Fauske, D.C. Kim, J. Huh, J.F. Reinertsen, L. Ahtapodov, K.D. Lee, B. Heidari, A.T.J. van Helvoort, B.O. Fimland, H. Weman, Position-controlled uniform GaAs nanowires on silicon using nanoimprint lithography, Nano Lett. 14 (2) (2014) 960–966. http://dx.doi.org/10.1021/nl404376m, pMID: 24467394; URL arxiv:hepth/10.1021/nl404376m.

[50] K. Subannajui, F. Güder, M. Zacharias, Bringing order to the world of nanowire devices by phase shift lithography, Nano Lett. 11 (9) (2011) 3513–3518. http://dx.doi.org/10.1021/nl102103w, pMID: 21077688.

[51] U. Krishnamachari, M. Borgstrom, B.J. Ohlsson, N. Panev, L. Samuelson, W. Seifert, M.W. Larsson, L.R. Wallenberg, Defect-free InP nanowires grown in 001 direction on InP (001), Appl. Phys. Lett. 85 (11) (2004) 2077–2079.

[52] W. Guo, A. Banerjee, P. Bhattacharya, B.S. Ooi, InGaN/GaN disk-in-nanowire white light emitting diodes on (001) silicon, Appl. Phys. Lett. 98 (19) (2011), http://dx.doi.org/10.1063/1.3588201.

[53] J.W. Grebinski, K.L. Hull, J. Zhang, T.H. Kosel, M. Kuno, Solution-based straight and branched CdSe nanowires, Chem. Mater. 16 (25) (2004) 5260–5272. http://dx.doi.org/10.1021/cm048498h http://arxiv:hepth/0511259arxiv:hepth/10.1021/cm048498h.

[54] K.L. Hull, J.W. Grebinski, T.H. Kosel, M. Kuno, Induced branching in confined PbSe nanowires, Chem. Mater. 17 (17) (2005) 4416–4425. http://dx.doi.org/10.1021/cm050952+.

[55] D.J. Milliron, S.M. Hughes, Y. Cui, L. Manna, J. Li, L.-W. Wang, A. Paul Alivisatos, Colloidal nanocrystal heterostructures with linear and branched topology, Nature 430 (6996) (2004) 190–195. http://dx.doi.org/10.1038/nature02695.
[56] S. Mandal, A. Dhar, S. Ray, Growth and photoluminescence characteristics of ZnO tripods, J. Appl. Phys. 105 (3) (2009), http://dx.doi.org/10.1063/1.3074094 033513–033513-6.
[57] Y. Jun, S. Lee, N. Kang, J. Cheon, Controlled synthesis of multi-armed CdS nanorod architectures using monosurfactant system, J. Am. Chem. Soc. 123 (21) (2001) 5150–5151.
[58] A. Koma, van der Waals epitaxy for highly lattice-mismatched systems, J. Cryst. Growth 201–202 (0) (1999) 236–241. http://dx.doi.org/10.1016/S0022-0248(98)01329-3, URL 〈http://www.sciencedirect.com/science/article/pii/S0022024898013293〉.
[59] S.H. Wolff, S. Wagner, J.C. Bean, R. Hull, J.M. Gibson, Hydrogen surface coverage: raising the silicon epitaxial growth temperature, Appl. Phys. Lett. 55 (19) (1989) 2017–2019. http://dx.doi.org/10.1063/1.102149.
[60] J. Belk, C. McConville, J. Sudijono, T. Jones, B. Joyce, Surface alloying at InAs–GaAs interfaces grown on (001) surfaces by molecular beam epitaxy, Surf. Sci. 387 (1–3) (1997) 213–226. http://dx.doi.org/10.1016/S0039-6028(97)00355-5.
[61] G.S. Higashi, Y.J. Chabal, G.W. Trucks, K. Raghavachari,Ideal, hydrogen termination of the Si(111) surface, Appl. Phys. Lett. 56 (7) (1990) 656–658. http://dx.doi.org/10.1063/1.102728.
[62] U. Neuwald, H. Hessel, A. Feltz, U. Memmert, R. Behm, Wet chemical etching of Si(100) surfaces in concentrated NH_4F solution: formation of (2x1)h reconstructed Si(100) terraces versus (111) facetting, Surf. Sci. Lett. 296 (1993) L8.
[63] J. An, Y. Shi, Z. Liu, R. Cui, T. Sun, T. Chen, J. Wang, X. Xu, J. Wang, J. Huang, X. Li, C. Wu, J. Du, The Influence of NH_4F on Silicon Etching in $HF/HNO_3/H_2O$ System, Vols. I–V, Springer, Berlin, Heidelberg, 2009. http://dx.doi.org/10.1007/978-3-540-75997-3-204.
[64] L. Jones, G. Taylor, F.-X. Wei, D. Thomas, Chemical etching of silicon: smooth, rough, and glowing surfaces, Progr. Surf. Sci. 50 (1–4) (1995) 283–293. http://dx.doi.org/10.1016/0079-6816(95)00062-3.
[65] R. Hull, Properties of Crystalline Silicon, Institution of Engineering and Technology, Stevenage, 1999.
[66] V.P. of the International Symposium (Ed.), Cleaning Technology in Semiconductor Device Manufacturing, Electrochemical Society, New Jersey, 2004.
[67] S. Moss, A. Ledwith, Chemistry of Semiconductor Industry, Springer, Berlin, 1989.
[68] R.V. Kukta, Mechanics of quantum-dot self-organization by epitaxial growth on small areas, J. Appl. Mech. 77 (4) (2010) 041001. http://dx.doi.org/10.1115/1.4000903.
[69] C. Hedlund, H.-O. Blom, S. Berg, Microloading effect in reactive ion etching, J. Vac. Sci. Technol. A 12 (4) (1994) 1962–1965.
[70] G.S. Oehrlein, Dry etching damage of silicon: a review, Mater. Sci. Eng.: B 4 (1–4) (1989) 441–450. http://dx.doi.org/10.1016/0921-5107(89)90284-5.
[71] Y.J. Chabal, G.S. Higashi, K. Raghavachari, V.A. Burrows, Infrared spectroscopy of Si(111) and Si(100) surfaces after HF treatment: hydrogen termination and surface morphology, J. Vac. Sci. Technol. A 7 (3) (1989) 2104–2109. http://dx.doi.org/10.1116/1.575980.
[72] Y. Chabal, L. Feldman, Silicon surface and interface issues for nanoelectronics, Electrochem. Soc. Interface 14 (2005) 31.