Mixed-Signal Power System Emulator Extension to Solve Unbalanced Fault Transient Stability Analysis

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***Abstract*— This paper presents the extension of a platform originally devoted to symmetrical transient stability analysis, into the domain of unbalanced faults. The aim of this solver is to increase the speed of dynamic stability assessment for power systems. It is based on an analog representation of the grid alongside dedicated digital resources for the simulation of the models of power network components. Using the symmetrical components theory, this platform can be adapted to handle unsymmetrical disturbances, such as single-phase-to-ground faults, and the tripping of single-phase circuit breakers.**

Keywords—mixed analog digital circuits; power system dynamics; power system stability; programmable circuits.

I. INTRODUCTION

Transient stability analysis has always been key to power system studies. In recent years, this has been further solidified by the ever increasing volatility of the power system as it is shaping in the advent of the emerging smart grid. One of the most challenging research opportunities in the field of transient simulation arises in the reduction of the required computational time. Computational requirements become even more crucial as new business and operational models dictate the use of closed-loop real-time analysis and control.

The work presented in this paper is based on the dedicated mixed-signal hardware platform presented in [1]. This platform can be interfaced to co-engineered PC software and acts as a hardware accelerator dedicated to the simulation of power systems. In it, the interconnection elements of a power system, e.g. transmission lines, are mapped onto a reconfigurable analog grid that acts as a fully parallel *analog* computer that solves the matrix equations of the system. This matrix operation (1) links the voltages ($\underline{U}$) to the current injections ($\underline{I}$) at the nodes of a power system of n nodes. $\underline{Y}$ is the admittance matrix.

$$[\underline{I}_i]_{(i=1\ldots n)} = [\underline{Y}_{ij}]_{(i=1\ldots n)*(j=1\ldots n)} * [\underline{U}_j]_{(j=1\ldots n)} \qquad (1)$$

The equations of the models of the components that constitute the nodal injections, e.g. generators and loads, are handled by dedicated *digital* computing hardware that is interfaced to the analog part through an array of analog to digital (A/D) and digital to analog (D/A) converters. This architecture achieves massive parallelization, and hence greatly overperforms traditional software solvers that run on general-purpose computer hardware (three orders of magnitude faster for n-1 dynamic stability assessment (DSA) reported in [2]).

The motivation for the extension of this work comes from the fact that in the existing system an assumption is made that all the analyzed phenomena are balanced in nature. Unfortunately this assumption is very restrictive in power system stability studies, since a lot of unbalanced electrical phenomena do exist, such as unequal phase faults or unbalanced loads. Thus, a modification of the existing system to perform unbalanced fault analysis is of large interest.

This paper is organized as follows. The next chapter exposes the motives of adapting the existing platform for unbalanced fault analysis. Sections III and IV cover the concept and the realization of a power system transient stability analyzer based on power grid analog emulation. Section V is devoted to the solution of adapting the existing prototype to study unbalanced phenomena. Section VI is an overview of the next generation prototype that will take advantage of integrated circuit technologies. Section VII incorporates transient stability results of balanced and unbalanced faults analysis using the dedicated platform and compares it with a purely digital solver implemented in Matlab.

II. NEED FOR UNBALANCED FAULT MODELING

They are two main types of unbalanced faults in transmission lines, namely shunt and series imbalances. This paper considers only short-circuit (shunt) connections, while open-phase (series) faults are omitted for simplicity reasons. However, most conclusions of this document can be applied to series imbalances identically.

A. Importance of Unbalanced Fault Current Quantities

Three-phase-to-ground short-circuits and three-phase clear of ground short-circuits are the only two types of balanced faults that can occur in power systems. All the remaining short-circuit faults are unbalanced.

A first reason to represent unbalanced faults is linked to the design of protection equipment. Indeed, the critical clearing time of single-phase faults is an important information used to define the characteristics of single-phase protections in the power system. Additional useful unbalanced fault variables are the resulting negative sequence and zero sequence currents. These currents do not appear in balanced faults, since the overall system stays balanced even during the perturbation. Negative sequence currents created by the existence of an unbalanced area in the network can for instance, increase the fatigue of the rotor of synchronous machines due to heating. Again, this value is used to design system protection schemes.

A second motivation is that unbalanced short-circuit currents can be detected by ground relays. These devices operate on the measurement of zero sequence current value. Unbalanced fault analysis helps therefore the setting of the breaking threshold current of these protective units [3].

B. *Occurrence of Insulation Faults*

While three-phase-to-ground faults are generally the most harmful insulation failures that can happen in power systems, their rate of occurrence is relatively low with respect to other types of insulation faults. Considering overhead lines only, the literature provides occurrence rate of about 5% for three-phase faults [4-5], against 95% for the remaining single-phase-to-ground, double-phase-to-ground, and phase-to-phase faults. This means that the majority of insulation failures are unbalanced in nature.

III. MIXED-SIGNAL EMULATION CONCEPT

A. *The High Speed Challenge*

The mixed-signal platform of [1], mentioned earlier in this paper, has been motivated by the relatively low solving speed of conventional digital power system simulators. Nowadays, this drawback is becoming more and more pronounced, since many power networks studies attempt to achieve real-time execution performance. Our research has been oriented towards decreasing the computation time of a common power system stability simulation. Transient stability analysis (TSA) has been taken as a benchmark for validating the concept on which the tool is based.

In order to reduce the time spent for such an analysis, one needs to understand and to highlight the speed limiting process of a time domain simulation. Fig. 1 shows a synoptic view of the operations requested for such a study. The solution of two key equation sets is needed, respectively for:

- the models of the components connected to the grid,
- the model of the grid.

The component models are described by differential algebraic equations that are independent for each element. Therefore, they can be solved numerically in parallel, fact that allows the optimization of resource utilization. On the contrary, the modeling of the grid requires a large matrix operation that represents the interconnections of the nodes of the network. Its complexity increases with the size of the system and parallel implementations are hindered by high degrees of data dependency in the operations. The latter is the limiting process for conventional digital simulators in terms of speed.

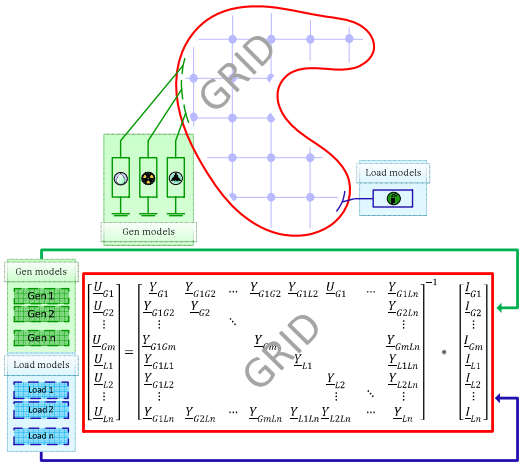

Fig. 1. Synoptic view of transient stability analysis operations

B. *Grid Analog Representation*

In order to reduce the time spent for the grid matrix operation, it was demonstrated in [6-8] that an *emulation* of the grid using analog dedicated components was of great interest. It allows a physical representation of the grid as an alternative to using a mathematical abstract model. We can therefore expect an almost instantaneous solution of the grid equation due to the physical nature of the emulator. However, the accuracy of the analog components and their capability of representing accurately the power grid is a key challenge that needs to be addressed.

A single phasor representation is used to emulate the power network grid, considering a fully balanced system. The coordinate method is based on a *phasor emulation approach* [1] that describes voltage and current using complex notation. The transmission lines are considered as their equivalent π-line model. We develop (1) by separating the admittance matrix $\underline{Y}_{ij}$ in a real part (G_{ij}) and an imaginary part (B_{ij}).

$$\begin{aligned} \underline{I}_i &= Re\{\underline{I}_i\} + j * Im\{\underline{I}_i\} \\ &= \underbrace{\sum_{j=1}^{n} (\boldsymbol{G}_{ij} * Re\{\underline{U}_j\})}_{Network\ 1} + \underbrace{\sum_{j=1}^{n} (\boldsymbol{B}_{ij} * Im\{\underline{U}_j\})}_{Network\ 2} \\ &\underbrace{-j \sum_{i=1}^{n} (\boldsymbol{B}_{ij} * Re\{\underline{U}_j\})}_{Network\ 3} + \underbrace{j \sum_{i=1}^{n} (\boldsymbol{G}_{ij} * Im\{\underline{U}_j\})}_{Network\ 4} \end{aligned} \quad (2)$$

The four networks of (2) are coupled together in pairs, which renders their separated emulation difficult. However, for high voltage transmission systems, the hypothesis that the resistive part of the lines impedance is negligible with regard to the reactive one is extensively used [3-4]. Modifying (2) according to this assumption shows that the system reduces to two *uncoupled* networks.

The emulation of the grid can therefore be realized using two purely resistive networks, representing the imaginary part of the impedance of the lines. These two system representations compute respectively:

- The imaginary voltages knowing the real part of the current injection at the nodes (network 2 in fig. 2),
- The real voltages knowing the imaginary part of the current injection at the nodes (network 3 in fig. 2).

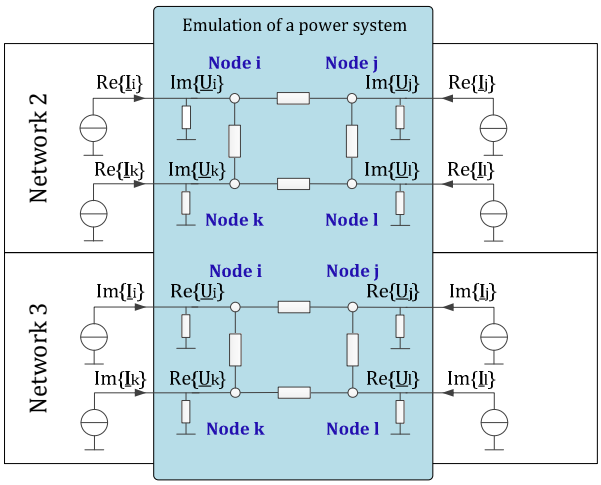

Fig. 2. Analog emulation using two uncoupled networks

C. *Models of the Components Connected to the Grid*

These models are computed using a digital processing core. The equations considered in this paper are:

- the generator swing equation (3),
- the constant impedance load equation (4).

The generator equation (3) is the classical second order differential algebraic equation used to model the electro-mechanical machine dynamic behavior. H_i and δ_i are the inertia and the rotor angle of the machine *i*, w_0 is the power system angular frequency. P_{mi} is the mechanical power that supplies the generator and P_{ei} is the active power that the generator provides to the system. The machine is represented by its Thevenin's equivalent circuit, with E' the internal voltage, and X_d' the transient reactance.

$$\frac{2 * H_i}{w_0} * \frac{d^2\delta_i}{dt^2} = P_{mi} - P_{ei}$$

$$P_{ei} = Re\{\underline{U}_i * \underline{I}_i^*\} = Re\{\underline{U}_i\} * Re\{\underline{I}_i\} + Im\{\underline{U}_i\} * Im\{\underline{I}_i\} \quad (3)$$

$$Re\{\underline{I}_i\} = \cos(\delta) * \frac{E'}{X_d'} \quad ; \quad Im\{\underline{I}_i\} = \sin(\delta) * \frac{E'}{X_d'}$$

Equation (4) is the constant impedance load model. $\underline{Y}_i$ stands for the admittance of the load *i*. This load model is widely used in the literature for transient stability analysis.

$$\begin{aligned} Re\{\underline{I}_i\} &= Re\{\underline{Y}_i\} * Re\{\underline{U}_i\} - Im\{\underline{Y}_i\} * Im\{\underline{U}_i\} \\ Im\{\underline{I}_i\} &= Re\{\underline{Y}_i\} * Im\{\underline{U}_i\} + Im\{\underline{Y}_i\} * Re\{\underline{U}_i\} \end{aligned} \quad (4)$$

IV. Existing Platform Implementation

A prototype based on the concept described in section III has been implemented and validated [1]. The platform uses mixed-signal electronics to perform TSA according to fig. 1. It has already been mentioned that the grid modeling is realized using dedicated analog electronics. The components model (generators and loads) are computed digitally using a field programmable gate array (FPGA), since their handling is less critical in terms of speed (section III-A). Reference [1] gives details about the digital computation architecture.

A. *Existing Prototype Hardware Architecture*

Fig. 3 shows the overall system architecture. The bottom part of the figure contains the two resistive networks used for the emulation of the grid. The top part depicts the FPGA implementation. It highlights the use of a pipelined architecture to simulate the models of different network components. This architecture is a tradeoff between a fully parallel implementation that is fast, but resource consuming, and a fully serial implementation that is slower, but resource sparing. The interface between digital and analog electronics is implemented using digital to analog (DACs) and analog to digital (ADCs) converters.

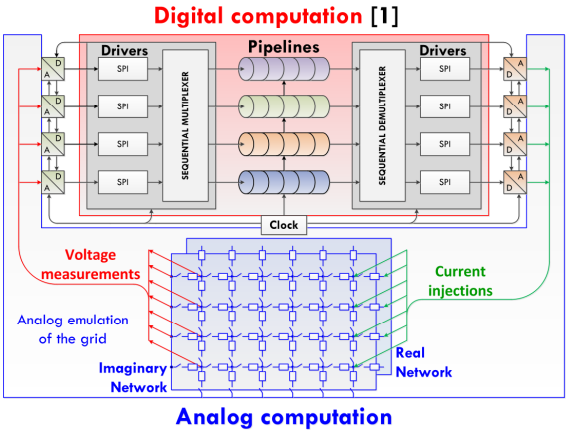

Fig. 3. Existing prototype architecture

B. *Hardware Implementation*

The architecture described above was used for the hardware design of the mixed-signal platform. Fig. 4 shows a slice of this prototype that is able to emulate up to 24 power network nodes. The analog components used to emulate the grid are highlighted in blue. They are mainly programmable resistors that represent the impedance of the transmission lines, and programmable switches that allow the connection of nodes together. The digital processing unit is colored in red. The converters allowing the translation between digital and analog data are highlighted in green and orange.

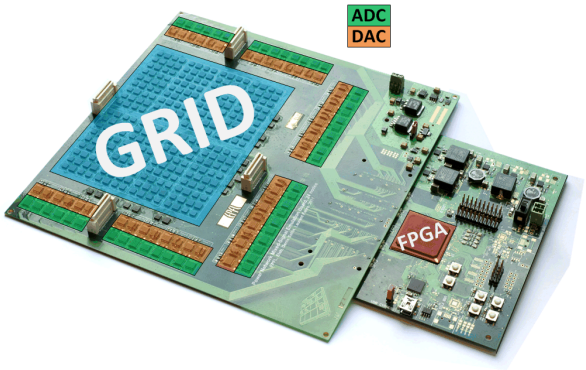

Fig. 4. One hardware slice board of the existing prototype

The final platform contains four slices such as the one described in fig. 4 that are stacked in a 3D fashion. Extension connectors allow the link between the slices. The maximum achievable size of power network representation is of 96 (4x24) programmable nodes. Fig. 5 shows a schematic view of this 3D connection used to realize the mixed-signal power network emulator.

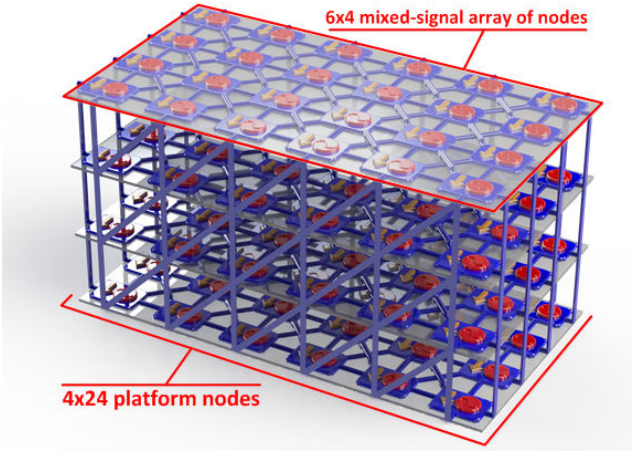

Fig. 5. 96 programmable nodes power network emulator schematic

V. Adaptation of the Existing Solver for Unbalanced Faults Analysis

A. Symmetrical Components Sequence Networks Building

The theory of symmetrical components is used to represent the effect of a faulted unbalanced point in a power system. This principle is a coordinate transformation that uses three balanced, uncoupled and separated sequence networks, namely a positive, a negative and a zero sequence to represent a power system. An unbalanced point in the system is modeled by a dedicated connection of these networks. Interested readers can refer to [4-5].

The fact that the three sequences used for the symmetrical components transformation are balanced, separated and uncoupled allow the use of the single phasor representation introduced in section III-B. We can thus dedicate each slice of our platform (fig. 4) to represent one of these sequence quantities. Using the 3D connections shown in fig. 5, slices and therefore sequences are connected together, which allows the representation of an unbalanced point in the network. Fig. 6 shows how the unbalanced platform is built.

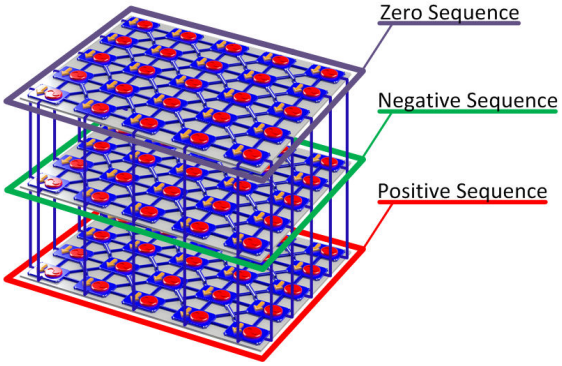

Fig. 6. Modified TSA solver for unbalanced point analysis

B. Fault Type Implementation

The sequence components are a common method to deal with fault analysis on power systems. As it was mentioned in section II-B, the majority of power system faults are unbalanced in nature, requiring a dedicated connection of the three networks, as described above. Unfortunately, as it can be seen on fig. 6, as of the current prototype, inter-slice connections are not available for all nodes of the solver. Indeed, only nodes located at the boundary of each slice can be connected with the other sequences. Thus, the point of imbalance has to be mapped at the boundary of a slice.

C. Ground Separation

Depending on the type of imbalance that needs to be represented, two or three of the sequence networks have to be connected either in series or in parallel. The parallel connection is less problematic, since the slices are already stacked in parallel and their respective grounds are connected together. Fig. 7 shows a typical parallel connection used to model a phase-to-phase fault.

However, the series connection requires separated ground level for each of the symmetrical quantities. The existing platform was not intended to be compatible with this ground

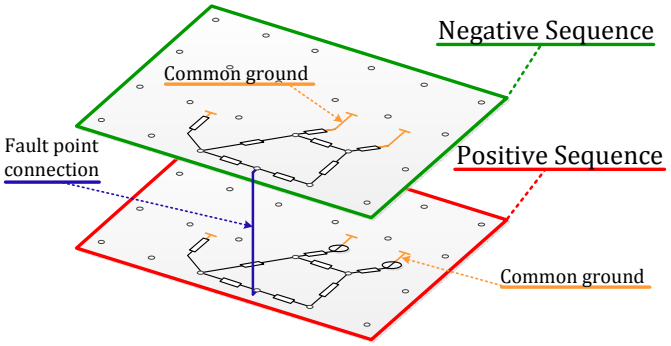

Fig. 7. Parallel connection used to model a phase-to-phase fault

level separation, as explained above. Therefore, additional nodes need to be used in order to separate for instance, the ground of the negative sequence from the ground of the positive sequence. This reduces the number of nodes available for the network representation. Fig. 8 shows this ground separation implementation for a single-phase-to-ground fault connection.

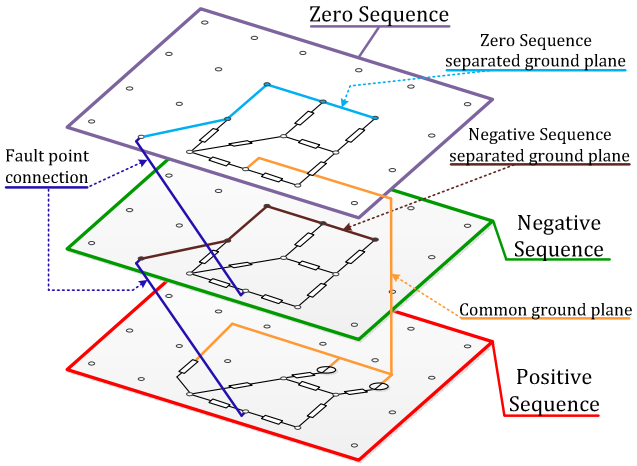

Fig. 8. Series connection used to model a phase-to-ground fault

D. Easy Access to Components Sequence Voltage

One major advantage of this way of implementing symmetrical components is that using the node voltage measurements (through the ADC), the sequence current flowing through each component of the network can be directly measured. Indeed this faithful representation of the symmetrical modeling of a power system avoids many network reduction techniques that are used in common digital solvers (Thevenin's equivalent, current distribution factors, etc.), without decreasing the processing speed of the emulator. These reduction procedures are used in conventional numerical simulators to decrease the overall system complexity by keeping the size of the admittance matrix of (1) constant. If no reduction technique is used, the size of this matrix is multiplied by two or three making it more difficult to achieve acceptable computation time. However, these simplifications come at an additional pre- and post-processing computation cost that in our case is avoided.

VI. Towards Integrated Technology Solution

A. Power Network Emulator Prototyping Flow

The existing platform described in section III is the latest version of a series of 4 prototypes developed in the frame of analog power network emulation [9]. The first two platforms contained less than eight nodes and were implemented as a proof of the concept of power grid emulation. The third one marked a first attempt to represent more realistic systems and was able to emulate sixteen nodes of real networks. The fourth prototype, described in this paper, had the target of increasing even more the size of the power systems that can be analyzed while investigating for the optimal dedicated digital processing core solution using the knowledge acquired during the development of the first three prototypes. All these platforms were using discrete analog electronics to model the grid. This kind of implementation decreases the manufacturing time and simplifies the debugging procedure. They were built as prototyping development steps towards the design of an integrated technology solution platform.

B. Benefits of Integrated Technology for this Application

The four power network emulator implementations listed above have highlighted two features that can be further optimized:

- the overall platform cost,
- the accuracy of the analog components.

The large number of discrete components used to build one slice of the existing platform (fig. 4) increases the overall cost drastically. In addition to this, the soldering process and the printed circuit board manufacturing have to be added.

Discrete electronics suffer from inaccuracies. For instance, the programmable resistors used to implement the π-line model of fig. 2 are limited to a 20% relative precision. This deviation is not acceptable when targeting high performance network analysis, since they translate directly into power flow variations. Therefore, an additional calibration step is required to reduce this effect [10].

A solution to improve the two points listed above is in using integrated circuit technologies. The latter allow large cost reduction and increase the matching between the components. However, the developing time is increased, and the debugging procedure is more complicated. These are the major reasons why this kind of implementation was not used in the development of the early prototypes.

C. Dedicated Fault Type Connection Capability

The future prototype will integrate design changes that will simplify the representation of unbalanced points in the power system. Section V-B showed that connections between the three symmetrical sequences are available only at slice boundary nodes using the existing prototype. A dedicated wiring interface is a solution to make connection of the sequence networks at each node possible. Three wires are required to enable all symmetrical sequence connections. Fig. 9 shows the concept of the three wires plane that is used in addition with programmable switches to easily represent shunt unbalanced faults.

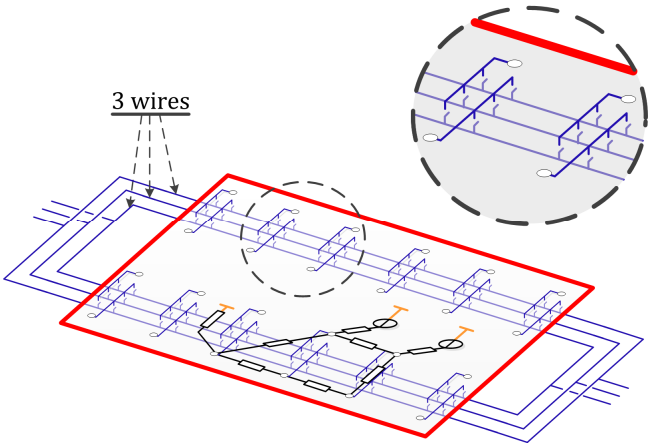

Fig. 9. Three wires interface for unbalanced fault modeling

D. Increased Power Network Size

The integrated circuit (IC) solution for the analog part of the solver allows a large increase in the number of nodes. As it was mentioned above, it offers cost reduction and better matching between the analog components. The inherent inaccuracy introduced by the analog models propagates with respect to the power system size. Therefore, the building of larger networks is simplified by the use of this technology. It allows targeting power network sizes in the order of hundreds to thousands of nodes, which cover the sizes that are found in more realistic systems.

VII. Results

To illustrate the concept presented above, a five nodes test case topology is analyzed using the mixed-signal emulator for balanced and unbalanced fault conditions. The results are compared with simulator calculations done in Matlab.

A sample software implementation has been developed that uses the sequence networks reduction technique and represents the imbalance by inserting an equivalent impedance between the fault point and the ground. Thus, the size of the matrix operation of (1) is not increased, avoiding a reduction in computation speed. However, as mentioned in section V-D, the unbalanced current flowing through each component of the network cannot be directly extracted, and for that post-analysis operations are required.

The time spent for the computation of each of the scenarios presented in this section using the mixed-signal emulator is given. It allows the illustration of the typical solving speed that can be achieved using our platform.

A. *Five Nodes Topology Test Case*

The power system under analysis is represented in fig. 10. It contains three generators, an infinite bus connection and a constant impedance load. The fault appears as a single- or multiple-phase short-circuit in the middle of the branch connecting nodes 4 and 5. For each of the cases listed hereunder, the fault details will be given.

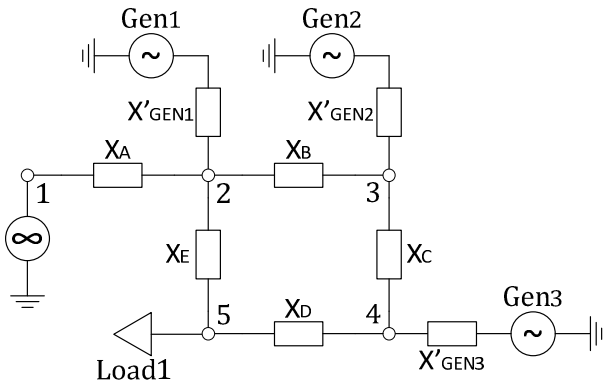

Fig. 10. Five nodes topology test case

B. *Applying the Symmetrical Components*

The dedicated modeling of the test case topology in the positive, negative and zero sequence components considers the most general rules that can be found in the literature [3-5]. Table 1 contains the values used for the five nodes power system.

The impedance of a transmission line is considered to be equal in the positive and negative sequence. The zero sequence line impedance is different, since it is a loop impedance. It is commonly considered to be equal to about three times the positive sequence value.

The load values follow the same rule with the one used for transmission lines. This is only valid when considering static wye-connected solidly grounded loads.

All the generators are considered as round-rotor machines, which leads to an equal positive and negative internal impedance. The value of the zero sequence impedance is usually very small and variable depending on the winding design. When not known, the literature [3] considers value from five to six times less than the value of the positive sequence for not solidly grounded machines.

TABLE I. Sequence impedances of the five nodes topology

Impedance	Pos-sequence value [pu]	Neg-sequence value [pu]	Zero-sequence value [pu]
X_A	0.1j	0.1j	0.3j
X_B	0.18j	0.18j	0.54j
X_C	0.1j	0.1j	0.3j
X_D	0.1j	0.1j	0.3j
X_E	0.1j	0.1j	0.3j
X_{GEN1}	0.125j	0.125j	0.025j
X_{GEN2}	0.125j	0.125j	0.025j
X_{GEN3}	0.125j	0.125j	0.025j
Z_{load}	0.27-0.09j	0.27-0.09j	0.82-0.26j

C. *Three-Phase-to-Ground Fault Analysis*

This study uses only the positive sequence of the symmetrical components, since the fault preserves the balanced nature of the system. The scenario that is applied to the power system is a three-phase-to-ground short-circuit connection appearing at the middle of the branch connecting nodes 4 and 5. The perturbation starts at time 2s and stops after 200ms.

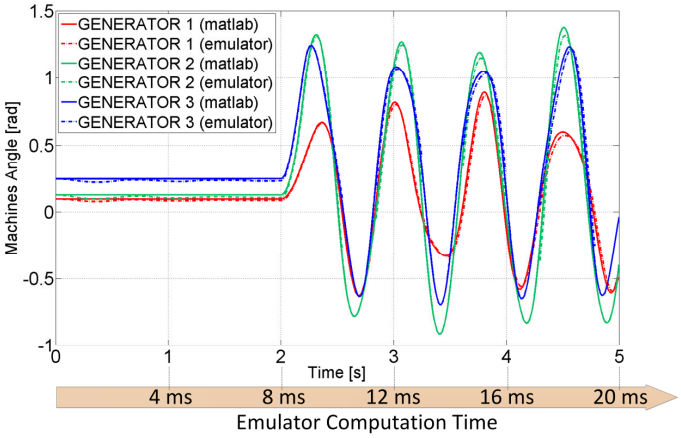

Fig. 11. Three-phase-to-ground TSA

Fig. 11 shows the results of such an analysis using the two tools mentioned in the introduction of this section. The arrow located at the bottom part of fig. 11 contains the time spent by the emulator to run such an analysis. The integration time step is 0.25ms (digital computation in fig. 3).

D. *Single-Phase-to-Ground Fault Analysis*

The use of the extended implementation of the emulator is requested to perform the analysis of the transient behavior of the system of fig. 10 in case of an unbalanced fault event, such as a single-phase-to-ground short-circuit. This particular perturbation requires a connection of the sequence networks in series (fig. 8). The Matlab simulator uses an equivalent impedance of this sequence connection that is equal to the negative and zero sequence impedance summation (fig. 12).

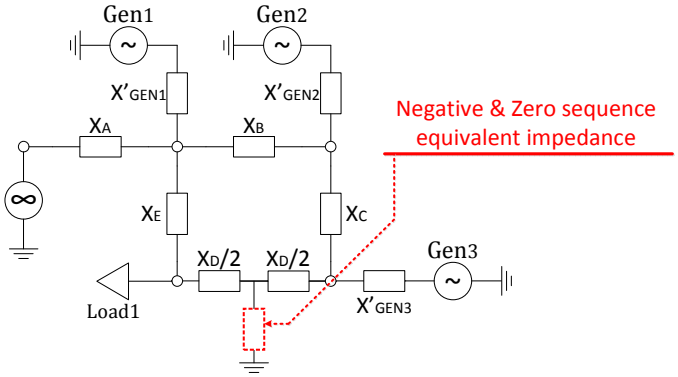

Fig. 12. Simulator single-phase-to-ground short-circuits modeling

The scenario of this fault type is the same as in section C, except that the fault occurs on a single-phase and that it stays active for 800ms. It can be observed on fig. 13 that the results computed by the emulator follow the trend of the simulated values. Slight inaccuracies can be attributed to the fact that for this analysis, no calibration of the computational analog hardware is performed. The calibration stage tries to decrease the relative error of the analog components such as

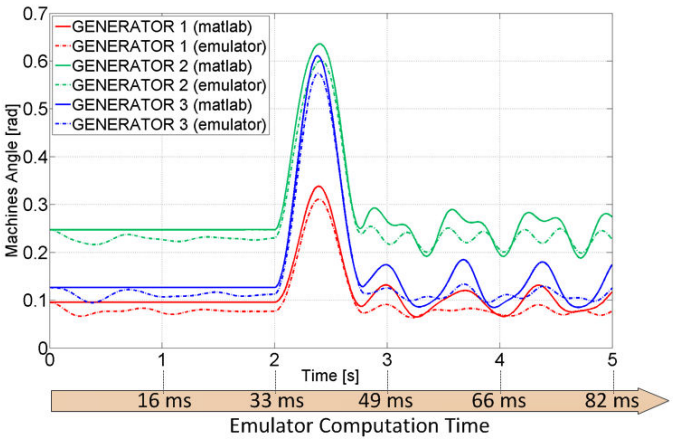

Fig. 13. Single-phase-to-ground fault TSA

programmable resistors, using a successive measurements-rectification approach. An uncalibrated analog grid leads therefore to power flow variations in the emulated transmission lines, and consequently to generator angle deviations. Reference [10] shows the effect of the analog grid calibration on generators angles results. In the same reference, details are given for the calibration procedure that has been implemented for balanced systems. There are plans to port the latter into the unbalanced version of the platform in the future.

We can observe on fig. 13 that the time spent for this analysis using the emulator is increased with respect to the previous study. The explanation to this comes from the fact that a smaller time step of about 60us was used in order to increase the accuracy of the numerical integration, since the absence of calibration already adds significant errors.

E. Computation Speed

Reference [1] contains dedicated sections on the speed capabilities of the platform presented in this paper. A comparison with the sample software that was created in Matlab would be of low interest, since this tool was developed for debug and validation purposes only. The time arrows bellow fig. 11 and 13 provide a hint on the emulator computation time for the respective scenarios.

VIII. CONCLUSIONS

This paper presented and validated the concept of a power network transient stability emulator extension to perform unbalanced faults studies. The challenges of adding the symmetrical components sequences to the simple single phasor positive sequence were highlighted and partly addressed in an overview covering a future prototype implementation. The validation of the concept was verified by comparisons of TSA results with dedicated Matlab software.

Typical information obtained in TSA studies is the critical clearing time of a particular fault occurring in a power system. This piece of information is particularly useful when selecting dedicated circuit breakers for a specific region of the network. Another reason of investing effort in the unbalanced fault representation is their property of producing either negative or zero sequence current. It is well known that, for instance, negative sequence current can cause stresses on the rotor of generating units and is therefore, very useful information when selecting and designing protection systems. Negative sequence current is also very helpful to detect line-to-line faults. Zero sequence current is of major interest when trying to detect ground faults in power systems. Therefore, ground protective relays operate on the zero sequence current.

The main advantage of using the concept of analog grid emulation to solve (1) is that the increase in the number of nodes required by the negative and zero sequence modeling does not slow down the solving speed. This comes from the fact that the solver uses the physics of the analog components to solve (1). The two scenarios presented in section VII indicate computation speeds of 250 and 60 times faster than real time respectively. A second advantage is that the solver allows direct access to the quantities of every sequence, without any additional post-analysis processing, as it is often the case with conventional digital solvers.

Open-phase faults were left out of the scope of this paper. However, they are plans to include open-phase capabilities in an improved version of the emulator. This projected improvement will particularly increase the utility of our platform for the design of protection schemes for synchronous machines.

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