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2014 IEEE 28-th Convention of Electrical and Electronics Engineers in Israel

Single Event Upset Mitigation in Low Power SRAM Design

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***Abstract*—Technology advancements in recent years have led to an increase in the employment of integrated circuits in space applications. However, these applications operate in a highly radiated environment, causing a high probability of single event upsets (SEU). Continuous transistor scaling exacerbates the situation, as susceptibility to SEUs is increased in advanced process technologies. The most vulnerable of these circuits are memory arrays that cover large areas of the silicon die and often store critical data. Accordingly, maintaining data integrity in light of SEUs has become an integral aspect of memory cell design. This paper introduces recently proposed methods for mitigating SEUs, and reviews the advantages and disadvantages of leading memory radiation hardening solutions. A brief comparison of radiation hardened bitcells is provided, based on Monte Carlo simulations in a 65 nm CMOS process under slightly scaled supply voltages.**

I. Introduction

Radiation hardening (rad-hard) design of electronic components and integrated circuits (ICs) has become an increased area of interest among VLSI research groups in recent years. Technology developments have driven continuously increasing rad-hard design efforts in modern ICs – mainly due to the fact that soft error rates (SERs) have become non-negligible, even within terrestrial environments [1]. Furthermore, technology advancement is forcing the development of new rad-hard solutions to protect hardware from single event upsets (SEUs) in order to replace the traditional solutions that are often unsuitable for low power, small area components.

Rad-hard research has been around for approximately four decades [2]. Previously published solutions can be divided into three main approaches, according to the design level at which they are integrated: architectural approaches, technology solutions, and circuit levels implementations. When designing an application intended for operation in a highly radiated environment, a significant trade-off between reliability, silicon area, power consumption, and fabrication costs must be considered. Therefore, each application should adopt the suitable approach according to the design demands, as each solution provides different advantages and disadvantages, as compared to the others.

The unequivocally most investigated component in terms of rad-hardening is the static random access memory (SRAM) cell [3]. SRAM blocks occupy the majority of the chip area and are the primary contributors to leakage power in many modern systems, including those intended for space applications [4]. These power and area trends, which are expected to continue in future systems, lead to two major conclusions. First, due to their static power consumption, scaling the supply voltage of the SRAM macros is an efficient method to reduce total chip power [5]. Second, the probability of a radiation strike on an SRAM bitcell is relatively high, due to the large area that the SRAM core occupies. However, these two conclusions contradict each other, as the sensitivity to a radiation strike grows with the reduction of the supply voltage, resulting in an increase in SER. Therefore, SRAM soft-error mitigation has become essential for robust system design [6]. When designing a cell for high-radiation environments, silicon area often takes a step back in favor of stability and soft-error suppression.

In this paper we provide a short overview of SEU modeling in SRAMs and present the leading solutions for limiting the resulting SER. While we overview several architectural and technology approaches, we focus on circuit level implementations, and provide a brief comparison between leading rad-hard bitcells and their compatibility with low-power space applications, implemented in nano-scaled process technologies.

The rest of this paper is organized as follows: Section II provides a short overview of SEU modeling, followed by a discussion of mitigation methods and popular solutions in Section III, focusing on circuit level solutions. Section IV provides a brief comparison between rad-hard bitcells and Section V concludes the paper.

II. SEU Modeling

In order to design a memory circuit capable of suppressing SEUs, it is important to first understand the phenomena leading to an error. Radiation attacks occur when an energetic particle hits and passes through a semiconductor material, potentially causing a bit-flip in the memory cell [7], [8]. The energetic particle frees electron-hole (e–h) pairs along its path in the material as it loses energy. When the particle hits a reverse-biased pn-junction, such as a transistor diffusion-bulk junction, the injected charge is transported by drift and causes a transient current pulse that changes the node voltage. Data loss occurs when the collected charge ($Q_{\rm coll}$) exceeds the critical charge ($Q_{\rm crit}$) that is stored in the sensitive node. This transient current ($I(t)$) is characterized by a fast rise time (t_r) and a gradual fall time (t_f), according to the double exponential model [9]:

$$I\left(t\right)=\frac{Q_{coll}}{t_f-t_r}\left(e^{-\frac{t}{t_f}}-e^{-\frac{t}{t_r}}\right), \quad (1)$$

where $Q_{\rm coll}$ depends on the type, trajectory, energy value, and impact location of the ionizing particle, and t_r and t_f are technology dependent.

The total charge deposited by a particle strike can be calculated by numerically integrating the transient current pulse, and $Q_{\rm crit}$ is defined as the minimum charge deposited in a sensitive

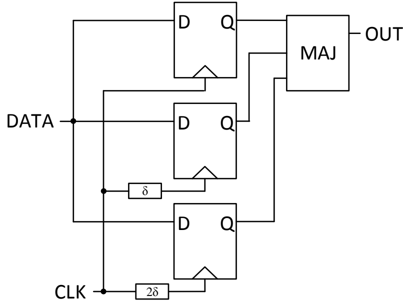


Fig. 1. The TMR Temporal Sampling implementation.

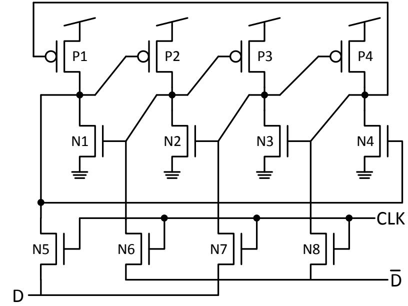


Fig. 2. The DICE bitcell.

node that results in a memory bit-flip [10]. Technology scaling is accompanied by the reduction of Q_{crit}, which leads to an increase in SER [11]. This, in turn, makes radiation hardening more challenging in advanced technologies. Simulation of a particle strike with the SEU model of (1) is the most popular technique for evaluation of the rad-hardening ability of an SRAM bitcell, and is therefore, the basis for the comparisons provided in Section IV.

III. SEU Mitigation Methods

A variety of techniques have been implemented in order to mitigate and prevent SEUs according to the SEU model, presented in Section II. This section presents several of these solutions, divided into the three, previously mentioned, major approaches: architectural level, technology level, and circuit level solutions.

A. Architectural Solutions

The main approach to soft-error mitigation over the past two decades has been to provide full immunity to single soft-errors through circuit redundancy. Circuit redundancy schemes, such as triple modular redundancy (TMR) and dual modular redundancy (DMR), can offer several orders-of-magnitude improvement in soft-error reduction, by replicating identical circuit elements. These approaches assume that a particle strike will only affect some, but not all circuit elements, which enables the circuit to recover from partial failure by voting on the results of each replicated element. These circuit redundancy schemes can make sequential circuits immune to SEUs or single errors due to radiation strikes affecting a circuit node.

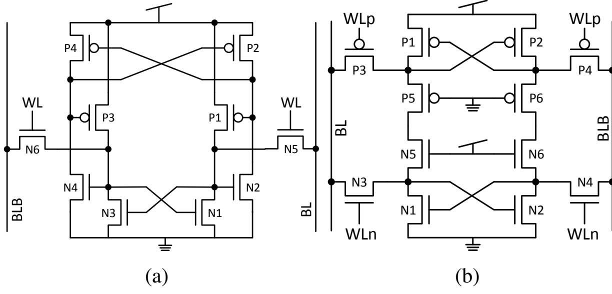
1) Triple Modular Redundancy: The most popular technique in use today involves replicating a storage node three times and adding a three-input majority gate to filter out unwanted SEUs. This technique assumes that the probability of a particle strike at two separate places on the chip within a defined timespan is extremely low. When a single error occurs at any of the three storage nodes, a three-input majority gate acts as a voting circuit to recover the correct value.

Two common TMR implementations are *spatial sampling* (SS) the *temporal sampling* (TS). The SS implementation simply uses three identical cells for redundancy, while the TS implementation, illustrated in Fig 1, also uses delay elements in order to protect against SEUs on the clock and data inputs. Three versions of the sampling clock can be created by incorporating delay elements with delays of δ and 2δ. TS can prevent SEUs of widths smaller than δ on the clock and data inputs from simultaneously corrupting the three storage elements, since each latch samples at clock edges separated by δ. TS can also be incorporated directly into the latch structure by replicating the storage node and implementing similar delay elements internally.

TMR is popular among ASIC and FPGA designers, since it does not introduce any new circuit elements to the existing standard cell library. However, TMR requires an increase in both area and power of at least $3\times$. In addition, TMR institutes a non-negligible delay overhead, due to the triplication of the sequential cells and the addition of the delay elements and majority gate.

2) Dual Modular Redundancy: As its name suggests, DMR is a similar solution to TMR, implemented with dual, rather than triple, redundancy. By integrating non-standard logic gates and SRAM cells, DMR can provide approximately the same soft-error resilience as TMR, albeit with a significant reduction in the resulting area and power overheads. A rich assortment of techniques has been proposed to implement DMR [12]–[14]; however, their incorporation into the standard ASIC design flow has been limited, due to the reluctance of vendors to provide specialized circuit designs outside the standard cell library. One example of of a bitcell that can be implemented in this method is a zero-hardened cell, *i.e.* a cell that is fully hardened against '0' to '1' flips. A-priori knowledge of such a cell's failure characteristics, enables duplicating the array instead of triplicating it, while providing the same resilience. Note that DMR can also be implemented in sequential cell design for further system rad-hardening [15].

3) Error Correction Codes: Another architectural level solution is the integration of error correction code (ECC) circuits. ECCs implement a known algorithm through a fully synthesizable design to provide an efficient and easy to use rad-hardening solution. For large memory arrays, ECCs can replace the need for individually hardened memory cells, as will be presented, as part of the circuit level solutions. However, this comes at a relatively large area and power cost. For example, single error correct - double error detect (SECDED) ECC incurs an overhead of 8 bits per 64 bits of data and requires a XOR gate based logic circuit in order to implement the ECC algorithm. In addition, ECC requires extra



(a) (b)

Fig. 3. (a) The Quatro-10T radiation hardened SRAM. (b) The 12T improvement.

cycles to verify the data, resulting in a substantial performance penalty. Therefore, such an approach is less-suitable for ultra low power (ULP) applications, where longer timing paths will further impair already deteriorated performance.

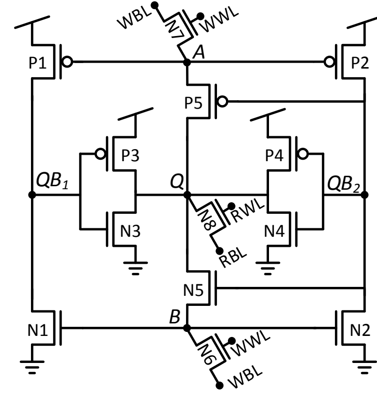
B. Technology and Packaging Solutions

A key process technology that can help reduce the SER is silicon-on-insulator (SOI). Unlike bulk CMOS, SOI devices collect less charge from an alpha or neutron particle strike, due to the significantly thinner silicon layer. IBM reports a 5× reduction in the SER of SRAM devices in their partially-depleted SOI technology [16]. Similarly, other process based solutions such as higher doping of the p-well and triple-well processes can provide some additional protection from radiation strikes. However, modifications to the process often incur significant fabrication costs that may not be tolerated in volume manufacturing.

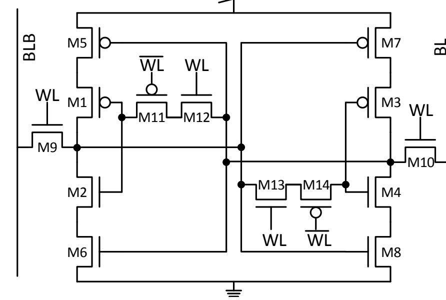
An additional method to reduce the exposure of a circuit to radiation, is to shield it with several thick metal layers, thereby altering the energy and concentration of incoming particles. However, the payload considerations of a spacecraft limit the thickness of the shielding metal, and increasing the thickness of the shielding results in diminishing returns beyond a particular thickness [17]. In fact, thick shielding can actually increase the SER, as secondary particles are generated when incoming particles pass through the shielding. One example of this is Bremsstrahlung radiation in the form of x-rays that is emitted when energetic electrons decelerate in the shielding. Therefore, while still one of the common methods to protect from SEUs, shielding is often insufficient on its own.

C. Circuit Level Solutions

Circuit-level rad-hardening solutions often include modification of the SRAM bitcell in order to achieve improved robustness to SEUs. The conventional 6T SRAM memory cell utilizes an active feedback loop between cross-coupled inverters in order to retain its stored data value. This circuit is very sensitive to SEUs, as any upset that causes one of the data nodes to cross the switching threshold of the adjacent inverter will result in a bit flip. This failure risk increases with process scaling, and therefore, many alternative SRAM circuits have been proposed in recent years. Recently proposed rad-hard designs include the temporal latch [18], DICE [19],



(a) The 13T radiation hardened SRAM.



(b) The SHIELD SRAM.

Fig. 4. Rad-hard bitcells targeted at low-power applications.

the Quatro-10T and 12T bitcells [21], [22], the 13T sub-threshold bitcell [20], and SHIELD [23]. These solutions can be fabricated in commercially available state-of-the-art manufacturing processes at the expense of an increase in the silicon area of the bitcell.

1) DICE: The dual interlocked storage cell (DICE), is the best known SEU hardened bitcell. The concept of the DICE design is using the DMR of its internal circuit nodes to achieve immunity to errors affecting a single node. This is achieved with 12 transistors, implementing a dual node feedback control mechanism, as seen in Fig. 2. The storage element utilizes four internal circuit nodes to store one memory bit. When a single event temporarily upsets one of these four nodes, only one additional node is affected by the upset through positive feedback. In this way a single node upset (SNU) will not propagate the error to the other nodes, and the unaffected nodes can correct the circuit value. However, it still remains sensitive to multi-node upsets (MNU) and also suffers from high power consumption, due to its many transistors and leakage paths. Additionally, the cell recovery time severely increases with supply voltage scaling, making the DICE bitcell inefficient for ULP operation.

2) Quatro-10T and 12T Rad-hard Bitcells: The authors of [21] proposed a quad-node, ten transistor, soft-error tolerant SRAM bitcell for robust operation in high-radiation environments. As opposed to the DICE, which relies on four access transistors, the 10T bitcell uses only two access transistors for functionality, as can be seen in the circuit schematic of

TABLE I
COMPARISON OF Q_{crit} VALUES

SEU Simulation	6 T	Quatro-10 T [24]	DICE [15]	SHIELD [23]
Q_1:'1' →'0'	2.2 fC	>1 pC	>1 pC	>1 pC
Q_1:'0' →'1'	5.6 fC	3.7 fC	>1 pC	>1 pC
Q_2:'1' →'0'	-	2.5 fC	>1 pC	NP
Q_2:'0' →'1'	-	>1 pC	>1 pC	>1 pC
Q_{crit}	2.2 fC	2.5 fC	>1 pC	>1 pC

NP - Not Possible (Junction is not reverse biased)

Fig. 3(a). This decreases the area and the leakage current of the bitcell through the access transistors, but results in a much higher write access time, and requires careful sizing for functionality. In spite of the multiplication of the storage data nodes, the 10T bitcell still has a sensitive node that can flip it after a radiation particle hit. While it still provides an advantage over the standard 6T SRAM bitcell in terms of SEU rate, it is mainly a candidate for sea-level SEU hardening, as its error resilience is insufficient for space applications. Accordingly, the authors of [22] proposed adding two additional devices to the 10T cell to improve its SEU tolerance. In the improved 12T design, shown in Fig. 3(b), transistors P5, P6, N5, and N6 are always turned on, thereby acting as a low pass filter to reduce the magnitude of a transient pulse. This limits the amplitude of the noise pulse, ensuring that one side of the symmetric cell will always have approximately the same potential on the drain and body of one of its devices, which provides immunity to SEUs. The main disadvantage of the 12T bitcell is its high static power consumption, caused by the four always-on middle transistors, P5, N5, P6 and N6, and the four weakly gated lateral transistors, P1, N1, P2 and N2. Consequently, the 12T cell is unsuitable for use in low power applications.

3) The 13T and SHIELD: While all of the previously proposed rad-hard bitcells were designed for error resilience under nominal supply voltages, the circuits proposed in [20] and [23] specifically target ULP space applications, operated at scaled voltages. The 13T bitcell, shown in Fig. 4(a), achieves radiation hardening by employing a dual-feedback, separated storage mechanism to overcome the increased vulnerability due to supply voltage scaling. The storage mechanism of this circuit comprises five separate nodes: Q, QB_1, QB_2, A, and B, with the acute data value stored at Q. This node is driven by a pair of CMOS inverters made up of transistors N3, P3, N4, and P4 that are respectively driven by the inverted data level, stored at QB_1 and QB_2. QB_1 and QB_2 are respectively driven to V_{DD} or *GND* through devices P1, P2, N1, and N2 that are controlled by the weak feedback nodes, A and B, that are connected to Q through a pair of complementary devices (P5 and N5) gated by QB_2. By driving the acute data level with a pair of equipotentially driven, but independent, inverters, a strong, dual-driven feedback mechanism is applied with node separation for SEU protection. This setup effectively protects Q from an upset on QB_1 or QB_2, while achieving a high critical charge at node Q. The 13T bitcell was shown

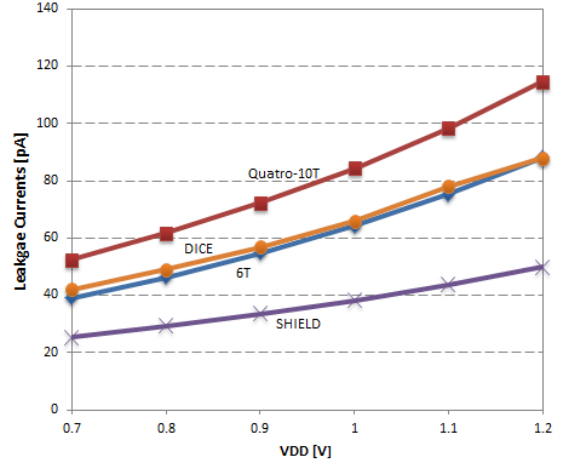


Fig. 5. Comparison of leakage currents of different bitcells across a range of supply voltages.

to be fully functional at sub-threshold voltages in [20] for an 0.18 μm implementation.

Another approach to ULP rad-hard operation is taken by the SHIELD bitcell [23], shown in Fig. 4(b). This bitcell uses a pair of gated inverters (M5-M1-M2-M6 and M7-M3-M4-M8) to mitigate SEUs. These inverters incorporate an additional input gate that dynamically latches the previous output state when the primary and secondary inputs are different. A pair of these gated inverters is cross-coupled through a cut-off network (M11-M12 and M13-M14) to provide radiation tolerance. This results in two sets of separate dual-data nodes, which exhibit high SEU tolerance under scaled supply voltages.

IV. SEU IMMUNITY COMPARISON

The previous section presented the various approaches to SEU mitigation, concentrating on the leading rad-hard bitcells that have been proposed in recent years. Each of these circuit level solutions incorporates a different and unique approach, leading to inherent deviations between the behavior and efficiency of the various designs. In this section, a brief comparison between the previously presented bitcells is provided to evaluate the efficiency of these solutions as a rad-hard bitcell in a low-power application, fabricated in a modern process technology. For the purpose of this comparison, all circuits were implemented in a standard CMOS 65 nm technology and operated at a slightly scaled, 700 mV operating supply.

To measure the SEU tolerance of the circuits, positive and negative particle strikes were applied to each of the internal data nodes of the cells. These strikes were emulated according to the double-exponential model, previously shown in (1). For each type of disrupt event, 1000 MC samples, taking into account both local and global variations, were simulated. Table I presents the SEU tolerance of four bitcells – the standard 6T, the DICE [15], the Quatro-10T [24], and the recently proposed SHIELD cell [23]. Assuming a natural space environment with a charge deposition of 1 pC [25], the results show that the DICE and SHIELD circuits are both suitable

candidates, while the 6T and Quatro-10T cells do not provide sufficient immunity.

A second aspect of comparison is leakage power, which has become the primary source of power dissipation at scaled technology with large amounts of on-chip memory. The leakage currents of the simulated bitcells are presented in Fig. 5 for supply voltages ranging from 0.7 V–1.2 V. All curves represent mean values interpolated from 1 k MC samples. For the purpose of simulation, bit-lines were pre-charged to worst case scenario voltage levels, opposite of the level stored in the adjacent data node. The results clearly show the advantage of using the SHIELD implementation, which displays the lowest leakage power across the full range of voltages, due to the use of gated inverters. While the Quatro-12T cell provides the required >1 pC resilience for space applications, its leakage power was much higher than all other considered bitcells, and therefore it was removed from this comparison, as it is not a viable candidate for low-power implementations.

V. Conclusion

This paper presents a brief review of the leading solutions to the inherent challenges of designing embedded memories for operation in highly radiated environments, such as those encountered by space applications. While standard 6T-based SRAM arrays are insufficient for SEU tolerant operation in such environments, the system immunity can be improved by incorporating solutions at the technology, architecture, and/or circuit levels. In this review, we chose to focus on several circuit level solutions to provide inherent SEU tolerance, without the overheads of architectural solutions or the additional costs of technology solutions. Several alternative bitcells were overviewed, including a discussion of their advantages and disadvantages, when targeting ultra-low power operation in high-radiation environments. Simulation results show that both the DICE and the recently proposed SHIELD bitcells are worthwhile candidates for rad-hard operation in modern technologies with scaled supply voltages.

Acknowledgment

This work was supported by Israeli Ministry of Science and Technology under grant number 9081.

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