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Low-Power and Compact Successive Approximation ADC for Bio-Electronic Chips

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Abstract

For both the electrical stimulation and recording of cultured neurons, the CMOS-based microelectrode arrays (MEAs) are one of the most promising electronic devices used nowadays. To ensure a robust transmission of the information between the chip and external devices, the MEA chip requires integrated analog-to-digital converters (ADCs). Moreover, the presence of a large number of read-out channels on chip poses stringent requirements on both area and power consumption for the design of the ADCs. Thus, this Master's thesis work proposes a low-power and compact successive approximation register (SAR) ADC for such bio-electronic chips.

In this thesis, some low-power ADC topologies are first investigated and the SAR ADC is finally chosen, that is the optimum solution for the application. The choice of multiplexing the read-out channels of the MEA chip for the analog-to-digital conversion is then presented while the requirements for the ADC are derived. In this work, the design of each part of the converter is described, starting from the switched-capacitor array which is usually used as a sample and hold (S/H) as well as a digital-to-analog converter (DAC). The size of the switches that are providing the signals to the DAC is optimized considering the timing requirements. Furthermore, low power solutions are proposed for the comparator while good performances are achieved for both noise and speed. A successive approximation register logic is finally used to provide the digital control signals.

The performance of the SAR ADC is evaluated with post-layout simulations. All the preliminary requirements are met and the proposed converter represents a promising solution for low-power applications. In conclusion, the specifications of the entire data-conversion system are compared with the ADCs currently implemented on the MEA device and a possible improvement of the chip is presented.

Key words: Microelectrode Array (MEA), Switched-Capacitor (SC) Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC), Low-Power, Split Capacitor Array, Offset Cancellation.

Sommario

Fra i dispositivi che permettono la stimolazione e la misura dell'attività elettrica di colture neuronali, i CMOS microelectrode array (MEA) sono una delle migliori soluzioni utilizzate oggigiorno. Per una sicura trasmissione di informazioni dal chip ai dispositivi esterni, il dispositivo MEA richiede convertitori analogico-digitali (ADC) da integrare nel chip. In particolare, la progettazione di tali circuiti deve essere eseguita limitando il consumo di area e potenza in quanto il numero di canali di lettura integrati è elevato. Per questo motivo, la presente tesi propone un ADC ad approssimazioni successive (SAR) compatto e a basso consumo di potenza per chip bioelettronici.

In questa tesi, diverse tipologie di ADC a risparmio di potenza sono inizialmente investigate e il modello SAR è infine scelto, in quanto dimostra di essere la soluzione ottimale per l'applicazione studiata. La scelta di utilizzare il multiplexing dei canali di lettura per la conversione analogico-digitale è quindi presentata assieme alle specifiche dell'ADC. La progettazione di ogni componente elettronico del convertitore è poi descritta, iniziando dall'array a capacità commutate che è usato sia come sample and hold (S/H), sia come convertitore digitale-analogico (DAC). Le dimensioni degli interruttori che forniscono i segnali al DAC sono ottimizzate considerando le specifiche del tempo di assestamento. Una soluzione a basso consumo di potenza è proposta per il comparatore e un registro ad approssimazioni successive è usato per generare i segnali digitali di controllo.

Le prestazioni dell'ADC SAR sono valutate con simulazioni post-layout. Tutte le specifiche stabilite sono soddisfatte e il convertitore proposto rappresenta una promettente soluzione per applicazioni a basso consumo di potenza. La performance dell'intero sistema di ADC integrabile nel dispositivo MEA è dunque confrontata con quella degli ADC a singola rampa al momento implementati sul chip e un possibile miglioramento del dispositivo è presentato.

Parole chiave: Microelectrode Array (MEA), Convertitore Analogico-Digitale (ADC) ad Approssimazioni Successive (SAR) a Capacità Commutate (SC), Basso Consumo di Potenza, Array a Capacità Commutate, Cancellazione dell'Offset.

Chapter 1

Introduction

1.1 Motivation

The CMOS-based microelectrode arrays (MEAs) [1] are sophisticated devices, which can be used to bidirectionally communicate with cultured neurons. They can perform measurements at a high spatial and temporal resolution, which is hardly achievable with passive MEAs. A switch-matrix-based high-density MEA chip [2] has been developed at Bio Engineering Laboratory of ETH Zürich. With the switch-matrix scheme, an arbitrary subset of around 11'000 electrodes can be selected for recording and stimulation. By placing the front-end amplifiers outside the array, a high signal-to-noise ratio (SNR) has been achieved together with a subcellular spatial resolution.

To ensure robust and stable transmissions of the information between the chip and other devices on the printed circuit board (Figure 1.1), the amplified and filtered neural signals are usually digitized by on-chip analog-to-digital converters (ADCs). The number of neural signals which can be recorded simultaneously is limited by the number of read-out channels integrated on the chip, hence, in order to observe the electrical activity of a large scale neural network, the 126 read-out channels of the previous design are not sufficient. Therefore, the new version of the chip integrates much more channels, posing stringent area and power consumption constraints on the individual read-out channel and ADC.

1.2 MEA Chips Developed at BEL

1.2.1 Interfacing Electrogenetic Cells *in Vitro* with CMOS Microelectrode Arrays

Complementary semiconductor-metal-oxide (CMOS) technology is a very powerful technology used to realize substrate-integrated microelectrode arrays. These devices are arrangements of electrodes that can be more or

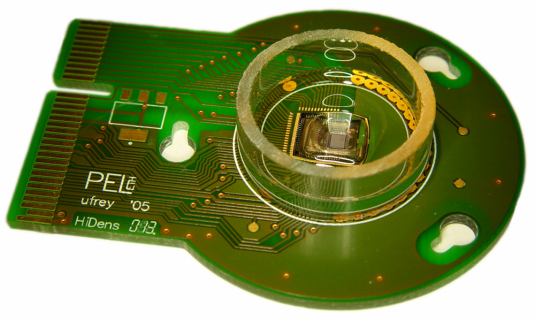

Figure 1.1: Packaged MEA chip on a custom-designed printed circuit board.

less directly interfaced to electrogenetic cells, like heart or brain cells. It is therefore possible to study fundamentals of learning processes and assess the behavior of electrogenetic cells *in vitro* by culturing or placing them directly atop the electronic chips, as shown in Figure 1.2.

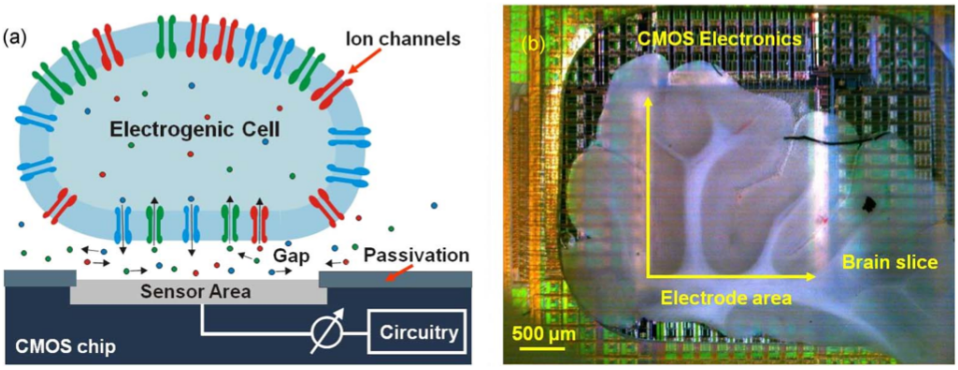

Figure 1.2: (a) Schematic of a cell attached to a sensor surface. (b) Micrograph of an acute cerebellar brain slice (parasagittal cut) placed on a CMOS high-density electrode chip for measurements.

The CMOS technology plays an important role for such devices since it allows the possibility to address a large number of microelectrodes on the same chip, leading to a spatial sub-cellular resolution. Another advantage of using CMOS integrated circuits (ICs) is the high signal quality provided and the relative low-noise electrophysiological recordings that can be performed from a variety of biological preparations. Many functions can be programmed via software and digital interfaces. The recording technique is extracellular and noninvasive, enabling long-term measurements.

Applications areas for such devices include neuroscience as well as medical diagnostics and pharmacology. The most common biological preparations studied using microelectrode arrays are *acute* tissue preparations (e.g, slices) which are recorded from immediately after they have been cut from

the animal and *cell cultures*.

1.2.2 The High-Density MEA Chip

The Bio Engineering Laboratory (BEL) of ETH Zürich designed a CMOS-based microelectrode array [1] featuring 11'011 metal electrodes and 126 read-out channels for extracellular bidirectional communication with electrogenetic cells. The micrograph of the chip is shown in Figure 1.3. The most important features include:

- High spatial resolution at (sub)cellular level with 3'150 electrodes per mm^2. The electrode diameter is 7 μm and the electrode pitch is 18 μm.
- A reconfigurable routing of the recording sites to the 126 read-out channels.
- A low front-end input referred noise of 2.4 μV_{rms}.

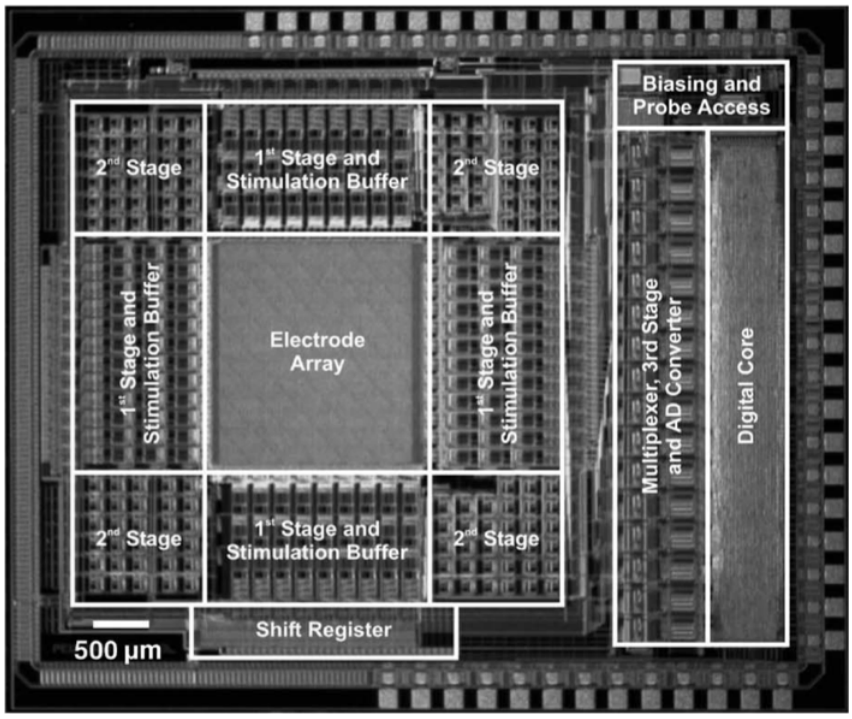

Figure 1.3: Micrograph of the MEA chip (7.5 × 6.1 mm^2).

The high-density arrays are usually CMOS-based devices that overcome the connectivity limitation by making use of on-chip signal multiplexing. The simultaneous recording from all electrodes requires the front-end amplifiers being placed in each pixel (recording site), which, due to

area constraints, entails rather high noise levels. Instead of scanning the entire electrode array, the approach of this device provides a reconfigurable electrode/readout-channel routing to select an arbitrary subset of electrodes for recording and stimulation. This enables both, low-noise signal recording, and cellular or subcellular resolution, since the front-end circuitry can be placed outside the array.

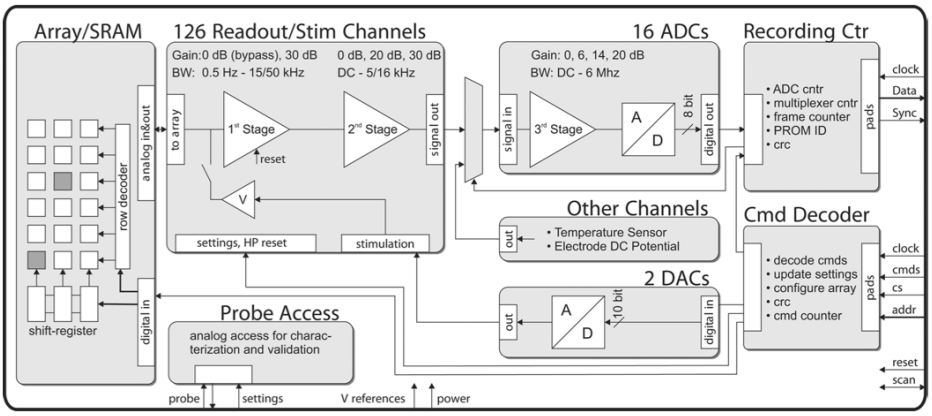

Figure 1.4: Block diagram of the MEA chip.

In the MEA chip designed by BEL [2] the read-out 126 channels and the associated signal amplification and stimulation circuitry are located outside the reconfigurable electrode array, where sufficient area for a low-noise circuit implementation is available (Figure 1.3). The readout channels includes two amplification and filter stages. Both stages feature digitally configurable gain and filter settings. The first stage provides bandpass filtering (BPF) and a gain of 30 dB. The second stage provides an additional gain of either 0 dB, 20 dB or 30 dB with a second LPF. Eight channels are then multiplexed and buffered by a third stage with an additional gain of 0 dB, 6 dB, 14 dB or 20 dB, and finally digitized at 20 kHz using successive-approximation analog-to-digital converters (ADCs) with a resolution of 8-bit. The digital recording controller then transfers the data off chip by means of a 9-bit bus together with chip-status information and a CRC (cyclic redundancy check) for error detection.

The chip was fabricated in an industrial 0.6 μm 3-metal 2-polysilicon CMOS-process. The total area of the device is 7.5 $\times$ 6.1 mm^2, while the electrode array covers an area of 2.0 $\times$ 1.75 mm^2. The front-end input-referred noise within the band of 1 Hz to 100 KHz is 2.4 μV_{rms}. The maximum gain of the entire read-out circuit is 80 dB. The power consumption of the front-end (first and second stage) is 160 μW/channel while the overall power consumption of the chip is 135 mW. The most relevant specifications characterizing the chip are summarized in Table 1.1.

Parameter	**Value**
Technology	0.6μm 3M2P CMOS
Area	7.5 $\times$ 6.1 mm^2
Supply voltage analog	5.0 V
Supply voltage digital	3.0 V
Clock frequency recording controller	3.2 MHz
Clock frequency comand controller	8 MHz
Number of electrodes	11'011
Sensor area	2.0 $\times$ 1.75 mm^2
Electrode density	3'150 1/mm^2
Power consumption overall	135 mW
Power consumption front-end (stage 1&2)	160 μW/channel
Front-end input-referred noise (1 Hz to 100 kHz)	2.4 μV_{rms}
Amplification	0-80 dB (18 steps)

Table 1.1: Performance summary of the MEA chip presented in [1]. The reported values are based on experimental measurements.

1.3 Thesis Organization

Requirements and specifications of the ADC for the new version of the MEA chip are defined in Chapter 2 where different topologies of converters are analyzed. Chapter 3 presents the design of the SAR ADC, showing the analysis and simulations of the switched-capacitor array, switches, comparator and SAR control logic. The characterization of the converter is shown in Chapter 4 where the conclusions are reported. Finally, Chapter 5 is reserved for the appendix.

Chapter 2

Specifications and ADC Topologies

This chapter provides the key design aspects for the new version of the chip. The choice of multiplexing the read-out channels for the analog-to-digital conversion is then presented and the requirements for the ADC are derived. Finally, some low-power ADC topologies are investigated and the optimum solution for our application is chosen.

2.1 Required ADC for the New Version of the Chip

The presence of on-chip ADCs is an essential requirement for allowing a robust signal transmission between the chip and the printed-circuit board (PCB). For the MEA chip presented in [2], 16 successive approximation ADCs with a 8-bit resolution have been employed.

In order to observe the electrical activity of a large-scale neural network, the new version of the chip needs to provide an increased number of channels $N_{Channels}$ equal to 1'024, which poses stringent area and power consumption constraints on the individual read-out channel and ADC. In order to improve the signal quality, in the new design, the number of bits is increased to 10. For this reason, a thorough noise and offset analyses of the converter are key aspects that have to be considered during the design.

2.2 Elaboration of Specifications

The frequency band for typical neural signals is roughly 10 Hz $\sim$ 5 KHz [3]. In order to avoid aliasing and ease spike sorting, the sampling frequency for a single read-out channel is set to 20 KHz. The number of ADCs is reduced by multiplexing the signals before their effective conversion. For the new

design, a number of 16 ADCs has been aimed to be integrated on the chip, leading to the following sampling frequency f_S for each converter:

$$f_S = \frac{N_{Channels}}{N_{ADCs}} f_N = \frac{1024}{16} \times 20kHz = 1.28\ MS/s \tag{2.1}$$

Due to limited chip area, the area for each ADC is restricted to 1 mm^2. To reduce quantization error, 10-bit resolution is chosen while the signal-to-noise and distortion ratio (SNDR) is set to be larger than 56 dB, which corresponds to an effective number of bits (ENOB) equal to 9. The new version of the chip will be designed using a 0.35 μm CMOS technology and a 3.3 V power supply, aiming to a maximum power consumption of 1 mW for each ADC. The preliminary specifications are summarized in Table 2.1.

Parameter	**Value**
Resolution	10 bits
Sampling rate	1.28 MS/s
SNDR	$\geq$ 56 dB
Power consumption	$\leq$ 1 mW
Supply voltage	3.3 V
Technology	0.35 μm CMOS
Area	$\leq$ 1 mm^2

Table 2.1: Specifications for a single ADC.

2.3 Low Power ADC Topologies Overview

In order to evaluate to evaluate which ADC architecture [4] best satisfies the presented requirements, some of the most important topologies are briefly reviewed in this section.

Integrating ADC

The Integrating ADC can be an appropriate solution for low-speed applications where low power consumptions are required. A possible implementation of this topology is the single-slope architecture, shown in Figure 2.1, where the input signal is compared with a voltage ramp. Counting the time required by the ramp to reach the signal value, it is possible to perform the analog-to-digital conversion. Even if this solution presents a very simple structure (a comparator, the voltage ramp generator and the counter in principle), it suffers from several drawbacks. A stable and precise ramp generator is required since voltage and temperature coefficients can affect

the linearity of the conversion. Moreover, a high clock frequency is desired in order to reach a sufficient resolution.

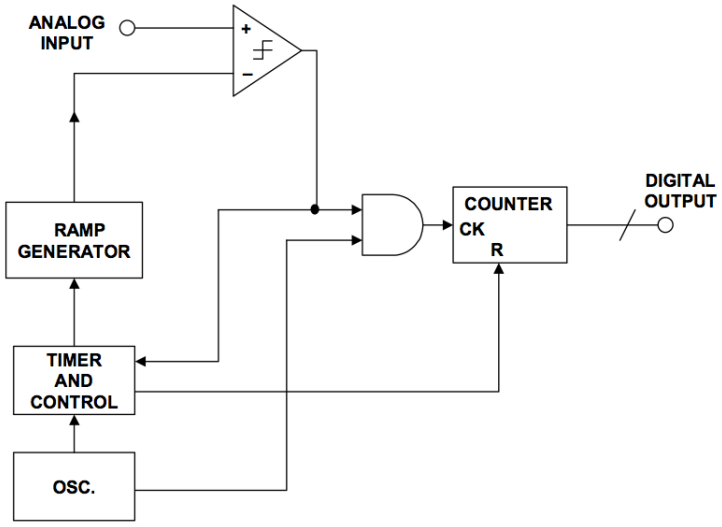

Figure 2.1: Single-slope ADC [4].

Successive-Approximation ADC

The successive-approximation ADC is based on the binary search algorithm and it requires a simple structure based on a sample and hold (S/H), comparator, digital-to-analog converter (DAC) and the successive approximation register (SAR). This is a topology mostly used to design medium-high resolution ADCs for medium-low speed applications. The DAC is controlled by the SAR logic and its output voltage varies depending on the decision of the comparator, as shown in Figure 2.2. Besides the simple structure, the converter presents a low power consumption as well.

Sigma-Delta ADC

The Sigma-Delta ADC is one of the best solutions if high resolution is required in low frequency applications. The converter is based on the oversampling and noise shaping techniques and it can achieve high signal-to-noise ratio (SNR). The analog part of the circuit is simple since only a comparator, voltage reference, integrators and analog summing circuits are required. On the other hand, the digital circuitry is quite complex and it consists of a digital signal processor (DSP) which acts as a digital filter and decimator (Figure 2.3). The delta modulation is used to achieve higher transmission efficiency by transmitting the changes (delta) in value between consecutive samples. Combining the oversampling with the sigma-delta modulator it

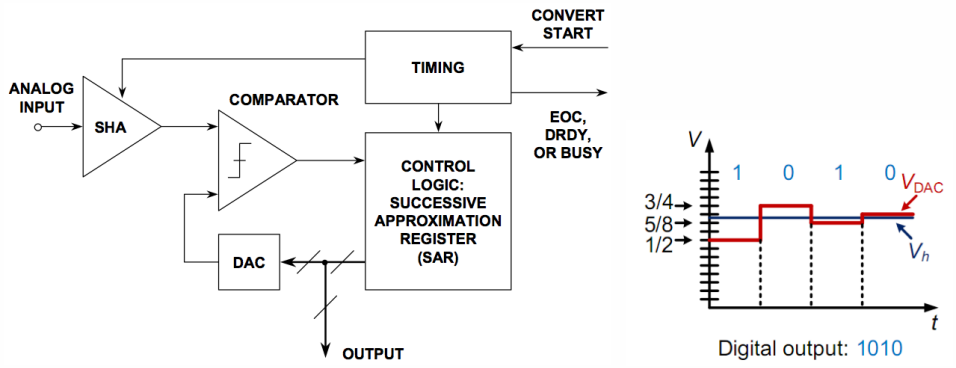

Figure 2.2: Successive-approximation ADC structure [4] and a 4-bit analog-to-digital conversion.

is possible to obtain a high SNR at low frequencies by shaping the quantization noise such that most of it occurs outside the bandwidth of interest. The noise outside the frequency bandwidth of interest will be removed by the digital filter while the decimator will reduce the output data rate back to the Nyquist rate. Some of the disadvantages of this structure are the high clock frequency required and the large silicon area consumed by the digital part.

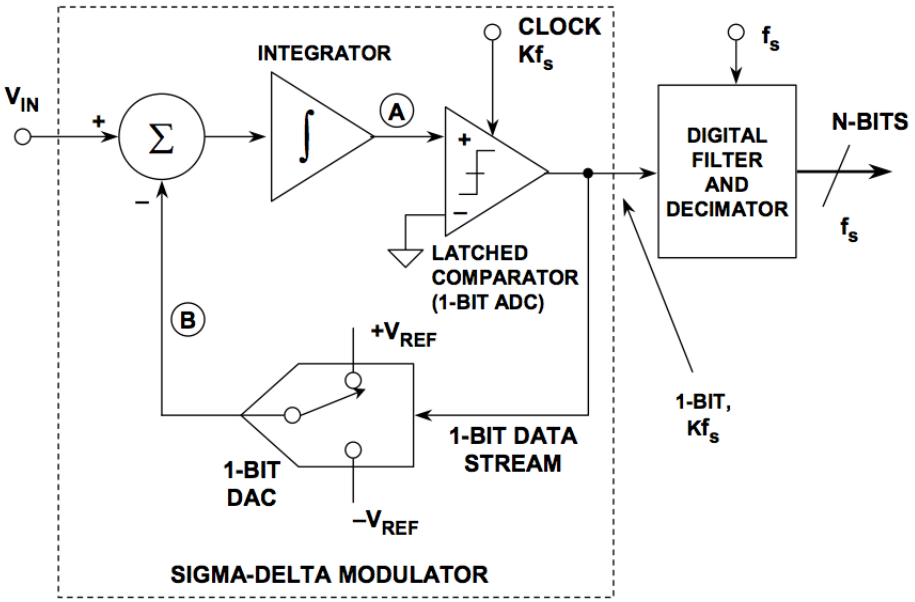

Figure 2.3: First-order sigma-delta ADC [4]

2.4 Fully Differential Switched-Capacitor SAR ADC

Considering the ADC specifications mentioned in Section 2.2, the successive approximation ADC has been preferred among the three different low-power ADC topologies presented. The most relevant advantages of this topology are the following:

- *Low power consumption*: Since the SAR ADC does not contain any power-hungry operational amplifiers (OpAmps), it is a well-known topology for its power efficiency. In fact, the comparator usually consumes less than an OpAmp since it does not need linear settling.
- *Simple structure*: The low complexity of the circuit ease its implementation on chips where compact realizations are required. This is also due to the very simple principle on which the ADC is based, the binary search algorithm. Moreover, promising solutions can also be evaluated in order to reduce even more the total area required by the ADC.

In particular, the converter presented in this work is a fully differential switched-capacitor or charge-redistribution SAR ADC [5]. This circuit incorporates an array of capacitors that is usually used as a S/H as well as a DAC. In order to better understand the operation, we first consider a simple single-ended 3-bit switched-capacitor ADC with a binary weighted capacitive array [6], which is shown in Figure 2.4. The main parts of the circuit are: the capacitive array, the switches, the comparator and the SAR control logic.

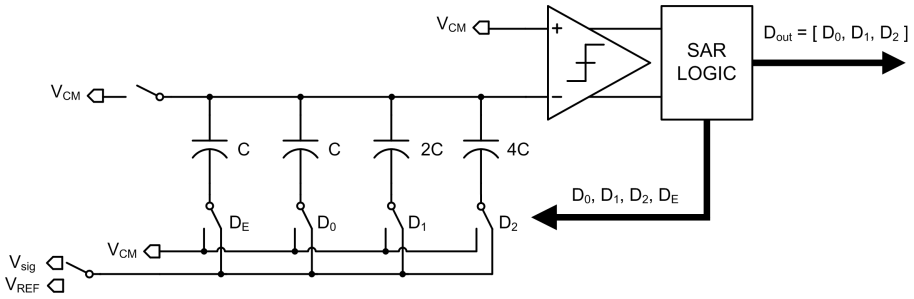

Figure 2.4: 3-bit single-ended switched-capacitor SAR ADC.

During the sampling phase, the top plates of the capacitors are reset to the common voltage V_{CM} while all the bottom plates of the capacitors are connected to the input signal source V_{sig} that is equal to the sum of V_{CM} and the input signal component ΔV_{sig}. The switches resetting the input node of the comparator are then turned off and all the bottom plate nodes are connected to V_{CM}, performing the so-called 'bottom plate sampling' [7]. Now that the voltage $V_{CM} - \Delta V_{sig}$ is stored on the top plate node of the

capacitors, the switch controlled by D_2 is connected to V_{REF} and a voltage equal to $V_{REF}/2$ is added to $V_{CM} - \Delta V_{sig}$. The comparator can therefore determine the most significant bit (MSB) by comparing this value with V_{CM}. The SAR control logic either leaves the switch controlled by D_2 connected to V_{REF} or connects it back to V_{CM} depending on the comparator output. A similar process is followed for the remaining two bits leading to the determination of the digital output value. All the switches are then reset again to the initial positions and the converter can start another cycle of conversion [4]. Note that the extra LSB capacitor (C in the case of the 3-bit DAC) is required to make the total value of the capacitive array equal to $8C$, so that binary division is accomplished when the individual bit capacitors are manipulated.

Using the same switched-capacitor array of the previous example and considering a fully differential topology of the circuit, the 4-bit ADC shown in Figure 2.5 is obtained. This new structure differs from the single-ended one in Figure 2.4 in various aspects, i. e., the differential input signal for the comparator, two identical capacitive arrays and two different references voltages V_{REFP} and V_{REFN}. Note that this structure gains an additional bit D_3 that is the 'sign bit' and it is determined once the differential input signals are sampled on the input nodes of the comparator. Hence, the MSB bit corresponds to the sign of the output digital value. Each reference voltage is assigned to a capacitive array depending on the result of the sign bit decision. At this point, the switch controlled by D_2 in each array is connected to the respective reference voltage and the values of the remaining 3 bits are determined using the binary search algorithm, as explained in the single-ended example. The voltages at the input nodes of the comparator, V_{ipA} and V_{inA}, during the sampling and conversion phases are shown in Figure 2.6.

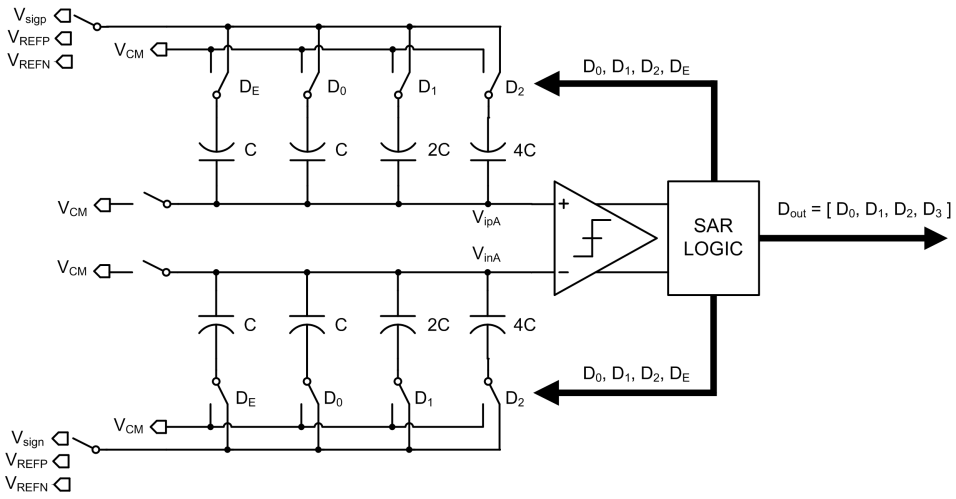

Figure 2.5: 4-bit fully differential switched-capacitor SAR ADC.

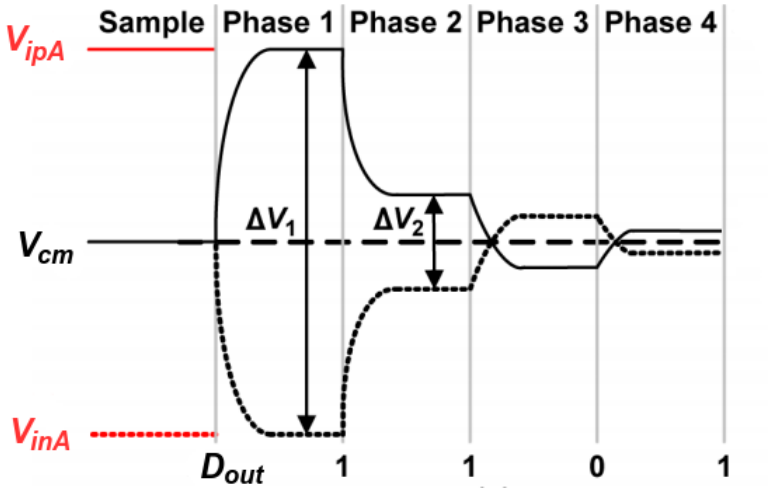

Figure 2.6: Voltages at V_{ipA} and V_{inA} during the sampling and conversion phases for the 4-bit fully differential switched-capacitor SAR ADC [8].

Since the overall accuracy and linearity of the SAR ADC is primarily determined by the internal DAC, the switched-capacitor realizations of it have become very popular in newer SAR ADCs due to their high accuracy and linearity. A high degree of temperature stability is another advantage of these capacitive DACs. Moreover, the fully differential analog signal path has been preferred respect to a single-ended one for the following main reasons:

- Immunity to common-mode noise.
- The input dynamic range is doubled, which relaxes the design requirements of the comparator.

Chapter 3

Design implementation

3.1 Design Guidelines

The design of the SAR ADC has been conducted focusing on the power and area constraints while maintaining good linearity performances for the analog-to-digital conversion. Switched-capacitor arrays are used to implement both the S/H and DAC while minimizing the area of the unit capacitor. Parasitic capacitances and matching properties have been taken into account during the analysis. Switches are providing the signals to the DAC and their size has been optimized focusing on the timing requirements. A low power solution is proposed for the comparator while achieving good noise performances and speed requirements. The input-offset storage technique has been chosen for this stage and a dynamic latch has been preferred. The digital control signals are provided by a successive approximation register.

3.2 Switched-Capacitor Array

The design of the switched-capacitor array is a key aspect for the overall performance of the entire SAR ADC. Generally, the array is used as:

- S/H: the differential input voltage can be stored at the input nodes of the comparator using the bottom plate sampling technique [7].
- DAC: in combination with the SAR control logic, the switched-capacitor array can provide the required voltage variations to perform the binary search.

Usually the capacitive array is the part of the circuit that requires the largest silicon area due to a large number of capacitors. Different design solutions can be taken into account to reduce the size of the array while maintaining a good linearity performance for both S/H and DAC. In particular, the structure of the array can be modified and the unit capacitor can be minimized.

However, these design choices can lead to larger parasitic capacitances and worse matching. For this reason, an accurate and precise analysis is required in order to choose the best solution.

The analysis should cover also the choice of the type of capacitor. The available technology offered two main types: poly-poly (cpp) capacitors and metal-metal (cmm) capacitors. The most relevant parameters describing these topologies in terms of capacitance, bottom plate parasitic capacitance and matching parameters are summarized in Table 3.1.

	cpp capacitor	**cmm capacitor**
Area capacitance	0.85 fF/μm^2	1.25 fF/μm^2
Perimeter capacitance	0.021 fF/μm	0.111 fF/μm
Parasitic area capacitance	105 aF/μm^2	12 aF/μm^2
Parasitic perimeter capacitance	57 aF/μm	36 aF/μm
Minimum area	17.24 μm^2	25 μm^2
Minimum unit capacitance	15 fF	33.47 fF
Matching parameter A_C	1.25% μm	0.65% μm

Table 3.1: Summary of the most relevant parameters for the available types of capacitors.

The capacitor matching is described by the following equation:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{WL}} \tag{3.1}$$

where $\sigma\left(\frac{\Delta C}{C}\right)$ is the standard deviation of the difference ΔC of identically designed capacitors, normalized to their absolute value C. The parameters W and L define the geometric size of the capacitor.

Since the MSB is the sign bit, two identical 9-bit capacitive arrays are required for the SAR ADC. Most of the analyses have been conducted considering only one capacitive array, extending then the results to the differential case. For this reason, it is better to differentiate the least significant bit (LSB) definition in the two following cases:

- *Differential signal path*: the required resolution n of the ADC is 10 bits for a differential dynamic input range of $FS_{d-e} = 4V$. The input signal for the ADC is in fact differential and each single-ended signal has a range of 2V. This results in a differential LSB_{d-e} equal to:

$$LSB_{d-e} = \frac{FS_{d-e}}{2^n} = \frac{4V}{2^{10}} \approx 3.906\ mV \tag{3.2}$$

- *Single-ended signal path*: since the switched-capacitor DAC is controlled by a 9-bit digital input signal D_{IN}, it is possible to define

the single-ended LSB_{s-e}. This value is useful to evaluate the performance of each DAC and then estimate the differential performance while adding linearly this error, which represents the worst case.

$$LSB_{s-e} = \frac{V_{REFP} - V_{CM}}{2^9} = \frac{1V}{2^9} \approx 1.953\ mV \tag{3.3}$$

Note that, depending on the sign bit, the analog input range of the single-ended signals becomes either [1.65 , 2.65] V or [0.65 , 1.65] V. However, the value of the single-ended full scale range FS_{s-e} is equal to 2 V, as expected.

Split Capacitive Array

The most popular switched capacitor DAC is an array of parallel binary-weighted capacitors [6]. The structure is shown in Figure 3.1 for a 9-bit DAC where the capacitor C is equal to the unit capacitor chosen. After being discharged, the bottom plates of the capacitors are connected either to a reference voltage or to V_{CM}, determining an output voltage V_m which is a function of the voltage division between the capacitors. The equivalent circuit of the DAC is shown in Figure 3.2. Considering m as the number of capacitors connected to the reference voltage V_{REFP}, the equation giving the value of V_m is the following:

$$V_m = V_{CM} + (V_{REFP} - V_{CM})\frac{m}{2^9} \tag{3.4}$$

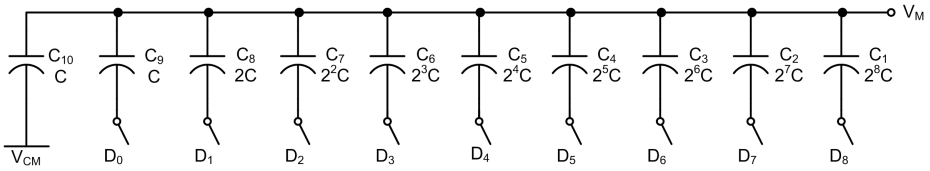

Figure 3.1: Binary weighted switched-capacitor array.

As a drawback, the presented capacitive array requires a large area due to the large number of capacitors. The total capacitance of the array is in fact 2^9C, which can result also in a large dynamic power consumption. A possible solution that can be considered is splitting the array in parts using one or more series capacitors [6]. Maintaining the binary weighted capacitor size for the sub-arrays and choosing the correct values for the series capacitors, it is possible to maintain the same ratios for the voltage division, obtaining the identical equation given in (3.4). For the 9-bit switched capacitor DAC, the array can be split in two parts (2bw1Cs array), five parts (5bw4Cs array) or it can be even realized with a C-2C ladder (C2C array) [9]. These topologies are shown in Figures 3.3, 3.4 and 3.5 where the total capacitance is in fact

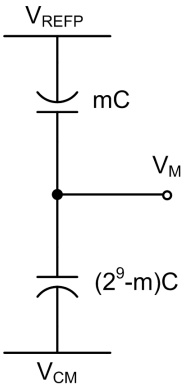

Figure 3.2: Binary weighted switched-capacitor array equivalent circuit.

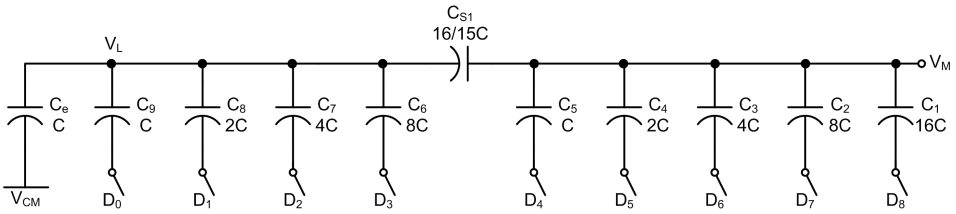

Figure 3.3: 2bw1Cs capacitive array.

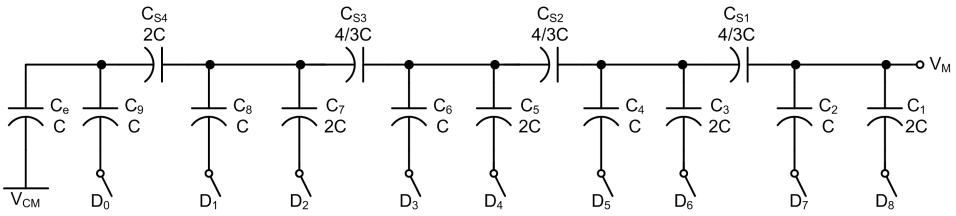

Figure 3.4: 5bw4Cs capacitive array.

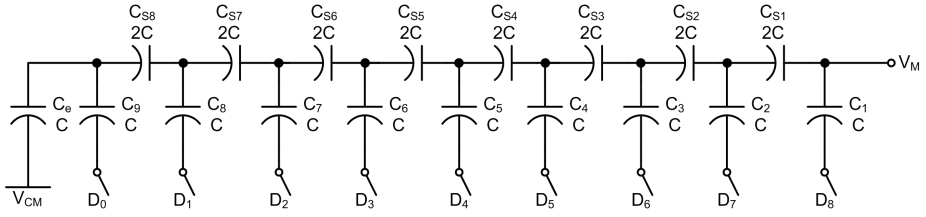

Figure 3.5: C2C capacitive array.

reduced (e.g., the 2bw1Cs presents a total capacitance of approximately 48.07C).

However, the series capacitors introduce bottom-plate parasitic capacitances that are affecting the top-plate nodes of the sub-arrays, hence decreasing the linearity of the ADC. In addition, the matching is also degraded due to the

capacitors whose value is a fraction of the unit capacitor, such as $\frac{16}{15}C$ and $\frac{4}{3}C$. An accurate analysis of these effects is therefore required in order to choose a split capacitive array that provides the required linearity and matching for the DAC, while occupies the smallest chip area.

3.2.1 Capacitive Array Design

Thermal Noise (kTC Noise)

The first limiting factor for the minimum acceptable size of the capacitors is the Johnson-Nyquist noise (thermal noise) that is usually referred as kTC noise for the sampling circuits [6]. Considering that the entire ADC has two capacitive arrays, the mean-square value expressing the thermal noise for each array is summed up while considering the SNR of the entire structure. Since the two arrays are identical, the worst SNR due to the kTC noise can be written as follows:

$$SNR_{Thermal} = \frac{P_{Signal}}{P_{Thermal}} = 10log_{10}\left[\frac{\frac{1}{2}\left(\frac{FS_{d-e}}{2}\right)^2}{2\frac{k_BT}{C_u}}\right] \tag{3.5}$$

where k_B is the Boltzmann constant, T is the temperature expressed in Kelvin and C_u is unit capacitor considered. Since for all the different split capacitive array topologies there is always a unit capacitor connected to the output node of the DAC, this capacitive value has been considered for the calculation as worst case. Comparing this SNR with the theoretical signal-to-quantization-noise-ratio (SNQR) of the ADC, it is possible to find a value of the capacitor C_u that returns a negligible kTC noise. The definition of the SQNR is the following:

$$SQNR = 10log_{10}\left[\frac{\frac{1}{2}\left(\frac{FS_{d-e}}{2}\right)^2}{\frac{LSB_{d-e}}{12}}\right] = 6.02n + 1.76 \tag{3.6}$$

For a 10-bit ADC, the theoretical SQNR is equal to 62 dB. The value of the unit capacitor is therefore found considering the following condition:

$$SNR_{Thermal} \geq SQNR \tag{3.7}$$

That results in the a minimum capacitor values at a temperature T of 300 K equal to:

$$C_u \geq 10^{\frac{6.02n+1.76}{10}} \times 4k_BT\left(\frac{2}{FS_{d-e}}\right)^2 \approx 6.55\ fF \tag{3.8}$$

Being 15 fF and 33.47 fF respectively the minimum unit capacitance $C_{cpp,min}$ and $C_{cmm,min}$ for the technology considered (Table 3.1), the effect of the kTC noise is not relevant and it can be neglected in the future considerations.

Parasitic Capacitances

Every integrated capacitor presents parasitic capacitances between its plates and the surrounding layers. This parasitics can be therefore summarized in two groups: top-plate (TP) parasitic capacitances and bottom-plate (BP) parasitic capacitances, depending on which plate is considered. Since usually the BP parasitic capacitances presents the highest value, the effect of the TP parasitic capacitances has been neglected during the presented analysis. Considering first the bw capacitive array (Figure 3.1), the BP nodes of all the capacitors are always connected to a fixed voltage value (either to a reference voltage or V_{CM}), hence the parasitic capacitances are not affecting the DAC characteristic of the output voltage. This is not true for the split arrays where the series capacitors are adding parasitics on the TP nodes of the sub-arrays, giving a gain error and decreasing the linearity of the DAC. As an example, the 2bw1Cs capacitive array is shown in Figure 3.6 where the BP parasitic capacitance C_{p1} of the series capacitor C_{s1} has been added. Note that C_{p1} is considered to be connected between the top-plate of the LSB sub-array and the n-well where the capacitive array is placed. This well is tied to V_{DD}.

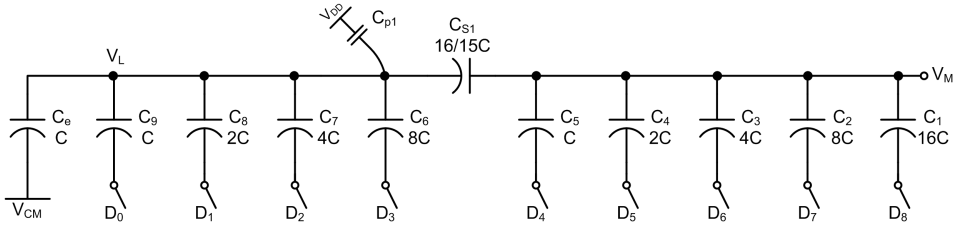

Figure 3.6: 2bw1Cs switched-capacitor array with the bottom-plate parasitic capacitance added.

Both effects can be highlighted in the equation of the output voltage of the DAC, which is obtained by solving the system of equations given by the charge conservation principle. Considering the 2bw1Cs capacitive array as an example, the equivalent circuit of the DAC is shown in Figure 3.7 where m and p are the sums of the unit capacitors connected in parallel to the reference voltage in the LSB sub-array (C_{6-9}) and MSB sub-array (C_{1-5}) respectively. The values of m and p depend on the digital input D_{IN} of the DAC, for example: if $D_{IN} = 256 = 100...0$, then $m = 0$ and $p = 16$.
Assuming that all the capacitors are discharged before applying the digital input signal, the equations given by the charge conservation principle are the following:

$$\begin{aligned} C_{p1}(V_{CM} - V_{DD}) &= mC(V_L - V_{REFP}) + (16 - m)C(V_L - V_{CM}) + \\ &\quad + \frac{16}{15}C(V_L - V_M) + C_{p1}(V_L - V_{DD}) \end{aligned}$$

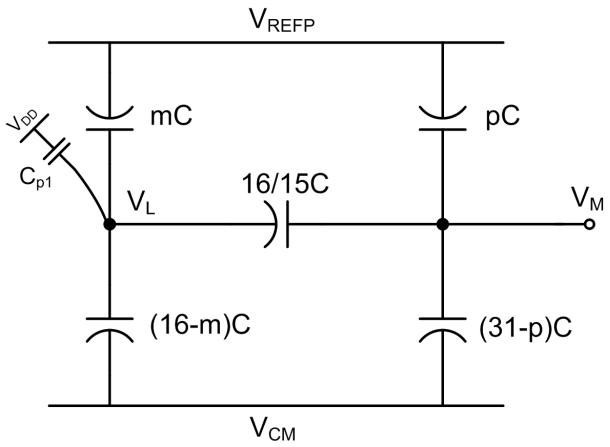

Figure 3.7: 2bw1Cs switched-capacitor array equivalent circuit.

$$0 = pC(V_M - V_{REFP}) + (31-p)C(V_M - V_{CM}) + \frac{16}{15}C(V_M - V_L) \quad (3.9)$$

Solving the previous system of equations, the output voltage V_M of the DAC is:

$$V_M = V_{CM} + (V_{REFP} - V_{CM}) \left[\frac{16(m+16p)C}{8192C + 481C_{p1}} + \frac{15pC_{p1}}{8192C + 481C_{p1}} \right] \quad (3.10)$$

While not considering the parasitic capacitance ($C_{p1} = 0$) the equation is reduced to the output voltage equation of an ideal 9-bit DAC:

$$V_M = V_{CM} + (V_{REFP} - V_{CM}) \frac{m+16p}{512} \quad (3.11)$$

Comparing (3.10) with (3.11) it is therefore possible to note how the parasitic capacitance C_{p1} is affecting both gain error and linearity.

Focusing on the linearity of the DAC, the integral nonlinearity (INL) graph can be estimated for each presented topology. This can be done by solving the equations given by the charge conservation principle while considering the BP parasitic capacitances, finding the equation of the output voltage and proceeding then with the INL estimation. The INL values have been found comparing the effective output voltage with its best fitting line in order to eliminate the gain error [4]. As an example, the estimated INL graph for each split capacitive array topology is shown in Figure 3.8 where minimum-size cmm capacitors have been used. The binary weighted solution has not been considered since no BP parasitic capacitances are connected to the TP node of the array. Note that each graph has been found while considering only one capacitive array, hence the LSB considered is referred to the single-ended case, that has been estimated in (3.3). The results can be extended to the differential case since both capacitive arrays in the ADC

are identical. From the INL results shown in Figure 3.8, it is possible to notice that the more the array is divided into parts, the more it is affected by the parasitic components. Hence, the area of the unit capacitor should be increased in order to reduce the parasitic capacitances and limit this effect. The tradeoff between the linearity and required area will be therefore considered while comparing all the results, aiming the following requirement:

$$INL \leq 0.5LSB_{s-e} \tag{3.12}$$

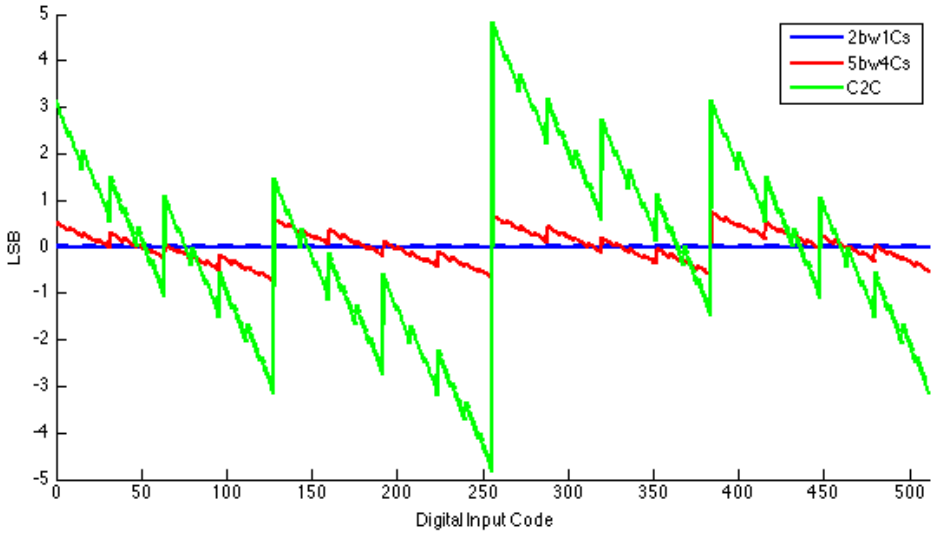

Figure 3.8: INL graph estimation of each split capacitive array.

Matching of the Capacitors

The matching of the capacitors is another key aspect that has to be taken into account in order to achieve a desired performance from the capacitive DAC. The matching properties of capacitors depend on the technology used, the capacitor size and the layout employed. While for the layout design a common-centroid technique has been considered (Section 3.6), in this section, a pre-layout estimation of the capacitors matching has been studied [10]. The output voltage of each 9-bit DAC for the half-range digital input code ($D_{IN} = 256 = 100...0$) presents the worst case in terms of mismatch among the capacitors [11], hence the standard deviation of this voltage should be constrained with the following condition:

$$3\sigma(V_{M,D_{IN}=256}) \leq 0.5LSB_{s-e} \tag{3.13}$$

where $V_{M,D_{IN}=256}$ is the output voltage value for the half-range digital input code and is ideally equal to:

$$V_{M,D_{IN}=256} = V_{CM} + \frac{V_{REFP} - V_{CM}}{2} = 2.15\ V \tag{3.14}$$

If (3.13) is satisfied, the linearity performance of the DAC is met. Note that if the requirement is met considering only one capacitive array, the result can be extended also for the differential case. Considering the parametric expression of the output voltage of the DAC and assuming that the mismatch of each capacitor is independent, it is possible to estimate both the mean value and the standard deviation of $\sigma(V_{M,D_{IN}=256})$. The calculations have been conducted using the properties of the variance from the statistics theory. A simplified example of this type of calculation is reported in Appendix 5.2 for a 3-bit capacitive DAC. This type of estimation has been conducted for each capacitive array topology presented before. The values of $\sigma(V_{M,D_{IN}=256})$ for both the bw and 2bw1Cs capacitive array are presented in Table 3.2, where μ_C is the mean value of the unit capacitor considering both area and perimeter capacitance (Table 3.1) and σ_C is the standard deviation of the unit capacitor, that is defined as follows:

$$\sigma_C = \sigma\left(\frac{\delta C}{C}\right)\mu_C = \frac{\sigma\left(\frac{\Delta C}{C}\right)}{\sqrt{2}}\mu_C \tag{3.15}$$

Capacitive array topology	$\boldsymbol{\sigma(V_{M,D_{IN}=256})}$
bw	$(V_{REFP} - V_{CM})\frac{\sqrt{3}\sigma_C}{32\sqrt{2}\mu_C}$
2bw1Cs	$(V_{REFP} - V_{CM})\frac{\sigma_C\sqrt{24591\mu_C^2 + 15\sigma_C^2}}{1024\mu_C^2}$

Table 3.2: Examples of the resulting parametric estimation of $\sigma(V_{M,D_{IN}=256})$ for the bw and 2bw1Cs capacitive arrays.

Since both μ_C and σ_C depend on the area of the unit capacitor, by substituting the parametric expressions in (3.13), one can determine the minimum unit capacitor area that satisfies the condition. The results found with the analytical method have been compared with MATLAB simulations where the $\sigma(V_{M,D_{IN}=256})$ value has been calculated considering the capacitor variables as 100-points gaussian distributions. The comparison shows that the proposed method overestimates the minimum unit capacitor area and this is probably due to the independent-variables assumption. However, this type of analysis can still be used to roughly determine the unit capacitance with some margin.

Results and Considerations

Summarizing all the results found in the previous analyses, one can decide the capacitive array topology, the type of capacitor and its unit area that best fit for our application. Since the kTC noise can be considered negligible, the minimum unit capacitor area WL that satisfies both the parasitic capacitance (PC) condition (3.12) and the capacitive matching (CM) condition (3.13) are summarized in Table 3.3.

	PC WL [μm^2]	**CM WL [μm^2]**	**Overall WL [μm^2]**	**# C_u**	**C_{Tot} [fF]**
bw					
cpp	*min*	*min*	*min*	512	7'682
cmm	*min*	*min*	*min*	512	17'137
2bw1Cs					
cpp	17.28	*min*	17.28	48.07	722
cmm	*min*	*min*	*min*	48.07	1609
5bw4Cs					
cpp	140.63	>1'000	>1'000	-	-
cmm	38.03	105	105	20.50	2'784
C2C					
cpp	248.27	>1'000	>1'000	-	-
cmm	74.95	>1'000	>1'000	-	-

Table 3.3: Summary of the results for the design of the capacitive array.

The total number of unit capacitors required in the array is # C_u and C_{Tot} is the total capacitance of the array. The *min* value states that the minimum-size unit capacitor satisfies the considered design condition. On the other hand, when a unit capacitance area less than 1'000 μm^2 cannot satisfy the matching condition for a certain condition, the topology is discarded. As expected, it is possible to notice how the split topologies are affected by both parasitics and mismatch. In particular, the 5bw1Cs and C2C can be discarded since they require a very large unit capacitor mostly due to the presence of BP parasitic capacitances. Hence, the 2bw1Cs capacitive array has been chosen since it meets the requirements with the minimum unit capacitance value. Furthermore, cmm capacitors have been preferred due to their better matching characteristic and less parasitic capacitances.

Split Capacitive Array Realization

The 2bw1Cs capacitive array chosen includes a series capacitor C_{s1} with a value of $\frac{16}{15}C$ whose layout design could be cumbersome. In addition, its matching properties could be worse than those of the other capacitors since

its capacitance is not an integer multiple of the unit capacitor C. Therefore, the modified split capacitive array presented in [13] has been adopted in this work. The modified array, shown in Figure 3.9, differs from the common 2bw1Cs structure for the following two aspects:

- The series capacitor is substituted with a unit capacitor, i. e., C_{s1} is equal to C.
- The additional parallel capacitor C_e of the LSB sub-array is removed.

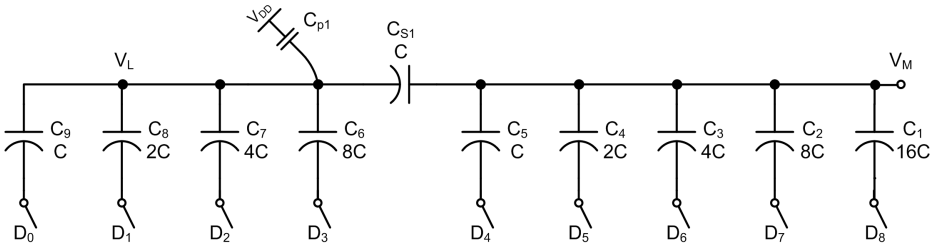

Figure 3.9: Modified split capacitive array.

In order to check the accuracy of the proposed solution, it is possible to study the equivalent circuit of the DAC, which is shown in Figure 3.10. Assuming that all the capacitors are discharged before applying the digital input signal and neglecting the effect of the parasitic capacitance ($C_{p1} = 0$), the equations given by the charge conservation principle are the following:

$$\begin{aligned} 0 &= mC(V_L - V_{REFP}) + (15-m)C(V_L - V_{CM}) + C(V_L - V_M) \\ 0 &= pC(V_M - V_{REFP}) + (31-p)C(V_M - V_{CM}) + C(V_M - V_L) \end{aligned} \tag{3.16}$$

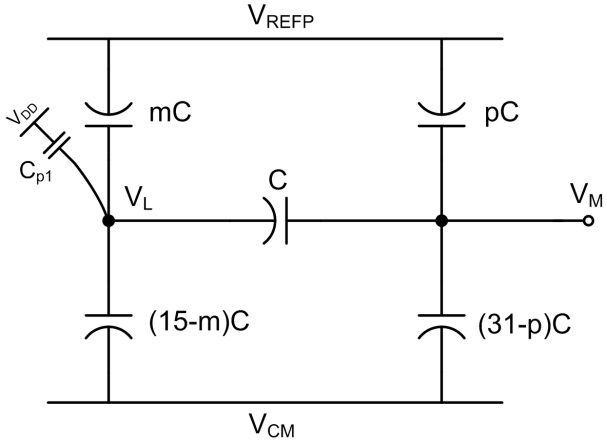

Figure 3.10: Modified split capacitive array equivalent circuit.

Solving the previous system of equations, the output voltage V_M of the DAC is found as follows:

$$V_M = V_{CM} + (V_{REFP} - V_{CM})\frac{m + 16p}{511} \tag{3.17}$$

Comparing (3.11) with (3.17), it can be noticed that a gain error of 1 LSB introduced by the proposed array. However, this is not severe since the gain error caused by the input capacitance of the comparator is even larger (Appendix 5.1).

DAC Post-Layout Simulations on Cadence

The reliability of the previous analyses can be verified by simulating the DAC with Cadence. First of all, the linearity of the DAC is evaluated by running an INL analysis which, however, takes into account only the effects of the parasitic capacitances. The results given by the pre-layout simulations match the previous estimated values. Nevertheless, the performance of the DAC decreases while checking the post-layout simulations. This is due to the two following aspects:

- The parameters describing the different capacitor technologies (Table 3.1) are defined as mean values. The minimum unit capacitance can be considered as a boundary case, hence the estimations could be not accurate enough.
- The post-layout simulations take into account the coupling effects between the capacitors and wires, that are difficult to estimate. This aspect can be critical since the unit capacitance could be comparable to the parasitic and wiring capacitances.

For this reason, the layout design of the capacitive array has been conducted in order to reduce the parasitic effects and maximize the DAC performance. The common-centroid technique [15] has been chosen to reduce the complexity of the structure and, hence, minimize the wiring. In addition, while the metal layers MET2 and MET3 have been reserved for the capacitors and the internal connections, MET1 has been used to wire the input signals and to reduce capacitive unbalances of the structure due to the asymmetric structure. The capacitive array floorplan is shown in Figure 3.11 where C_{sd} is the dummy capacitor of C_{s1}.
The modified split capacitive array implemented with minimum unit capacitors (C_u=33.47 fF) manifests an INL that is always less than 0.5 LSB_{s-e}. However, the unit capacitor C_u has been finally increased to 64.36 fF in order to have some margin on the performance. The INL graphs of both cases are shown in Figure 3.12.

The DAC non-linearity caused by the capacitance mismatch has been verified with a 1'000-runs Monte Carlo simulation. The worst-case value of $V_{M,D_{IN}=256}$ has been considered and measured. The following results have been obtained:

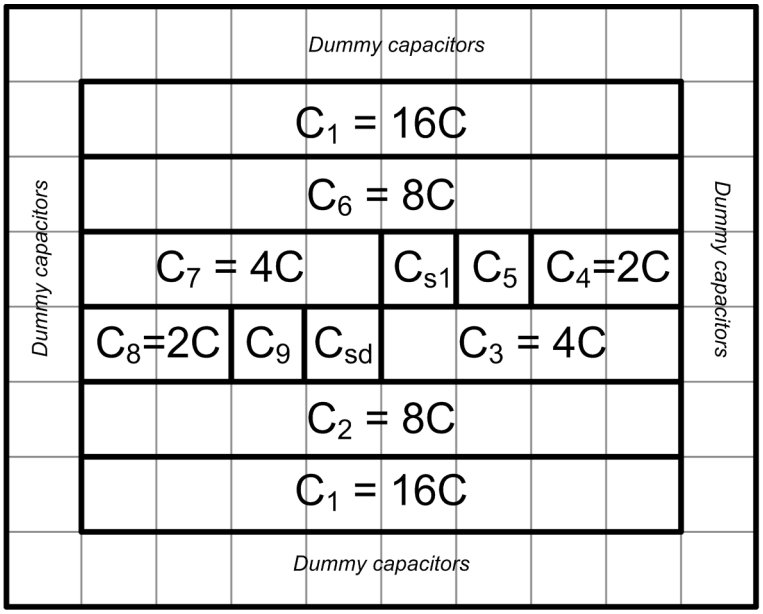

Figure 3.11: Floorplan of the capacitive array.

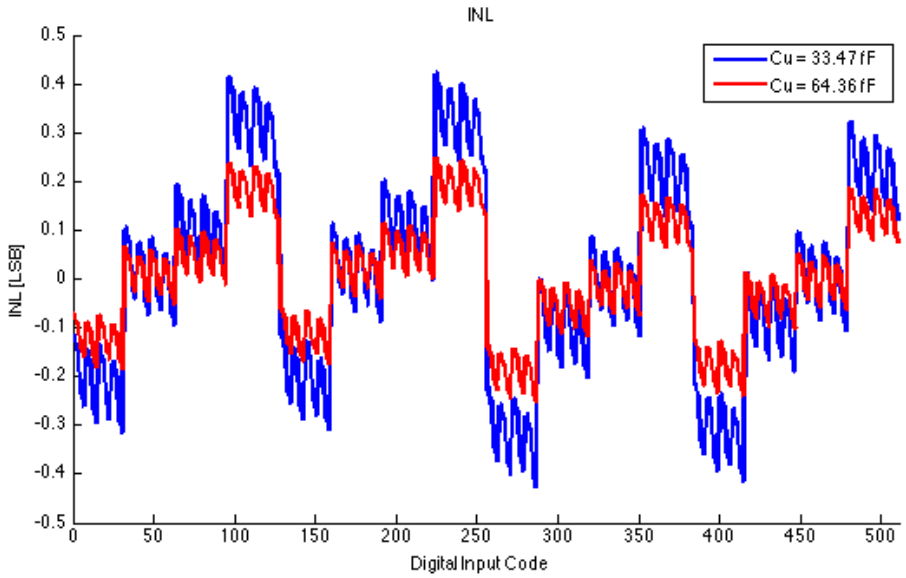

Figure 3.12: INL graphs of the 9-bit DAC comparing two different values for the unit capacitance.

- $\mu(V_{M,D_{IN}=256}) = 2.150\ V$
- $\sigma(V_{M,D_{IN}=256}) = 82.30\ \mu V$

It is possible to compare the standard deviation of $V_{M,D_{IN}=256}$ with the 0.5 LSB_{s-e} reference value as follows:

$$3\sigma(V_{M,D_{IN}=256}) = 246.90\ \mu V \ll 0.5\ LSB_{s-e} \approx 1.953\ mV \tag{3.18}$$

Hence, the estimations about the DAC non-linearity are reliable.

Dynamic Power Consumption

The dynamic power consumed in the array can be estimated considering both the power required by the DAC and the power delivered during the sampling phase [14]. Considering only one capacitive array, it is possible to estimate these values as follows:

$$P_{DAC} = f_S \sum_{i=1}^{9} E_i \approx f_S C_{Charged} V_{REF}^2 \tag{3.19}$$

$$P_{Samp} = f_S E_{Samp} = f_S C_{Charged} \left(\frac{FS_{s-e}}{2}\right)^2 \tag{3.20}$$

where f_S is the sampling frequency which is equal to 1.28 MS/s, E_i the energy required by the DAC for the i-th digital input applied, $C_{Charged}$ is the total capacitance charged during the DAC phases (note that the voltage across the series capacitor is assumed to remain the same) and is equal to 46C, V_{REF} is the voltage at which each capacitor is charged and is equal to 1 V and E_{Samp} is the energy required by the sampling phase. Considering both capacitive arrays, their total dynamic consumption is therefore the following:

$$P_{Tot} = 2(P_{DAC} + P_{Samp}) \approx 2 f_S C_{Charged} \left[V_{REF}^2 + \left(\frac{FS_{s-e}}{2}\right)^2\right] \tag{3.21}$$

Which results in a total power consumption P_{Tot} equal to 15.16 μW. Since the total power required to charge the array is proportional to $C_{Charged}$, it is favorable to split the array. For a conventional binary weighted array, the equivalent charged capacitance is 512C which leads to a P_{Tot} of 168.72 μW for the same unit capacitance.

The previous estimated values can be verified by a simple simulation on Cadence. Considering first the DAC phase, the switching behavior can be simplified in two steps: while the top-plate nodes of both MSB and LSB sub-arrays are first maintained at V_{CM}, the bottom-plate nodes of all capacitors excluding C_{s1} are switched between V_{REFP} and V_{CM}. The

switching frequency of this circuit has to be equal to 1.28MS/s that is the sampling frequency f_S. Hence, the power consumed by the DAC can be estimated as follows:

$$P_{DAC,Sim} \approx (V_{REFP} - V_{CM})I_{Avg} \tag{3.22}$$

where I_{Avg} is the average current delivered by the reference voltage source calculated on 1'000 cycles. For the sampling phase, the switching behavior is the same and, instead of V_{REFP}, the maximum input voltage value is applied. Since this value is theoretically equal to 2.65V, that is actually V_{REFP}, both the circuit and the conditions are exactly equal to the previous case. Hence, $P_{Samp,Sim}$ is equal to $P_{DAC,Sim}$, as obtained also in the previous calculations. The total dynamic consumption estimated before is verified by this simulation, as it can be noticed from the results:

$$P_{Tot,Sim} = P_{DAC,Sim} + P_{Samp,Sim} \approx 2(V_{REFP} - V_{CM})I_{Avg} = 15.59\ \mu W \tag{3.23}$$

3.3 Switches

Each capacitive array requires a relatively high number of switches that are used both for passing signals and reset the voltage values at specific nodes. A design analysis based on the settling time and sampling linearity has been conducted in order to optimize the size of each switch.

3.3.1 Switch Structures

The switched-capacitor array is used both for sampling the input signal and providing comparing reference voltages required by the SAR algorithm. Input and reference signals are applied to the bottom-plate of the capacitors using switches. On the other hand, the top-plates of the capacitors belonging to the LSB sub-array are reset by applying the common-mode voltage V_{CM} through only one switch (Figure 3.13) while the node V_M is reset by the preamplifier stage during the offset-cancellation phase, as shown in Section 3.4. For this reason, the switches used can be divided into two groups:

- *Bottom-plate switches*: they pass the input voltage signal, the common voltage or one of the two reference voltages to the bottom-plate of the capacitors.
- *Top-plate switch*: it resets the voltage value at the V_L node passing the common voltage.

The structure of the entire capacitive array with the switches is shown in Figure 3.13 where V_{BP} can be one of the four voltages mentioned before and here summarized with their voltage values or range:

- $0.65\ V \leq V_{Sig} \leq 2.65\ V$
- $V_{CM} = 1.65\ V$
- $V_{REFP} = V_{CM} + V_{REF} = 1.65\ V + 1\ V = 2.65\ V$
- $V_{REFN} = V_{CM} - V_{REF} = 1.65\ V - 1\ V = 0.65\ V$

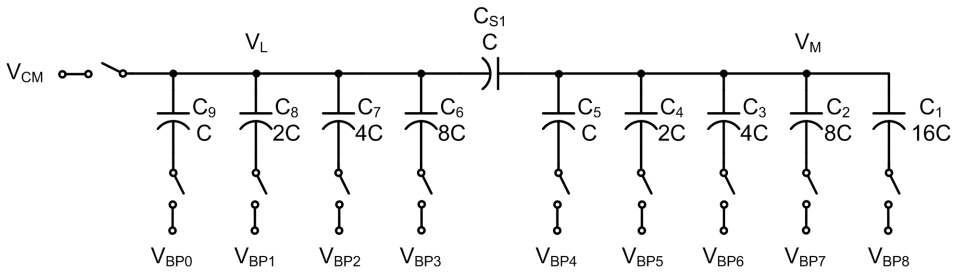

Figure 3.13: Capacitive array with ideal bottom-plate and top-plate switches.

Starting first the design of the BP switches, they can be organized choosing one of the following main structures:

- *Mux-like (ML) structure*: four different switches are connected to the bottom plate of each capacitor in the array, respectively passing the voltages V_{Sig}, V_{REFP}, V_{REFN} and V_{CM}. Figure 3.14 shows the structure connected to the bottom plate of one capacitor.
- *Shared-block (SB) structure*: the bottom plate of each capacitor is directly connected to two switches only. While one switch is passing V_{CM}, the other is connected to a structure shared among all the capacitors belonging to the array. This structure is made up of three switches that are providing the remaining voltages (V_{Sig}, V_{REFP} and V_{REFN}). This topology is shown in Figure 3.15 where the shared block has been highlighted.

The SB structure has been implemented because it requires a less complicated control logic and routing due to the shared structure. Although the switches are connected in series, this solution does not need very low switch on-resistance. Still good performances can be achieved while maintaining small gate-width and minimum gate-length for all the transistors used.

Only NMOS pass-transistors (NMOS PTs) have been used to implement the switches passing the negative reference voltage V_{REFN} and common voltage V_{CM} while PMOS pass-transistors (PMOS PTs) are used to provide the highest reference voltage V_{REFP}. On the other hand, transmission-gates (TGs) are preferred while passing the input voltage, whose range is from 0.65 V to 2.65 V. Considering the SB structure, the switch TG_{BP} that controls the passage of V_{Sig}, V_{REFP} and V_{REFN} for each capacitor is also a

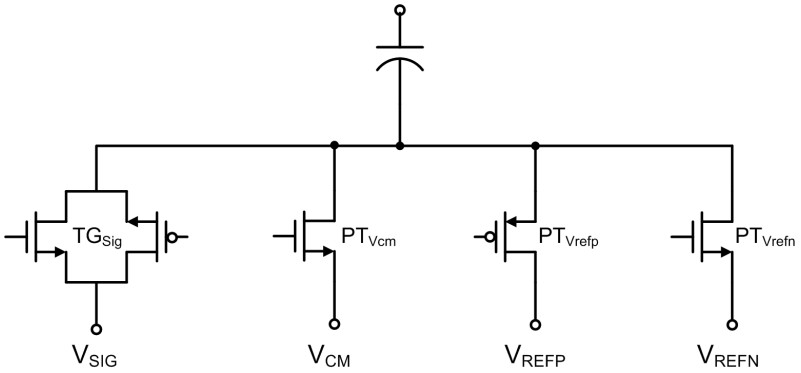

Figure 3.14: Mux-like structure for the switches of the capacitive array.

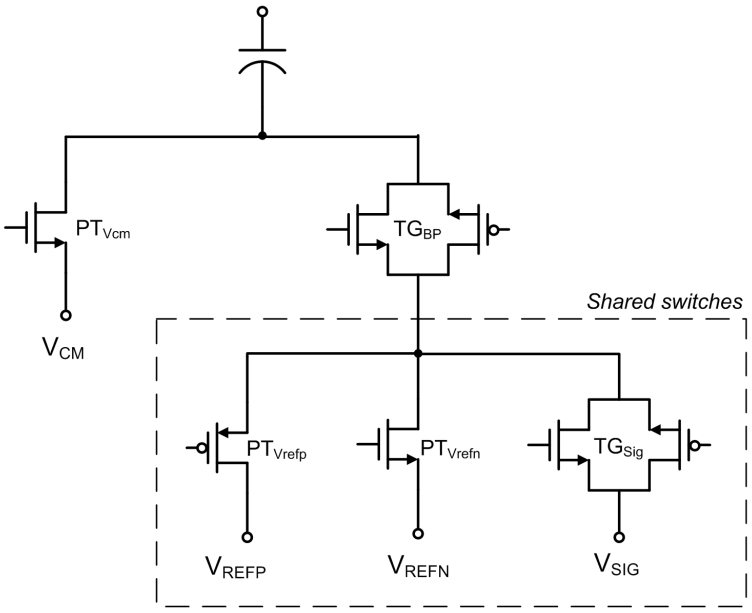

Figure 3.15: Shared-block structure for the switches of the capacitive array.

transmission-gate. The on-resistance values of both NMOS PT and PMOS PT depend on the input signal V_{Sig} and their definitions are shown in (3.24) and (3.25) respectively [12].

$$R_{on,N} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{DD} - V_{Sig} - V_{TN})} \tag{3.24}$$

$$R_{on,P} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_P (V_{Sig} - |V_{TP}|)} \tag{3.25}$$

where C_{ox} is the MOS gate capacitance per unit area, $\frac{W}{L}$ the aspect ratio and V_T the threshold voltage. Since the electron mobility μ_n of the NMOS transistors is approximately three times larger than the hole mobility μ_p of the PMOS transistors for our technology, a scaled value of the minimum gate-width can be used while sizing the PMOS switches. Hence, assigning W_P for the gate-width of the PMOS transistor and W_N the gate-width of the NMOS transistor, the relation between them is expressed as follows:

$$W_P = 3W_N \tag{3.26}$$

Therefore, following the relation given by (3.26) and minimum gate-length for the design of all the PTs, it is possible to reach a low on-resistance value for the PMOS PTs that is comparable to the one of the minimum-size NMOS switches for the respective input voltage ranges. Using the same design choice for the design of the transmission-gates, the variation of its on-resistance as a function of the input voltage will be much less compared to that of a pass-transistor. This result is shown in Figure 3.16 where this function has been plotted considering different values for W_N and maintaining the ratio given by (3.26). Finally, as a reference value, the minimum size and aspect ratio for the gate of the NMOS transistors of the switches provided by the technology used in this thesis are the following:

$$\left(\frac{W}{L}\right)_{N,min} = \frac{W_{min}}{L_{min}} = \frac{0.7\ \mu m}{0.35\ \mu m} = \frac{2}{1} \tag{3.27}$$

3.3.2 DAC Settling Time

Most of the switches has been sized considering the settling time requirement of the DAC. During the settling phase, all the BP switches are involved except for the shared transmission-gate that is directly passing the input signal. It is therefore useful to study the RC equivalent model of the switched-capacitor array where the switches are represented with their on-resistance.

The settling time of the output voltage provided by the 9-bit DAC reaches its largest value when the digital input is switched from $D_{IN} = 0$ to $D_{IN} = 256$, since the voltage difference between the initial and the final value presents its maximum value which is $\Delta V \approx \frac{V_{REF}}{2} = 0.5\ V$. For the digital input value $D_{IN} = 256$, the bottom plate of the capacitor C_1 is therefore connected to the series of the switches composed by TG_{BP} and one pass-transistor (NMOS or PMOS depending on the reference voltage) while the bottom-plate of each other capacitor is connected to V_{CM} through the NMOS switch. Note, at this moment the TP reset switch is turned off. The equivalent RC model is shown in Figure 3.17.

In order to obtain a rough estimation of the settling time, it is generally common to use the Open Circuit Time Constant (OCTC) analysis that

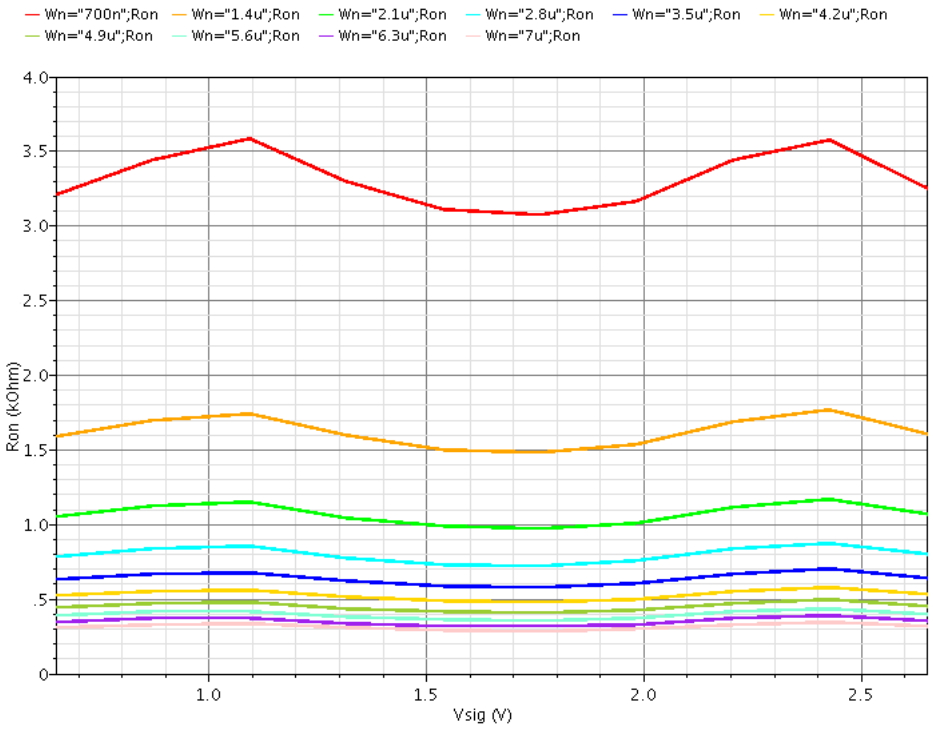

Figure 3.16: Dependance of the on-resistance value of the transmission-gate on the input voltage value. While maintaing the relation (3.26), the value of W_N has been swept from 0.7 μm to 7 μm.

can be used to estimate the dominant time constant of the network. Unfortunately, in the case studied, this method is not accurate because there are several poles having comparable frequencies. For this reason, another approach has been used considering the following assumptions:

- For the LSB sub-array in Figure 3.17, each branch has a time constant whose value is comparable with the others. Hence, as an assumption, the voltage at the bottom-plate of each capacitor connected to the pass-transistor providing V_{CM} is considered to be equal during the transition. Therefore, these nodes can be shorted in the equivalent circuit and the equivalent impedance of the LSB sub-array will be:

$$Z_{BP,C_{s1}} \approx \frac{1}{15sC} + \frac{R_{PT,V_{cm}}}{4} \tag{3.28}$$

  The impedance seen from the top-plate of the splitting capacitor C_{s1} to V_{CM} is approximately the following:

$$Z_{TP,C_{s1}} = \frac{1}{sC} + Z_{BP,C_{s1}} \approx \frac{1}{sC} + \frac{R_{PT,V_{cm}}}{4} \tag{3.29}$$

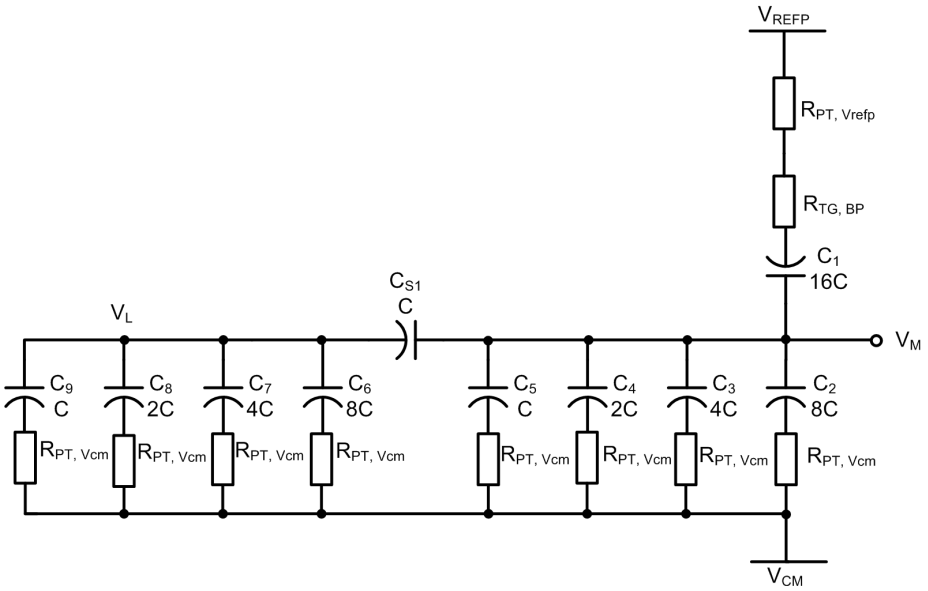

Figure 3.17: Equivalent RC model of the 9-bit DAC for $D_{IN} = 256$.

The resulting equivalent circuit is shown in Figure 3.18.

- At this point, the same assumption can be made once again since the time constants of each branch are still comparable. The bottom-plate nodes of each capacitor connected to the pass-transistor providing V_{CM} are shorted together and the final equivalent model is shown in Figure 3.19.

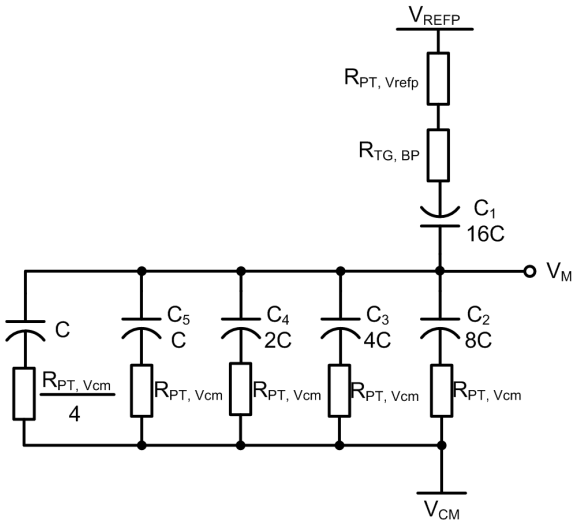

Figure 3.18: Simplified equivalent RC model of the 9-bit DAC for $D_{IN} = 256$.

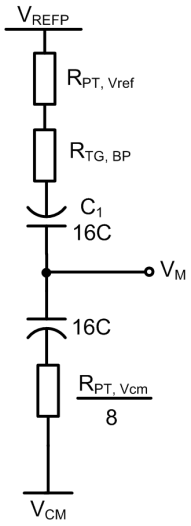

Figure 3.19: First-order equivalent RC model of the 9-bit DAC for $D_{IN} = 256$.

Now the equivalent model corresponds to a simple first order RC network and the settling time can be easily estimated. Considering V_{REFP} as reference voltage, the step response of the voltage node V_M is described by the following expression:

$$V_M(t) = V_{M_0} + \left(V_{CM} + \frac{V_{REFP} - V_{CM}}{2} - V_{M_0} \right) (1 - e^{-t/\tau}) \tag{3.30}$$

where V_{M_0} is the instant voltage value of V_M when the digital input is switched from Din=0 to Din=256 and it is equal to:

$$V_{M_0} = V_{CM} + (V_{REFP} - V_{CM}) \frac{\frac{R_{PT,V_{CM}}}{8}}{\frac{R_{PT,V_{CM}}}{8} + R_{PT,V_{REFP}} + R_{TG,BP}} \tag{3.31}$$

Once the voltage signal $V_M(t)$ is settled, it reaches the final value due to the voltage divider given by the capacitors. Therefore, the difference between the final and initial voltage is equal to:

$$\Delta V = V_{CM} + \frac{V_{REFP} - V_{CM}}{2} - V_{M_0} \tag{3.32}$$

While the time constant of the RC network is calculated as follows:

$$\tau = (\frac{R_{PT,V_{CM}}}{8} + R_{PT,V_{REFP}} + R_{TG,BP}) \times 8C \tag{3.33}$$

The settling time is then obtained by considering the time needed by the output voltage to reach the final value within an error of $0.5LSB_{s-e}$, i.e.:

$$V_M(t_{sett}) = \epsilon = 0.5LSB_{s-e} \tag{3.34}$$

From Equation (3.30), the settling time is found as follows:

$$t_{sett} = -\tau ln\left(\frac{\epsilon}{\Delta V}\right) \tag{3.35}$$

Considering minimum-size switches, the settling time $t_{sett,calc}$ estimated from (3.35) for the worst case of D_{IN} is 12 ns. The ADC presented in this work reserves approximately 60 ns for the DAC settling time and the preamplification. In order to relax the requirements on both speed of the preamplifier and output resistance of the circuit providing the reference voltages, a DAC settling time less than 5 ns is aimed. This can be easily achieved by increasing the size of the switches in order to reduce their on-resistance, calculating again the settling time and checking if it is short enough. In this work the following dimensions have been used:

$$\left(\frac{W}{L}\right)_{PT,V_{REFN}} = \frac{6}{1} \quad \left(\frac{W}{L}\right)_{PT,V_{REFP}} = \frac{18}{1}$$
$$\left(\frac{W}{L}\right)_{TG,BP,N} = \frac{6}{1} \quad \left(\frac{W}{L}\right)_{TG,BP,P} = \frac{18}{1} \quad \left(\frac{W}{L}\right)_{PT,V_{CM}} = \frac{4}{1}$$

where $PT_{V_{REFN}}$ and $PT_{V_{REFP}}$ are the pass-transistors providing V_{REFN} and V_{REFP} respectively, $PT_{V_{CM}}$ is the pass-transistor passing V_{CM} and $TG_{BP,N}$ and $TG_{BP,P}$ the NMOS and the PMOS transistors composing the transmission gate TG_{BP}. Considering V_{REFP} as reference voltage, the settling time $t_{sett,calc}$ calculated using Equation (3.35) is 4.10 ns, while the Cadence simulation of the circuit returns $t_{sett,sim} = 5.17\ ns$. Some values calculated using this method are reported in Table 3.4 and compared with the results given by the simulation using different switches sizes and both reference voltages. As shown, it is possible to obtain a first rough estimation of the worst-case settling time with this method.

	$t_{sett,calc}$ [ns]	$t_{sett,sim}$ [ns]
Minimum-size switches		
$V_{REFP} = 2.65\ V$	12.00	13.91
$V_{REFN} = 0.65\ V$	11.87	13.15
Chosen switches		
$V_{REFP} = 2.65\ V$	4.10	5.17
$V_{REFN} = 0.65\ V$	4.05	5.18

Table 3.4: Calculated and simulated settling time for D_{IN} transiting from 0 to 256.

3.3.3 Other Switches

So far, all the bottom-plate switches have been sized except the transmission-gate TG_{Sig} which is directly connected to the input signal. This has been

sized to achieve a short settling time and good linearity, which will be further discussed and analyzed in Section 3.4. Finally, for the top-plate NMOS pass-transistor which resets the V_L node, since low parasitic capacitance are required on that node (Appendix 5.1), a minimum-size transistor has been used. The LSB-subarray presents a relatively small equivalent capacitance, hence even the minimum-size switch is sufficient to perform the reset. The aspect ratios of the transistors composing these switches are summarized as follows:

$$\left(\frac{W}{L}\right)_{TG,Sig,N} = \frac{10}{1} \quad \left(\frac{W}{L}\right)_{TG,Sig,P} = \frac{30}{1} \quad \left(\frac{W}{L}\right)_{PT,Res} = \frac{2}{1}$$

3.4 Comparator

The comparator is an essential part in the SAR ADC to perform the binary search algorithm. It has to discriminate voltage values as small as the differential LSB_{d-e}. In addition, since it is usually the most power-hungry part of the ADC, a power-efficient solution has to be found during the design.

3.4.1 Overview

During the binary search phase, the comparator has to discriminate which of the MSB sub-array top-plate nodes has higher voltage. This information is passed then to the SAR logic control which can provide the correct digital input value for the DAC. Ideally, only one latch is required to perform the comparison. However, this is not feasible in reality because the latch usually has a very high offset voltage and can introduce large kickback noise. In this work, the comparator is composed of two preamplifiers and a latch, as shown in Figure 3.20. The latch is then loaded with a digital logic that reduces the metastability effect.

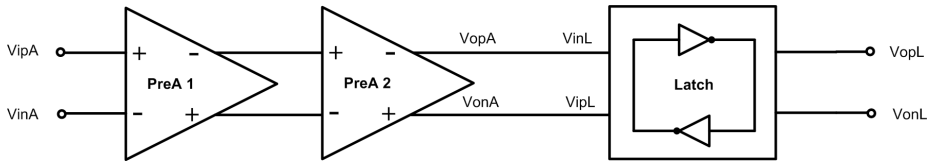

Figure 3.20: Structure of the comparator stage.

The proposed structure has been chosen for the following main reasons:

- Preamplification is required to overcome the offset voltage of the latch, especially for small input voltage values.
- Offset-cancellation techniques can easily be applied to the preamplifier stage, allowing a correct decision for the comparison.

- The large kickback noise coming from the latch and affecting the capacitive array is reduced due to the presence of the preamplifier.
- There is a minor kickback noise given by the preamplifiers. This can be reduced using two preamplifier stages while limiting the voltage gain of the first one.

3.4.2 Latch

In order to derive the design choices for the preamplifier, the latch stage is first presented. The dynamic latch [16, 17] shown in Figure 3.21 has been chosen to reduce the power consumption. When the control signal LatxS is low, the reset phase is performed and the output nodes are pulled to V_{DD}. During the regeneration phase, LatxS is set to '1' and the circuit determines which input signal is higher with the aid of the two cross-coupled inverters M19, M23 and M20, M22. The decision is therefore taken on the rising edge of the signal LatxS, as shown in Figure 3.22.

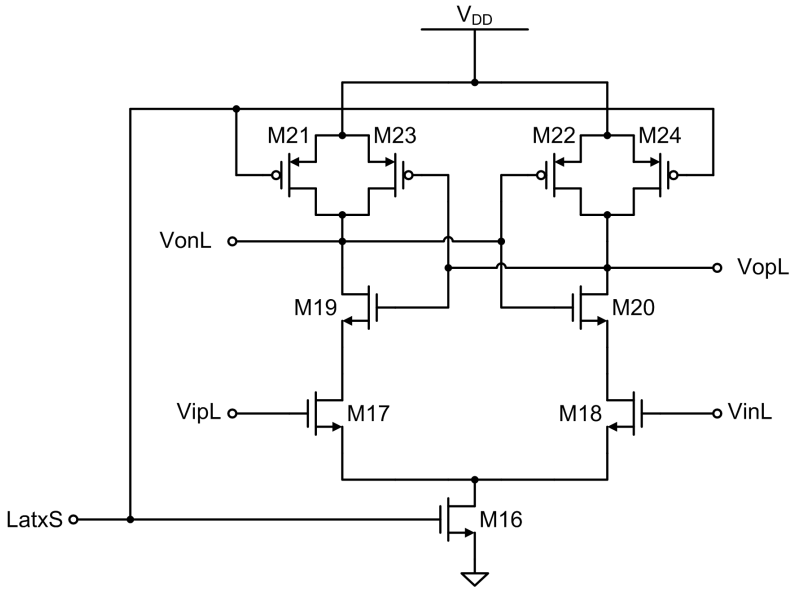

Figure 3.21: Dynamic latch.

Since this latch is dynamic, the power consumption is reduced. This is true because the latch consumes power only when it is triggered. Otherwise, during the reset phase, no static current is flowing through it. In addition, it presents a high speed operation because the NMOS transistors M17-20 immediately enter the active region when the latch is triggered. This is happening since, immediately after the reset phase, the source node voltages of M19 and M20 are equal to $V_{DD} - V_T$ while the drain node voltage of M16 is V_T below the latch input common mode voltage [18].

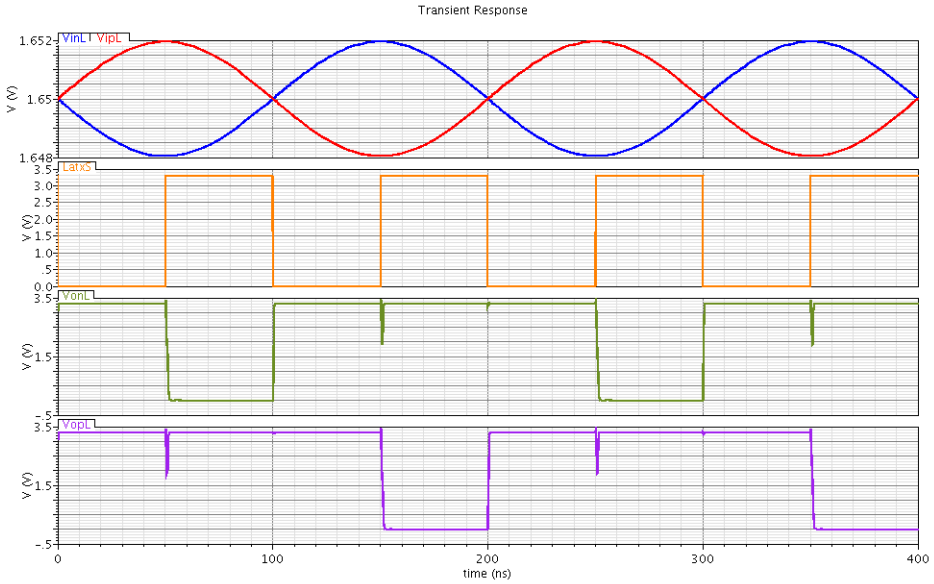

Figure 3.22: Output response of the latch for a differential sinusoid input signal.

Metastability is an important issue while designing comparators, hence the logic shown in Figure 3.23 has been chosen as load of the latch in order to limit its influence. During the reset phase (LatxS signal low) the output logic states Q and $\overline{Q}$ are kept at the same value, while during the regeneration phase (LatxS signal high) they provide the output of the result given by the latch. In case of a metastability error, both output nodes of the latch remain close to V_{DD} and the output logic maintains the previous values. Hence, the error due to metastability is bounded in a range equal to ± 1 LSB_{d-e}.

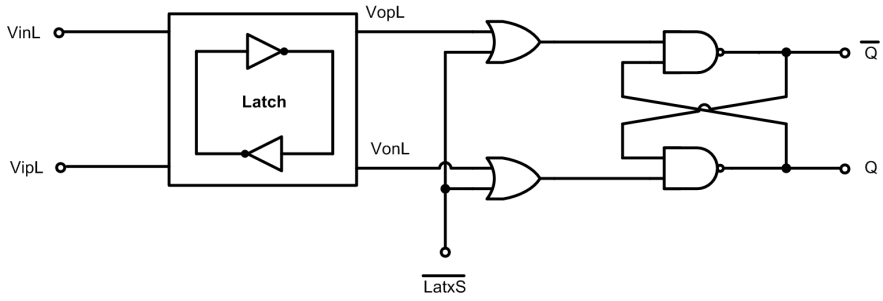

Figure 3.23: Load of the dynamic latch.

Since the input capacitance of the OR gates is approximately 4 fF, the performance of the latch has been tested considering a generic output load C_L of 20 fF in order to have some margin. Considering the maximum transition of 3.3 V as reference value for the differential output, both regeneration and reset time have been measured to be always less than 3 ns (Figure 3.24),

even for the voltage input as small as 1 LSB_{d-e}. However, given that the following OR gates can toggle with a smaller than 3.3 V differential output voltage and the input signal of the latch is already amplified by the previous stages, enough margin is reserved. Therefore, for the timing diagrams, the interval between the rising edge of LatxS and a valid output logic state of Q is chosen to be equal to 3 ns.

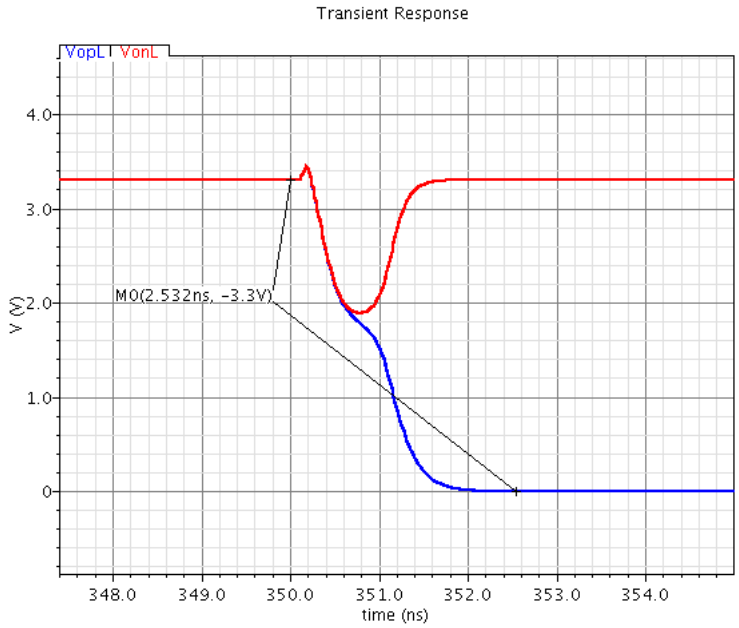

Figure 3.24: Output response of the latch during the regeneration phase..

The power consumption of the latch can be estimated considering the following formula where I_{Avg} is the average current provided by the power supply:

$$P_{Latch,Sim} \approx V_{DD} I_{Avg} \tag{3.36}$$

Considering that both the regeneration and reset phase are performed ten times over a 781 ns conversion time and 1'000 cycles are simulated, the estimated power consumption of the latch $P_{Latch,Sim}$ is approximately 7.68 μW.

The input-referred offset voltage of the latch, $V_{OS,Latch}$, has been estimated using the test bench [19] shown in Figure 3.25. The common-mode voltage V_{CM} is applied to an input node of the latch while a ramp signal is controlling the other one. The ramp signal starts with a value lower than V_{CM} and increases with 1 mV steps. The regeneration phase is therefore performed for each voltage level given by the ramp signal. Ideally, the latch starts toggling when the ramp signal is larger than V_{CM}. In a real circuit, the corresponding differential input voltage is equal to $V_{OS,Latch}$ instead of zero, as shown in Figure 3.25. The value of the input-referred offset voltage

of the latch is therefore estimated by carrying out a 1'000-runs Monte Carlo simulation and measuring the differential input voltage. The results are the following:

- $\mu(V_{OS,Latch}) = 122\ \mu V$
- $\sigma(V_{OS,Latch}) = 13.294\ mV$

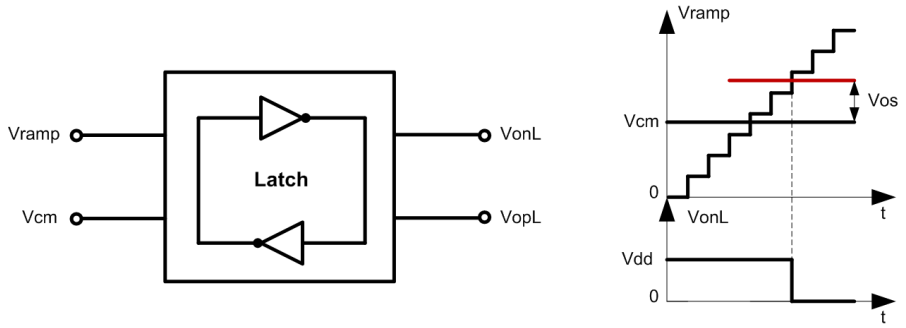

Figure 3.25: Test bench for the input-referred offset voltage estimation of the latch.

Since the standard deviation of $V_{OS,Latch}$ is much larger than its mean value, an estimation of the input-referred offset voltage value is obtained as follows:

$$V_{OS,Latch} \approx 3\sigma(V_{OS,Latch}) = 39.883\ mV \tag{3.37}$$

The offset value $V_{OS,Latch}$ of 40 mV will be considered in the forthcoming calculations. Note, from the above estimation, the preamplifier stage is essential since the smallest differential input to be discriminated by the comparator should be less than 1 LSB_{d-e}.

3.4.3 Preamplifier

Requirements

The preamplifier stage is mainly added to suppress the effect of the large kickback noise and offset voltage from the latch. It is a critical part in this design, and the following specifications have to be met:

- The preamplifier has to overcome the input-referred offset voltage $V_{OS,Latch}$ of the latch, which is approximately 40 mV. Since the minimum differential input value to be discriminated by the ADC is LSB_{d-e}, a required voltage gain $A_{V,OS}$ of the preamplifier can be estimated as follows:

$$A_{V,OS} = \frac{V_{OS,Latch}}{LSB_{s-e}} = \frac{40\ mV}{3.906\ mV} = 10.23 \approx 21\ dB \tag{3.38}$$

A 9 dB of margin can be added and thus the minimum voltage gain $A_{V,min}$ is equal to:

$$A_{V,min} = 21\ dB + 9\ dB = 30\ dB = 32 \tag{3.39}$$

- Considering 12 cycles for the SAR analog-to-digital conversion (Section 3.5) and 1.28 MS/s as sampling frequency, each cycle lasts 65 ns. In addition, reserving approximately 10 ns for both the regeneration phase of the latch and the settling time of the DAC, the preamplification of the input signal has to be performed in a time interval t_{PreAmp} less than 55 ns. In other words, the minimum differential input value LSB_{d-e} has to be correctly amplified during t_{PreAmp}.

- The power consumption of the entire ADC should be less than 1 mW, hence reserving half of this value to the preamplifier stage, the maximum power consumption for this part will be:

$$P_{PreAmp,max} = \frac{P_{ADC,max}}{2} = 500\ \mu W \tag{3.40}$$

- High values for the input capacitance of the preamplifier result in a large gain error for the DAC (Appendix 5.1). Therefore, the gate-area of the input transistors has to be minimized.

Two-stage preamplifier and kickback noise

The preamplifier chosen has two stages and its structure is shown in Figure 3.26. Since the required minimum gain is not particularly high for this type of structure, diode-connected PMOS transistors have been used as loads for the first stage while the second stage employs a resistive common-mode feedback (R-CMFB) circuit [12, 20] where both resistors R are 110 kΩ. Therefore, no active common-mode feedback network is required, leading to a low power consumption. Furthermore, the area occupied by the resistors is small because the process used provides a high-ohmic resistor option.

Since a small unit capacitor is used for the capacitor array, the preamplifier stage can influence the charge redistribution in the capacitor array due to its kickback noise. When the input signal is sampled on the top-plate node (V_M) of the MSB sub-array, this value is immediately amplified by the preamplifier. However, due to the presence of the gate-to-drain overlap capacitance C_{GD1} of the input transistor, the larger variation of the output voltage of the first preamplifier can affect the node V_M through this capacitive path (Figure 3.27). This effect is called kickback noise [21]. If there is a positive voltage step of V_M, the kickback noise effect will decrease this step size like that in a negative feedback loop. Clearly, the kickback noise also affects the reference voltages given by the DAC during the binary search.

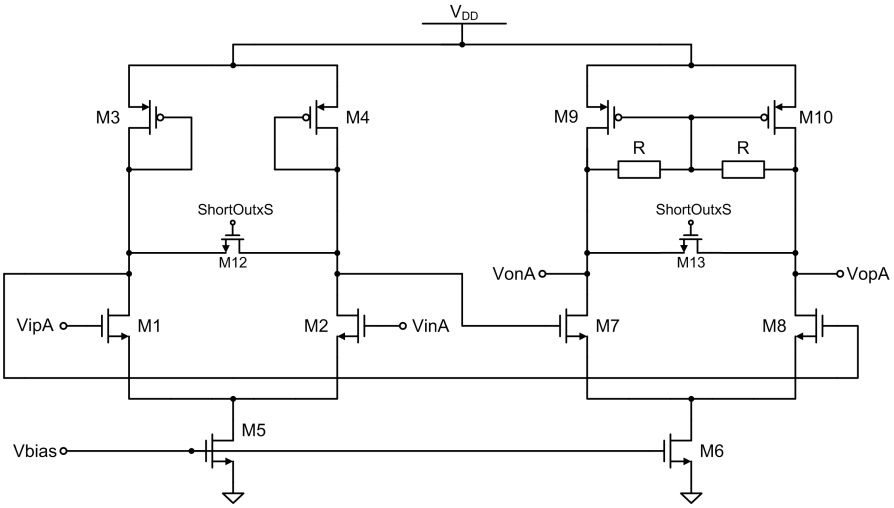

Figure 3.26: Two-stage preamplifier.

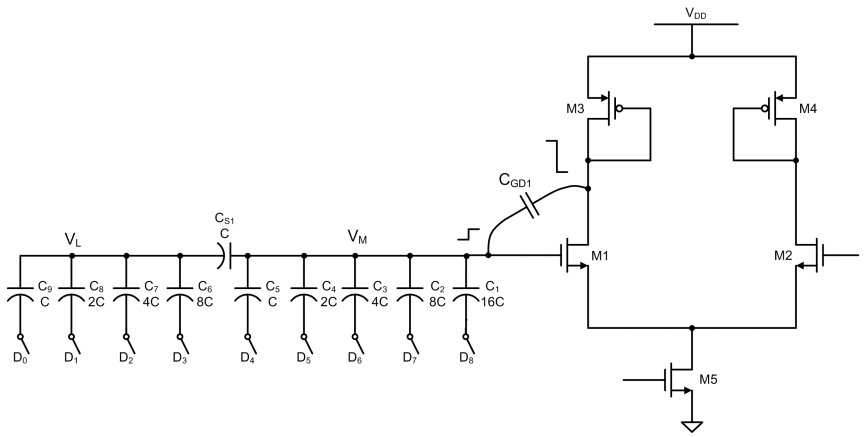

Figure 3.27: Kickback noise in the first stage of the preamplifier.

The analysis with the linear small-signal model of the transistors shows that the given error is proportional to the voltage gain of the preamplifier, as expected. Hence, the input voltage values of the comparator should be always scaled by the same factor, avoiding any distortion on the signal. However, since the range of the input voltage is relatively large (equal to 2 V considering only one of the two branches), the first stage of the preamplifier may saturate. In this case, the output response of the preamplifier is not linear anymore and the kickback noise is causing a distortion on the input signal and, hence, limiting the linearity of the ADC.

For this reason, a two-stage structure has been chosen for the preamplifier where the first stage has a low voltage gain, which helps to reduce the error caused by the kickback noise. Note that this design choice allows

also the use of small input transistors, leading to a small input capacitance from the preamplifier as well. The linearity of the sampled signal has been evaluated with a FFT analysis. For this simulation, a differential sinusoidal voltage signal has been applied to the input of the ADC with peak-to-peak amplitude close to FS_{d-e} and a frequency equal to BW_{Sig}. This results in an SNDR equal to 69.92 dB (ENOB=11.32). Since the value obtained is larger than 62 dB (ENOB = 10), a sufficient linearity is achieved during the sampling phase. However, it is preferable to have some margin on this value. This is obtainable by reducing the effect of the kickback noise even more with the the capacitive neutralization technique [21, 22]. Since the output voltages are affecting the input nodes through the gate-drain overlap capacitances of the input transistors, it is possible to add two dummy transistors that approximately present an input capacitance close to C_{GD1} as shown in Figure 3.28. To achieve this requirement, the dummy transistors are sized using the same channel length and half of the width of the input pair M1, M2:

$$\left(\frac{W}{L}\right)_{Dummy} = \frac{1}{2}\left(\frac{W}{L}\right)_{1} \tag{3.41}$$

Therefore, the kickback noise through these overlap capacitances is reduced and the improvement on the sampling linearity can be checked again with a FFT analysis that returns an increased SNDR of 81 dB (ENOB=13.21).

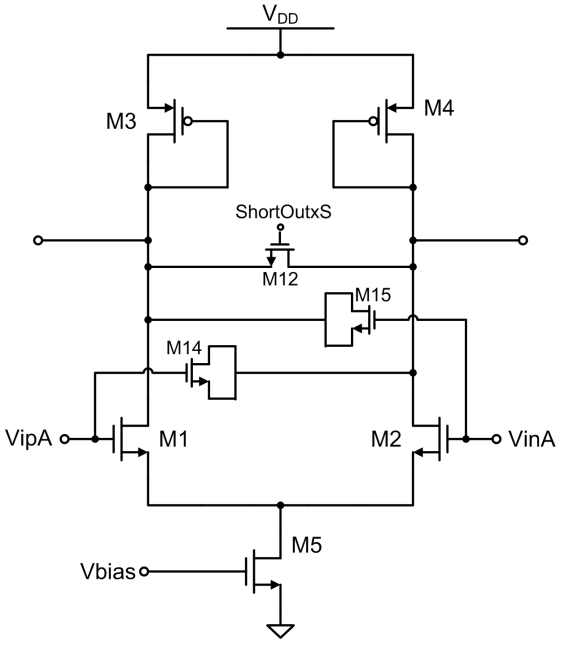

Figure 3.28: First preamplifier stage with dummy transistors using the capacitive neutralization technique.

Offset Cancellation and Sampling

The offset of the comparator, which is constant and signal-independent, causes also an offset of the ADC. This problem can be avoided limiting or cancelling the offset at the comparator stage. The most famous offset cancellation techniques [12, 23] are summarized as follows:

- *Input offset storage (IOS)*: two relatively large series capacitors are added to the input nodes of the comparator and the preamplifier is placed in a unity-gain negative-feedback loop operation. The offset of the circuit is therefore measured and stored across the capacitors. The residual input-referred offset voltage after the cancellation is the following:

$$V_{OS,Residual} = \frac{V_{OS,PreAmp}}{1 + A_V} + \frac{\Delta Q}{C} + \frac{V_{OS,Latch}}{A_V} \tag{3.42}$$

  where C is the value of each series capacitor and ΔQ the charge-injection due to the mismatch of the loop switches. As a drawback, this technique requires a high gain value A_V and also a large capacitance to limit the the charge-injection error.

- *Output offset storage (OOS)*: the series capacitors are now added to the output nodes of the preamplifier and the input nodes of the preamplifier shorted together during the offset cancellation. The nodes of the capacitors not connected to the preamplifier are also shorted together and thus the amplified offset voltage is stored on the capacitors. The residual offset is given by the following equation:

$$V_{OS,Residual} = \frac{\Delta Q}{A_V C} + \frac{V_{OS,Latch}}{A_V} \tag{3.43}$$

  Hence, the offset of the preamplifier is completely cancelled and the value of the series capacitor can be chosen smaller than before. However, since the preamplifier is performing an open-loop amplification, it should not saturate. For this reason, the voltage gain is usually limited to be less than 10.

- *Active offset cancellation*: The main drawback of the previous offset cancellation techniques is that they introduce capacitors in the signal path. A possible solution is to perform the offset cancellation using an auxiliary amplifier. The introduced amplifier can sense and subtract the offset of the stage in a negative feedback loop. Obviously, this technique is adding a new active element to the circuit, increasing the overall power consumption.

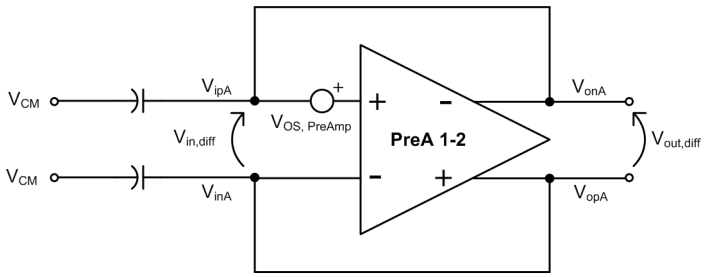

Figure 3.29: Closed-loop operation of the preamplifier performing the input offset storage.

In order to achieve a low-power operation for the presented SAR ADC, the active offset cancellation can be discarded. Also the OOS technique is not a promising solution because it requires additional output series capacitors and limits the gain of the preamplifier. Hence, the IOS has been chosen since the capacitor arrays can be used as input series capacitances and there is no limitation on the voltage gain. In addition, the entire array of capacitors present a large equivalent capacitance that reduce the residue offset caused by the charge injection mismatch, as shown in Equation (3.42), while providing a sufficient phase margin during the closed-loop operation of the preamplifier.

In order to better understand the offset cancellation technique chosen, the equivalent circuit of the preamplifier placed in the closed-loop operation is shown in Figure 3.29 where the offset voltage $V_{OS,PreAmp}$ is added and each capacitive array is replaced with a series capacitor, respectively. Defining $V_{in,d}$ and $V_{out,d}$ as the differential input and output voltage of the entire preamplifier, the system of equations to be solved is the following:

$$\begin{aligned} V_{out,d} &= V_{in,d} \\ V_{out,d} &= (V_{in,d} + V_{OS,PreAmp})(-A_V) \end{aligned} \tag{3.44}$$

where the DC gain of the preamplifier is equal to $-A_V$ (unity-gain negative-feedback). Solving the above equations, the result is the following:

$$V_{out,d} = V_{OS,PreAmp}\frac{-A_V}{1+A_V} \tag{3.45}$$

Referring the value obtained back to the input:

$$V_{in,diff} = \frac{V_{out,diff}}{A_V} = -\frac{V_{OS,PreAmp}}{1+A_V} \tag{3.46}$$

That is the residual offset voltage of the preamplifier mentioned in Equation (3.42).

At this point, it is possible to have an overview of the whole analog part of the SAR ADC and better understand how both sampling and offset

cancellation are performed. The simplified equivalent circuit of the previous designed circuits is shown in Figure 3.30 and the corresponding timing diagram is represented in Figure 3.31.

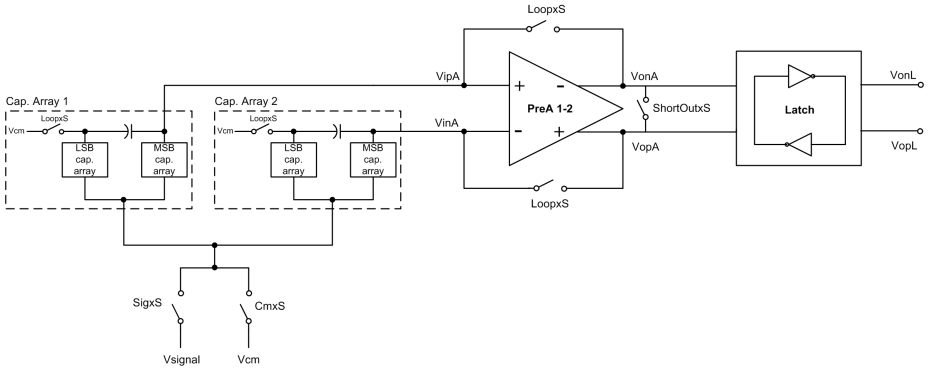

Figure 3.30: Simplified equivalent circuit of the analog part of the ADC.

In Figure 3.30 the preamplifier stages are represented as 'PreA 1-2'. Initially, the input signal is applied to the bottom-plate nodes of the capacitive array, the loop for the offset cancellation is closed and the output nodes of each preamplifier are shorted together using switches. In this way, each stage of the preamplifier is reset in a short period of time. After turning off the ShortOutxS control signal, the loop can effectively perform the offset cancellation. Once the loop is open, also the path passing the input signal can be disconnected and the common-mode voltage is connected to the bottom-plate of each capacitor in the arrays. In order to correctly perform the bottom-plate sampling, the loop switches have to be open before the switches connected to the input signal, whose charge injection is signal-dependent. Therefore, any distortion effect is avoided on the sampled signal at the input nodes of the comparator.

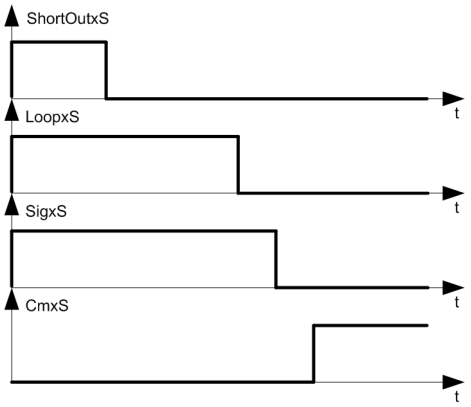

Figure 3.31: Sampling timing diagram example.

Using the resistive common-mode feedback for the second stage, the top-plate nodes of the MSB capacitor arrays are correctly reset during the offset cancellation phase by the closed-loop operation, without the need of other switches. The reset voltage value V_{RES} for these nodes is approximately 1.70 V while the top-plate nodes of the LSB sub-array are reset to V_{CM} using two minimum-sized switches. After the signal has been sampled on the input nodes of the preamplifier, the circuit can start the binary search algorithm.

Design, Analysis and Simulation

The optimization of the preamplifier stage requires a thorough study of the most relevant parameters in order to meet all the requirements. An analytical analysis has been first conducted and the performances are checked with Cadence simulations.

Considering first the power-speed trade-off, a tail current I_{Tail} of 10 μA is reserved for each stage. The power consumption of the preamplifier is therefore estimated as follows:

$$P_{PreAmp} \approx 2V_{DD}I_{Tail} = 66\ \mu W \tag{3.47}$$

Considering also the bias current, an overall power consumption of 75 μW can be expected, which is less than the value reserved during the definition of the requirements.

The differential voltage gain A_V of the preamplifier is defined as the product of the differential voltage gains of the first and second stage, A_{V1} and A_{V2} respectively:

$$A_V = A_{V1}A_{V2} \tag{3.48}$$

where the differential gain of each preamplifier stage is approximately the following:

$$A_{V1} = \frac{g_{m1}}{g_{m3} + g_{ds1}} \approx \frac{g_{m1}}{g_{m3}} \tag{3.49}$$

$$A_{V2} = \frac{g_{m7}}{g_{ds9} + \dfrac{1}{R} + g_{ds7}} \approx g_{m7}R \tag{3.50}$$

where g_m is the transconductance and g_{ds} the output conductance of the transistors. The input transistors of both stages are operated in moderate inversion to improve the values of the respective transconductances while all the other transistors are operated in strong inversion.

Since the input capacitance of the latch is approximately 4 fF, the circuit has been simulated in Cadence considering a generic capacitive output load C_L of 20 fF to have some margin. The results obtained are summarized in Table 3.5 while the magnitude and phase diagrams of the open-loop transfer function is shown in Figure 3.32.

Parameter	Value
A_V	30.57 dB
$f_{-3\ dB}$	33.54 MHz
$GBWP$	1.13 GHz
Power	72.60 μW

Table 3.5: Preamplifier specifications.

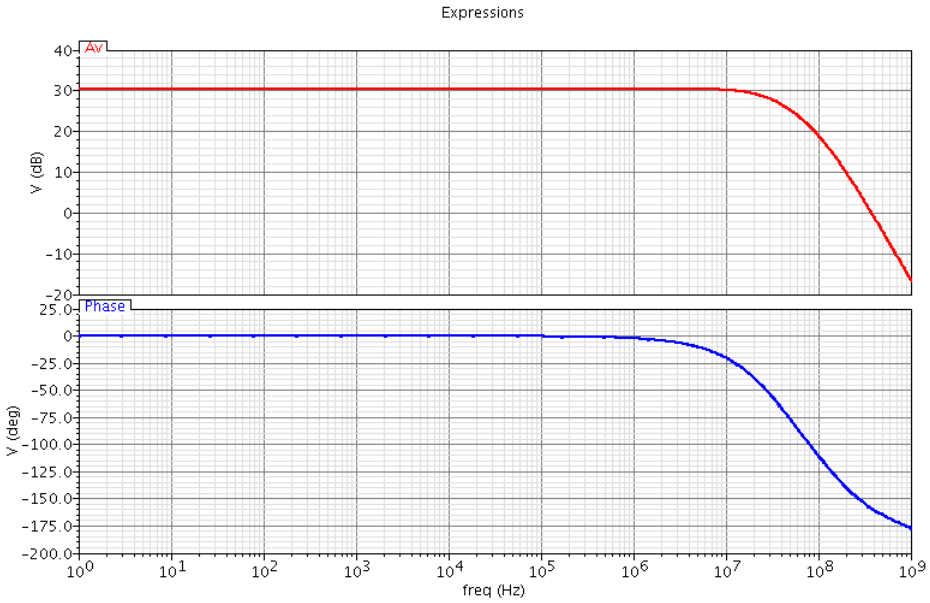

Figure 3.32: Magnitude and phase diagrams of the open-loop preamplifier transfer function.

The speed of the preamplifier is another important requirement to be considered during the design. Considering that a bit decision has to be taken approximately every 65 ns, the input signal should be correctly preamplified in a time interval t_{PreAmp} less than 55 ns. Applying a step input voltage equal to LSB_{d-e}, which is the minimum input value to be discriminated, the differential output voltage reaches 129.4 mV after only 20 ns. Hence, the input signal is sufficiently amplified in a short time interval since the output reaches a value larger than the input-referred offset voltage of the latch. Obviously, higher input values will achieve the requirements even faster. The step responses of the differential outputs for both the preamplifier stages are shown in Figure 3.33.

When the noise is considered, the first stage of the preamplifier is analyzed since it is the major contributor. Both thermal and flicker ($1/f$)

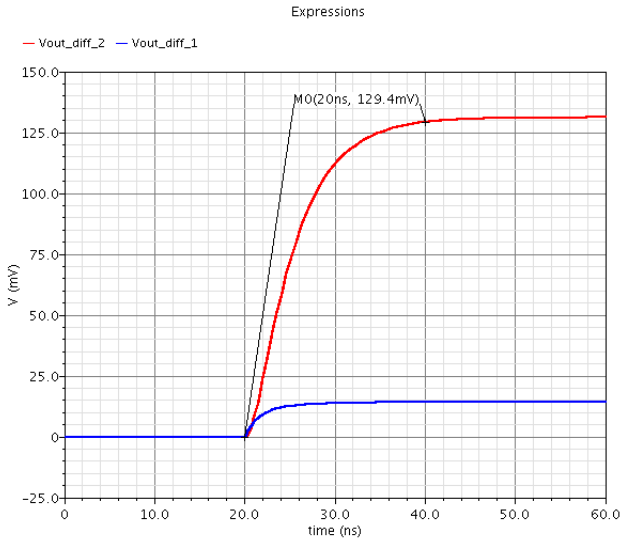

Figure 3.33: Step responses of the preamplifier stages for a LSB_{d-e} differential input. The blue trace represents the differential output voltage of the first stage, while the red trace shows the differential output voltage of the second stage.

input-referred voltage noises can be estimated respectively as follows:

$$\overline{e^2_{Thermal,in}} = \frac{8k_BT\gamma}{g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}\right) \tag{3.51}$$

$$\overline{e^2_{Flicker,in}} = \frac{2K_n^{(1/f)}}{C_{ox}W_1L_1}\frac{1}{f} + \frac{2K_p^{(1/f)}}{C_{ox}W_3L_3}\frac{1}{f}\left(\frac{g_{m3}}{g_{m1}}\right)^2 \tag{3.52}$$

where k_B is the Boltzmann constant, T the temperature expressed in Kelvin, $K^{(1/f)}$ a constant that depends on the technology, f the frequency, and γ a coefficient which is around $\frac{2}{3}$ for long channel devices and can be larger for deep sub-micron CMOS technologies. In order to evaluate the performance of the circuit, the noise of the entire preamplifier can be integrated over its frequency bandwidth and referred back to the input. In this way, it is possible to compare it with the $0.5LSB_{d-e}$ reference value. The noise bandwidth is the following:

$$BW_{Noise} = \frac{\pi}{2}f_{-3\ dB} = 52.68\ MHz \tag{3.53}$$

where $f_{-3\ dB}$ is the bandwidth of the preamplifier stage. In order to have some margin, a noise bandwidth BW_{Noise} equal to 1 GHz has been considered during the simulation. The integrated input-referred RMS value of the noise of the stage is:

$$[\sigma_{Noise,in}]_{1\ Hz}^{1\ GHz} = \frac{[\sigma_{Noise,out}]_{1\ Hz}^{1\ GHz}}{A_V} = 138.33\ \mu V_{RMS} \tag{3.54}$$

where $[\sigma_{Noise,out}]_{1\ Hz}^{1\ GHz}$ is the RMS value of the noise at the output nodes of the stage integrated on the 1 GHz bandwidth. Therefore, it is possible to estimate the input-referred noise and compare it with the $0.5LSB_{d-e}$ reference value as follows:

$$V_{Noise,PreAmp} \approx 3\,[\sigma_{Noise,in}]_{1\ Hz}^{1\ GHz} = 415.00\ \mu V \ll 0.5LSB_{d-e} \tag{3.55}$$

Since $V_{Noise,PreAmp}$ is much less than the $0.5LSB_{d-e}$ reference value, the stage has a good noise performance.

Statistic offset voltage can affect the performance of the preamplifier and hence of the entire ADC. The input-referred offset voltage of the first stage can be estimated as follows:

$$V_{OS,PreAmp} = V_{OS,1} + V_{OS,3}\frac{g_{m3}}{g_{m1}} \tag{3.56}$$

where $V_{OS,1}$ and $V_{OS,3}$ are the variables representing the equivalent statistic offset voltage values of M1, M2 and M3, M4 respectively. The variance of these variables can be found as follows:

$$\sigma^2(V_{OS}) = \sigma^2(\Delta V_T) + \sigma^2\left(\frac{\Delta\beta}{\beta}\right)\left(\frac{I_D}{g_m}\right)^2 \tag{3.57}$$

where ΔV_T and $\Delta\beta$ represent the threshold voltage and current factor mismatch respectively. Using Pelgrom coefficients [24, 25]:

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}} \tag{3.58}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} \tag{3.59}$$

From a 1'000-runs Monte Carlo simulation, the input-referred offset voltage $V_{OS,PreAmp}$ is estimated as follows:

$$V_{OS,PreAmp} \approx \frac{3\sigma(\Delta V_{OUT})}{A_V} = 20.66\ mV \tag{3.60}$$

where ΔV_{OUT} is the difference between the DC values of V_{opA} and V_{onA}. Since the offset voltage of the preamplifier stage is larger than LSB_{d-e}, an offset cancellation technique is required. The chosen input offset storage technique returns the following residual input-referred offset voltage after the cancellation:

$$V_{OS,Residual} = \frac{V_{OS,PreAmp}}{1 + A_V} = 594.40\ \mu V \tag{3.61}$$

Again, this residual voltage value can be compared to the $0.5LSB_{d-e}$ reference value and note that the smallest differential input signal can be therefore estimated after the cancellation.

The offset cancellation is performed in an unity-gain negative-feedback loop configuration during the sampling phase, hence, the stability of the stage has to be checked. The preamplifier reaches a phase margin PM of 78.40° during the closed-loop mode, providing a safe margin for the stability. Due to the large equivalent capacitance at the input nodes of the comparator provided by the capacitive array, the first dominant pole of the loop gain transfer function is shifted towards low frequencies, improving the stability of the system. The magnitude and phase diagram of the loop gain are shown in Figure 3.34.

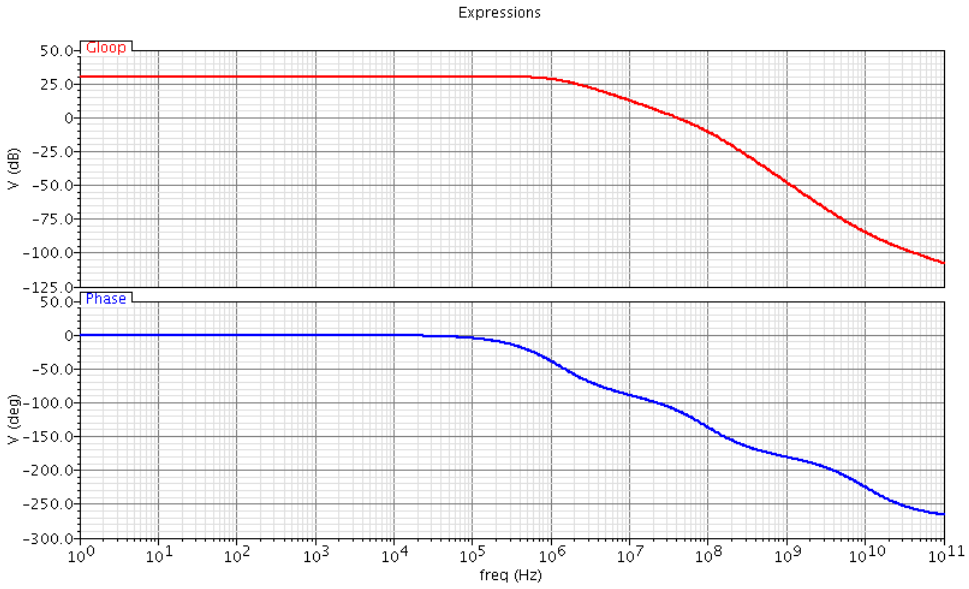

Figure 3.34: Magnitude and phase diagrams of the loop gain transfer function.

3.5 SAR Control Logic

A control logic is required to control both the S/H and the DAC, to finally perform the binary search algorithm. Once the latch has made its decision, the result is stored in the register and the DAC digital input is updated according to the decision. During this closed-loop operation, timing requirements have to be met and, again, low-power solutions are preferred.

3.5.1 Timing Diagrams

Since 16 ADCs are going to be implemented in the chip, a sampling frequency f_s of 1.28 MHz has been chosen during the elaboration of specifications in Section 2.2. Therefore, each ADC has a conversion time t_{conv} equal

to:

$$t_{conv} = \frac{1}{f_s} \approx 781\ ns \tag{3.62}$$

One analog-to-digital conversion is carried out in 12 clock cycles as designed in this work. While the first cycle is reserved to reset the output voltage of the comparator stages, the second one is used to sample the input signal. The remaining 10 cycles are required for the 10-bit conversion. Therefore, for each cycle the following time interval t_{cycle} is needed:

$$t_{cycle} = \frac{t_{conv}}{12} \approx 65\ ns \tag{3.63}$$

Hence, a master clock frequency f_{clk} equal to 15.36 MHz is required. The timing diagrams of the conversion are represented in Figure 3.35. All the digital control signals are generated from the master clock signal $ClkxC$ and a second clock signal $ClkdxC$ which is delayed by 3 ns with respect to $ClkxC$. Note that the digital signal $ClkdxC$ is mostly used to generate the short pulses that trigger the latch and allows the circuit to perform the bottom-plate sampling. Moreover, the digital signal $ShortOutxS$ is high to short the output nodes of each preamplifier, $LoopxS$ is the control signal that closes the loop, $SelInxS$ becomes high when the input signal is applied to the capacitive array, D_{IN} is the digital input of the DAC and $LatxS$ is the control signal for the latch. The signal $DigOutxS$ represents the first 9 bits of the output digital value while $SignxS$ is the MSB (sign bit). It is important to observe that D_{IN} is equal to $DigOutxS$ when its first 8 bits are determined (from cycle #4 to cycle #12) but it is reset at the beginning of the new conversion. The value of the last bit of $DigOutxS$ is instead assigned at this time, therefore the 10-bit output digital value is ready to be saved in a register during cycle #2, when the end-of-conversion signal $EocxS$ is high. During the first cycle the preamplifier stages are reset, as indicated from the digital control signal $ShortOutxS$ that is set to '1'. The input signal is effectively sampled on the bottom-plate nodes of the capacitors in the second cycle since $LoopxS$ and $SelInxS$ are both high. At this time the preamplifier is operating in closed-loop, hence also the offset cancellation is performed. $LoopxS$ is set to '0' before the ending of the cycle in order to realize the bottom-plate sampling. At the third cycle, all the bottom-plate nodes of the capacitors are connected to the common voltage (D_{IN} equal to '0') and the sampled charge is redistributed on the input nodes of the comparator. The first comparison can be therefore executed and the MSB is determined at the beginning of the fourth cycle when the latch is triggered. The timing diagrams of the first three cycles are shown in Figure 3.36.
At the beginning of the cycle #4 the reference voltages (V_{REFP} and V_{REFN}) are assigned to the corresponding capacitor arrays depending on the result of the last comparison and the DAC input signal is set to its half-range value. Hence, the cycles from #4 to #12 are used to determine the remaining 9

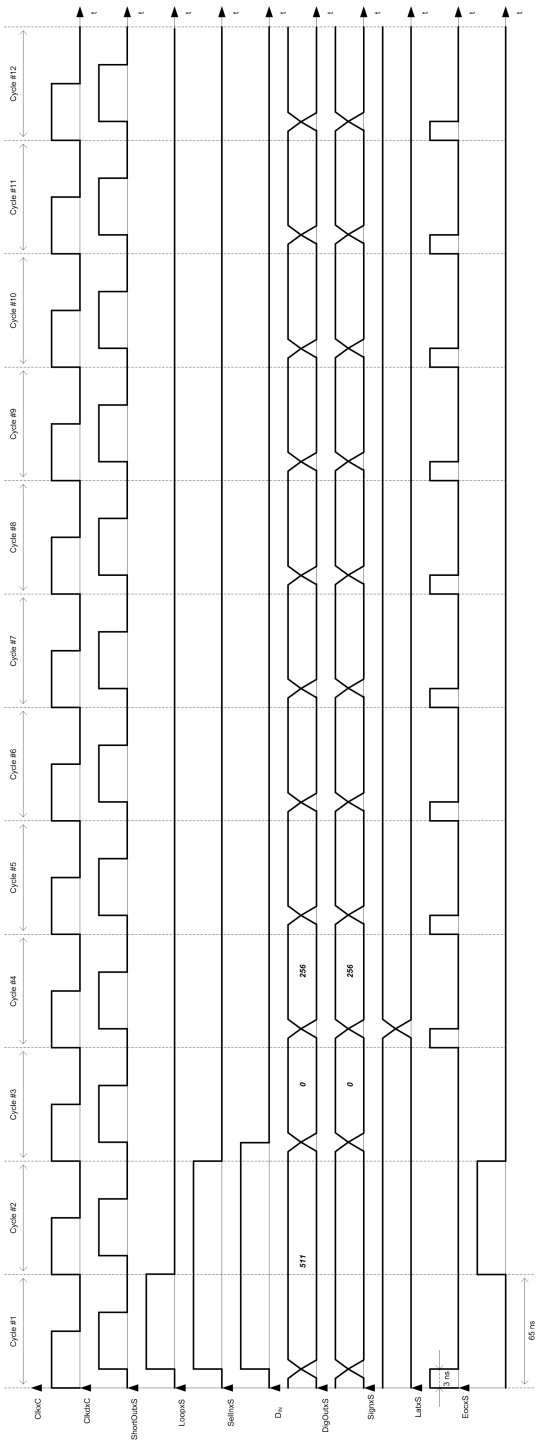

Figure 3.35: Timing diagrams of the SAR control logic.

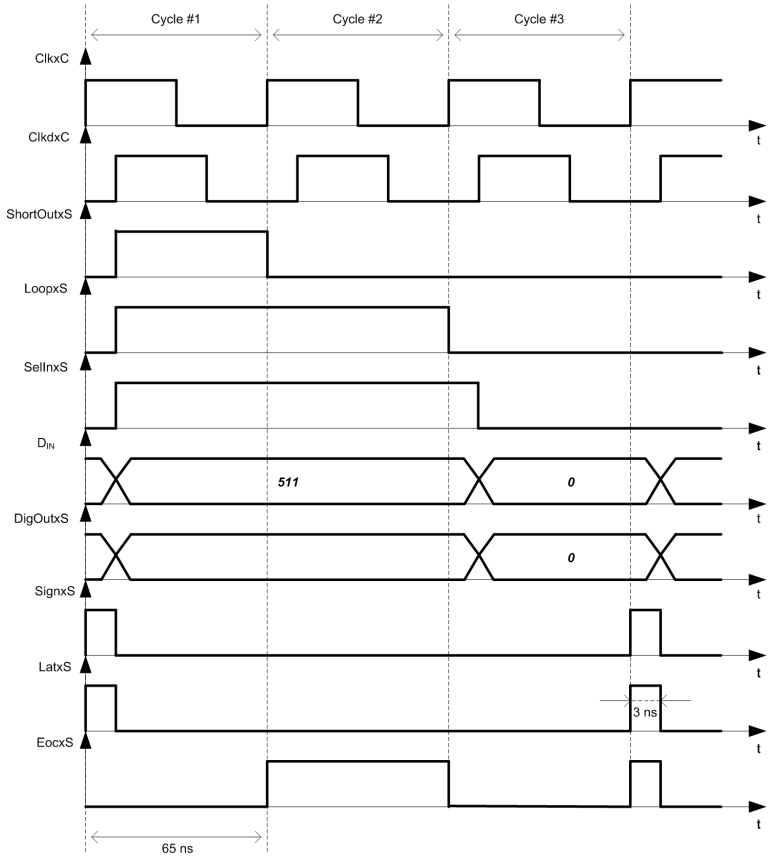

Figure 3.36: Timing diagrams for the first three cycles of a conversion.

bits with the binary search algorithm. In particular, at the beginning of each cycle, each DAC provides a new voltage value based on the previous bit-decision, while the preamplifier amplifies the difference between its input nodes and the latch makes a decision once it is triggered (when the $LatxS$ signal goes high). On the new cycle, the digital input D_{IN} of the DAC will be eventually updated depending on the previous comparison result and a new voltage value will be provided. A part from the fourth cycle, the remaining cycles are clearly all equal, as shown in Figure 3.37 where cycles #4, #5 and #6 are illustrated.

3.5.2 SAR Control Logic Implementation

The digital part of this ADC has been implemented as a successive approximation register (SAR) whose simplified structure is shown in Figure 3.38. Two rows of flip-flops are used to generate the digital input signal D_{IN} for the DAC: the first row is a shift register that shifts a logical '1' while each flip-flop of the second row is first set to logical '1' and then is eventually reset

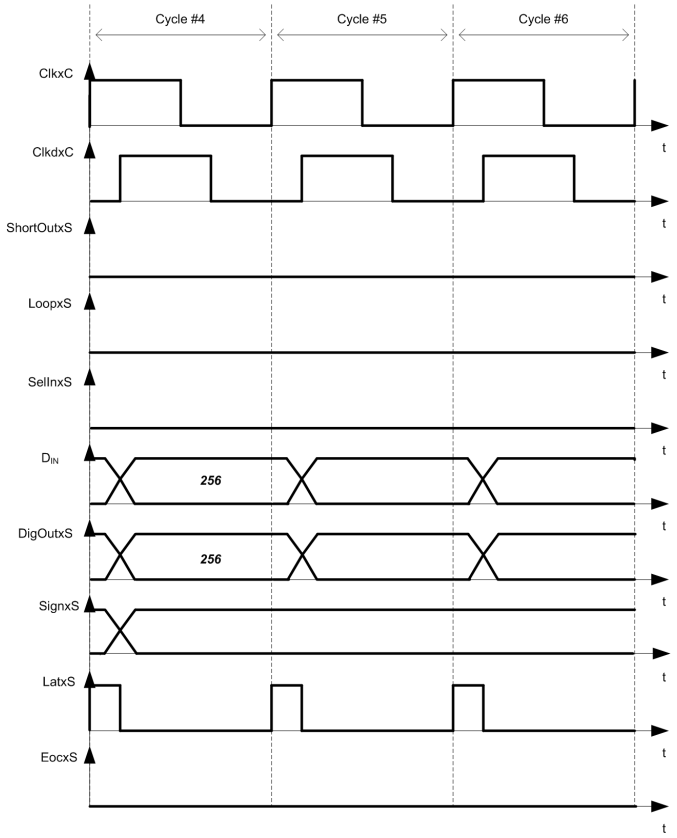

Figure 3.37: Timing diagrams of the cycles used to determine the last 9 bits of the digital output.

to logical '0', depending on the result of the comparison given by the signal $CompxS$. The solution presented is quite popular in SAR ADCs [26, 27] and it based on the design proposed in [28]. Considering the entire chip that will host the 16 SAR ADCs, the shift register can be shared among them in order to reduce both overall area and power consumption.

3.5.3 Delay Elements

A second clock signal delayed by 3 ns is required by the SAR control logic and it is generated using a chain of inverters accurately sized. In order to increase the delay, as shown in Figure 3.39, the chain consists of two inverters using transistors with larger length L equal to 4.2 μm and two minimum-sized inverters added both to the input and the output of the chain. This design choice allows to have larger output resistance for the sized inverters, increasing the time delay while minimizing the capacitive load for the driving circuit. The first two minimum-sized inverters are used to drive the structure while the last two one allow the circuit to achieve

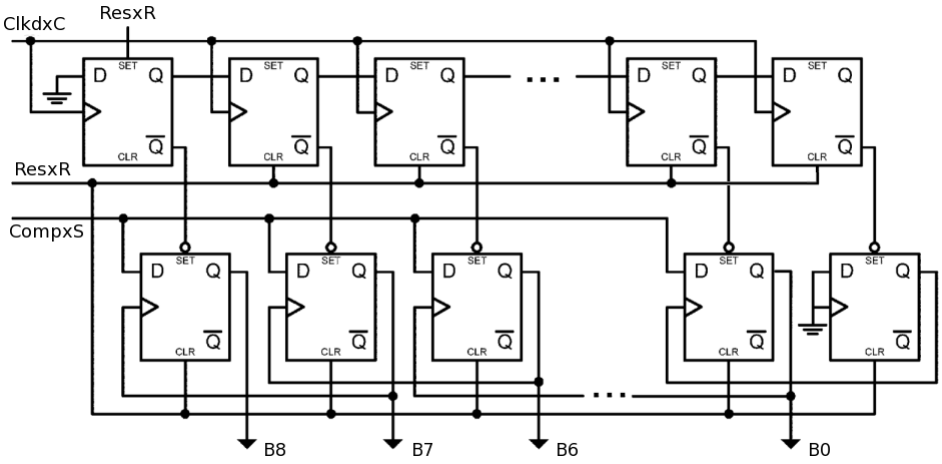

Figure 3.38: Successive approximation register for binary search.

shorter rise and fall time. A generic output load C_L of 10 fF has been used to evaluate the time delay t_D, the 10%-to-90% rise time t_R, the 90%-to-10% fall time t_F and the dynamic power consumption. Simulating the circuit, the values obtained are the following: a delay time t_D of 3.446 ns is achived, rise time and fall time are respectively equal to 248 ps and 186 ps, while the power consumption is equal to 21.043 μW. Nevertheless, this block can be shared among all the ADCs present on chip.

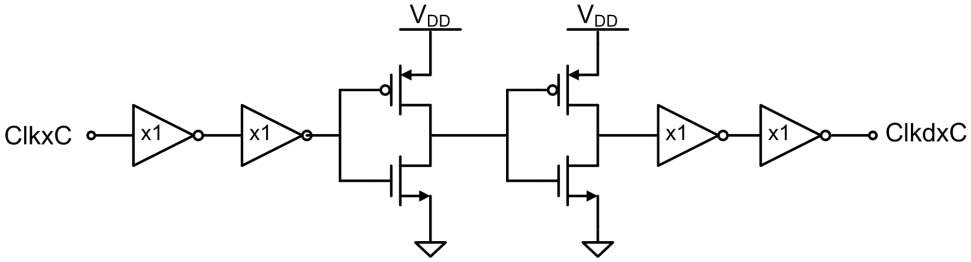

Figure 3.39: Chain of inverters to generate the delayed clock signal.

3.6 Layout

The layout of the entire SAR ADC is shown in Figure 3.40. The dimensions of this block are 395×391 μm^2, leading to an overall area A_{ADC} of $154'445$ μm^2. The floorplan is illustrated in Figure 3.41 where the different parts have been highlighted. These parts are the two capacitive arrays and their relative switches, the comparator and the digital part required for each ADC. As expected, the capacitive array occupies the largest amount of area among all blocks. The layout has been conducted while in a way to make

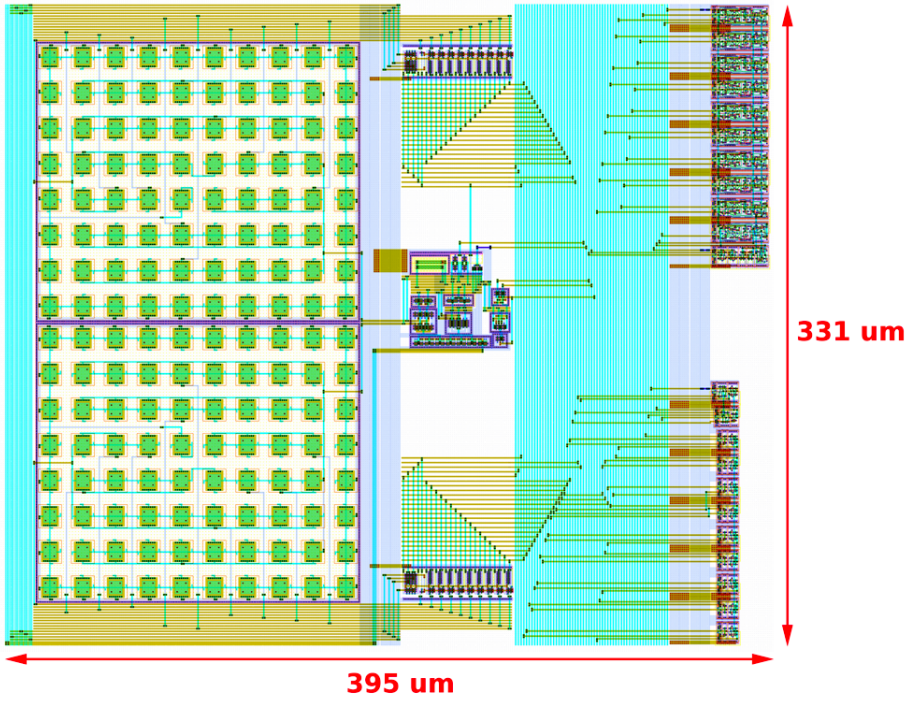

Figure 3.40: Floorplan of the SAR ADC.

a compact structure. However, the analog part has been placed at a safety distance of approximately 100 μm from the digital circuits to reduce the coupling noise coming through the substrate [29].
Some of the digital part of the ADC is shared among all the ADCs on chip (Section 3.5) and its layout is shown in Figure 3.42. The dimensions of this part are 142×87 μm^2, for an area $A_{DigShared}$ of $12'354$ μm^2.

Considering again the implementation of all the SAR ADCs on chip, at this point it is possible to estimate the overall required area. One possible floorplan for the MEA chip is to place 1'024 read-out channels on two sides of the chip, i. e., 512 channels are reserved for each side. Thus, the 16 SAR ADCs can also be split in two groups while adding the digital shared logic to each of them. The floorplan of the ADCs implemented on chip is shown in Figure 3.43. Hence, the overall area required on chip can be estimated as follows:

$$A_{ADC,Chip} = 16A_{ADC} + 2A_{DigShared} \approx 2.50mm^2 \tag{3.64}$$

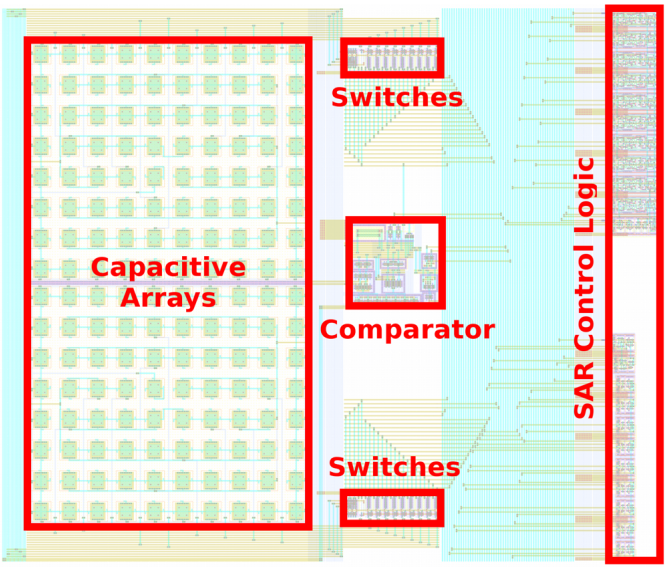

Figure 3.41: Analog and digital blocks composing the SAR ADC.

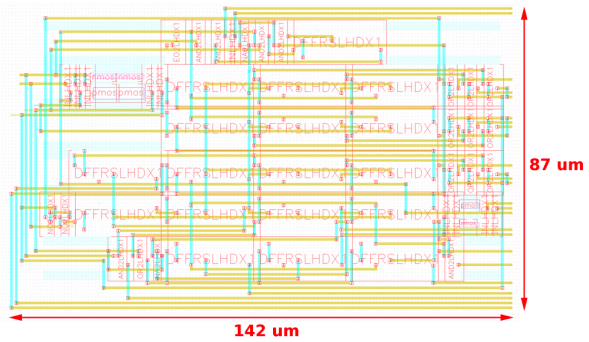

Figure 3.42: Layout of the shared digital logic among all the ADCs on chip.

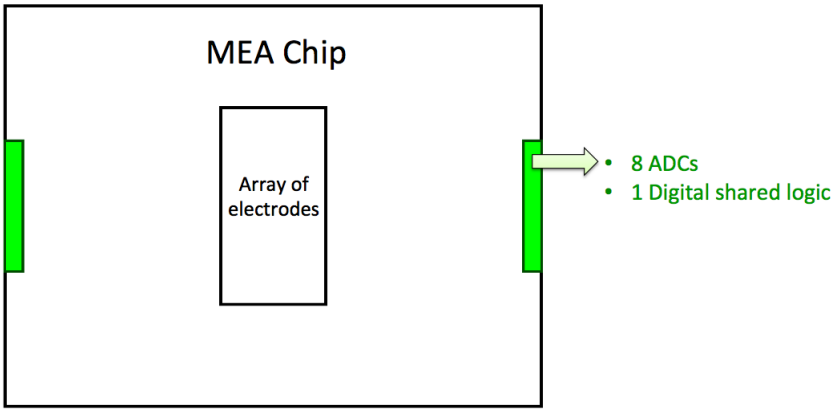

Figure 3.43: Floorplan of the ADCs integrated on the MEA chip.

Chapter 4

Simulations and Conclusions

4.1 Simulation Results

In order to evaluate the performance of the designed circuit, the characterization of the SAR ADC has to be conducted running different post-layout simulations. First of all, an example of analog-to-digital conversion is presented in Figure 4.1 where the reported voltage signals are measured at the input nodes of the preamplifier (V_{ipA} and V_{inA}). Both the sign-bit $SignxS$ and the remaining 9 bits $DigOutxS$ composing the digital output are shown as well. The conversion has been done for a constant analog input value whose amplitude is equal to the differential full-scale FS_{d-e}. Hence, the SAR ADC provides the highest value for the digital output. Note that $SignxS$ is equal to '1' if the differential input voltage is positive, while the remaining 9 bits are given by $DigOutxS$.

Differential and integral linearity errors (DNL and INL respectively) can be evaluated using the histogram test with a linear ramp input [4]. In this kind of simulation consists a large number of digitized samples is collected from the ADC for an input signal with known probability density function, such as a linear ramp. From the simulation results, both DNL and INL histogram plots can be derived and they are shown in Figures 4.2 and 4.3 respectively. Both DNL and INL errors are less than 0.5 LSB_{d-e} for each digital output. The resolution of the presented linearity analysis is equal to 0.05 LSB_{d-e}.

A 2'048-points FFT analysis is run to evaluate both the SNDR and SFDR of the converter. The sampling frequency f_s is set to 1.28 MS/s while the frequency of the input sinusoidal wave is close to 10 KHz which is the bandwidth BW_{sig} of the neural signals. The output of the FFT analysis is a power spectral density graph and is shown in Figure 4.4. The SFDR measured is 76.51 dB while the SNDR reaches 60.74 dB that leads to an ENOB of 9.79.

The power consumptions of both analog and digital parts of the ADC

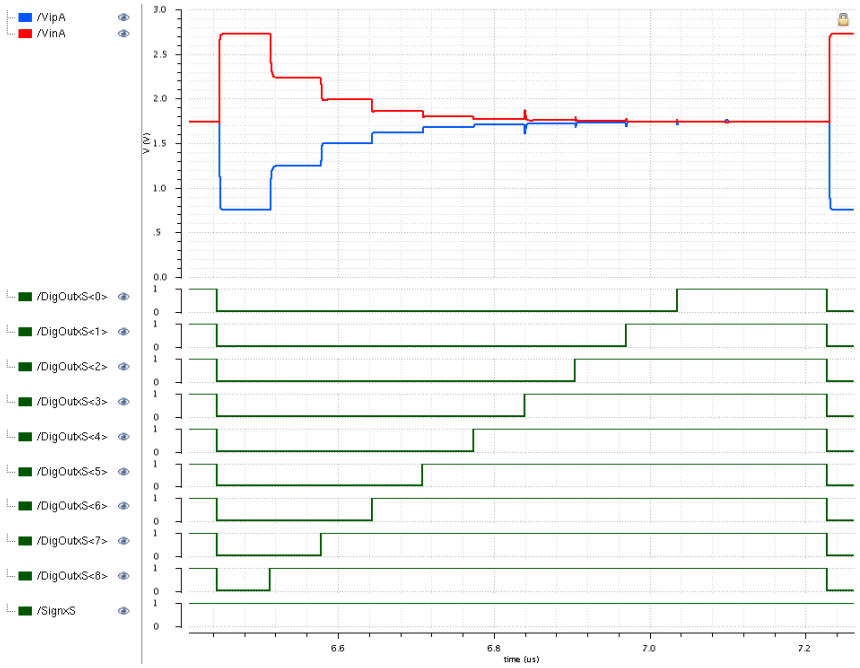

Figure 4.1: Example of an analog-to-digital conversion performed by the SAR ADC.

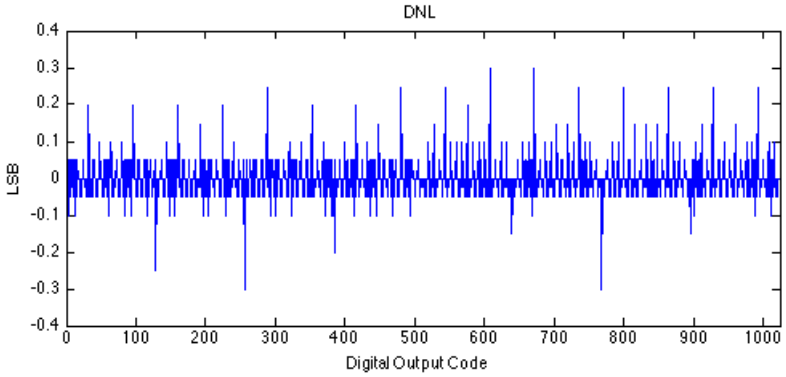

Figure 4.2: DNL histogram plot of the SAR ADC.

are finally measured. Note, the digital control logic is divided into two parts: one part is added to each converter (Digital) while the other one is shared all the ADCs (Shared digital) present on chip, as explained in Section 3.6. For this reason, in Table 4.1 the two different digital power consumptions are distinguished.
For the MEA chip application, the overall power consumption of the ADCs is therefore estimated as follows:

$$P_{Tot} = 16(P_{Analog} + P_{Digital}) + 2P_{SharedDigital} = 2.25\ mW \tag{4.1}$$

Altough the proposed data converter is not supposed to be general-purpose,

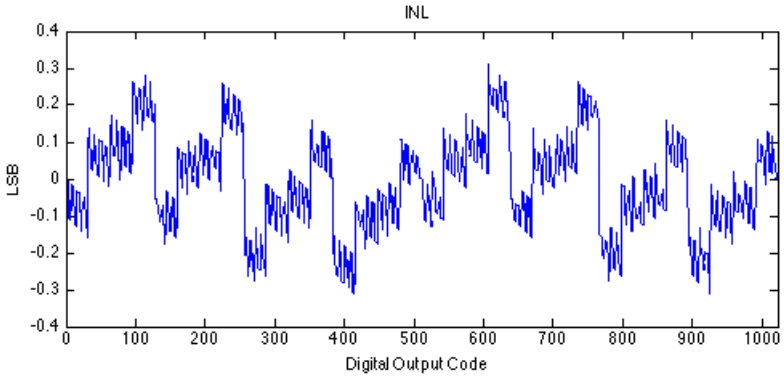

Figure 4.3: INL histogram plot of the SAR ADC.

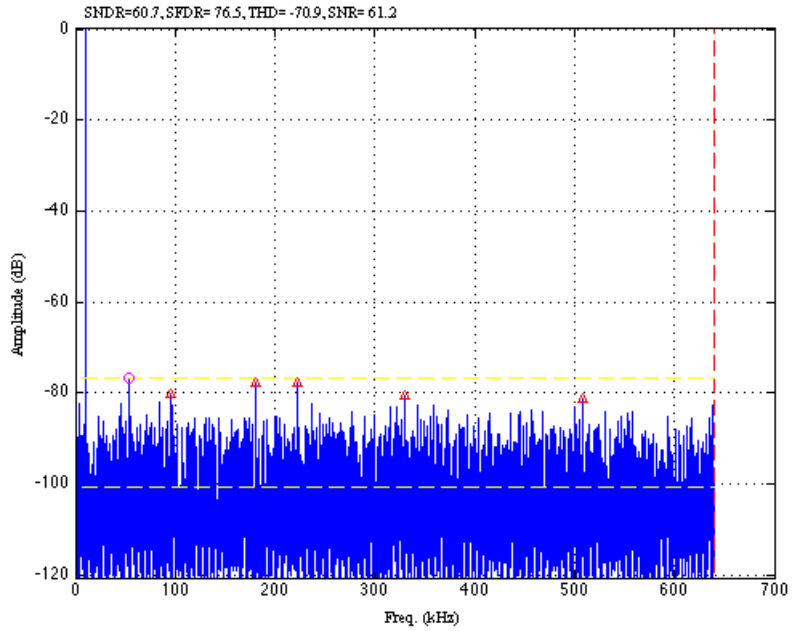

Figure 4.4: 2'048-points FFT output of the SAR ADC.

Part	**Power** $[\mu W]$
Analog	95.24
Digital	31.88
Shared digital	105.80

Table 4.1: Summary of the ADC power consumption.

its power efficiency can be estimated with the following figure of merit:

$$FoM = \frac{P_{ADC}}{2^{ENOB} f_S} \tag{4.2}$$

where P_{ADC} is the total power consumption of one ADC and, for the case presented, is estimated as:

$$P_{ADC} = \frac{P_{Tot}}{16} = 140.63\ \mu W \tag{4.3}$$

That leads to a FoM of 125 fJ/conv-step. Note that this figure of merit is calculated without considering the power consumptions of the multiplexers and buffers required by the system.

Table 4.2 summarizes and compare both the requirements and the estimated specifications for the designed SAR ADC. In addition, the performance of the proposed data-conversion system that can be integrated on the MEA chip is shown in Table 4.3. These results are compared with the specifications of the single-slope ADCs currently integrated on the latest version of the MEA chip.

Parameter	**Requirements**	**Estimated values**
Resolution	10 bits	
Sampling Rate	1.28 MS/s	
Supply Voltage	3.3 V	
Full Scale Range	2.0 V_{pp} (differential)	
DNL	< 0.5 LSB	+ 0.35 / - 0.35 LSB
INL	< 1 LSB	+ 0.35 / - 0.35 LSB
ENOB	9 bits	9.79 bits
SNDR	≥ 56 dB	60.74 dB
SFDR	-	76.51 dB
Area	≤ 1 mm^2	0.157 mm^2
Power Consumption	≤ 1 mW	140.7 μW
Technology	0.35 μm CMOS	

Table 4.2: Requirements and estimated performance of a single SAR ADC.

ADC	**Single-Slope**	**SAR**
Resolution	10 bits	
ENOB	9.7 bits	9.79 bits
Area	7.04 mm^2	2.50 mm^2
Analog Power Consumption	6.19 mW	1.53 mW

Table 4.3: Specifications of the single-slope data-conversion system currently implemented on chip, compared to the performance of the SAR ADCs.

4.2 Conclusions

The presence of integrated analog-to-digital converters on chip is an essential requirement for allowing a good signal transmission between the chip and the external devices. After comparing the most relevant topologies for data converters, the SAR ADC has been chosen since it is a promising solution that could meet the required specifications by multiplexing the read-out channels on the MEA chip. Both low power consumption and low complexity of the circuit are relevant advantages of the chosen ADC and key aspects to succeed in the design.

Switched-capacitor arrays are used to implement both the S/H and DAC while minimizing the value of the unit capacitor. The arrays are split in two parts to reduce the overall equivalent capacitance which is equal to 6.05 pF for a unit capacitor of only 64.36 fF. The capacitance provided by this part can be used to store the offset voltage of the preamplifier and cancel its effect on the ADC performance. In fact, the residual input-referred offset voltage of the amplifier is 594.40 μV after the cancellation, that is largely less than the LSB value. While considering the timing requirements, the sizes of the switches are optimized to reduce their area. In this work, the switches occupy only 1.72 % of the total area of the ADC. A low-power two-stage preamplifier is designed to improve the efficiency of the comparison and drive the input nodes of the latch. In fact, the preamplifier can overcome the large offset voltage of the latch, that is estimated to be 40 mV in the worst case. Moreover, the effect of the kickback noise caused by the preamplifier is reduced by using the capacitive neutralization technique, leading to ENOB of 13.21 for the linearity quality of the sampling. The digital part is implemented adopting a successive approximation register whose shift register is shared among all the ADCs present on chip, therefore saving the 67.23 % of the digital power consumption.

The ADC occupies an area of 0.157 mm^2 and presents an overall power consumption of 140.63 μW for a sampling frequency of 1.28 MS/s. From the post-layout simulation results, both DNL and INL errors are bounded in a 0.35 LSB range. Concerning the linearity of the ADC, an ENOB of 9.79 is obtained. The power efficiency is estimated with the FoM defined in (4.2), that is equal to 125 fJ/conv-step. Finally, comparing this simulation results with the specifications of the single-slope ADCs currently integrated on the latest version of the MEA chip, the proposed data-conversion system presents an improvement of 64.49 % in terms of area reduction and its analog power consumption is 4 times less.

In conclusion, the presented SAR ADC has proved to be a promising solution for low-power applications. All the preliminary requirements have been met and a good performance achieved. The specifications of the data-conversion system have been compared with the ADCs currently implemented on the MEA chip and a possible improvement of its performances

has been presented. The designed circuit is therefore ready to be integrated on chip for a final characterization based on real measurements.

Chapter 5

Appendix

5.1 Effects of the parasitic capacitances in the DAC

The equivalent circuit of the switched-capacitor DAC is shown in Figure 5.1 where m and p are the sums of the unit capacitors connected in parallel to the reference voltage in the LSB sub-array and MSB sub-array respectively (Section 3.2). In addition, the parasitic capacitances affecting both V_L and V_M nodes, C_{p1} and C_{p2} respectively, are added to the equivalent circuit. While C_{p1} is the bottom-plate parasitic capacitance of the series capacitor C, C_{p2} represents the gate capacitance of the input transistors of the comparator.

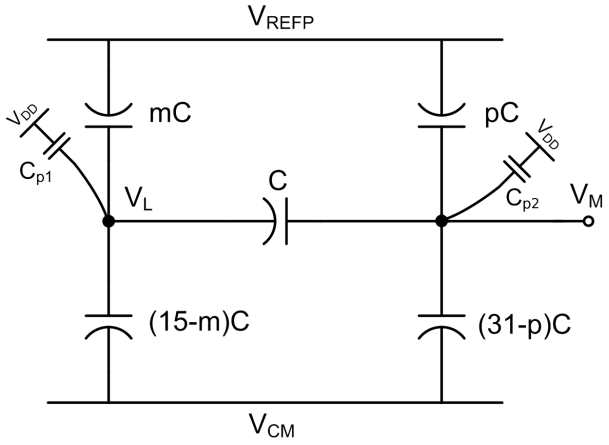

Figure 5.1: Switched-capacitor DAC equivalent circuit.

Considering first the ideal case where no parasitic capacitances are present in the circuit ($C_{p1} = 0$ and $C_{p2} = 0$) and assuming that all the capacitors are discharged before applying the digital input signal, the equations given

by the charge conservation principle are the following:

$$0 = mC(V_L - V_{REFP}) + (15 - m)C(V_L - V_{CM}) + C(V_L - V_M)$$

$$0 = pC(V_M - V_{REFP}) + (31 - p)C(V_M - V_{CM}) + C(V_M - V_L)$$

Solving the previous system of equations, the output voltage V_M of the DAC is:

$$V_M = V_{CM} + (V_{REFP} - V_{CM})\frac{m + 16p}{511} \tag{5.1}$$

If the parasitic capacitances are taken into account, the previous system of equations is modified as follows:

$$\begin{aligned} C_{p1}(V_{CM} - V_{DD}) &= mC(V_L - V_{REFP}) + (15 - m)C(V_L - V_{CM}) + \\ &\quad + C(V_L - V_M) + C_{p1}(V_L - V_{DD}) \end{aligned}$$

$$\begin{aligned} C_{p2}(V_{CM} - V_{DD}) &= pC(V_M - V_{REFP}) + (31 - p)C(V_M - V_{CM}) + \\ &\quad + C(V_M - V_L) + C_{p2}(V_M - V_{DD}) \end{aligned}$$

that results in the following output voltage V_M for the DAC:

$$V_M = V_{CM} + (V_{REFP} - V_{CM})\frac{m + 16p + pC_{p1}}{511 + 32C_{p1} + 16C_{p2} + C_{p1}C_{p2}} \tag{5.2}$$

It is therefore possible to study the influence of the parasitic capacitances on the DAC by comparing (5.2) with (5.1). In fact, while both parasitic capacitances are introducing a gain error, only C_{p1} is causing a distortion on the DAC, hence limiting its linearity. Finally, note that, since the gate capacitance C_{p2} is usually larger than C_{p1}, the gain error is mostly given by the gate capacitance of the comparator's input transistors.

5.2 Standard deviation estimation of the DAC output voltage

Considering a simple 3-bit binary-weighted switched-capacitor DAC, the analytical estimation of the standard deviation for its output voltage is presented in this section. The capacitive array and the equivalent circuit are shown in Figure 5.2. The output voltage of the 3-bit DAC for the half-range digital input code ($D_{IN} = 4 = 100$) presents the worst case in terms of mismatch among the capacitors [11], hence the constriction on the standard deviation of this voltage should satisfy the following condition:

$$3\sigma(V_{M,D_{IN}=4}) \leq 0.5LSB \tag{5.3}$$

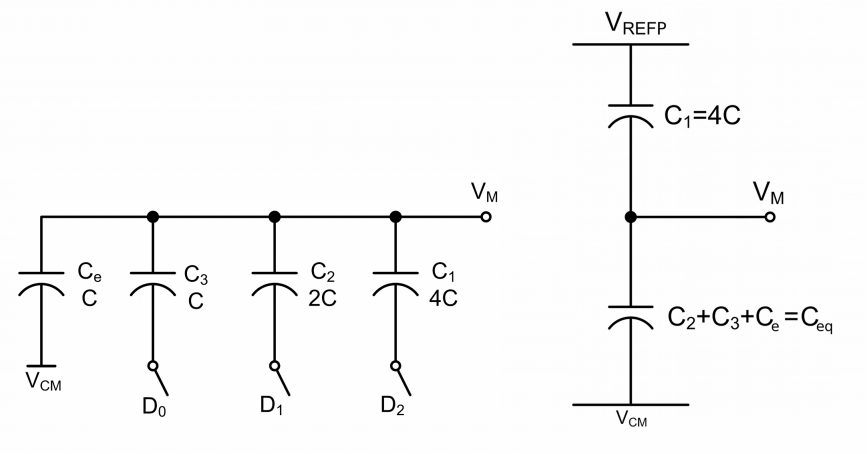

Figure 5.2: 3-bit switched-capacitor DAC and its equivalent circuit.

Defining C_{eq}=C+C+2C, the output voltage value for the half-range digital input code is the following:

$$V_{M,D_{IN}=4} = V_{CM} + (V_{REFP} - V_{CM})\frac{4C}{4C + C_{eq}} = 2.15\ V \tag{5.4}$$

Considering the capacitances as independent random variables, the mean value of $V_{M,D_{IN}=4}$ is:

$$\mu(V_{M,D_{IN}=4}) = 2.15\ V \tag{5.5}$$

On the other hand, the calculation of the standard deviation $\sigma(V_{M,D_{IN}=4})$ requires more steps. Calculating first both the mean value and the variance of the equivalent capacitance C_{eq}:

$$\mu(C_{eq}) = \mu(C) + \mu(C) + \mu(2C) = 4\mu(C)$$
$$\sigma^2(C_{eq}) = \sigma^2(C) + \sigma^2(C) + \sigma^2(2C) = 4\sigma^2(C)$$

Adding the value of the MSB capacitance $4C$:

$$\mu(4C + C_{eq}) = \mu(4C) + \mu(C_{eq}) = 8\mu(C)$$
$$\sigma^2(4C + C_{eq}) = \sigma^2(4C) + \sigma^2(C_{eq}) = 8\sigma^2(C)$$

Hence, the variance of the capacitive-divider ratio is:

$$\sigma^2\left(\frac{4C}{4C + C_{eq}}\right) = \left[\frac{\mu(4C)}{\mu(4C + C_{eq})}\right]^2 \left[\frac{\sigma^2(4C)}{\mu^2(4C)} + \frac{\sigma^2(4C + C_{eq})}{\mu^2(4C + C_{eq})}\right]^2 = \frac{3\sigma^2(C)}{32\mu^2(C)}$$

The variance of $V_{M,D_{IN}=4}$ is therefore found as follows:

$$\begin{aligned}\sigma^2(V_{M,D_{IN}=4}) &= \sigma^2\left[V_{CM} + (V_{REFP} - V_{CM})\frac{4C}{4C + C_{eq}}\right] = \\ &= (V_{REFP} - V_{CM})^2\frac{3\sigma^2(C)}{32\mu^2(C)}\end{aligned}$$

Writing $\mu(C)$ as μ_C and $\sigma(C)$ as σ_C, the standard deviation of $V_{M,D_{IN}=4}$ is the following:

$$\sigma(V_{M,D_{IN}=4}) = (V_{REFP} - V_{CM})\frac{\sqrt{6}\sigma_C}{8\mu_C} \tag{5.6}$$

Since both μ_C and σ_C depend on the area of the unit capacitor, by substituting the parametric expressions in (5.3), one can determine the minimum unit capacitor area that satisfies the condition.

Bibliography

[1] A. Hierlemann, U. Frey, S. Hafizovic et al., "Growing cells atop microelectronic chips: Interfacing electrogenic cells in vitro with CMOS-based microelectrode arrays," *Proc. IEEE*, vol.99, pp.252-284, Feb. 2011.

[2] U. Frey, J. Sedivy, F. Heer et al., "Switch-matrix-based high-density microelectrode array in CMOS technology," *IEEE J. Solid-State Circuits*, vol.45, pp.467-482, Feb. 2010.

[3] R. R. Harrison, "The Design of Integrated Circuits to Observe Brain Activity," *Proc. IEEE*, vol.96, no.7, pp.1203-1216, Jul. 2008.

[4] W. Kester, "The Data Conversion Handbook," *Analog Devices, Inc.*, 2005.

[5] J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques-Part I," *IEEE J. Solid-State Circuits*, vol.SC-10, no.6, pp.371-379, Dec. 1975.

[6] R. J. Baker, "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE Press*, 2010.

[7] B. Razavi, "Data Conversion System Design," *IEEE Press*, 1995.

[8] C. Liu, S. Chang, G. Huang and Y. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE J. Solid-State Circuits*, vol.45, no.4, pp.731-740, Apr. 2010.

[9] L. Cong, "Pseudo C-2C ladder-based data converter technique," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol.48, no.10, pp.927-929, Oct. 2001.

[10] S. Haenzsche, S. Henker and R. Schuffny, "Modelling of capacitor mismatch and non-linearity effects ini charge redistribution SAR ADCs," *Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference*, pp.300-305, 24-26 Jun. 2010.

[11] Z. Lin, H. Yang, L. Zhong, J. Sun and S. Xia, "Modeling of capacitor array mismatch effect in embedded CMOS CR SAR ADC," *ASIC, 2005. ASICON 2005. 6th International Conference On*, vol.2, no., pp.982-986, 24-27 Oct. 2005.

[12] B. Razavi, "Design of Analog CMOS Integrated Circuits," *McGraw-Hill*, 2001.

[13] A. Agnes, E. Bonizzoni, P. Malcovati and F. Maloberti, "A 9.4 EnoB, 1V, 3.8uW, 100kS/s SAR-ADC with Time-Domain Comparator," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2008.

[14] N. H. E. Weste and D. M. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," *Addison-Wesley*, Fourth Edition, 2011.

[15] A. Hastings, "The Art of Analog Layout," *Prentice Hall*, Second Edition, 2006.

[16] T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *Solid-State Circuits, IEEE Journal*, vol.28, no.4, pp.523-527, Apr. 1993.

[17] S. Cho, C. Lee, J. Kwon and S. Ryu, "A 550-μW 10-b 40-MS/s SAR ADC With Multistep Addition-Only Digital Error Correction," *Solid-State Circuits, IEEE Journal*, vol.46, no.8, pp.1881-1892, Apr. 2011.

[18] K. Y. Kim, "A 10-bit, 100 MS/s Analog-to-Digital Converter in 1-μm CMOS," PhD Thesis, Integrated Circuits & Systems Laboratory Electrical Engineering Department, University of California, Jun. 2006.

[19] A. Graupner, "A Methodology for the Offset Simulation of Comparators," *The Designer's Guide Community*, www.designers-guide.org, 2006.

[20] B. Song, M. Choe, P. Rakers and S. Gillig, "A 1 V 6 b 50 MHz current-interpolating CMOS ADC," *VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium*, pp.79-80, 1999.

[21] P. M. Figueiredo and J. C. Vital, "Low kickback noise techniques for CMOS latched comparators," *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium*, vol.1, pp.I- 537-40 Vol.1, May 2004.

[22] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits," *John Wiley & Sons, INC.*, Fourth Edition, 2001.

[23] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," *Solid-State Circuits, IEEE Journal*, vol.27, no.12, pp.1916-1926, Dec. 1992.

[24] M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching properties of MOS transistors," *Solid-State Circuits, IEEE Journal*, vol.24, no.5, pp. 1433- 1439, Oct. 1989.

[25] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *Solid-State Circuits, IEEE Journal*, vol.40, no.6, pp. 1212-1224, Jun. 2005.

[26] M. D. Scott, B. E. Bose and K. S. J. Pister, "An ultralow-energy ADC for Smart Dust," *Solid-State Circuits, IEEE Journal*, vol.38, no.7, pp. 1123- 1129, Jul. 2003.

[27] Y. Zhu, C. Chan, U. Chio, S. Sin, S. Sin, S. U, R. P. Martins and F. Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," *Solid-State Circuits, IEEE Journal*, vol.45, no.6, pp.1111-1121, Jun. 2010.

[28] T. O. Anderson, "Optimum Control Logic for Successive Approximation Analog-to-Digital Converters," *Comput. Design*, vol.11, no.7, pp.81-86, Jul. 1972.

[29] D. K. Su, M. J. Loinaz, S. Masui and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *Solid-State Circuits*, vol.28, no.4, pp.420-430, Apr. 1993.