Fault Modeling in Controllable Polarity Silicon Nanowire Circuits

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Abstract-Controllable polarity silicon nanowire transistors are among the promising candidates to replace current CMOS in the near future owing to their superior electrostatic characteristics and advanced functionalities. From a circuit testing point of view, it is unclear if the current CMOS and FinFET fault models are comprehensive enough to model all defects of controllable polarity nanowires. In this paper, we deal with the above problem using inductive fault analysis on *three-independent-gate silicon nanowire FETs*. Simulations revealed that the current fault models, i.e. stuck-open faults, are insufficient to cover all modes of operation. The newly introduced test algorithm for stuck open can adequately capture the malfunction behavior of controllable polarity logic gates in the presence of nanowire break and bridge on polarity terminals.

I. Introduction

The continued feature-size scaling trend for extending Moore's law has faced the significant challenges of short-channel effect and leakage power. To discover possibilities for further performance and functionality, a huge research effort has devoted on innovative device structures. FinFET transistors [1], as an example of multigate devices, are successfully replacing bulk CMOS transistors beyond the 22nm technology node. Following the trend toward one-dimensional structures, *Silicon NanoWires* (SiNWs) with *Gate-All-Around* (GAA) structures [2] provide an even better electrostatic control over the channel and reduce leakage current.

Beyond 45 nm, many devices exhibit Schottky characteristic at source and drain contacts such as SiNWs, carbon nanotubes, and graphene [3]. These junctions have ambipolar behavior, i.e., they support the flow of both n and p carriers. While ambipolarity is usually suppressed by fabrication process to provide unipolar devices [4], it can be used to enhance the logic functionality [5]. *Double-Gate* (DG) [6] and *Three-Independent-Gate* (TIG) [7] devices based on SiNWs are examples of devices with enhanced functionality.

To reveal fabrication defects and circuits malfunctioning, a number of structural fault models for planar single-gate CMOS and FinFET technologies have been proposed and proved to be efficient. For instance, stuck-at [8], delay [9], stuck-open [10], and bridging fault [11] are among the most commonly-used models for CMOS technology. For FinFETs, a few number of studies have been conducted in modeling defects such as floating gates and shorts [12, 13], stuck-open/stuck-on [14, 15], and *Gate Oxide Short* (GOS) [16]. These studies revealed the deficiency of current CMOS fault models for detecting defects in FinFET circuits, and necessitated a new fault model for test generation purpose.

In this paper, we perform an inductive fault modeling to investigate the specific faults of *Controllable Polarity Silicon NanoWire FETs* (CP-SiNWFETs). We follow the major steps of fabrication process to realistically model the possible defects that may affect device functionality or performance. To perform our experiments, we used *Three-Independent-Gate Silicon NanoWire FETs* (TIG-SiNWFETs) as a target technology. However, the proposed fault model is quite general and can be used for any other *Controllable Polarity* (CP) devices. To the best of our knowledge, this is the first work on fault modeling for CP-SiNWFET circuits that include open and bridging faults on the polarity terminal which are unique to CP devices. The main contributions of this paper are as follows.

- Considering the fabrication process, the possible defects occur on CP-SiNWFETs are modeled. The behavior of the defects on various types of CP logic gates is investigated to show the inefficiency of the traditional fault models for covering the defects in CP transistors.
- Stuck-at p-type and n-type fault models are introduced for CP-SiNWFETs and their efficiencies are verified for unique faults that occur in this technology.
- The current test methods are unable to detect stuck-at opens in dynamic polarity CP-SiNWFET logics. A new test algorithm for revealing the defect is proposed.

The remainder of the paper is organized as follows. The background of fault modeling is presented in Section II. In Section III, the CP devices are briefly reviewed and the structure of logic gates designed in this technology are detailed by introducing the static/dynamic polarity concept. The detail of the defect modeling for CP silicon nanowires demonstrated in Section IV. The fault modeling for CP logic gates is investigated in Section V and the paper is concluded in Section VI.

II. Background and Motivation

Moving toward nano-scaled technologies, process variation

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negatively affects the driving current of transistors and consequently results in delay faults. Moreover, undetected design rules violations increase the chance of bridge faults as unintended resistive connections between two or more conductive parts. Bridge faults could be efficiently diagnosed by supply current monitoring through IDDQ test [17] for bulk planar CMOS, but the test is becoming less effective for the deeply nanoscaled technologies [18]. Last but not least, *Line Edge Roughness* (LER) is an inevitable limitation of etching process and leads in non-homogeneous deposition of dielectrics when the dielectric thickness goes beyond 5nm. This may result into the *Gate Oxide Short* (GOS) defect [19].

Proper fault modeling for testing manufacturing defects plays a significant role for quality of circuits and their correct functionality. Currently, few researches have been carried out on fault modeling of the FinFET, and *Carbon NanoTubes* (CNTs). The authors in [12, 13] investigated open and short faults on FinFETs, and they showed that *Stuck-at Open Faults* (SOFs) on the back gate of FinFET have a unique effect on the leakage and delay. In [16], the GOS defect on the FinFET dielectric have been studied . The amount of *Saturation Drain Current* ($I_{D(SAT)}$) vastly increases with GOS at the front gate dielectric. However, GOS occurrence in the back-gate dielectric causes much lower carrier density in the device channel. The SOF, Stuck-On and GOS on different number of Fins in a FinFET have been examined by [14, 15]. The results manifested that when the number of faults is large enough, the defect can be captured by SOF or delay fault tests. In [10] authors presented the problem of SOF detection for small nanometer technologies. They proposed a new multiple test vector mechanism to enhance the probability of SOF detection.

While stuck-at, SOF, bridge, and delay faults efficiently model the defects in CMOS, FinFET, and CNT devices, the particular structure of devices with controllable polarity necessitates further study to see whether these fault models can properly capture the manufacturing defects. There is no available comprehensive fault model for circuits designed with these devices. In the following, we analyze the possible manufacturing defects of CP transistors, and then investigate their impact of the functionality of the various types of CP logic gates.

III. Controllable Polarity: From Device to Logic Gates

In this section, we introduce the transistors with *controllable polarity* (CP). We present the realization of the logic gates in this technology and discuss how CP devices help the compact implementation of logic gates. We briefly review the main steps of manufacturing process which is necessary for our defect modeling.

A. Transistors with Controllable Polarity

Ambipolar conduction of the nanoscaled devices can be controlled by adjusting the device polarity online. Such transistors with Controllable Polarity have been successfully implemented in *Silicon NanoWires* (SiNWs) [6, 7] and carbon nanotube [20]. In the transistor, one electrode gate, the *Control Gate* (CG), works similar to conventional MOSFETs, and provides the conduction by controlling potential barriers. At least one another electrode gate, the *Polarity Gate* (PG), is needed to control the n-type or p-type characteristics of the device. Indeed, the type of carriers that flow in the device channel is adjustable through the applied voltage on PG.

Among various technologies of CP transistors, SiNWs have a CMOS compatible fabrication process. Different architectures have been proposed for their implementations [6, 7, 21, 22]. As an example, Figure 1 represents a *Three Independent Gate* (TIG) SiNWFET with a CG and two PGs (PGS and PGD). Here, the side regions (PGS and PGD) determine the majority carriers through adjusting the barrier thickness at the source/drain junctions. Thus, the device can exhibit a controllable n-type and p-type characteristics. In this paper, we use the TIG-SiNWFET as the target device. Nevertheless, the fault modeling for other CP devices, i.e. DG-SiNWFET, can be obtained straightforward following the same methodology. Accordingly, without loss of generality, we provide our discussion based on this device.

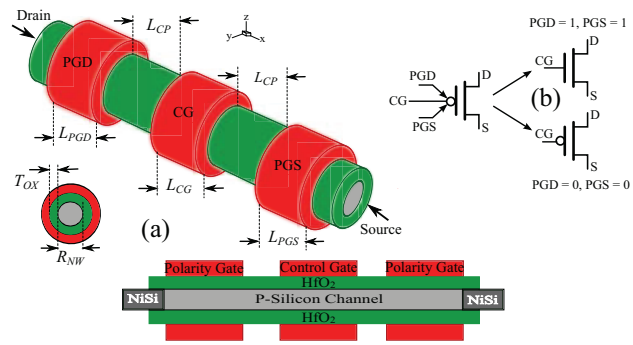


Fig. 1. TIG-SiNWFET structure as used for 3D TCAD simulation

B. Fabrication Process

As shown in [6], the TIG-SiNWFET devices are fabricated in a top-down approach. Table I summarizes the fabrications process of the device along with the outcome of each step. The Bosch etching process [23] is utilized to form the device pattern. Gate dielectric is then formed by self-limiting oxidation which provides tiny oxide layer ($\leq 5nm$) around the channel. Oxidation process is followed by a conformal polysilicon deposition to shape the polarity gates around the nanowires. Finally, the control gate structure is self-aligned to polarity gates. Thus, a three-gate device is obtained in which polarity gates are electrically isolated by the control gate oxidation.

C. Logic Gate Realization of CP Circuits

The CP transistors as configurable structures can be efficiently utilized to implement the logic gates. The functionality can be configured by feeding the correct polarity whether it is placed in the pull-up or pull-down network. According to the different configuration of PGs, the CP logic gates are divided into two categories.

The first group, called *Static Polarity* (SP), is characterized with the PGs directly connected to either power supply (V_{dd}) or ground (GND) rails to provide the desired polarity. In SP logic gates, the polarity of all devices remains the same during the whole device life-time. Figure 2a illustrates the three

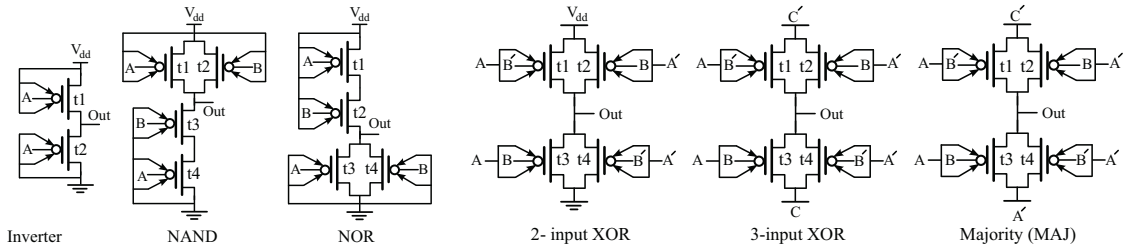


Fig. 2. Logic gate realization in TIG-SiNWFET. Inverter, NAND, and NOR gates are the examples of the SP logic gates. Accordingly, 2-input XOR, 3-input XOR and Majority (MAJ) logic gates are those of DP logic structures.

TABLE I
TIG-SiNWFET FABRICATION PROCESS STEPS AND RELATED DEFECT MODEL

TIG-SiNWFET fabrication process		
Process	**Outcome**	**Possible defects**
(1) HSQ-based nanowire patterning	Initial pattern of nanowires	Nanowire break
(2) Bosch process	Nanowire formation	Nanowire break
(3) Oxidation process	Dielectric formation	Gate oxide short
(4) Polysilicon deposition	Polarity and control gates	Bridge between two or more terminals
(5) Metal layer(s) deposition	Interconnections	Bridge among interconnects, Floating gates

examples of SP logic gates (INV, NAND, and NOR gates) realized in TIG-SiNWFET technology.

The second group called *Dynamic Polarity* (DP), consists of logic gates in which the polarity gates are derived by input signals to configure the correct polarity of the transistor. This property expresses that the conductivity of the transistor is possible when the conditions of $CG = PGS = PGD = 1$ and $CG = PGS = PGD = 0$ exist for the n- type and p-type transistors respectively (Figure 2). Similarly the transistor has no conductivity when $CG \oplus (PGS \cdot PGD) = 1$. This property notifies the intrinsic XOR characteristics of the CP transistors, when combined with transmission gate structure, leads to compact realization of the binate logic gates. Figure 2b represents the implementation of three DP logic gates (XOR, XOR-3, and MAJ gates) in TIG-SiNWFET.

D. Simulation Setup

A two-step simulation environment, that integrates the Sentaurus and HSPICE simulators into a single framework, is used to facilitate high-level simulations. First, we build a TCAD model of the TIG-SiNWFET, for which the I-V curves are calibrated with those of our fabricated devices. The typical parameters of the TIG-SiNWFET shown in the Figure 1 are listed in Table II. The supply voltage used in the simulations is $1.2V$ as a typical value in 22nm technology.

In the next phase, circuit level simulations are realized by a simple compact model based on a table model in Verilog-A. The result of the TCAD simulations from previous step, makes a look-up table model that characterizing the channel conductivity as a function of the V_{CG}, V_{PGS}, and V_{PGD}. Moreover, it provides the value of the parasitic capacitance among various terminals and the access resistance corresponding to the source and drain. This model is used in our simulations to efficiently implement the functional behavior of the TIG-SiNWFET.

IV. TIG-SiNWFETs: Device Level Defect Modeling

In this section, the possible defects of TIG-SiNWFETs are analyzed by considering major device manufacturing steps.

TABLE II
TIG-SiNWFET STRUCTURAL AND PHYSICAL PARAMETERS

Device Parameter	Value
$Length\,of\,Control\,Gate\,(L_{CG})$	$22nm$
$Length\,of\,Polarity\,Gates\,(L_{PGS},\,L_{PGD})$	$22nm$
$Length\,of\,Spacer\,(L_{CP})$	$18nm$
$Channel\,Dopping\,Concentaration$	$10^{15}cm^{-3}$
$Schottky\,Barrier\,Height$	$0.41eV$
$Oxide\,Thickness\,(T_{Ox})$	$5.1nm$
$Radius\,of\,NanoWire\,(R_{NW})$	$7.5nm$

The defect model then is used for inductive fault analysis.

A. Manufacturing Defects

Following the fabrication process provides the opportunity to find the possible defects that may occur during manufacturing. This defect model helps us to find a realistic fault model for non-classical CMOS devices with complex architectures.

Table I also summarizes the possible defects for TIG-SiNWFETs. During the nanowire patterning and etching, variations along with LER contribute to lowering the pattern sharpness that may lead to nanowire break. The defect can drastically limit the driving current of the device or lead to SOF. When the dielectric thickness is scaled beyond the 5nm, the control for conformal oxide formation is reduced, and this eventually leads in poor insulator coverage. The *Gate Oxide Short* (GOS) defects may consequently happen. This defect may degrade the performance of device, which is discussed in Section IV-B. The similar mechanisms may result in bridge defect between the control gate and each adjacent polarity gate. Finally, the gate deposition process contributes to various defect mechanisms such as under/over polishing, poorly planarized surfaces, and scratches, result in combinations of shorts and opens [24]. Open defects form floating regions that are very challenging for emerging technologies since they may affect either the performance or functionality of devices. In Section V, we investigate all the mentioned defects to provide a realistic fault model.

B. TIG-SiNWFET Performance in Presence of GOS

For the TIG-SiNWFET, three gates (PGS, CG, and PGD) contribute to the functionality of the device. Therefore, three locations are possible for the GOS defect. The defect injection on TCAD model of the device is accomplished as the following steps. First, one of the gates is selected. For the selected one, a tiny cuboid of the dielectric layer is removed. Then, the hole is filled with slightly doped silicon similar to that of the device channel. Finally, the dielectric and the GOS are covered with the gate material. Consequently, a conductive pass is created between the defective gate and the channel.

As control and ploarity gates are symmetric along the device channel, the occurrence of GOS in each part of the transistor causes similar behavior. Thus, we need to inject the defect once for the defect analysis purpose. Here, we provide detailed explanation of the n-type device. The behavior of the p-type one is similar to n-type device. Figure 3a–3c depict the behavior of n-type TIG-SiNWFETs in the presence of GOS. Figure 3a represents the I-V curves of using n-type TIG-SiNWFET with and without occurrence of a GOS on the PGS. The black IVs illustrate the behavior of a defect free device, and the red ones demonstrate the defective device. Here, GOS causes a significant reduction of $I_{D(SAT)}$ similar to bulk CMOS. Moreover, GOS causes a weak inversion and tightens the channel for carriers, leads to a slight increase of $V_{Th}(\Delta V_{Th} = 170mV)$. The negative I_D when the $V_{DD} = low$, which happens in bulk CMOS and FinFET [25, 16] , is observed here when the remaining gates of the transistor allow carriers to pass through the channel. For example, for faulty n-type devices used in SP logic gates, polarity controls constantly permit electrons to pass through channel, and therefore negative I_D exists when the V_D decreases. The effect of GOS occurrence on CG is shown in Figure 3b. The black curves belong to the fault free device. Red curves are of the faulty ones. The defect here results in similar behavior of reduced $I_{D(SAT)}$, shifted V_{Th}, and negative I_D. The reduction of $I_{D(SAT)}$ is lower than that of previous case. Figure 3c also shows the consequence of the GOS defect on PGD. In this case, the defect leads to some extent the increase of the I_D and has no impact on the V_{Th}.

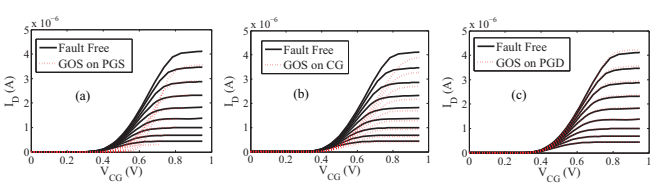


Fig. 3. The behaviors of defective n-type TIG-SiNWFETs in the presence of GOS

In order to closely investigate the fault role, the carrier density function of the device is extracted under saturation region from TCAD simulation (Figure 4). As in the n-type configuration gates have positive polarities, holes are injected into the channel from the gate results in electron density reduction near the GOS. This phenomenon reduces the driving current of the device and shift the V_{Th}. When the GOS happens near the source, the carrier density is decreased since the high electron density of the source accelerates the hole injection into the channel. Indeed, the $I_{D(SAT)}$ drop is proportional to the electron absorption capability of the defects, determined by the

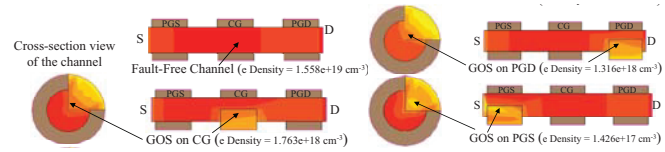


Fig. 4. Electron density distribution of an n-type TIG-SiNWFET with/without GOS at control gate dielectric

size of the GOS. The GOS occurrence near drain slightly enhances the carrier injection into the drain. This phenomenon slightly increases the drain current. Here GOS enhances the field inside the channel while its electron absorption capability is decreased owing to the quasi-ballistic transport inside channel near drain.

V. Fault Modeling in Controllable polarity Silicon Nanowire Circuits

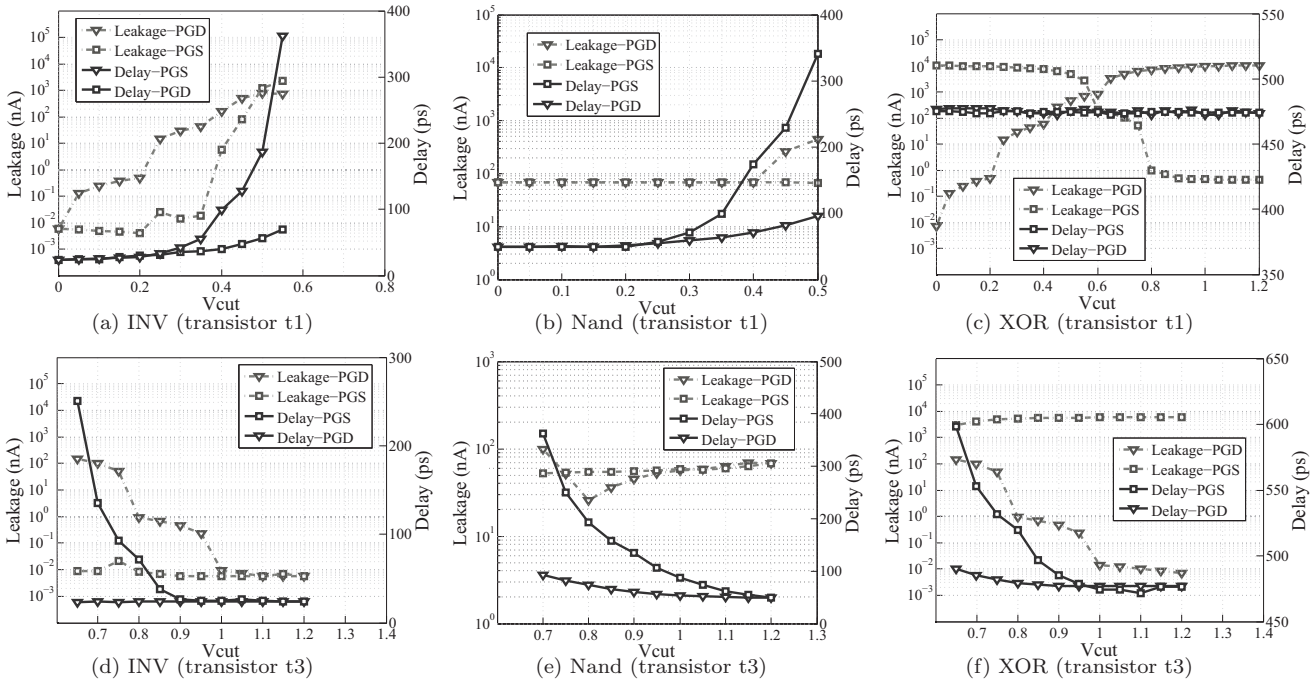
In this section, we study the behavior of SP and DP TIG-SiNWFET logic gates in the presence of fabrication defects, discussed in the previous section.

A. Open CGs and PGs in the SP and DP logic gates

We simulated SP (INV and NAND) and DP (2-input XOR) logic gates with the open faults on the polarity gates of the pull up and pull down transistors. The defect-free PG biases were set to their nominal values (for SP logic gates $PGS = PGD = '0'$ and $PGS = PGD = '1'$ for pull up and pull down devices respectively, and for the DP gates $PGS = PGD =$ *appropriate input signals*). When open defect happens, because of coupling effects, it is necessary to analyze the logic gates for a range of possible voltages which may be exhibited on the floating node. The voltage value for an open fault, Vcut, is varied from V_{Lo} to V_{Hi}. The (V_{Lo}, V_{Hi}) is a subset of (GND, V_{dd}) in which the functionality of the logic gate under test is correct.

Figures 5a and 5d illustrate the leakage-delay variation with respect to V_{Cut} for the polarity gates of the pull-up (t1) and pull-down (t3) transistors in a INV gate. In the former figure, the delays of PGD and PGS stay relatively constant up to the $V_{Cut} = 0.3V$. When the V_{Cut} further increases to $0.56V$, the transition low-to-high delay of PGD rises exponentially ($7\times$) but the delay of PGS increases slightly. Since carrier transportation regime under PGD is quasi-ballistic, PGD plays a less important role in control of carrier concentrations. The leakage shows a drastically increase for both cases ($5\times$). This is due to the fact that, here, the leakage is dominated by the p-type transistor. Finally, beyond $V_{Cut} = 0.56$, the p-type is always off. Figure 5d also shows a similar trend to p-type device as discussed. Consequently, open defect on the TIG-SiNWFETs in INV logic gates get along with several fault models, corresponding to the voltage of the cut. For V_{Cut} below $0.56V$, the delay fault and stuck-on can be used for testing purpose. Beyond this threshold the SOF can reveal the defected logic gate.

In Figures 5b, and 5e, the variation in leakage and delay of the pull up (t1) and pull-down (t3) transistors of the TIG-SiNWFET NAND are shown. A drastic increase in delay occurs as Vcut changes from its intended bias similar to what is observed for the INV gate. For t3, the leakage represents a relatively small variation . This is due to the fact that leakage



(a) INV (transistor t1) (b) Nand (transistor t1) (c) XOR (transistor t1)

(d) INV (transistor t3) (e) Nand (transistor t3) (f) XOR (transistor t3)

Fig. 5. Leakage-delay variation with different biases on PGS and PGD of the TIG-SiNWFET transistors in the SP and DP logic gates

of n-type device (t3) is dominated by the other transistor (t4) of the pull down in NAND gate. Therefore, the open defect in TIG-SiNWFET NAND can be detected using the combination of delay fault and SOF.

The leakage-delay characteristics of the 2-input XOR , as a DP logic gate, is illustrated in Figures 5c, and 5f. The functionality of the XOR does not change when the cut happens in the pull up (t1 transistor). Against the SP gates, here only the leakage represents a considerable variation (6 orders of magnitude) for the various Vcut (Figure 5c). Thus, the defect can be tested only with stuck-on fault model. Figure 5f also represents the behavior of XOR when the open fault happens in the pull down (t3). Here, the delay-leakage variation trend is similar to that of the INV gate. Therefore, the test of open defect for TIG-SiNWFET XOR requires a combination of delay fault, SOF, and stuck-on fault models.

TABLE III
DETECTION OF POLARITY DEFECT FOR DIFFERENT TRANSISTOR OF THE 2-INPUT TIG-SINWFET XOR

Logic Gate	Fault type	Fault Location	Input for Detection	Fault Behavior	
				Leakage Current	Output Voltage
2-input XOR	Stuck-at $n-$type	t1	00	Yes	No
		t2	11	Yes	No
		t3	01	Yes	Yes
		t4	10	Yes	Yes
	Stuck-at $p-$type	t1	00	Yes	No
		t2	11	Yes	No
		t3	01	Yes	Yes
		t4	10	Yes	Yes

B. Bridge characterization in the SP and DP logic gates

Among various type of bridge defects, short between polarity terminals and supply voltage is exclusive to CP logic gates. In SP logic gates, the bridge connection between polarity controls and V_{DD} in pull-up network changes the desired polarity of the device from p to n. Similarly, bridge defect between polarity controls and GND in pull-down network leads to the polarity change from n to p. This defect in SP logic gates represents similar behavior to channel break which can be easily covered by SOF. For the DP logic circuit, this defect can be masked depending on the location of the faulty transistor in the circuit. As polarity gates come from input signals, and polarity terminals are accessible from circuit inputs, it is possible to define a logic level fault model for this defect to facilitate the test process. we define the stuck-at n-type fault to represent the bridge defect in the pull-up network. The stuck-at n-type defect can be applied on the circuits using $V_{stuck-at-n-type} = \begin{bmatrix} PGD : '1' \\ PGS : '1' \end{bmatrix}$. Similarly, the stuck-at p-type defect is defined by $V_{stuck-at-p-type} = \begin{bmatrix} PGD : '0' \\ PGS : '0' \end{bmatrix}$.

In order to evaluate the performance of this model, we analyzed the TIG-SiNWFETs XOR by exhaustive fault injection. Table III represents the possible input vector and corresponding fault behavior for this type of bridge defect. If the faulty device is located in pull-down network, the wrong output of the logic gate reveals the fault. For the pull-up network, the fault detection is only possible by leakage observation. Here, the leakage variation is more than $\times 10^6$. This variation is high enough to be sensible by the I_{DDQ} test.

C. Channel break in the SP and DP logic gates

Channel break demonstrates a similar behavior like stuck-open faults in SP logic gates. The detection of this defect requires the application of a two-pattern test. The first vector initializes the gate output and the second one evaluates the wrong output value in the presence of a fault. For example, a NAND gate as a SP logic contains three vectors of two-pattern tests ($v1 = (11 \rightarrow 01)$, $v2 = (11 \rightarrow 10)$, $v3 = (00 \rightarrow 11)$), by which all the channel break defects for the TIG-SiNWFET

NAND can be detected. Although it is possible to detect all faults related to the SP logic gates such as FinFET NAND gates, detection of open faults in DP logic gates is non-trivial. When a channel break happens on a transistor of a DP TIG-SiNWFET gate, the redundant structure of the pass transistors masks the effect of faulty transistor. Here, the fault masking depends on the capacitances that couple to the output node and the polarity of the fault free transistor. In order to simulate this situation, we performed fault injection using vectors $V_{P_{Off}} = \begin{bmatrix} CG: '1' \\ PG: '0' \end{bmatrix}$ (p-type off transistor) and $V_{N_{Off}} = \begin{bmatrix} CG: '0' \\ PG: '1' \end{bmatrix}$ (n-type off transistor). When the negated value of the CG signal is applied to PGs, the transistor goes to the turn off mode. The vectors have been applied on the 2-input TIG-SiNWFET XOR (FO4) to evaluate the channel break on the DP logic gates. Here, all the injected faults are masked by the pass transistors in the pull-up and pull-down networks. Indeed, the channel break defect does not change the logic gate functionality. The defect only affects the performance parameters of the gate such as delay and leakage. Our simulation results on 2-input XOR revealed that the variation of performance parameters are too low for the purpose of fault detection ($\Delta leakage \leq 100\%$, and $\Delta delay \leq 58\%$). In the following, we use a procedure based on stuck-at n- and p- fault model which can be efficiently used for channel break detection of DP logic gates.

In order to detect channel break defect of DP logic gates, the following steps are consequently is required. First, the polarity of the target device is deliberately changed to the complemented of fault free value. This means that we inject the stuck-at n-type and stuck-at p-type faults on the device under test. Secondly, the appropriate test vectors are applied to the faulty circuit similar to what listed in the Table III. In the case of channel break, the effect of stuck-at n-type/stuck-at p-type fault is masked since the device with channel break does not contribute to circuit output. Therefore, the fault free output in the present of stuck-at n-type/stuck-at p-type faults reveal the channel break in the target device. While, for the fault free device, the similar injected faults result in wrong functionality or leakage variation greater than $\times 10^6$.

VI. Conclusion

Further scaling of the planar CMOS technology has been faced with serious challenges such as increased leakage and process variation. Among the alternative technology, controllable polarity silicon nanowires such as TIG-SiNWFETs are promising owing to their lower leakage and great electrostatic control. As one of the necessary design steps, fault modeling is needed for this new technology. In this paper, we performed an inductive fault analysis on the TIG-SiNWFETs. According to the fabrication process steps, a defect model was extracted. This model contains channel break, gate oxide short, bridge and float defects. We simulated the effect of these defects on both categories of static and dynamic CP circuits. We introduced a new fault model for CP devices such as stuck-at n-type and stuck-at p-type which can be efficiently used for detection of channel break and polarity defects in CP logic gates. We also showed that the gate oxide short and floats on the polarity gates are detectable by analyzing the performance parameters like delay and leakage.

VII. Acknowledgements

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