Modular Multilevel Converters with Integrated Split Battery Energy Storage

THÈSE N^O 6406 (2014)

PRÉSENTÉE LE 13 NOVEMBRE 2014
À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE D'ÉLECTRONIQUE INDUSTRIELLE
PROGRAMME DOCTORAL EN ENERGIE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Michail VASILADIOTIS

acceptée sur proposition du jury:

Dr S.-R. Cherkaoui, président du jury
Prof. A. Rufer, directeur de thèse
Prof. H. Akagi, rapporteur
Prof. D. Dujic, rapporteur
Dr N. Oikonomou, rapporteur

(EPFL

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Suisse
2014

Acknowledgements

Acknowledgements

with administrative issues has been lifesaving. Martel with his cheerful character, the Imperix team Simon and again Nicolas, Roberto, Sébastien, Hardi with his unconventional sense of humor, Mahbod, Fred, Gina and all scientific and technical LEI staff are also acknowledged for their contribution in the everyday working life as well as their help in various matters. Being in a lab that gives a strong emphasis on education, I had the chance to supervise and give lectures to many students, a process which I have most enjoyed. I would like to express my appreciation to them as well. Finally, many thanks to Endika Bilbao, with whom I shared an office during my first few months only in LEI, but made his stay something to remember.

Last but not least, I am grateful to all my friends in Lausanne and throughout the world as well as my family. I always feel blessed to have them around me in good and bad times. Nothing would have ever been the same without them and their endless support.

Lausanne, 1 October 2014 M.V.

Abstract

The electric power grid is undergoing significant changes and updates nowadays, especially on a production and transmission level. Initially, the move towards a distributed generation in contrast to the existing centralized one implies a significant integration of renewable energy sources and electricity storage systems. In addition, environmental awareness and related concerns regarding pollutant emissions have given rise to a high interest in electrical mobility. Advanced power electronics interfacing systems are expected to play a key role in the development of such modern controllable and efficient large-scale grids and associated infrastructures.

During the last decade, a global research and development interest has been stimulated in the field of modular multilevel conversion, due to the well-known offered advantages over conventional solutions in the medium- and high-voltage and power range. In the context of battery energy storage systems, the Modular Multilevel Converter (MMC) family exhibits an additional attractive feature, i.e., the capability of embedding such storage elements in a split manner, given the existence of several submodules operating at significantly lower voltages. This thesis deals with several technical challenges associated with Modular Multilevel Converters as well as their enhancement with battery energy storage elements.

Initially, the accurate submodule capacitor voltage ripple estimation for a DC/AC MMC is derived analytically, avoiding any strong assumptions. This is beneficial for converter dimensioning purposes as well as for the implementation improvement of several control schemes, which have been proposed in the literature. The impact of unbalanced grid conditions on the operation and design of an MMC is then investigated, drawing important conclusions regarding the choice of line current control and required capacitive storage energy during grid faults.

Subsequently, the concept of Modular Multilevel Converters with integrated split battery energy storage systems (BESS) is treated. Several solutions for the submodule/battery interfacing problem are presented and discussed. A global system control method is developed in detail, where all objectives are split into several subproblems and handled by means of topology-specific degree of freedom exploitation. These objectives include capacitor voltage control, independent active power control as well as battery state of charge balancing. The application of the developed method in three different conversion structures, i.e. the star- and delta-configured Cascaded H-Bridge converter and the DC/AC Modular Multilevel Converter, proves that it is extendable to any type of

Abstract

MMC-based conversion structure with only minor topology-specific modifications.

In a final step, a modular versatile Power Electronic Transformer-based multiport converter architecture is proposed and investigated for the implementation of a medium voltage ultra-fast EV charging station. This benefits from the shift of the isolation requirements to the medium frequency range. The chosen DC/DC converter topology, i.e., the Dual Half-Bridge is analyzed in terms of soft-switching regions for wide input and output voltage variations. Due to the system high-order and nonlinearities, an advanced current control design method is employed, based on optimized loop shaping using nonparametric models. An overall control algorithm is finally derived, capable of stabilizing the system under all possible operating modes and power flow directions.

Key words: Modular Multilevel Converters, Cascaded H-Bridge converters, battery energy storage systems, power electronic transformer, ultra-fast EV charging, integrated split energy storage, Dual Half-Bridge, active power control, state of charge balancing, unbalanced grids.

Résumé

Les infrastructures électriques font face de nos jours à des changements et mises à jour importants, particulièrement au niveau de la production et de la transmission de l'énergie électrique. Tout d'abord, l'évolution vers une génération distribuée contrairement à celle centralisée existante implique une intégration significative des sources d'énergie renouvelables et des systèmes de stockage d'énergie électrique. En outre, la sensibilisation à la cause environnementale et les préoccupations liées aux émissions de polluants ont donné lieu à un vif intérêt pour la mobilité électrique. Les systèmes d'électronique de puissance avancés sont appelés à jouer un rôle clé dans le développement de tels réseaux à grande échelle modernes et des infrastructures associées, en mettant l'accent sur la contrôlabilité et l'efficacité.

Au cours de la dernière décennie, un intérêt mondial a été porté sur la recherche et le développement dans le domaine de la conversion modulaire multiniveaux, en raison des avantages offerts par rapport aux solutions classiques des gammes moyenne et haute tension et puissance. Dans le contexte des systèmes de stockage d'énergie basés sur des batteries, la famille des Convertisseurs Modulaires Multiniveaux (MMC) présente une caractéristique supplémentaire attrayante, c'est-à-dire, la possibilité d'incorporer ces éléments de stockage d'une manière divisée, grâce à l'existence de plusieurs sous-modules fonctionnant à des tensions beaucoup plus faibles. Cette thèse traite de plusieurs défis techniques associés aux Convertisseurs Modulaires Multiniveaux ainsi qu'à leur renforcement avec des éléments de stockage d'énergie utilisant des batteries.

Dans un premier temps, l'estimation précise de l'ondulation de la tension des condensateurs des sous-modules d'un MMC DC/AC est dérivée de façon analytique, en évitant de recourir à des hypothèses fortes. Ceci est bénéfique à des fins de dimensionnement du convertisseur ainsi que pour l'amélioration de la mise en œuvre de plusieurs systèmes de réglage proposés dans la littérature. Ensuite, l'impact des conditions de réseau asymétriques sur le fonctionnement et la conception d'un MMC est étudié, permettant de tirer des conclusions importantes concernant le choix du réglage des courants de ligne et du stockage d'énergie capacitif requise pendant les défauts du réseau.

Par la suite, le concept de convertisseurs modulaires multiniveaux avec de batteries intégrées et divisées est traité. Plusieurs solutions concernant le problème de l'interfaçage entre le sous-module et la batterie sont présentées et discutées. Une méthode globale pour le réglage du système est développée en détails, où tous les objectifs sont divisés en plusieurs sous-problèmes et manipulés en exploitant les dégrées de liberté spécifiques aux

topologies étudiées. Ces objectifs comprennent le réglage de la tension de condensateurs des sous-modules, le réglage indépendant de la puissance active ainsi que l'équilibrage de l'état de charge des batteries. L'application de la méthode développée dans trois structures de conversion différentes, c'est-à-dire, le convertisseur en Ponts-H Cascadés en configuration étoile et triangle et le Convertisseur Modulaire Multiniveaux DC/AC, prouve que la démarche utilisée est extensible à tout type de structure de conversion basée sur des MMCs avec seulement quelques modifications mineures pour chaque topologie.

Dans un dernier temps, une architecture de convertisseurs polyvalente et multi-porte à base de transformateurs d'électronique de puissance modulaires est proposée et étudiée pour la mise en œuvre d'une station de recharge ultra-rapide de véhicules électriques, permettant la connexion directe au réseau moyenne tension. Cela permet de déplacer les contraintes d'isolation galvanique dans le domaine de la moyenne fréquence. La topologie du convertisseur DC/DC choisie, c'est-à-dire, le Dual Half-Bridge (DHB) est analysée en termes de domaines de fonctionnement à commutation douce pour de grandes variations des tensions d'entrée et de sortie. En raison de l'ordre supérieur du système et des non-linéarités présentes, une méthode de conception de réglage du courant avancée est utilisée, basée sur le calibrage optimisé de la fonction de transfert en boucle ouverte, en utilisant des modèles non-paramétriques. Un algorithme de réglage global est finalement déduit, capable de stabiliser le système pour tous les modes de fonctionnement et directions du flux de puissance possibles.

Mots clefs : Convertisseurs Modulaires Multiniveaux, Convertisseurs en Ponts- H Cascadés, systèmes de stockage d'énergie basés sur des batteries, Transformateur d'Électronique de Puissance, recharge ultra-rapide des véhicules électriques, stockage d'énergie intégrée est divisée, Dual Half-Bridge, réglage de puissance active, équilibrage des états de charge, réseaux déséquilibrés.

Contents

Contents

List of Abbreviations

AAC Alternate Arm Converter.

API active parallel interface.

B2G Buffer-to-Grid.

BESS Battery Energy Storage Systems.

BMS battery management system.

BPFS branch power frequency-shifting.

CHB Cascaded H-Bridge.

CHB-BESS CHB converter with integrated split BESS.

DDSRF decoupled double synchronous reference frame.

DHB Dual Half-Bridge.

DPI direct passive interface.

ESR equivalent series resistance.

ESS energy storage systems.

EV electric vehicle.

FAE fictive axis emulation.

FPGA Field-Programmable Gate Array.

HVDC high-voltage direct current.

IAI indirect active interface.

MCU microcontroller unit.

List of Abbreviations

MF medium-frequency.

MMC Modular Multilevel Converter.

MMC-BESS MMC with integrated split BESS.

NLC nearest level control.

PCB printed circuit board.

PET Power Electronic Transformer.

PI proportional-integral.

PLL phase-locked loop.

PR proportional-resonant.

PRBS pseudo random binary sequence.

PWM pulse-width modulation.

RRF rotating reference frame.

SDP semi-definite problem.

SHE selective harmonic elimination.

SIP semi-infinite problem.

SISO single-input single-output.

SoC State of Charge.

SOGI second-order generalized integrator.

SPI Serial Peripheral Interface.

SRF stationary reference frame.

STATCOM static synchronous compensator.

UFCEV ultra-fast charging for electric vehicles.

UFEVCS ultra-fast EV charging station.

V2G Vehicle-to-Grid.

ZVS zero voltage switching.

List of Main Symbols

C_{1-4} DHB dividing capacitors.

C_{api} Active parallel interface capacitance.

C_{branch} Equivalent MMC branch capacitance.

C_{res} Direct passive interface resonant filter capacitance.

C_{sm} MMC submodule capacitance.

$E_{bat,n}^{sm}$ Nominal submodule battery energy.

$G_S^{circ}(s)$ DC/AC MMC circulating current transfer function.

$G_S^{line}(s)$ DC/AC MMC line current transfer function.

$G_R^I(s)$ IAI inner current controller.

$G_R^U(s)$ IAI outer voltage controller.

$G_{pE}(s)$ Equivalent small time constant transfer function.

I_S DC-link current of three-phase DC/AC MMC.

I_o DHB output current.

I_{bat} Battery current.

I_{sm} Submodule output current.

L Branch inductance.

L_D Desired open-loop transfer function for the optimization procedure.

L_T Three-phase MMC inductance (grid or machine or transformer and cable).

L_f Battery-side inductive filter.

L_σ DHB transformer leakage inductance.

L_{api} Active parallel interface inductance.

List of Main Symbols

L_o DHB secondary half-bridge inductance.

L_{res} Direct passive interface resonant filter inductance.

N Number of submodules/branch.

P_{AC} Average three-phase active power.

P_{DC} Average DC-link active power of the DC/AC MMC.

P_{br}^k CHB-BESS k-th branch power.

P_{ph}^k DC/AC MMC-BESS k-th phase power.

Q_{AC} Average three-phase reactive power.

$Q_{bat,n}^{sm}$ Nominal submodule battery capacity.

R Branch resistance.

R_T Three-phase MMC resistance (grid or machine or transformer and cable).

R_o DHB output resistance.

R_{bat} Battery equivalent series resistance.

SoC_{sm}^{ki} CHB-BESS ki-th submodule battery SoC value.

SoC_{sm}^{kji} DC/AC MMC-BESS kji-th submodule battery SoC value.

U_S DC-link voltage of three-phase DC/AC MMC.

U_o DHB output voltage.

U_{OC} Battery open-circuit voltage.

U_{api} Active parallel interface capacitor voltage.

U_{api}^{min} Minimum active parallel interface capacitor voltage.

$U_{bat,n}^{sm}$ Nominal submodule battery voltage.

U_{sm} Submodule capacitor voltage.

U_{sm}^{max} Maximum submodule capacitor voltage.

U_{sm}^{min} Minimum submodule capacitor voltage.

ΔE_k MMC branch energy variation.

ΔE_{sm} MMC submodule energy variation.

ΔP_{br}^k CHB-BESS and DC/AC MMC-BESS branch balancing power.

ΔP_{ph}^{k} DC/AC MMC-BESS phase balancing power.

ΔP_{sm}^{ki} CHB-BESS ki-th submodule balancing power.

ΔP_{sm}^{kji} DC/AC MMC-BESS kji-th submodule balancing power.

Σu_{sm}^{ku} DC/AC MMC k-th phase upper branch submodule voltages sum.

β_{ki} CHB-BESS ki-th submodule power ratio factor.

β_{kji} DC/AC MMC-BESS kji-th submodule power ratio factor.

δ DHB transformer primary-secondary voltage phase-shift.

$\hat{u}_{T}^{n}$ Negative sequence grid voltage vector magnitude.

$\hat{u}_{T}^{p}$ Positive sequence grid voltage vector magnitude.

$\mathscr{F}$ Fourier transform operator.

$\mathscr{G}$ Nonparametric model family.

$\mathscr{L}$ Open-loop transfer function family.

ω_{h} Resonant controller desired compensating angular frequency.

ω_{s} DHB angular switching frequency.

$\overline{SoC}_{3br}$ CHB-BESS mean SoC value of all three branches.

$\overline{SoC}_{3ph}$ DC/AC MMC-BESS mean SoC value of all three phases.

$\overline{SoC}_{br}^{k}$ CHB-BESS k-th branch mean SoC value.

$\overline{SoC}_{br}^{kj}$ DC/AC MMC-BESS kj-th branch mean SoC value.

$\overline{SoC}_{ph}^{k}$ DC/AC MMC-BESS k-th phase mean SoC value.

$\overline{U}_{api}$ Average active parallel interface capacitor voltage.

$\overline{U}_{sm}$ Average submodule capacitor voltage.

ϕ_{i} Line current angle.

ε DC/AC MMC-BESS DC-link to AC power ratio.

ζ Resonant controller damping ratio.

f_{sw}^{api} Active parallel interface switching frequency.

f_{sw}^{iai} Indirect active interface switching frequency.

f_{sw}^{sm} Submodule switching frequency.

List of Main Symbols

i_S Generalized common-terminal current of multi-phase MMC.

i_T^{max} Maximum tolerated grid phase current.

i_j^k DC/AC MMC k-th phase j-th branch current.

i_{Tk} Generalized AC-side current of three-phase MMC.

i_{api} Active parallel interface current.

i_{bal}^k DC/AC MMC-BESS k-th phase balancing circulating current.

i_{br}^{dim} Dimensioned branch current.

i_{circ}^k k-th phase circulating current.

k_1 Active reference current contribution factor.

k_2 Reactive reference current contribution factor.

k_p^{br} Branch SoC balancing loop proportional gain.

k_p^{ph} Phase SoC balancing loop proportional gain.

k_p^{sm} Submodule SoC balancing loop proportional gain.

k_r DHB input voltage allowable ripple factor variable.

k_u Submodule capacitor voltage ripple factor.

$k_{\Delta v}$ Tolerated submodule capacitor voltage variation.

m_u^k DC/AC MMC k-th phase upper branch normalized modulation reference.

n_p DHB transformer primary turns.

n_s DHB transformer secondary turns.

p_{AC} Instantaneous three-phase active power.

p_{DC} Instantaneous DC-link active power of the DC/AC MMC.

q_{AC} Instantaneous three-phase reactive power.

t_r^{br} Rise time of the branch SoC balancing control loop.

t_r^{ph} Rise time of the phase SoC balancing control loop.

t_r^{sm} Rise time of the submodule SoC balancing control loop.

u_S Generalized common-terminal voltage of multi-phase MMC.

u_g Grid voltage in CHB converter case.

u_k k-th phase converter voltage.

u_{Tk} Generalized AC-side voltage of three-phase MMC.

u_{br}^{dim} Dimensioned branch blocking voltage.

u_{cm} Common-mode voltage.

u_{pri} DHB transformer primary voltage.

u_{sec} DHB transformer secondary voltage.

u_u^k DC/AC MMC k-th phase upper branch inserted voltage.

1 Introduction

This chapter introduces the global context, in the framework of which this thesis has been carried out. The motivation for this work is drawn from three key principal axes:

- DC/AC Modular Multilevel Converter (MMC)

- Battery Energy Storage Systems (BESS) and their integration into an MMC

- Power electronics interfaces for ultra-fast electric vehicle (EV) charging

In the following, the basic concepts and terms that are utilized throughout this thesis document are presented. A review is carried out, including the most significant scientific contributions in all three aforementioned areas. The thesis motivation and outline finalize this introductory chapter.

1.1 Modular Multilevel Converters

The term Modular Multilevel Converter, often abbreviated as MMC, M2C or even M^{2}LC, was initially used to describe the DC/AC power conversion structure proposed by [1-3]. As its name implies, the main characteristic of such a converter regards the series connection of identical submodules within a branch. The latter is shown in Figure 1.1a. Such a feature was already known from the Cascaded H-Bridge (CHB) converter of [4]. It was not after almost twenty years that this topology started being investigated for static synchronous compensator (STATCOM) applications [5], electric drives [6] as well as traction converters [7]. An inductive element completes the converter branch [8], aiming at the limitation of undesirable currents caused by the parallel connections of voltage-source-behaving power circuits as well as enhancing the converter control and protection. The latter gives finally a current-source nature to the branch. During the last decade, however, research on different branch configurations for the achievement of

several conversion schemes, has rather led to a whole family of power converters, which the term MMC can be attributed to.

According to the framework of the application, several different choices for the implementation of the submodule exist. Figure 1.1b shows the two most common cases, i.e., the half-bridge and full-bridge submodules. In the simplest case, the choice between the two is made in regard to whether the converter branch needs to provide negative voltages or not. Throughout the years, other factors such as converter protection during faults, losses, component number reduction as well as smaller footprints, have given rise to the proposal of different submodule implementations. The latter include the twin submodule [9], the clamped double submodule [10], as well as neutral point clamped and flying capacitor-based designs [11].

(a)　　　　　　　　　　　　　　(b)
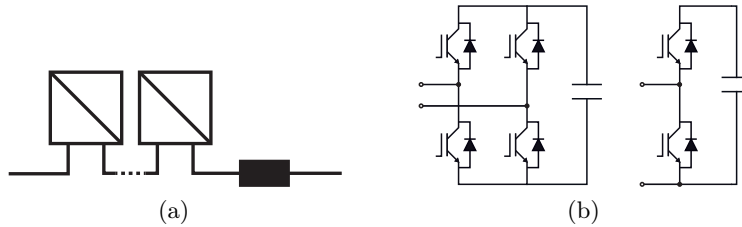
Figure 1.1: (a) A Modular Multilevel Converter branch consisting of series-connected identical submodules plus an inductor (b) possible implementations of a submodule.

The MMC has attracted a lot of industrial and academic interest during the last decade, due to the superior properties over conventional topologies for high-voltage and high-power applications [3]. The modular realization implies an easy scalability to any power and voltage levels through the utilization of standard components. Moreover, the high resolution of the produced converter waveform means that the injected currents feature very low harmonic contents, therefore any excessive filtering is avoided. This is especially beneficial in high-voltage direct current (HVDC) transmission systems, where a very large and bulky filter is normally needed in conventional IGBT-based voltage-source converter topologies. Other advantages regard the high availability as well as fault tolerance of such a modular system in case of device failures.

1.1.1 MMC Topologies and Applications

The MMC has been extensively studied during the recent years, resulting in an enormous amount of academic publications as well as patents. A wide range of applications have been considered, leading to several possible MMC configurations as illustrated in Figure 1.2.

Figure 1.2a shows the well known cases of the three-phase Cascaded H-Bridge converter in either star or delta configurations. Since the term CHB is well established in the literature, it will be kept throughout this thesis to refer to these two specific topologies,

whose implementation requires only three converter branches. Some applications of this converter were mentioned in the previous paragraphs.

Figure 1.2b illustrates an MMC structure consisting of two parallel-connected phase legs, in each one of which two branches are connected to a common midpoint[1]. The common terminals can be fed by either a DC or an AC sources. In the first case, this structure could be part of a back-to-back railway intertie [12,13]. In the second case, it can be used as a single-phase direct AC/AC converter for railway traction systems [14] or similar applications [15].

Figure 1.2c shows the most frequently encountered version of MMC in the literature. In the three-phase inverter version, this variant is used in systems requiring a DC/AC conversion. The latter include mainly HVDC systems [16-19] as well as medium voltage electric drives [9,20]. The common DC link can be substituted by an AC source. This leads to a single-/three-phase direct AC/AC conversion structure, which can be used for railway interties, i.e., the interconnection of the three-phase industrial grid with the single-phase railway supply commonly available in several European countries [12,21], or alternatively for gearless wind turbine generation systems [22]. It is noted that these are the applications, where the first commercial projects have been commissioned.

The conversion structure of Figure 1.2d is an MMC version of a DC/DC medium frequency transformer-based isolated topology. Its main use regards the interfacing of medium to high voltage DC grids as well as the converter protection enhancement against DC-link faults [23-25].

Finally, the topologies shown in Figure 1.2e-1.2f resemble the direct matrix and sparse matrix converters, respectively. They aim at the interconnection of different AC networks or electric drive applications. They have been proposed as alternatives to the typical AC/DC/AC back-to-back MMC configurations [26-30], due to their advantages mainly in the field of low-speed electric drives.

In order to achieve additional features, such as implementation with a lower number of required submodules, a number of hybrid MMC-related topologies have been also proposed in literature especially for DC/AC operation. The latter include the Alternate Arm Converter (AAC) [31] as well as the MMC with a middle cell [32].

Reference [33] proposes a general terminology for several members of the MMC family. However and since the number of available topologies is constantly evolving, this thesis work makes use of the names shown in Figure 1.2. It is also noted that this thesis deals with the first four topologies illustrated in Figure 1.2a-1.2c.

---

[1]This topology will be referred to as the two-phase DC/AC MMC, in order to distinguish it from the single phase-leg inverter considered by many researchers in the literature.

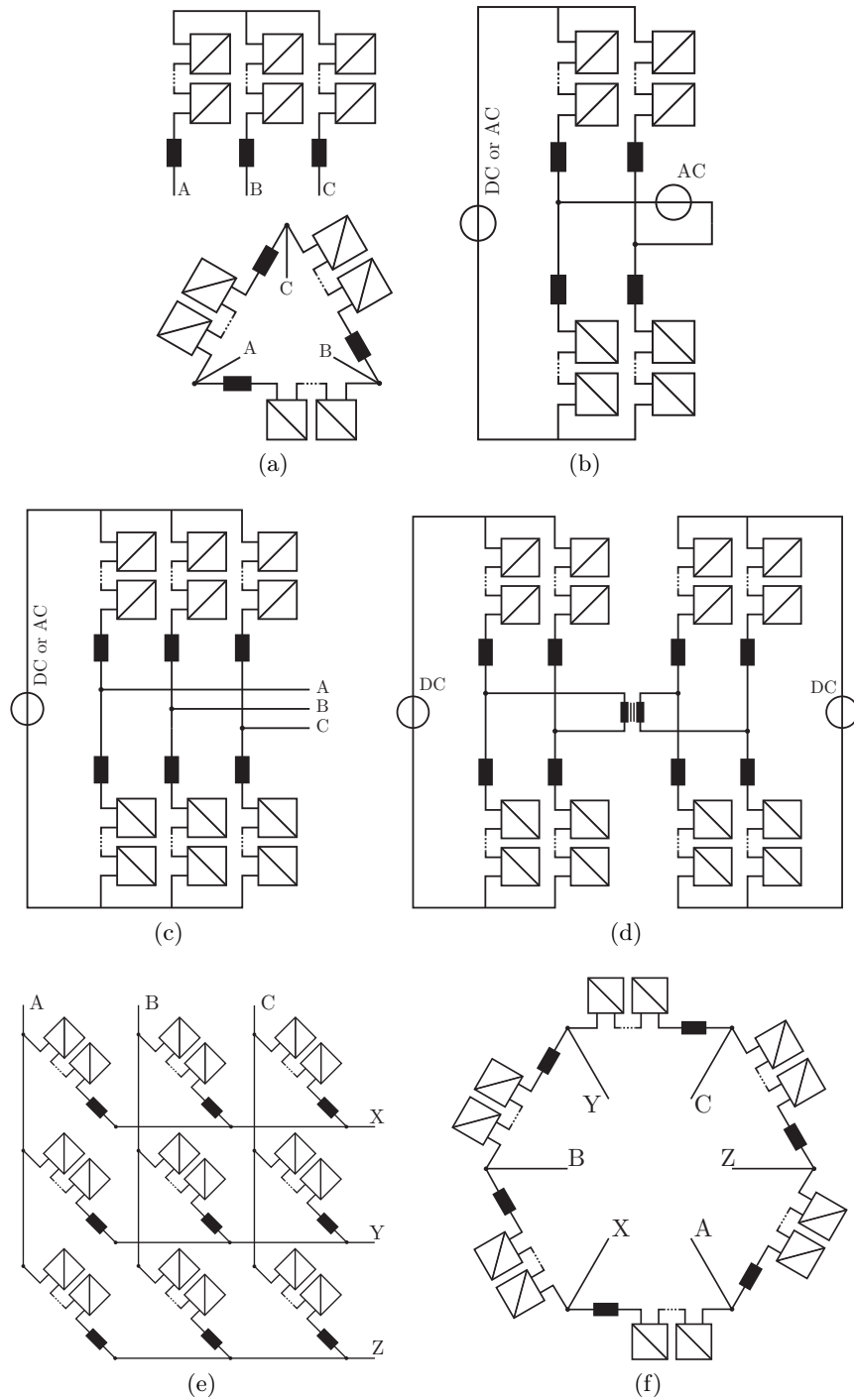Figure 1.2: Members of the Modular Multilevel Converter family found in the literature: (a) the CHB converter in either star or delta configurations, (b) two-phase DC/AC or single/single-phase direct AC/AC MMC, (c) DC/AC or single/three-phase direct AC/AC MMC, (d) isolated DC/DC MMC, (e) three/three-phase direct AC/AC MMC in matrix configuration, (f) three/three-phase direct AC/AC MMC in hexagonal configuration (Hexverter).

1.1.2 DC/AC MMC Modeling, Modulation and Control

The DC/AC Modular Multilevel Converter exhibits several topology-specific features, which make its analysis different than conventional power converters.

Initially, the converter branches are characterized by continuous current flow, contrary to the chopped currents of traditional topologies. In addition, a central DC-link capacitor does not exist, since the required storage elements are distributed within the converter branches. This capacitive nature of the phase legs, however, poses challenges in the converter design and operation, especially when the converter faces unbalanced grid conditions. Moreover and unless the submodule capacitance and branch inductance are unrealistically high, so-called circulating currents are expected to flow within the parallel-connected phase legs if the capacitor voltage ripples are not compensated for on a control or hardware level. Finally, the inversely proportional relation between the line current frequency and the submodule capacitor voltage ripples implies an impediment in the case of an MMC low output frequency operation, such as during motor drive startup or low-speed operation.

The aforementioned specificities require special attention for the comprehension of such a system's physical behavior and the development of converter control systems. The control problem of an MMC system features several sub-problems regarding the external converter magnitudes as well as inner converter quantities. In the following, some significant research contributions on the modulation and control of an MMC are referred to.

Modulation and Submodule Capacitor Voltage Balancing

The first MMC-related publications were treating the system as a typical three-phase converter case, applying line current and DC-link voltage control as needed. The only inner converter-related control regarded the even voltage distribution between the submodule capacitors of a converter branch [3,14]. The latter was performed on a space vector modulation level, by using a dynamic sorting and selection process algorithm for different submodule insert/bypass assignment according to the branch current polarity.

A similar balancing method but substituting space vector modulation by a PWM technique was proposed by [34] and has been followed by several researchers [35,36]. Such a sorting algorithm can result in non-periodic capacitor voltage peaks in low switching frequencies [37]. Tolerance-band modulation methods [38] and predictive-based algorithms [39,40] have been proposed to tackle this problem. A different approach of balancing the submodule capacitor voltages within a converter branch has been proposed by [41], which is based on individual capacitor voltage feedback loops in conjunction with the branch current polarity, similarly to what has been previously reported for the CHB converter [42,43]. The latter results in the change of each submodule's duty cycle, accordingly.

Other research works on MMC modulation concern the tailoring of several well-established multilevel converter methods, taking into account the system specificities. The latter include carrier-based methods [44], nearest level control (NLC) [45], selective harmonic elimination (SHE) [46], fundamental switching frequency modulation [47], as well as hysteresis-based modulation methods [38,48].

Modeling and Control of MMC Internal Quantities

As mentioned earlier, uncompensated capacitor voltage ripples can give rise to undesirable circulating current components within the converter branches. In addition, developed functional representation models [49,50] have illustrated the ability to handle independently the input from the output power, which is a very attractive feature of the MMC. Combining these considerations, questions have arisen about whether a superior performance can be gained by making use of all available system-specific degrees of freedom. Towards such direction, several inner converter-related variables can be specified and controlled, accordingly.

Assuming that the balancing of the submodule voltages within one converter branch is ensured by a mechanism on a modulation level, a switching-averaged MMC branch model can be deduced, such as the one proposed in [51] on a per-phase level. Similar generalized models for two- and three-phase converters are presented by other researchers as well [52,53]. Such models are mainly used for control system design as well as to decrease the simulation time when the pulse-width modulation (PWM) effects are of no interest. On a modeling level, it has to be noted that there are two different ways of describing the circulating current encountered in the literature: (a) as the one flowing on the external converter loop including the DC-link and one phase leg [41] and (b) as the one flowing between two adjacent phase legs [35]. The two definitions are of course equivalent and finally describe the same properties of the physical system.

The first publication dealing with the converter dynamics and their control was written by the authors of the conference paper [41], later published as a journal article in [54]. In these works, the total average phase-leg stored energies were controlled using cascaded outer voltage/inner circulating current loops, compensating therefore for branch capacitor voltage ripples. The same researchers added a branch voltage-difference feedback loop in [55], in order to ensure an equal energy distribution between the two branches of the same phase leg. Different implementations of this control scheme are proposed by [56] and [57] based on stationary and rotating reference frames, respectively. Contrary to the aforementioned cascaded-based control schemes, a multivariable optimal controller is proposed by [58]. In [51], the inner converter dynamics were described by means of average modeling and similar energy feedback loops were formed, acting directly on the branch modulation references and without explicit circulating current control. On the other hand, the so-called 'open-loop' MMC control scheme developed by [59] compensates

for the branch capacitor voltage ripples by using their real-time estimated values in order to appropriately change the modulation references. By doing so, the circulating current can be controlled in an indirect manner. Finally, the authors of [60] have extended this concept theoretically showing that when the estimated values are utilized in the selection of the modulation references, no additional balancing cascaded loops are necessary even if undesirable unbalances occur between the converter branches.

Operational Issues

The protection of a DC/AC MMC against DC bus short-circuits is an important field of ongoing research. Due to the fact that the submodule diodes remain forward-biased during such a fault, a solution is to be found for the very large currents that need to be supported by the latter. The solution to such a problem comes through the utilization of a thyristor switch at the terminals of each submodule [18] or the implementation of more advanced submodule topologies [10,61].

As mentioned before, the inversely proportional relation of the line current frequency to the submodule capacitor voltage ripples poses a significant impediment for the application of a DC/AC MMC in the field of medium voltage drives. The latter has been tackled by means of the employment of a special operation mode during motor startup operation by the researchers in [62]. However, this has a significant impact on the converter semiconductor dimensioning. For low-speed drives, the three/three-phase direct AC/AC converter of Figure 1.2e has been proven to be better suited [26].

Finally and as in any three-phase grid-connected system, the Modular Multilevel Converter is likely to face unbalanced conditions, such as phase-to-ground or phase-to-phase faults. However, the unique features of this converter type and especially the existence of three independent capacitive phase legs, require special attention under such a converter operation. Some research works have investigated the control of a Modular Multilevel Converter under unbalances [17,50,63,64], focusing mostly on symmetric current injection and DC-link oscillation cancellation. However, the impact of such unbalances on the converter components, such as the capacitor sizing, as well as alternative control targets under asymmetries is still an open issue requiring further investigation.

1.2 Battery Energy Storage Systems

The use of energy storage systems (ESS) nowadays can be divided into two main categories, mobile and stationary applications. In the first case, the ESS constitutes the primary power source, such as in EVs and portable consumer electronic devices (laptops, mobile phones etc.), aiming at the substitution of other types of supplies.

The second application group concerns mostly the handling of intermittent power sources on a grid-connection level. Indeed, a global trend and high expectations exist towards a more sustainable grid, where a large integration of renewable energy sources will take place and pollutant emissions will be significantly reduced. Such a distributed generation scheme is illustrated in Figure 1.3, where a sole central power plant is supplemented by several other production units, such as wind turbines and solar panels. It becomes evident that the fluctuating power nature of such units due to their dependence on external factors, such as wind and solar radiation conditions, poses several challenges. The latter includes the quick covering of the load demand at any time, as well as the handling of the electrical energy in cases of excessive generation. Battery energy storage systems play a significant role in the fulfillment of the two aforementioned conditions.
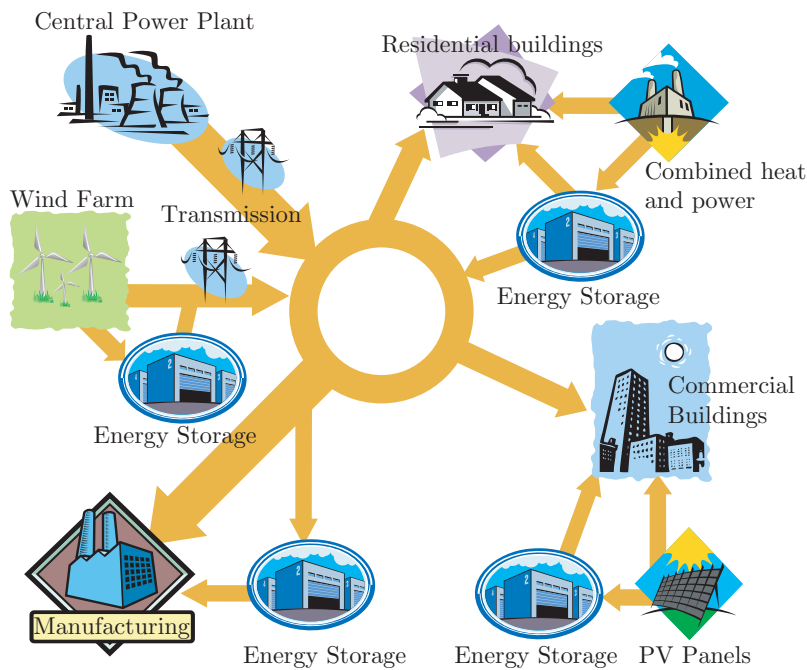
Figure 1.3: The concept of distributed generation with energy storage system components (source: [65]).

There are a great number of electrical energy storage technologies, ranging from mechanical storage systems (pumped hydro, flywheels, compressed air), electrical storage systems (superconducting magnetic energy storage, supercapacitors) as well as electrochemical storage systems (rechargeable batteries). The choice among the available energy storage technologies for a specific application is not a trivial task and depends on a large amount of design parameters. The latter include the power and discharge time ratings, capital cost, efficiency and lifetime of the energy storage system.

This thesis work focuses on general power electronic interface solutions for battery energy storage systems, therefore no considerations on application-specific storage system selection are made. The choice of a BESS is justified, however, by the increasing interest

towards such installations in modern large-scale power systems where ancillary services are needed. Table 1.1 shows such BESS-related commissioned projects in a worldwide scale. The Duke Energy Business Services Notrees Wind Storage Demonstration project in Texas, USA has the maximum rated power of 36 MW and is based on an advanced Lead Acid battery technology. However, the world record is held by the BESS project in Alaska, USA, which has a rated power of 27 MW but can support a maximum discharge of 46 MW for five minutes. The latter was completed in December 2003 and aims at the improvement of service reliability to the members of the Golden Valley Electric Association (GVEA). On the other hand, the Rokkasho village wind farm in Aomori, Japan, has the largest capacity of 238 MWh.

1.2.1 Modular Multilevel Converters and Battery Energy Storage

The choice of the power electronics interface for a battery energy storage system on a medium and high-voltage level is a very significant task, mainly due to the converter as well as battery management system (BMS) design. The Modular Multilevel Converter family offers the capability of embedding such energy storage elements in a split manner, given the existence of several submodules operating at significantly lower voltages. Indeed, contrary to utilizing only one central battery on the medium/high voltage level, aspects such as redundancy and straightforward battery management system designs can be achieved.

The integration of batteries into the sub-modules of a CHB converter has been already studied considerably [66-70]. The first real-scale 500 kW demonstrator has been developed and presented in [71]. Some works have been also discussing the use of the DC/AC MMC family member in battery energy storage applications, with the focus laid on system design [72-75]. However, [72,73] do not take advantage of the common DC-link, which is typically used to feed an external load as shown by [74]. On the other hand, [75] proposes the utilization of a single large DC-link battery, which does not benefit from the lower submodule voltage levels.

Therefore, some significant remarks are made at this point. The CHB converter offers the most straightforward and reasonable choice for a dedicated application-specific BESS unit implementation. The latter is due to the floating submodule nature, the required submodule number as well as the overall converter efficiency. However, the split accumulation concept is applicable to any kind of MMC topology given the individual DC bus existence. The global conversion character (DC/AC, AC/AC etc.) of the topology is then kept, but an enhancement of the converter with energy storage elements takes place, in cases where additional system active power capability is required.

Table 1.1: Worlwide Battery Energy Storage System Installations [76]

Name	Description	Technology	Energy (MW×h)	Location
Battery Energy Storage System (BESS)	Improve reliability of GVEA Services	Nickel cadmium (NiCd)	27×0.25 or 46×0.08	Alaska, USA
Rokkasho Village Wind Farm	Load leveling and spinning reserve	Sodium sulfur (NaS)	34×7	Aomori, Japan
National Wind and Solar Energy Storage and Transm. Demonstration Project (1-5)	Electric power interactive management	1-3) Lithium Iron Phosphate (LiFePO$_4$), 4) Lithium-ion, 5) Vanadium Redox Flow	1) 6×6, 2) 4×4, 3) 1×2, 4) 3×3, 5) 2×4	Hebei, China
Notrees Wind Energy Storage Project	Energy delivery optimization	Advanced Lead Acid	36×0.67	Texas, USA
EKZ Zurich 1 MW BESS	Frequency control, Peak shaving	Lithium-ion	1×0.5	Zurich, Switzerland
Younicos and Vattenfall Project	Fluctuation balancing	Lithium-ion, Sodium sulfur (NaS)	1.2×6.2	Berlin, Germany
Orkney Storage Park Project	Renewable power stabilization	Lithium-ion	2×0.25	Kirkwall, Orkney, UK
Auwahi Wind Farm	Wind ramp management	Lithium-ion	11×0.4	Hawai, USA
Tomamae Wind Farm	Wind smoothing	Vanadium Redox Flow	4×1.5	Hokkaido, Japan

1.3 Ultra-Fast Charging of Electric Vehicles

Similarly to what has been mentioned on a power grid level, environmental awareness and related concerns have given rise to a high interest towards electrical mobility based on battery energy storage during the recent years as well. Such an action aims mainly at the significant reduction of CO_2 and other pollutant emissions. In order to ensure the widespread utilization of such electric vehicles, however, significant effort is still needed regarding their competitive market launching over conventional combustion engine vehicles. The main impediment when it comes to electric vehicles concerns the limited battery autonomy in conjunction with the long charging times. Most often on-board chargers are utilized [77-79], fed by the domestic or public grid. When the charging power level increases, however, off-board chargers are preferred which are usually installed outside residential areas in charging stations conceptually similar to the gas filling ones [80].

A solution to the autonomy problem can be given through the utilization of the so-called battery-swap stations, where the discharged EV battery is directly replaced by a fully charged one. The latter has recently stimulated the research interest [81-83]. Some of the issues that arise, however, concern the different EV battery type compatibility as well as the charged battery availability of the station. A second attractive solution regards the fast and ultra-fast EV charging referring to less than thirty and ten minutes, respectively. The latter has been driven by the late high expectations regarding development of batteries using materials that can withstand very high charging rates [84,85] as well as the development of more advanced battery charging techniques [86].

Both industry and academia have been pushed towards the fast and ultra-fast charging for electric vehicles (UFCEV) concept exploration. The main focus has been initially laid on the infrastructure as well as grid impact [87,88]. In order not to overload the grid in such a power demanding application, the use of stationary energy storage elements has been proposed [89-92]. Such storage systems play the role of power buffers, aiming at the reduction of the instantaneous active power extracted from the grid.

Figure 1.4 illustrates an example of such a stationary battery energy storage system utilization in the framework of an ultra-fast EV charging station utilization. The fictive load profile generation has taken place based on real traffic density data [91,93] and assuming 5 minute charging times for a number of 200 EVs throughout a typical day. It is evident that especially during rush hours, the required instantaneous EV charging power can reach up to 1.6 MW, which could cause grid overloading issues. The grid power, however, can be significantly reduced through the use of the intermediate storage buffer. Figure 1.4 shows two possible examples of load leveling and shifting, respectively. In the first case, the moving average over an hour is drawn from the grid. In the second case the stationary battery absorbs energy mostly during nighttime, when the ultra-fast EV charging station load is minimal. Consequently, the energy is released during grid peak hours, when the station is heavily loaded.
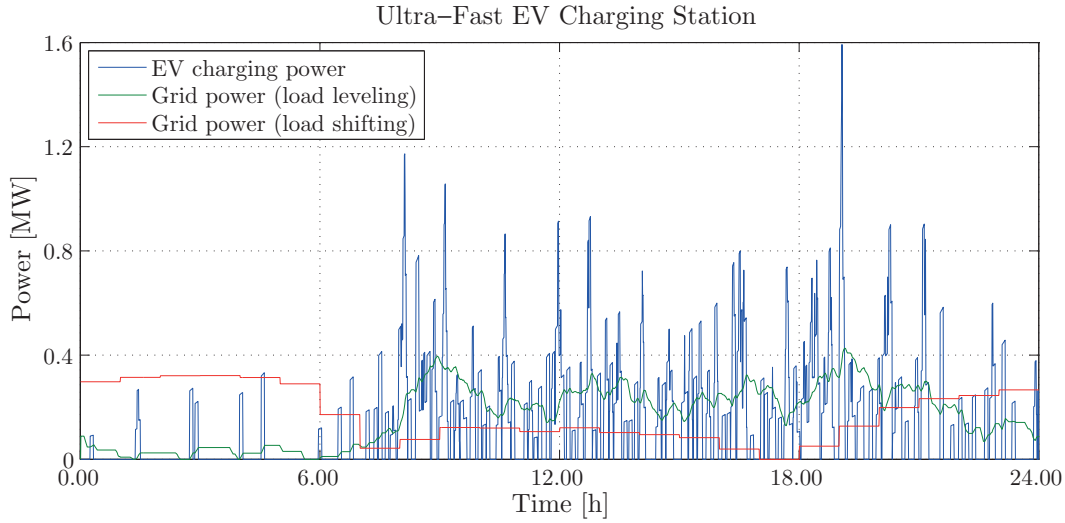
11

Figure 1.4: Load profile for a fictive ultra-fast 5 minute charging of 200 EVs/day utilizing intermediate battery energy storage buffer. Results are based on load traffic density statistical data [91].

1.3.1 Proposed PET-based UFEVCS implementation

Advanced and emerging converter technologies, such as power electronic transformers, are expected to play a key role in the development of the future charging stations, both in terms of flexibility and efficiency [69,87,93-96]. The Electric Power Research Institute (EPRI) claims an up to 8% overall system efficiency increase through their Utility Direct Fast Charger Technology [95]. The term Power Electronic Transformer (PET) refers to an active conversion structure featuring isolation in the medium-frequency (MF) range, contrary to the traditional utilization of low frequency power transformers. This leads to lower volume and size in the system due to the absence of the bulky low frequency transformer, additional control degree of freedoms due to the use of active devices, as well as better overall system efficiency in certain cases. Such converters have been already utilized in railway traction [7,97,98], network coupling and back-to-back loop power flow control [99,100], as well as microgrid applications [101,102].

In [69], we proposed a novel multiport converter architecture for the implementation of medium voltage ultra-fast EV charging station (UFEVCS), based on such a concept. The latter is shown in Figure 1.5. The costly and bulky low frequency transformer is avoided through the utilization of a CHB multilevel converter. The latter also offers the possibility to significantly reduce the filtering components on the grid side, since the injected currents exhibit very low harmonic content. As mentioned in the previous section, the CHB converter offers another advantage, i.e., the possibility to integrate battery energy storage elements on the level of each submodule in a split manner. This storage stage plays the role of the power buffer, as explained in the previous paragraph. Finally and as in any PET application, medium frequency transformer-based DC/DC

converters are connected in parallel. In this case such an action achieves the needed high output currents as well as meeting the EV battery galvanic isolation standards. Compared to the similar converter structure of [96], the proposed converter features two main advantages. Initially, no central high-capacity battery is needed due to the split accumulation concept, leading to the advantages mentioned in Section 1.2.1. In addition and since a high number of submodules are needed to block the medium voltage on the grid side, different configurations can be chosen on the parallel-connection level in order to achieve a multiport output, capable of charging different vehicles simultaneously. Therefore, additional high-power chargers are not needed, leading to higher efficiencies due to the equal power split between the existing isolated converters. However, the converter control becomes more complicated, due to the need for all power flow directions handling.
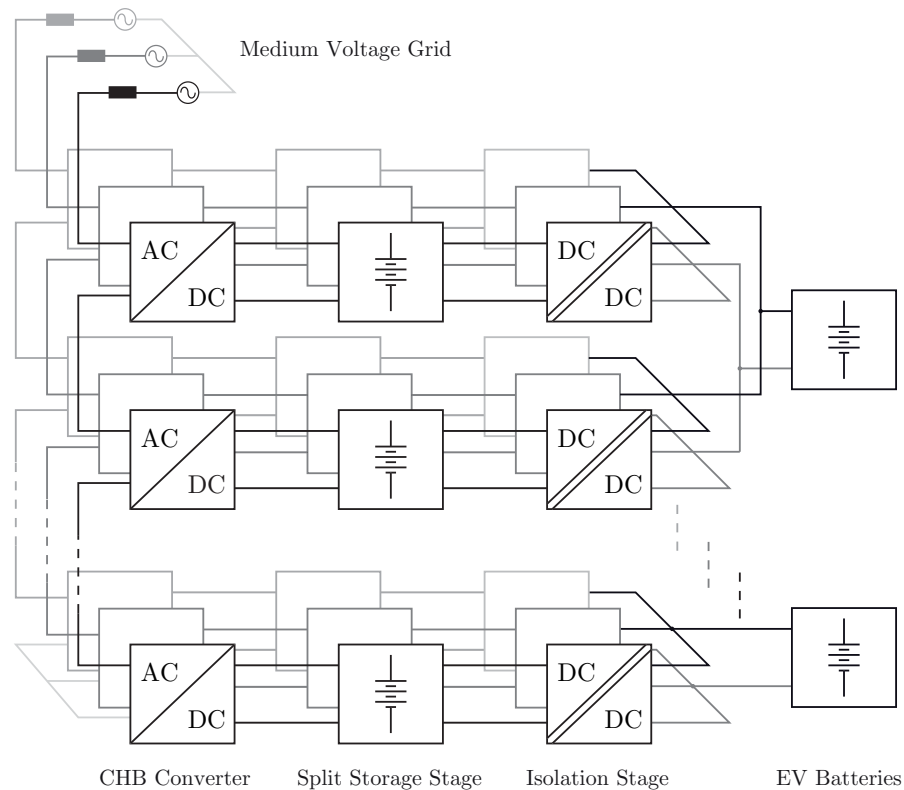

Figure 1.5: The proposed modular versatile Power Electronic Transformer-based multiport ultra-fast EV charging station

1.4   Thesis Motivation and Objectives

The previous sections have revealed that significant ongoing research is being carried out around the three aforementioned axes. Especially in the field of Modular Multilevel Converters, more than a number of 500 published papers, patents etc. have appeared in the last five years. Several associated problems, however, require further discussions and research and new directions are being constantly opened.

Initially, the accurate capacitor voltage ripple estimation in a DC/AC Modular Multilevel Converter is a very interesting feature for several reasons. It has been shown that the MMC is a complex converter topology requiring several different control layers. In general, it can be argued that the choice for control hardware configuration and hierarchy for an MMC is closely related to the respective choice for control system design and implementation. If the balancing of the individual submodule voltages is guaranteed by a localized mechanism, such as the one described in [3], it could be beneficial that the global MMC control will not need to acquire their measured values. Towards this direction, the submodule capacitor voltage ripple estimation implies the simplification of the communication scheme between the different hardware components, in the sense of exchanged data amount reduction. Therefore, the implementation of the so-called open-loop control schemes of works such as [59,60] is improved. The analytical solutions of the capacitor voltage ripples, however, can even be used in closed-loop capacitor voltage feedback control loops, such as the ones presented in [55-57]. Both the total phase leg and branch difference voltage controlled quantities exhibit low frequency components that are usually filtered out, decreasing therefore the control system bandwidth. By adding the estimated components to the reference values of these control loops, the average components can be directly extracted and fed to the respective regulators. This improves the control system behavior. Finally, the knowledge of the accurate submodule voltage variation is also significant for converter design purposes, since the resulted analytical expressions can be utilized for the dimensioning of the required MMC capacitive storage.

In addition, the operation of a three-phase grid-connected DC/AC MMC under unbalanced conditions needs to be investigated. As it has been already pointed out, the particularities of such a topology make its analysis different than conventional ones. In a typical three-phase converter comprising a central DC-link capacitor, several choices for grid current control have been established, which lead to different desired results for the system active and reactive power flows [103]. When the three-phase grid faults can be modeled by means of symmetrical components, which constitutes a fair assumption in the majority of real applications, such considerations can be done for the MMC case as well. However, the existence of three independent capacitive phase legs and the topology-specific circulating currents imply a different impact of the grid asymmetries on the dimensioning of the MMC components as well as additional degrees of freedom for the system control. Therefore, the tailoring of the well-known line current control for balanced current injection as well as active/reactive power oscillation elimination is to be carried out in order to discover

the potential trade-offs as well as make reasonable choices.

The integration of battery energy storage systems into Modular Multilevel Converter arises several topology-specific issues, which need to be overcome. The first impediment comes from the fact that the submodules of such converters buffer low frequency power components as a result of the independent phase-leg nature. Already published works on the CHB converter with integrated split BESS (CHB-BESS) unit [66,71] usually utilize oversized submodule capacitors to limit these components. However, it could be beneficial to prevent low frequency currents from flowing into the batteries. Therefore, active or passive interfacing solutions are worth being investigated as shown by [69,70,74,75], but also novel propositions are to be made. The analysis and control of MMC systems with integrated split energy storage also becomes different than their typical operation, given the need for handling all possible system power flows. Normally such converters reveal the need of balancing the submodule capacitor voltages in all unbalance directions. In the integrated BESS case, the additional control problem of battery balancing exists. It is noted that the trend in several modern battery technologies is to achieve as flat voltage curves as possible in function of their State of Charge (SoC) in a wide regime. This implies the need for a balancing algorithm targeting directly at the SoCs and no longer at the battery voltages. Such SoC balancing actions were initially proposed in the work of [66] for the case of the CHB-BESS system with direct submodule/battery interface. Although effective, there is room for improvement on the manipulated variable definition for control system design as well as an enhancement through their analytical controller gain limitation establishment. In addition, the operation of such a BESS system under unbalanced grid conditions poses the requirements for the extension of the existing independent system power flow equations. Finally, the application of the developed control methods in different topologies by appropriately tailoring the developed concepts and defining the SoC unbalance directions, will reveal the applicability on any MMC-based topology where such active power elements are added on the level of each submodule.

Finally, the proposed PET-based ultra-fast EV charging station needs to be investigated. A choice of a suitable topology for the implementation of the isolated DC/DC conversion stage is to be performed. This converter topology has to fulfill several requirements, such as low charging current ripple, bidirectional power flow as well as soft switching over a wide output voltage range. Since the ultra-fast charging can be performed up to almost 80% of the EV battery SoC due to the inner nonlinear electrochemical battery processes, a current control method must be deduced for a typical constant current (CC) charging technique. Finally, the global UFEVCS control system derivation will reveal the feasibility of the multiport implementation, in terms of independent power flow handling, SoC balancing etc.

1.5   Thesis Outline

Chapter 1 has provided the necessary material and a review on the three principal axes that are dealt with in this thesis report. The used MMC-related terminology has been introduced and the most significant publications of the domain have been referred to, including MMC topologies and applications, modeling, modulation and control as well as operating issues. The need for battery energy storage systems in modern large-scale power systems has been pointed out, along with the necessity for advanced power electronics interfacing converters. Finally, the concept of ultra-fast EV charging has been reviewed as found in existing literature, together with out proposal of a novel PET-based architecture for the implementation of future infrastructures of this type. The rest of this document is structured as follows:

Chapter 2 initially summarizes briefly the modeling principles of a Modular Multilevel Converter and derives the equations that form the basis for the submodule voltage ripple expressions. The analytical solutions for the example cases of a three- and two-phase DC/AC MMCs of Figure 1.2b and 1.2c. The latter aims at the generalization and enhancement of the voltage ripple estimation concepts presented in literature. Therefore, any strong assumptions are avoided and all passive elements as well as intentionally injected common-mode voltage and circulating current harmonics are taken into consideration. Moreover, the documentation and comprehensive illustration of the natural charge level mechanism of the branch capacitor voltages is provided. In a second step, current control considerations for grid-connected MMCs are made, deducing two independent feedback loops for the line and circulating currents. It is noted that for the two-phase case, the concept of fictive axis emulation (FAE) is chosen to achieve line current vector control. These concepts are also validated experimentally in a down-scaled laboratory prototype. In a third step, the operation of the three-phase grid-connected DC/AC MMC under unbalanced conditions in explored. Three cases of positive and negative sequence line current control are applied and compared in terms of impact on branch energy variation as well as maximum delivered active power.

Chapter 3 deals with the CHB-BESS unit in either star or delta configuration. Initially, it provides an overview of the passive and active solutions for the submodule/battery interface problem. The choice of a nonisolated DC/DC conversion stage in cascade is made and the rest of the converter analysis is based on this. The topology-specific degrees of freedom are exploited and the control problem is split in three sub-problems, namely submodule capacitor voltage, independent power as well as SoC balancing. Control algorithms are developed and analytical gain limitations are established. Moreover, several modes of operation are studied, including independent load feeding, SoC balancing as well as converter operation under grid faults. The SoC self-balancing operating mode of the delta-connected CHB-BESS unit is also introduced. The chapter is finalized by the presentation of experimental results from a down-scaled laboratory setup.

Chapter 4 tailors the developed concepts of Chapter 3 for the case of the three-phase DC/AC Modular Multilevel Converter with integrated split battery energy storage. An additional converter-specific submodule/battery interfacing solution is mentioned and discussed. All possible operating modes and power flow directions are described. The SoC balancing problem is augmented by the third unbalance direction, namely between the branches of the same phase leg, contrary to the only two existing unbalance direction of the respective CHB-BESS. The overall control system is deduced and verified by means of simulations. Finally, experimental results are provided using the same versatile prototype in a different configuration.

Chapter 5 deals with the proposed PET-based converter architecture for medium voltage ultra-fast EV charging stations. The motivation for the topology derivation is initially explained. Then, the Dual Half-Bridge (DHB), which is employed among a big number of available solutions for the isolation stage implementation, is analyzed in terms of duty cycle control and its impact on the soft-switching regions. The design of an output current digital control scheme is thoroughly described for two cases: high and low output resistance. The latter is based on the use of nonparametric models in conjunction with an optimization procedure. The parallel connection of different DC/DC modules and the control system design is validated through simulations and experimental results. In the second part of this chapter, a global control scheme for the UFEVCS is deduced, which is an extension of the method presented in Chapter 3. Simulations from a model of the whole station featuring four EV charging ports prove the stable operation of the proposed converter architecture.

Finally, **Chapter 6** provides the overall conclusions as well as main contributions of this thesis work. Perspectives and future research directions and developments are also pointed out.

2 DC/AC Modular Multilevel Converters

2.1 Introduction

This chapter deals with the DC/AC Modular Multilevel Converter. Initially the average modeling principles are presented, which are widely used in the literature, together with some topology-specific terminology. The accurate capacitor voltage ripple estimation is then treated, which is important for several reasons, including the submodule capacitance dimensioning as well as its use for the converter control.

The decoupled line and circulating current control for the grid-connected cases of the three- and two-phase MMC is then formed. The latter can be used to effectively control independently the input and output converter powers. This is a unique topology-related feature compared to conventional converter technologies.

Finally, the operation of an MMC under grid unbalances is investigated. Once again the MMC has distinctive features, which require further analysis during grid fault mode. Some established choices for converter control in such a scenario are applied on the MMC case, in order to analyze their impact on the MMC components.

2.2 Modeling Principles of an MMC

In Figure 2.1a a structural representation of a three-phase Modular Multilevel Converter is illustrated. As expected in a practical application, a large number of series-connected submodules results in a high apparent multilevel PWM frequency. The latter leads to an accurate average approximation of the branch quantities, motivating the modeling of the converter utilizing a unique *equivalent submodule* per branch. The mid-point of the common link is grounded for facilitation of the analysis. When the MMC is connected to a DC line, L_S and R_S represent the filter or line inductance and u_S is a DC voltage source. In the case of a transformerless single/three-phase direct AC/AC converter they denote the grid choke that handles short-circuit currents [12], and u_S is the single-phase AC

grid voltage. On the three-phase side, L_T and R_T represent the transformer or machine leakage inductance and cable resistance, whereas the branch inductances and resistances are symbolized with L and R accordingly. Finally, u_{Tk} is the grid or motor back emf, respectively.

It is noted that throughout this chapter, the following subscripts/superscripts are utilized: $k \in \{a, b, c\}$ referring to the studied phase and $j \in \{u, l\}$ to the upper/lower branches of the same phase leg.
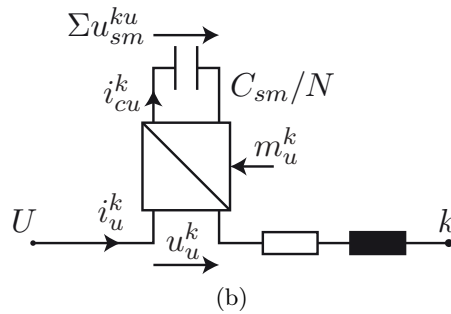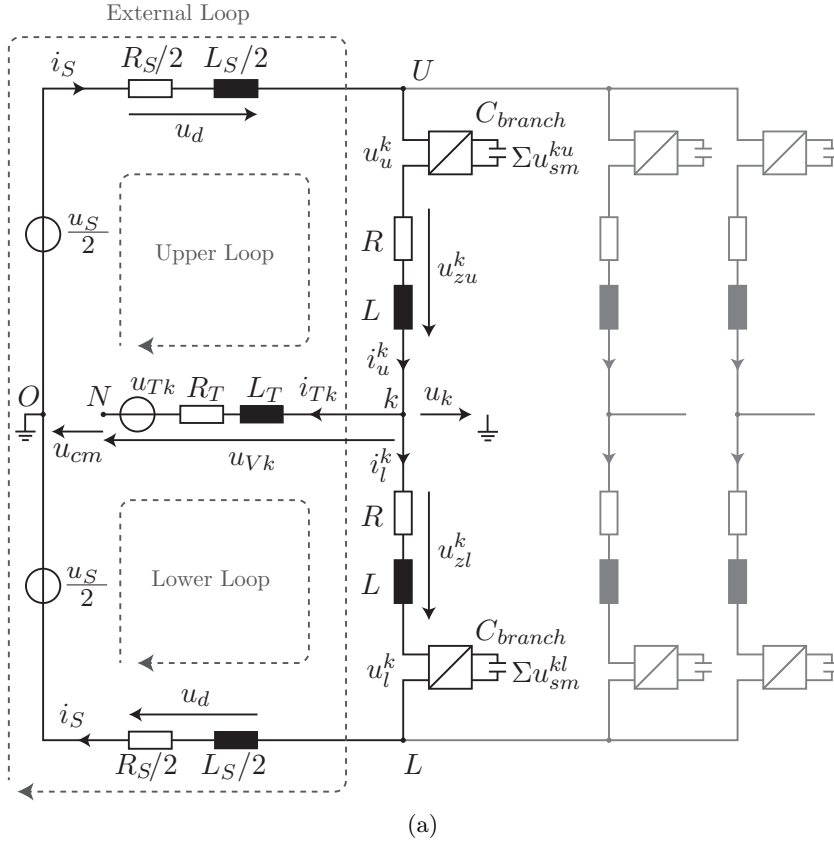

(a)

(b)

Figure 2.1: (a) Multi-phase Modular Multilevel Converter, (b) Detailed representation of a converter branch with one equivalent submodule.

2.2.1 Derivation of Total Submodule Voltage Ripples

In order to obtain the analytical expression for the submodule capacitor voltages of the Modular Multilevel Converter, the fundamental capacitor current equation is considered, taking as an example the upper branch of a converter phase leg. This relates the current i_{cu}^k that flows through the equivalent capacitance C_{branch} with the sum of all the submodule voltages Σu_{sm}^{ku} in one converter branch.

$$C_{branch}\frac{d\Sigma u_{sm}^{ku}}{dt} = i_{cu}^k \Leftrightarrow \frac{C_{sm}}{N}d\Sigma u_{sm}^{ku} = m_u^k i_u^k dt \Leftrightarrow \frac{C_{sm}}{N}d\Sigma u_{sm}^{uk}\Sigma u_{sm}^{ku} = u_u^k i_u^k dt \quad (2.1)$$

In the above equation (2.1), N denotes the number of submodules in one converter branch, each one of which having a capacitance of C_{sm}. The quantity m_u^k represents the normalized modulation reference for the upper branch and u_u^k is the voltage applied by the series connection of the branch submodules, which are PWM-controlled. By integrating (2.1), the following expression is derived,

$$\frac{C_{sm}}{2N}(\Sigma u_{sm}^{ku})^2 - \underbrace{\frac{C_{sm}}{2N}(\Sigma u_{sm0}^{ku})^2}_{\Sigma E_0^{sm}} = \int u_u^k i_u^k dt = \int p_c^{ku} dt \quad (2.2)$$

where the appearing integration constant ΣE_0^{sm} refers to the DC value of the total submodule stored energy. It is therefore clear that the product $u_u^k i_u^k$ corresponds to the power contribution of the submodules to the branch, and its integral forms the total stored capacitive energy. This equation is the basis for the voltage estimation of the capacitor voltage ripples.

Taking into consideration Figure 2.1a, the following relation (2.3) is formed for the capacitive instantaneous power,

$$p_c^{ku} = u_u^k i_u^k = \left(u_U - u_k - u_{zu}^k\right) i_u^k = \left[u_U - (u_{Vk} + u_{cm}) - \left(i_u^k R + L\frac{di_u^k}{dt}\right)\right] i_u^k$$

$$= \underbrace{[u_U - (u_{Vk} + u_{cm})]\,i_u^k}_{p_{branch}^{ku}} - \underbrace{\left(i_u^k\right)^2 R}_{p_R^{ku}} - \underbrace{L\frac{di_u^k}{dt}i_u^k}_{p_L^{ku}} \quad (2.3)$$

where the phase voltage u_k comprises the fundamental frequency (u_{Vk}) plus a common-mode (u_{cm}) components. The terms p_{branch}, p_R and p_L correspond to the total branch power, the losses in the branch resistance as well as the reactive power consumed by the inductor, respectively. For the lower branch, the power and energy equations become:

$$p_c^{kl} = u_l^k i_l^k = \left(u_k - u_L - u_{zl}^k\right) i_l = \left[-u_L + (u_{Vk} + u_{cm}) - \left(i_l^k R + L\frac{di_l^k}{dt}\right)\right] i_l^k$$

$$= \underbrace{[-u_L + (u_{Vk} + u_{cm})]\, i_l^k}_{p_{branch}^{kl}} - \underbrace{\left(i_l^k\right)^2 R}_{p_R^{kl}} - \underbrace{L\frac{di_l^k}{dt} i_l^k}_{p_L^{kl}} \qquad (2.4)$$

The integration finally gives the respective capacitive energy variation in upper and lower branches. Therefore, it becomes evident that (2.2) can be used for the accurate estimation of the submodule voltage ripples. It is noted that these equations are valid for any given DC/AC or AC/AC Modular Multilevel Converter configuration. The difference lies in the desirable shapes of the voltage u_S, current i_S (DC or AC respectively) as well as the intentional imposition of the so-called circulating currents within the converter phase-legs, which will cause different frequency components in the branch currents.

In the next section, two specific examples are chosen in order to apply this theory, namely the three-phase and two-phase DC/AC MMC cases. As a remark and for the simplification of the analysis, the voltage drop on R_S and L_S is disregarded in the modeling procedure. This implies that the voltage u_{UL} is considered to be known. The latter forms a fair assumption, since this magnitude can be either actively adjusted (in the case of a current-controlled single-phase AC grid), or directly measured (in typical DC/AC systems).

Capacitor Voltage Natural Charge Level Mechanism

The integration constant ΣE_0^{sm} of (2.2) is of significant importance and is not to be confused with the inner current control of an MMC, since their action mechanisms are different. As depicted in Figure 2.1b, the equivalent submodule should provide a specific voltage u_u^k. Once the voltage reference u_u^{k*} is defined as a result of the two current loops described in the following sections, the choice of m_u^k can be considered furthermore as a degree of freedom for the capacitor charge level, since its input/output power equilibrium is dictated by the physics of the system. Indeed, the following relation holds,

$$m_u^k = \frac{u_u^{k*}}{\Sigma u_{sm0}^{ku} + \Sigma \tilde{u}_{sm}^{ku}} \qquad (2.5)$$

where $\Sigma \tilde{u}_{sm}^{ku}$ denotes the sum of the branch capacitor voltage ripples.

The *normalization constant* Σu_{sm0}^{ku} can be freely chosen to charge/discharge the capacitor voltages as intended. This is better illustrated in the example of Figure 2.2. By increasing the normalization constant at t = 40 ms, the modulation reference m_u^k obviously decreases. The instantaneous difference of the voltage sum $(u_u^k + u_l^k)$ from the DC link voltage u_{UL} is capable of inducing a specific amount of current i_s/m in the branch (m being the number of parallel-connected phase-legs), which in turn charges the capacitors at a higher level. When the new equilibrium is reached, the quantities m_u^k and Σu_{sm0}^{ku} are changed, in order to maintain unaltered voltages u_{UO} and u_k, respectively. It should be noted that this

concept is valid even in the case of a direct modulation reference scheme without further control actions, justifying the attributed title of a *natural mechanism.*
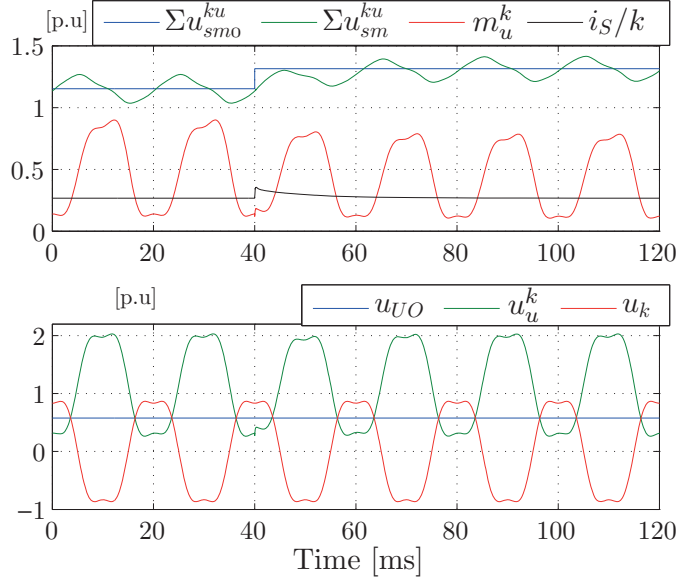

Figure 2.2: Illustrative demonstration of the branch capacitor voltage charge level control mechanism.

2.3 Accurate Capacitor Voltage Ripple Estimation for Modular Multilevel Converters

As already stated in the introductory chapter, the application areas of the three-phase grid-connected DC/AC Modular Multilevel Converter are wide and include HVDC systems, active front ends, as well as medium voltage electric drives. As far as the two-phase case is concerned, it can be found as an alternative proposal for back-to-back interties (e.g. the interconnection of the three-phase industrial grid with the single-phase railway supply).

2.3.1 Analytical Solution of the Power Equations

By exploring Figure 2.1a, it is clear that each phase leg forms two internal AC loops and one external loop, respectively. In the latter loop, which in the studied case can be considered as an independent 'DC loop' for each phase, the contribution of i_S to each branch current would ideally be i_S/k. However, additional undesirable currents are also flowing within a converter phase leg, if the capacitor voltage ripples are not taken into account in the control and modulation scheme. These currents are known as circulating currents and their mathematical definition varies in literature. In this paper, it is considered that the current through the DC terminals is part of the circulating current without any loss of generality. This means that the latter will essentially comprise DC

23

and AC components and can therefore be defined in its general form as

$$i_{circ}^k = \underbrace{I_{circ0}}_{i_S/k} + \sum_{n=1}^{\infty} \hat{i}_{circ,n} \cos(n\omega t + \theta_n) \tag{2.6}$$

Furthermore, the common-mode voltage of the three-phase MMC can also bear DC and AC components and can be defined similarly as

$$u_{cm} = U_{cm0} + \sum_{n=1}^{\infty} \hat{u}_{cm,n} \cos(n\omega t + \xi_n) \tag{2.7}$$

The line-side fundamental harmonic magnitudes are given by

$$u_{Vk} = \hat{u}_V \cos\left(\omega t - \frac{2\pi(m-1)}{3}\right) \tag{2.8}$$

$$i_{Tk} = \hat{i}_T \cos\left(\omega t + \phi_i - \frac{2\pi(m-1)}{3}\right) \tag{2.9}$$

where $m=1,2,3$ and a phase angle of ϕ_i between the converter voltage and the line current is assumed. In addition, the branch currents are defined as

$$i_u^k = \frac{i_{Tk}}{2} + i_{circ}^k \tag{2.10}$$

$$i_l^k = -\frac{i_{Tk}}{2} + i_{circ}^k \tag{2.11}$$

assuming that the branch impedances are symmetrical and therefore the line current splits equally between the upper and lower branches of the same phase leg.

At this point, it is also assumed that the circulating current can be explicitly controlled. This is verified in the next section.

Three-phase MMC

As stated in [104], if the circulating current is chosen to bear even harmonics, there will be no unbalance between the branches of the same phase leg. Other works have also shown that it is beneficial to intentionally inject a second-order harmonic, in terms of capacitor voltage ripple reduction [12,104,105], which in turn leads to decreased needs for embedded capacitive energy. Hence, taking phase leg a as an example the desirable circulating current becomes

$$i_{circ}^a = I_{circ0} + \hat{i}_{circ,2} \cos(2\omega t + \theta_2) \tag{2.12}$$

In such a three-phase application, the common-mode voltage can be chosen to correspond to a typical third harmonic injection, which results in the increase of the maximum modulation index:

$$u_{cm} = \hat{u}_{cm,3} \cos(3\omega t + \xi_3) = -\frac{1}{6}\hat{u}_V \cos(3\omega t) \tag{2.13}$$

Accordingly, the voltage drop on the branch inductances and resistances will finally become as follows:

$$u_{zu}^a = Ri_u^a + L\frac{di_u^a}{dt} = R\left[I_{circ0} + \frac{\hat{i}_T}{2}\cos(\omega t + \phi_i) + \hat{i}_{circ,2}\cos(2\omega t + \theta_2)\right]$$
$$+ \omega L\left[-\frac{\hat{i}_T}{2}\sin(\omega t + \phi_i) - 2\hat{i}_{circ,2}\sin(2\omega t + \theta_2)\right] \tag{2.14}$$

The instantaneous branch power is finally modified as in (2.15a), whereas the power terms referring to the respective branch resistance and inductance are obtained as in (2.15b) and (2.15c).

Two-phase MMC

The two-phase MMC can be treated similarly. It is obvious that adding a second-order harmonic component to the circulating current would affect the DC-link current [12,13], although this might not always be a disadvantage depending on the application. On the

$$p_{branch}^{au} = u_U I_{circ0} - \frac{\hat{u}_V \hat{i}_T}{4}\cos\phi_i + \frac{u_U \hat{i}_T}{2}\cos(\omega t + \phi_i) - \hat{u}_V I_{circ0}\cos(\omega t) - \frac{\hat{u}_V \hat{i}_{circ,2}}{2}\cos(\omega t + \theta_2)$$
$$+ \frac{\hat{u}_V \hat{i}_{circ,2}}{12}\cos(\omega t - \theta_2) + u_U \hat{i}_{circ,2}\cos(2\omega t + \theta_2) - \frac{\hat{u}_V \hat{i}_T}{4}\cos(2\omega t + \phi_i) + \frac{\hat{u}_V \hat{i}_T}{24}\cos(2\omega t - \phi_i)$$
$$- \frac{\hat{u}_V \hat{i}_{circ,2}}{2}\cos(3\omega t + \theta_2) + \frac{\hat{u}_V I_{circ0}}{6}\cos(3\omega t) + \frac{\hat{u}_V \hat{i}_T}{24}\cos(4\omega t + \phi_i) + \frac{\hat{u}_V \hat{i}_{circ,2}}{12}\cos(5\omega t + \theta_2) \tag{2.15a}$$

$$p_R^{au} = R\left(I_{circ0}^2 + \frac{\hat{i}_{circ,2}^2}{2} + \frac{\hat{i}_T^2}{8} + \hat{i}_T I_{circ0}\cos(\omega t + \phi_i) + \frac{\hat{i}_T \hat{i}_{circ,2}}{2}\cos(\omega t - \phi_i + \theta_2) + \frac{\hat{i}_T^2}{8}\cos(2\omega t + 2\phi_i)\right.$$
$$\left. + 2I_{circ0}\hat{i}_{circ,2}\cos(2\omega t + \theta_2) + \frac{\hat{i}_T \hat{i}_{circ,2}}{2}\cos(3\omega t + \phi_i + \theta_2) + \frac{\hat{i}_{circ,2}^2}{2}\cos(4\omega t + 2\theta_2)\right) \tag{2.15b}$$

$$p_L^{au} = \omega L\left(-\frac{\hat{i}_T I_{circ0}}{2}\sin(\omega t + \phi_i) - \frac{\hat{i}_T \hat{i}_{circ,2}}{4}\sin(\omega t - \phi_i + \theta_2) - 2\hat{i}_{circ,2}\sin(2\omega t + \theta_2)\right.$$
$$\left. - \frac{\hat{i}_T^2}{8}\sin(2\omega t + 2\phi_i) - \frac{3\hat{i}_T \hat{i}_{circ,2}}{4}\sin(3\omega t + \phi_i + \theta_2) - \hat{i}_{circ,2}^2\sin(4\omega t + 2\theta_2)\right) \tag{2.15c}$$

other hand, choosing a plain DC circulating current leads to constant power transfer to the DC-link, canceling therefore the intrinsic pulsating behavior of any single-phase system. This is useful when choosing to avoid placing passive resonant filters, which are widely used in railway interties, adding cost, volume and hardware complexity. Furthermore and taking into account that no third-order common-mode voltage injection can be added to a single-phase system for increase of the modulation index, (2.12)-(2.14) become as follows:

$$i_{circ}^a = I_{circ0} \tag{2.16}$$

$$u_{cm} = 0 \tag{2.17}$$

$$u_{zu}^a = Ri_u^a + L\frac{di_u^a}{dt} = R\left[I_{circ0} + \frac{\hat{i}_T}{2}\cos(\omega t + \phi_i)\right] - \omega L\frac{\hat{i}_T}{2}\sin(\omega t + \phi_i) \tag{2.18}$$

2.3.2 Choice of Circulating Current Components

The explicit relations for the circulating current components can now be derived by taking into account the fact that $p_c^{ku} = p_{branch}^{ku} - p_R^{ku} - p_L^{ku}$. The capacitor power should be of zero average, in order to maintain a stable charge. Therefore, the constant terms in the respective mathematical expression need to compensate for each other.

Three-phase MMC

The aforementioned considerations can be formulated in for the case of the three-phase MMC as follows:

$$u_U I_{circ0} - \frac{\hat{u}_V \hat{i}_T}{4}\cos\phi_i - R\left(I_{circ0}^2 - \frac{\hat{i}_{circ,2}^2}{2} - \frac{\hat{i}_T^2}{8}\right) = 0 \tag{2.19}$$

In the above relation, the first two terms denote the input and output powers. The three last terms refer to the resistive losses within the branch, which are caused by the squared DC (I_{circ0}) and AC *rms* values of the circulating current ($i_{circ,2}$), as well as half of the respective output current value ($i_{Tk}/2$). This means that if I_{circ0} is chosen according to power equilibrium, the total branch submodule capacitor voltages will be stable without the need for additional actions. In order to compensate for the losses within the converter branch, I_{circ0} is evaluated by solving the previous second-order equation (2.19).

Regarding the values of $\hat{i}_{circ,2}$ and θ_2, different possibilities exist. By examining the power equations (2.15a)-(2.15c), it can be observed that the second harmonic (2ω) is the dominant component of the submodule voltages after the one of the fundamental frequency (ω). Thus, a reasonable choice would be to compensate for this frequency, in order to suppress it significantly [12]:

$$u_U \hat{i}_{circ,2} \cos(2\omega t + \theta_2) - \frac{\hat{u}_V \hat{i}_T}{4} \cos(2\omega t + \phi_i) = 0 \overset{\theta_2 = \phi_i}{\Longrightarrow} \hat{i}_{circ,2} = \frac{\hat{u}_V \hat{i}_T}{4 u_U} \qquad (2.20)$$

By choosing the angle of the second-order harmonic component as $\theta_2 = \phi_i$, a constant value for $\hat{i}_{circ,2}$ is achieved in (2.20) and the steady-state analytical expressions are simplified significantly. The remaining power terms of second harmonic order in (2.15a)-(2.15c) will then be significantly smaller, due to their scaling factors ($1/24$, R and ωL).

After the elimination of the terms associated with (2.20) the power equations can be finally integrated, in order to acquire the explicit relations for the total capacitive energy fluctuation, which is stored in the upper branch of each phase leg. For the sake of completeness, this long equation is provided in the bottom of the page (2.21), taking into account the integration constant corresponding to the amount of DC capacitive stored energy in steady state operation. The respective formulas for the lower branches and other phase legs can be derived in a similar manner.

Two-phase MMC

The two-phase case can be obviously considered as a respective three-phase without imposition of second-order harmonic circulating current component and common-mode voltage injection. Therefore, the equations can be modified by setting the respective

$$E_c^{au} = \Sigma E_{sm}^0 + \frac{u_U \hat{i}_T}{2\omega} \sin(\omega t + \phi_i) - \frac{\hat{u}_V I_{circ0}}{\omega} \sin(\omega t) - \frac{R \hat{i}_T I_{circ0}}{\omega} \sin(\omega t + \phi_i) - \frac{L \hat{i}_T I_{circ0}}{2} \cos(\omega t + \phi_i)$$

$$+ \frac{R \hat{i}_T \hat{i}_{circ,2}}{2\omega} \sin(-\omega t + \phi_i - \theta_2) - \frac{\hat{u}_V \hat{i}_{circ,2}}{2\omega} \sin(\omega t + \theta_2) - \frac{L \hat{i}_T \hat{i}_{circ,2}}{4} \cos(-\omega t + \phi_i - \theta_2)$$

$$+ \frac{\hat{u}_V \hat{i}_{circ,2}}{12\omega} \sin(\omega t - \theta_2) - \frac{R I_{circ0} \hat{i}_{circ,2}}{\omega} \sin(2\omega t + \theta_2) - \frac{R \hat{i}_T^2}{16\omega} \sin(2\omega t + 2\phi_i) - \frac{L \hat{i}_T^2}{16} \cos(2\omega t + 2\phi_i)$$

$$- L I_{circ0} \hat{i}_{circ,2} \cos(2\omega t + \theta_2) - \frac{\hat{u}_V \hat{i}_T}{48\omega} \sin(-2\omega t + \phi_i) - \frac{R \hat{i}_T \hat{i}_{circ,2}}{6\omega} \sin(3\omega t + \phi_i + \theta_2)$$

$$- \frac{\hat{u}_V \hat{i}_{circ,2}}{6\omega} \sin(3\omega t + \theta_2) - \frac{L \hat{i}_T \hat{i}_{circ,2}}{4} \cos(3\omega t + \phi_i + \theta_2) + \frac{\hat{u}_V I_{circ0}}{18\omega} \sin(3\omega t) - \frac{L \hat{i}_{circ,2}^2}{4} \cos(4\omega t + 2\theta_2)$$

$$- \frac{R \hat{i}_{circ,2}^2}{8\omega} \sin(4\omega t + 2\theta_2) + \frac{\hat{u}_V \hat{i}_T}{96\omega} \sin(4\omega t + \phi_i) + \frac{\hat{u}_V \hat{i}_{circ,2}}{60\omega} \sin(5\omega t + \theta_2) \qquad (2.21)$$

$$p_c^{au} = \frac{u_U \hat{i}_T}{2} \cos(\omega t + \phi_i) - \hat{u}_V I_{circ0} \cos \omega t + \omega L \frac{\hat{i}_T I_{circ0}}{2} \sin(\omega t + \phi_i) - R \hat{i}_T I_{circ0} \cos(\omega t + \phi_i)$$

$$- \frac{\hat{u}_V \hat{i}_T}{4} \cos(2\omega t + \phi_i) + \frac{\omega L \hat{i}_T^2}{8} \sin(2\omega t + 2\phi_i) - \frac{R \hat{i}_T^2}{8} \cos(2\omega t + 2\phi_i) \qquad (2.22)$$

$$E_c^{au} = \Sigma E_{sm}^0 + \frac{u_U \hat{i}_T}{2\omega} \sin(\omega t + \phi_i) - \frac{\hat{u}_V I_{circ0}}{\omega} \sin \omega t - \frac{R \hat{i}_T I_{circ0}}{\omega} \sin(\omega t + \phi_i) - \frac{L \hat{i}_T I_{circ0}}{2} \cos(\omega t + \phi_i)$$

$$- \frac{\hat{u}_V \hat{i}_T}{8\omega} \sin(2\omega t + \phi_i) - \frac{L \hat{i}_T^2}{16} \cos(2\omega t + 2\phi_i) - \frac{R \hat{i}_T^2}{16\omega} \sin(2\omega t + 2\phi_i) \qquad (2.23)$$

parameters $\hat{i}_{circ,2}$ and θ_2 to zero as well as reintroducing the compensated term of (2.20). This results eventually in (2.22) and (2.23) provided at the bottom of the previous page.

Table 2.1: MMC Simulation/Down-Scaled Prototype Parameters

Quantity	Value	Comment
S_n	4.2 kVA/phase	Rated power
$\tilde{u}_T$	400 V	Rated line voltage (rms)
$\tilde{i}_T$	18 A	Rated current
N	4	Submodules/branch
k_u	0.1	Capacitor voltage ripple factor
L, R	2.3 mH, 0.2 Ω	Branch inductance/resistance
L_T, R_T	4 mH, 0.5 Ω	Grid inductance/resistance
L_S, R_S	0.1 mH, 0.1 Ω	DC-link inductance/resistance
u_S	750 V	DC-link voltage

2.3.3 Simulation Results

Both the three- and the two-phase systems have been simulated using the parameters summarized in Table 2.1, which regard the nominal values of a reduced-scale implemented laboratory setup. The converters are current-controlled in a closed-loop manner according to the considerations and implementation, which is developed in the next section. The results are given in Figure 2.3a and 2.3b, respectively. More specifically, the upper figures show the estimated as well as the numerically calculated values of the total submodule capacitor voltage ripples, which correspond to the upper branch of phase leg A for both cases. It can be observed that the two curves almost coincide. The middle figures illustrate that both upper and lower branches are balanced in terms of voltage level and shifted by π. Finally, the lower figures depict the respective values of the circulating current components. The latter comprises a DC as well as a superimposed AC components with the same amplitude at the second harmonic frequency for the three-phase MMC. On the contrary, only a DC value is considered for the two-phase case. In order to demonstrate the suppression of the second-order harmonic power oscillation, which also leads to a branch energy variation reduction, the same capacitance values were utilized for both simulations. It becomes therefore obvious that in the case of the pure DC circulating current and for the same input power, a larger voltage ripple can be observed in the total capacitor voltages.

2.3.4 Capacitive Storage Requirements

The solution of the branch capacitor energy fluctuation in (2.21) presents another significant contribution. It can be used to accurately identify the capacitive storage requirements for a specific converter design, extending the results introduced by [3]. The analytic calculation of the capacitor energy variation ΔE_{sm} would lead to complicated expressions
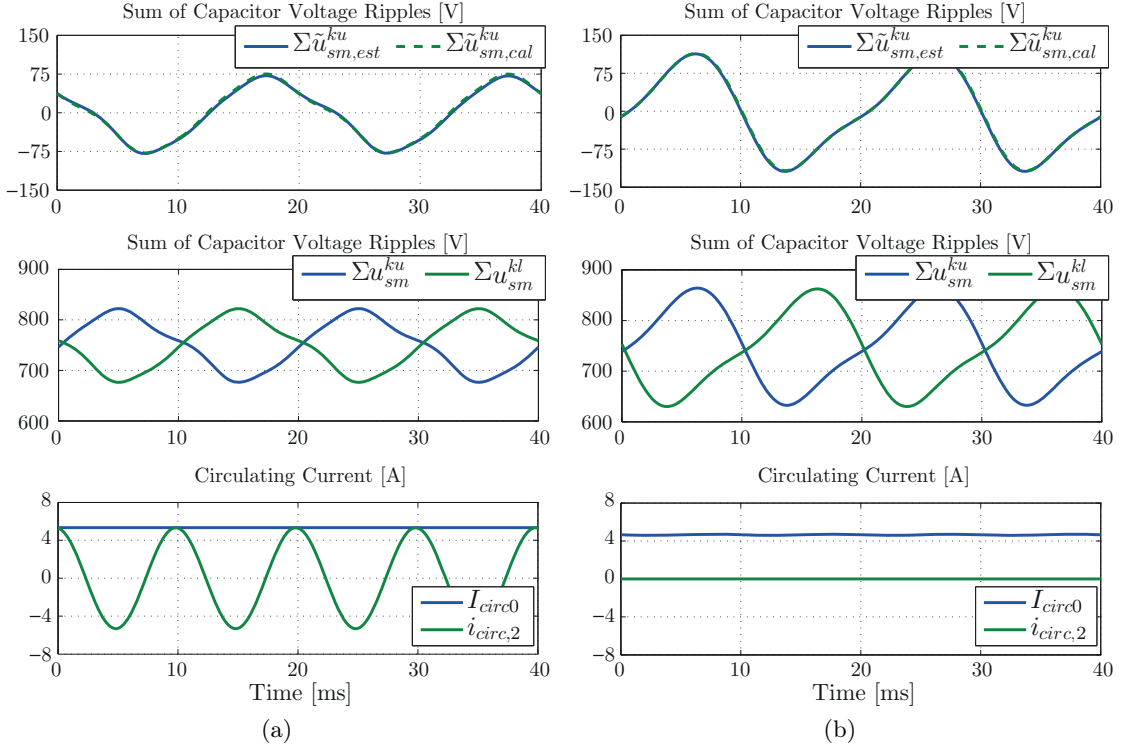
Figure 2.3: Numerically calculated sum of the submodule voltage ripples in upper branch of phase leg a in regard with the estimated value (upper figure). Middle figure shows the sum of submodule voltages in upper and lower branches. The circulating current components are shown in the lower figure: (a) three-phase and (b) two-phase MMC.

that cannot be easily handled. Instead, the global minimum and maximum of (2.21) within one period of the grid frequency can be evaluated numerically for any given operating point. For an allowable voltage deviation k_u from its average value (ripple factor), the following equation (2.24) can be utilized for the calculation of the required capacitance [3],

$$C_{sm} = \frac{2\Delta E_{sm}}{(U_{sm}^{max})^2 - (U_{sm}^{min})^2} = \frac{\Delta E_{sm}}{2k_u\overline{U}_{sm}^2} \tag{2.24}$$

where the maximum submodule capacitor voltage is defined as $U_{sm}^{max} = \overline{U}_{sm}(1 + k_u)$ and the respective minimum as $U_{sm}^{min} = \overline{U}_{sm}(1 - k_u)$.

Considering a balanced utilization of the submodules within one branch in terms of voltage sharing, the individual submodule energy fluctuation can be expressed as $\Delta E_{sm} = \Delta E_k/N$, linking therefore (2.24) with (2.21).

Table 2.2 shows the results for the numerical calculations performed for the cases of a pure DC circulating current as well as an imposed second-order harmonic. The simulated values are taken from the studied case of Table 2.1. It is clearly observed that the deliberate imposition of the harmonic component $i_{circ,2}$ achieves a capacitive reduction in the range of 30%. However, the branch current value will be higher, leading to an increased requirement for installed switching power [26], leading also to an expected decrease in the overall efficiency.

Table 2.2: MMC Capacitive Design Numerical Calculations

i_{circ}	ΔE_{sm} (J)	C_{sm} (mF)	i_u^{max} (A)
I_{circ0}	5.5	0.77	18.3
$I_{circ0} + i_{circ,2}$	3.62	0.52	24

The branch capacitor energy fluctuation ΔE_c can be estimated with great accuracy, given the high apparent branch PWM frequency. Very low switching frequencies, however, can lead to small inaccuracies in the individual capacitor energy variation estimations ΔE_{sm}. In a real application, the ripple margin k_u can be set higher to account for such imperfections, or more advanced advanced modulation algorithm can be implemented [38,39]. Taking into consideration the non-idealities of the balancing algorithms is beyond the scope of this thesis.

2.4 Current Control Considerations for an MMC

By formulating the upper and lower inner AC voltage loop laws in Figure 2.1a, the following differential equations can be obtained on a per-phase level,

$$\underbrace{\left(-\frac{u_S}{2} + u_d\right)}_{-u_U} + \left(u_u^k + Ri_u^k + L\frac{di_u^k}{dt}\right) + u_k = 0 \tag{2.25}$$

$$\underbrace{\left(-\frac{u_S}{2} + u_d\right)}_{u_L} + \left(u_l^k + Ri_l^k + L\frac{di_l^k}{dt}\right) - u_k = 0 \tag{2.26}$$

where $u_k = R_T i_{Tk} + L_T \frac{di_{Tk}}{dt} + u_{Tk} + u_{cm}$.

As only the fundamental harmonic of the line current needs to be controlled, the common-mode voltage component can be neglected in the disturbance vector. The continuous-time state space representation can be formulated by considering the states $x_k = (i_{Tk}\ i_{circ}^k)^T$, the manipulated variables[1] $u^k = (u_u^k\ u_l^k)^T$ as well as the disturbances $w_k = (u_{Tk}\ u_{UL})^T$.

---

[1]The symbol of the k-th phase manipulated variable vector u^k should not be confused with the fundamental harmonic component of the k-th phase converter voltage u_k.

Defining furthermore $L_{eq} = L + 2L_T$ and $R_{eq} = R + 2R_T$, the following relation is obtained

$$\dot{x}_k = Ax_k + Bu^k + Dw_k \qquad (2.27)$$

where

$$A = \begin{pmatrix} -\frac{R_{eq}}{L_{eq}} & 0 \\ 0 & -\frac{R}{L} \end{pmatrix}, \ B = \begin{pmatrix} -\frac{1}{L_{eq}} & \frac{1}{L_{eq}} \\ -\frac{1}{2L} & -\frac{1}{2L} \end{pmatrix}, \text{ and } D = \begin{pmatrix} -\frac{2}{L_{eq}} & 0 \\ 0 & -\frac{1}{2L} \end{pmatrix}.$$

The fact that A is a diagonal matrix shows that a decoupled current control of these two magnitudes is at hand. This statement is quite important and implies that in fact the input power can be controlled independently from the output power [49]. In the studied case, the circulating current has been modeled to bear a DC component associated with the output power. In the case where the common terminals are connected to a single-phase grid, such a property also holds with an appropriate and equivalent definition of i_{circ}^k.

Figure 2.4 shows the block diagrams for the proposed line and circulating current control loop implementations, again on a per phase leg basis. The block $G_{pe}(s)$ represents the first-order transfer function which models the application-specific delays T_{pe}^{line} and T_{pe}^{circ}, caused by the modulator, measurement and computational system as well as sampling time [106].

(a)

(b)
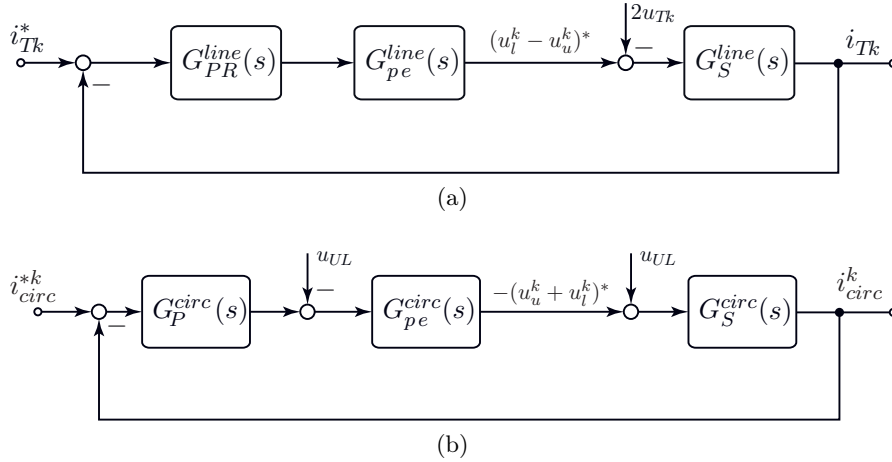
Figure 2.4: Current control loop block diagrams for: (a) line current and (b) circulating current.

The two respective system transfer functions $G_S^{line}(s)$ and $G_S^{circ}(s)$ are expressed as

$$G_S^{line}(s) = \frac{1}{R_{eq} + sL_{eq}} \qquad (2.28)$$

$$G_S^{circ}(s) = \frac{1}{2(R + sL)} \qquad (2.29)$$

which shows that they are typically of first-order. This is similar to [56] but considering the branch resistances as well.

2.4.1 Line Current Control

The line current control can be performed as for any grid-connected voltage source converter in a stationary reference frame (SRF) or rotating reference frame (RRF), and according to the transfer function $G_S^{line}(s)$ given by (2.28). Two different methods have been chosen for the cases of the three- and two-phase systems and are described in the following.

Three-phase MMC

A proportional-resonant (PR) controller has been chosen for the three-phase MMC case, which is expressed by (2.30) in a generalized manner [107].

$$G_{PR}^{line}(s) = K_p^{line} + \sum_{h=2n+1} \frac{2K_{ih}^{line}\omega_c s}{s^2 + 2\omega_c s + (h\omega)^2} \tag{2.30}$$

The transfer function of (2.30) comprises a proportional plus several resonant terms. These can be tuned to control odd harmonic frequencies ($h\omega$), which are the most prominent in a typical current spectrum [107,108]. This is especially beneficial in cases of harmonically polluted networks, where a Modular Multilevel Converter might also be required to provide active filtering services. The cutoff frequency ω_c is utilized in order to avoid the practical stability, real-time implementation, as well as parameter (such as grid frequency) variation issues associated with a theoretically infinite gain at the chosen AC frequencies [107,108]. An additional advantage of the PR controller is the fact that grid voltage disturbance feed-forwarding is not necessary, in contrast to the case of a rotating reference frame current controller where such an action is usually preferred. This is illustrated in Figure 2.4a. In such a case, the three-phase system will be controlled in a SRF, therefore two resonant controllers need to be implemented.

Two-phase MMC

A PR control would be suitable for the two-phase Modular Multilevel Converter as well. In this thesis report, however, an alternative solution is presented for the case where the RRF implementation is preferred. In order to imitate the behavior of a three-phase system and achieve a straightforward active/reactive power regulation through a current vector proportional-integral (PI)-based control scheme, a fictive axis emulator is utilized [109]. The general idea behind the concept is to utilize the β-component of the phase voltage $u_{T\beta}$ as well as the vector control output u_{ab}^β, in order to generate the imaginary component

of the line current $i_{T\beta}$ by means of the system transfer function itself. The block diagram of the algorithm is depicted in Figure 2.5. However, a modification needs to take place, in order to account for the branch inductances and resistances as well. Thus, the quantities L_{FAE} and R_{FAE} for the two-phase structure are given by (2.31).

$$L_{FAE} = L_{eq} \quad , \quad R_{FAE} = R_{eq} \tag{2.31}$$

It is noted that the imaginary component of the grid phase voltage $u_{T\beta}$ can be generated through the use of a second-order generalized integrator (SOGI) [110]. Finally, the block named u_{cmd} refers all the associated delays linked to modulation, measurements and computational time, which need to be modeled in order to keep the symmetry between the two axes.
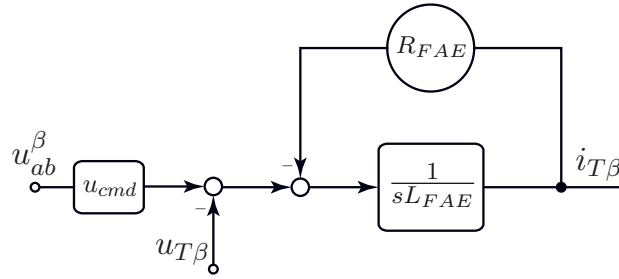
Figure 2.5: The Fictive Axis Emulation (FAE) concept for line current vector control of a two-phase Modular Multilevel Converter.

2.4.2 Circulating Current Control

For the circulating current control, a proportional term K_p^{circ} has been implemented as the transfer function of $G_P^{circ}(s)$. Figure 2.4b shows that in this case, a feed-forward disturbance rejection signal of the DC-link voltage u_{UL} is also used. Since an *abc* frame is kept, three such controllers need to be implemented in this case.

By using a proportional term for the circulating current control, a steady state error will appear between the reference and the measured values, especially in the case where a sinusoidal value has to be tracked. For the elimination of this error, two more terms could be added to the respective controller transfer function. Therefore, it would consist of a proportional term, an integral action for controlling the DC part of the circulating current as well as a resonant term for the imposed second-order harmonic component. This is shown in (2.32).

$$G_{PIR}^{circ}(s) = K_p^{circ} + \frac{K_i^{circ}}{s} + \frac{2K_{i2}^{circ}\omega_c s}{s^2 + 2\omega_c s + (2\omega)^2} \tag{2.32}$$

In such a case, the rejection of the disturbance u_{UL} in the sense of feed-forwarding would not be necessary.

2.4.3 Simulation Results

The dynamic performance of the closed-loop system has been tested with the parameters taken from Table 2.1, both for the cases of the three- and two-phase Modular Multilevel Converter. The time-domain implementation of the current controllers with the associated signal processing blocks are depicted in Figure 2.6.
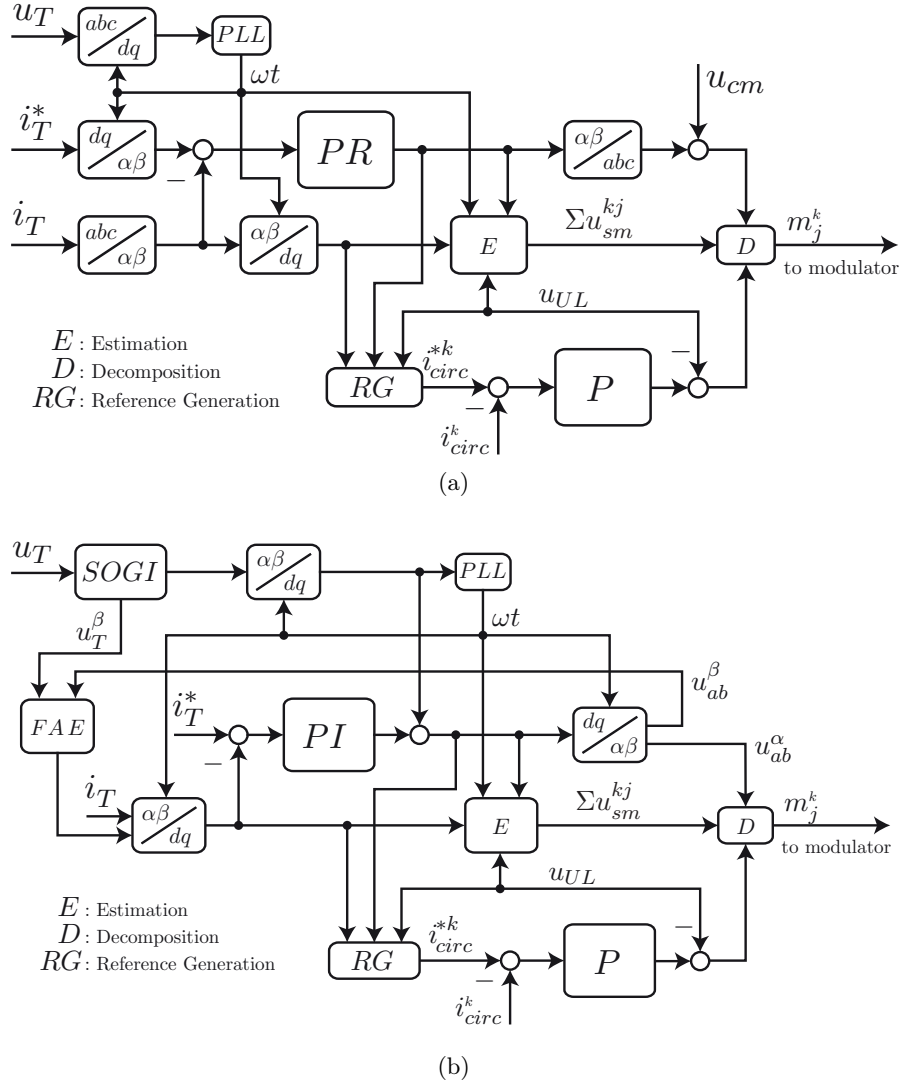

E : Estimation
D : Decomposition
RG : Reference Generation

(a)

E : Estimation
D : Decomposition
RG : Reference Generation

(b)

Figure 2.6: Time-domain MMC current control implementation with estimation of capacitor voltage ripples: (a) three-phase and (b) two-phase converter cases.

The control of line and circulating currents of the three-phase MMC is shown in Figure 2.7a, where for reasons of graphical clarity only the first phase is depicted. At $t = 120$ ms and while the line current of phase a is at its peak (≈ 24 A), a power flow reversal is executed to an active current of $\hat{i}_{Ta} = 22$ A. This is immediately followed by an injection of reactive power at $t = 160$ ms, which corresponds to a current component with a peak

value of 15 A in rotating reference frame. It can be clearly observed that both controllers bring the system to steady state after a few cycles, without threatening the stability. The DC bus current i_S is also illustrated, which is clearly a continuous current, since the AC components of the three-phase circulating currents add up to zero.

The same test has been performed for the case of the two-phase MMC and the results are displayed in Figure 2.7b. Here the effectiveness of the FAE is also well demonstrated. The orthogonal line current component $i_{T\beta}$ acts in a fast and accurate way, following closely all the transients of the actual current $i_{T\alpha}$. The circulating currents of both phase-legs contain only a DC component, and therefore lead to a constant power transfer, canceling therefore the second-order harmonic oscillating behavior of the DC-link current i_S, which is also therefore a continuous quantity.

(a) Three-phase MMC   (b) Two-phase MMC
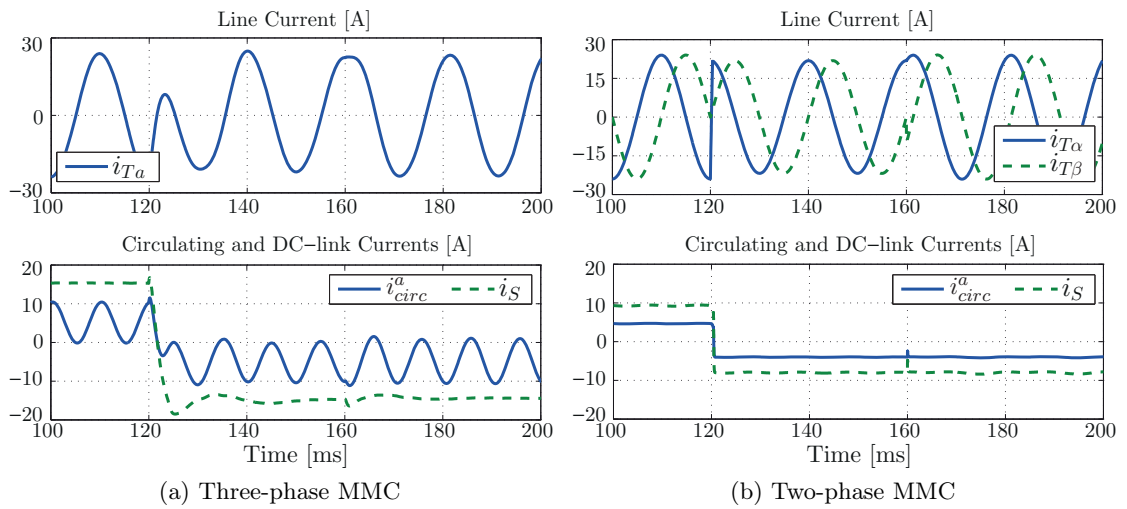
Figure 2.7: MMC control system response to consecutive current reference step changes: i) i_d^{ref} from 24 to -18A at t = 140 ms, followed by ii) i_q^{ref} from 0 to -15A at t = 160 ms. Only phase-leg a-related magnitudes are depicted.

2.5 Experimental Tests

A versatile multi-phase MMC prototype has been designed and realized in the Laboratory of Industrial Electronics at EPFL. This reduced-scale laboratory setup, which has been used for the validation of the proposed concepts, is shown in Figure 2.8. It has been also extended, accordingly, in order to experimentally test the concepts that are proposed in the next chapters. The design and development of the MMC prototype is the result of a team effort and is described in detail in the Appendix A.

Figure 2.9a illustrates the results from a three-phase converter rectifying operation. The power factor is controlled to be unity, therefore the line currents are in perfect phase opposition with their respective grid phase voltages. The line-line converter voltages are
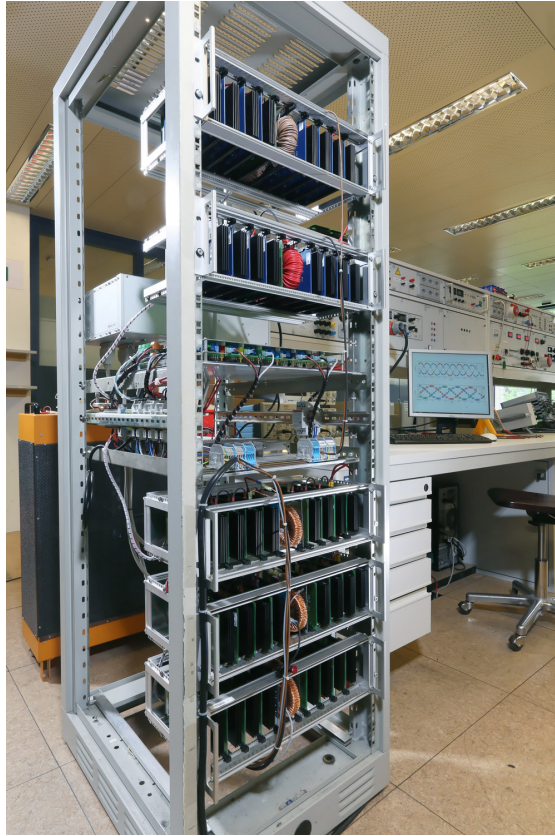
Figure 2.8: The multi-phase Modular Multilevel Converter prototype.

PWM-controlled with a triangular carrier signal of 5 kHz per branch and can comprise up to $(4N+1)$ distinct voltage levels at high modulation indexes. The intentional second-order harmonic on the circulating current of phase a is visible, which has been imposed according to (2.20). This in turn produces a respective component on the two branch currents without, however, affecting the output current.

In a second step, the setup is reconfigured so as to have a two phase-leg converter structure connected to a single-phase voltage source. The synchronization with the grid is carried out using a SOGI-phase-locked loop (PLL) structure. The representative results for a steady state operation are shown in Figure 2.9b. The dashed-lined curves in the graphs of line current and grid phase voltage are a direct result of the FAE and SOGI utilization, respectively. As the converter is operated at a high modulation index, the measured voltage u_{ab} between the converter terminals features all the possible levels. The circulating current is very closed to being continuous, leading to almost sinusoidal branch currents, obviously in contrast with the respective figure of the three-phase counterpart.

In order to validate the accuracy of the estimation equations in the three-phase MMC studied case, the total submodule voltage ripples in both upper and lower branches of phase a are illustrated in Figure 2.10. The measured values are in good agreement with

the estimated ones, although there are some slight differences which are mainly due to measurement and control inaccuracies. It is obvious, however, that the second harmonic component on the capacitive ripples has been suppressed by means of the respective harmonic injection ($i_{circ,2}$).
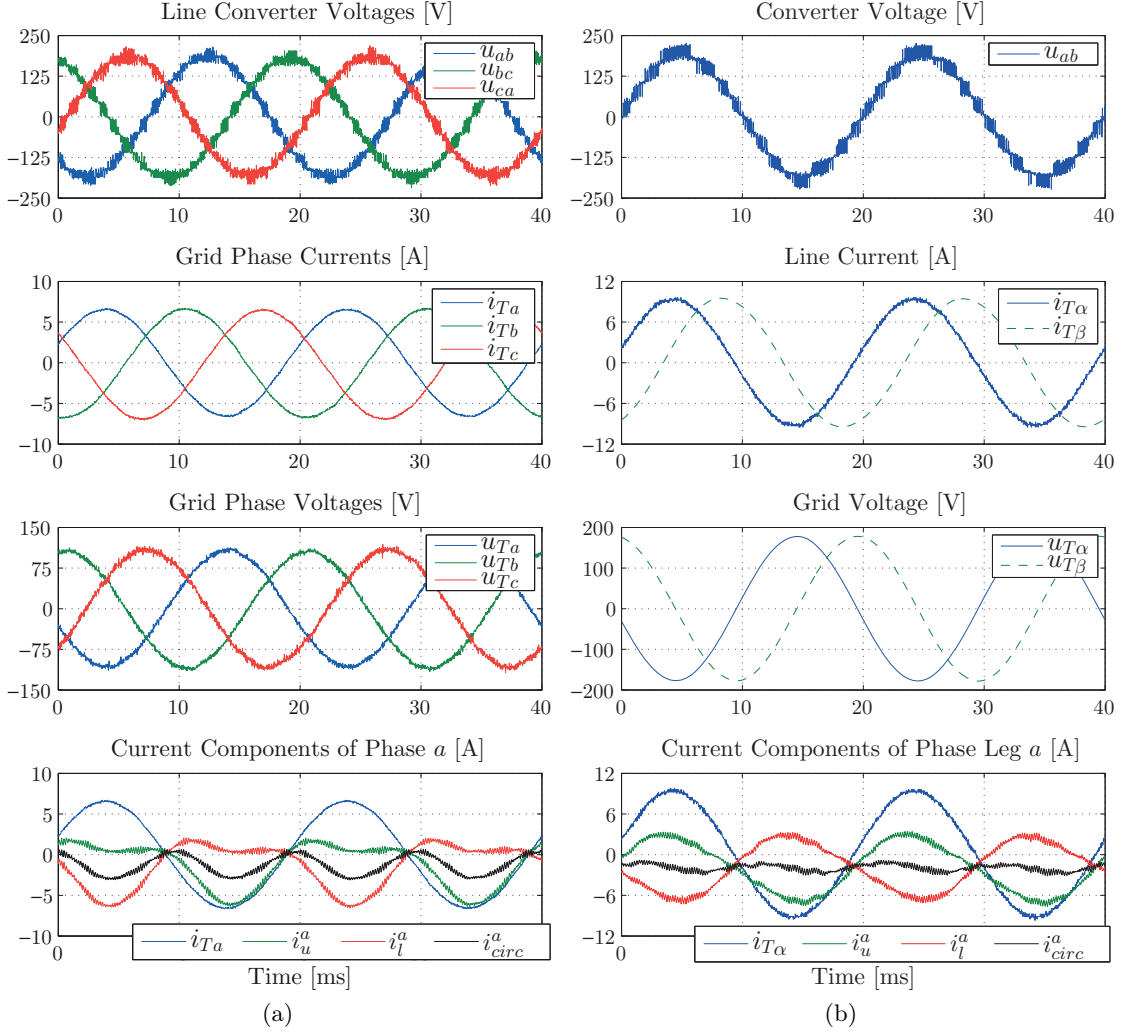

Figure 2.9: Experimental results for a: (a) three-phase DC/AC Modular Multilevel Converter and (b) two-phase DC/AC Modular Multilevel Converter hardware configurations.

Finally, the effect of a second-order harmonic injection in the circulating current is validated experimentally for the three-phase DC/AC MMC case in inverting operation. The results for phase a are shown in Figure 2.11. Initially, the circulating current is controlled to bear a DC component. At $t \approx 0.09$ s, the imposition of $i_{circ,2}$ takes place according to (2.12), leading to an expected increase of the branch current peak values. The top graph depicts the voltages for two submodules in the upper and lower branches of phase a, where the respective ripple decrease from 9 to 5.5V is visible. The capacitor voltage harmonics due to the second-order circulating current as well as third-order

common-mode voltage harmonic injections, as presented in (2.15), can be also observed. It is noted that due to some measurement noise, the full bandwidth of the circulating current control was not reached, which is the reason for the small oscillations until the moment that the respective desired harmonic is imposed.
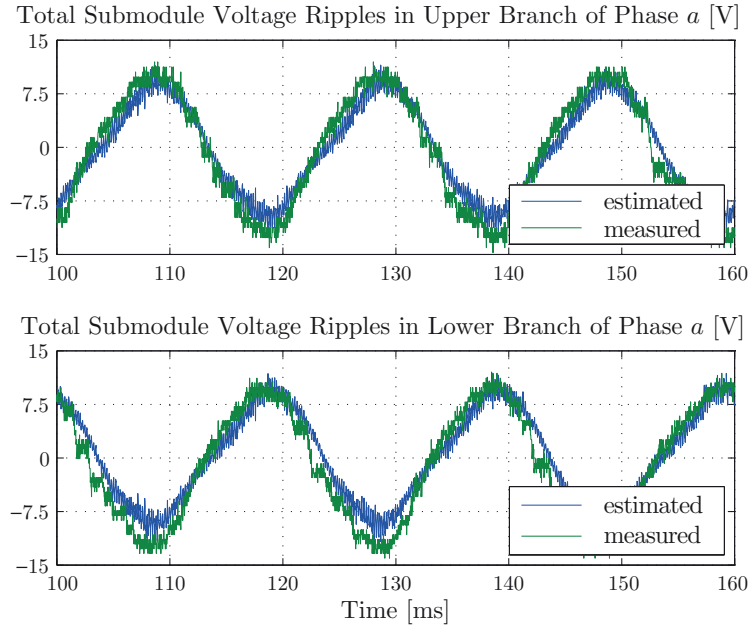
Figure 2.10: Experimental results for total estimated and measured submodule voltage ripples.
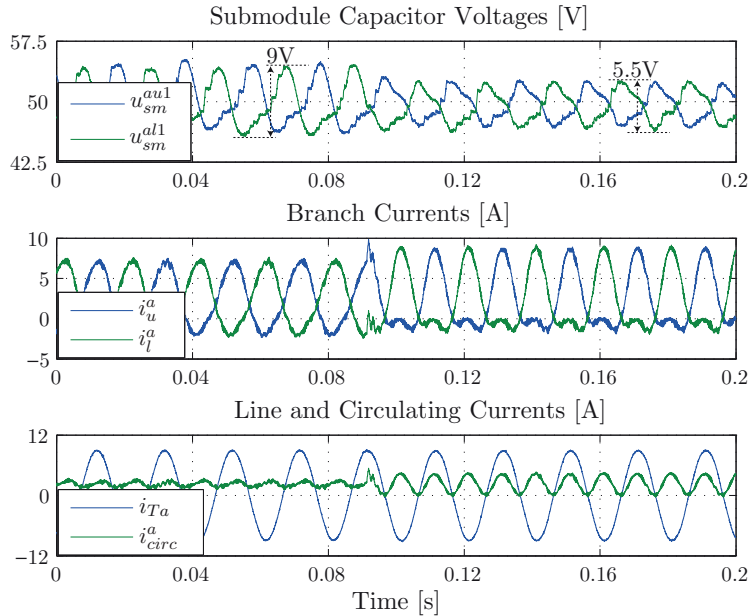

Figure 2.11: Experimental results for capacitor voltage ripple reduction due to a second-order circulating current harmonic injection in converter inverting operation.

2.6 Operation of MMC Under Grid Unbalances

As any three-phase grid-connected converter, the MMC is very likely to operate under unbalanced grid conditions. The choice for a specific line and circulating current control then implies a difference in the inner converter magnitudes as well. In the following, three different control concepts are evaluated, namely the balanced grid current injection and the negative sequence current injection for the elimination of either active or reactive power oscillations.

Taking again Figure 2.1a as reference, the three-phase grid quantities are now modeled by means of symmetrical components. This means that the k-th converter phase voltage u_k ($k = a, b, c$) can be written as

$$u_k = \hat{u}_V^p \cos\left(\omega t + \phi_u^p - \frac{2\pi(m-1)}{3}\right) + \hat{u}_V^n \cos\left(\omega t + \phi_u^n + \frac{2\pi(m-1)}{3}\right) + u_{cm} \quad (2.33)$$

where $m = 1, 2, 3$ and the superscripts p, n denote the respective positive and negative sequence terms. An optional common-mode voltage component u_{cm} has been added, which can be injected for balancing purposes or increase of the modulation index.

The k-th phase grid current can also be expressed through the use of the symmetrical components as

$$i_{Tk} = \hat{i}_T^p \cos\left(\omega t + \phi_i^p - \frac{2\pi(m-1)}{3}\right) + \hat{i}_T^n \cos\left(\omega t + \phi_i^n + \frac{2\pi(m-1)}{3}\right) \quad (2.34)$$

According to [111], the instantaneous active (p_{AC}) and reactive (q_{AC}) powers under unbalanced grid conditions can be written as

$$p_{AC} = P_{AC} + P_{c2} \cos(2\omega t) + P_{s2} \sin(2\omega t) \quad (2.35)$$

$$q_{AC} = Q_{AC} + Q_{c2} \cos(2\omega t) + Q_{s2} \sin(2\omega t) \quad (2.36)$$

In the above, P_{AC}, Q_{AC} represent the average values of the instantaneous active and reactive powers, respectively, and P_{c2}, P_{s2}, Q_{c2}, Q_{s2} denote the magnitude of the oscillating terms due to the negative sequence component existence. Considering a rotating reference frame transformation for the positive and negative sequence of the grid voltages and currents, the power terms of (2.36) can be expressed in the following matrix form

$$\begin{pmatrix} P_{AC} \\ P_{c2} \\ P_{s2} \\ Q_{AC} \\ Q_{c2} \\ Q_{s2} \end{pmatrix} = \frac{3}{2} \begin{pmatrix} u_{Td}^p & u_{Tq}^p & u_{Td}^n & u_{Tq}^n \\ u_{Td}^n & u_{Tq}^n & u_{Td}^p & u_{Tq}^p \\ u_{Tq}^n & -u_{Td}^n & -u_{Tq}^p & u_{Td}^p \\ u_{Tq}^p & -u_{Td}^p & u_{Tq}^n & -u_{Td}^n \\ u_{Tq}^n & -u_{Td}^n & u_{Tq}^p & -u_{Td}^p \\ -u_{Td}^n & -u_{Tq}^n & u_{Td}^p & u_{Tq}^p \end{pmatrix} \begin{pmatrix} i_{Td}^p \\ i_{Tq}^p \\ i_{Td}^n \\ i_{Tq}^n \end{pmatrix} \quad (2.37)$$

Assuming that the mean values of active (P_{AC}) and reactive (Q_{AC}) powers should always be controlled, the two resting degrees of freedom can be used to cancel either the active power oscillation amplitudes P_{c2} and P_{s2} or the respective reactive power ones Q_{c2} and Q_{s2}. Therefore and according to the control target, the matrix is modified and inverted in order to obtain the four respective current references i_{Td}^{p*}, i_{Tq}^{p*}, i_{Td}^{n*} and i_{Tq}^{n*}.

The authors of [103] have established a flexible relation between the symmetrical voltage components, the maximum phase currents as well as the mean active and reactive power values. The latter can be used for the derivation of the maximum achievable active power for a given reactive one and vice versa, without exceeding a given phase current amplitude related to the converter rating. The derivation of this equation can be found in [103] as the latter is provided here without further details as

$$
\begin{aligned}
0 = & \left(\frac{2Q_{AC}}{3}\right)^2 \left[k_2^2 \cdot (\hat{u}_T^n)^2 + (1-k_2)^2 \cdot \left(\hat{u}_T^p\right)^2 - 2k_2\left(1-k_2\right)\cos 2\underline{\gamma} \cdot \hat{u}_T^p \cdot \hat{u}_T^n \right] \\
& - \left(\frac{2P_{AC}}{3}\right)\left(\frac{2Q_{AC}}{3}\right)\left[(2k_1 + 2k_2 - 4k_1 k_2)\cdot \hat{u}_T^p \cdot \hat{u}_T^n \sin 2\underline{\gamma}\right] \\
& + \left(\frac{2P_{AC}}{3}\right)^2 \left[k_1^2 \cdot (\hat{u}_T^n)^2 + (1-k_1)^2 \cdot \left(\hat{u}_T^p\right)^2 + 2k_1\left(1-k_1\right)\cos 2\underline{\gamma}\cdot \hat{u}_T^p \cdot \hat{u}_T^n \right] \\
& - (i_T^{max})^2 \cdot \left(\hat{u}_T^p\right)^2 \cdot \left(\hat{u}_T^n\right)^2
\end{aligned}
\tag{2.38}
$$

In (2.38), $\hat{u}_T^p$ and $\hat{u}_T^n$ are the positive and negative sequence voltage vector magnitude, which is given in the rotating reference frame as

$$
\hat{u}_T^p = \sqrt{(u_{Td}^p)^2 + (u_{Tq}^p)^2}
\tag{2.39}
$$

$$
\hat{u}_T^n = \sqrt{(u_{Td}^n)^2 + (u_{Tq}^n)^2}
\tag{2.40}
$$

In addition, k_1 and k_2 represent two scalar parameters, whose purpose is to adjust the contribution of each voltage sequence component on the active and reactive reference currents, respectively. Their value will be given for each of the subcases that will be described in the following. The symbol i_T^{max} refers to the maximum tolerated grid phase current, which should not be exceeded for a safe converter operation. Finally, the rotation angle vector $\underline{\gamma} = [\gamma_a \ \gamma_b \ \gamma_c]$ is related to the determination of the maximum grid phase current during a network unbalance and can be calculated as [103]

$$
\underline{\gamma} = \begin{cases} \gamma_a = \dfrac{|\phi_u^p| - |\phi_u^n|}{2} \\[2mm] \gamma_b = \dfrac{|\phi_u^p| - |\phi_u^n|}{2} + \dfrac{\pi}{3} \\[2mm] \gamma_c = \dfrac{|\phi_u^p| - |\phi_u^n|}{2} - \dfrac{\pi}{3} \end{cases}
\tag{2.41}
$$

2.6.1 Control for Symmetric Grid Current Injection with Current Limitation

During this mode of operation, the control target is to set the negative sequence grid current references to zero, i.e. to inject perfectly symmetrical sinusoidally varying currents into the three-phase asymmetrical grid. For this operation mode, the current references are given as

$$
\begin{pmatrix} i_{Td}^{p*} \\ i_{Tq}^{p*} \\ i_{Td}^{n*} \\ i_{Tq}^{n*} \end{pmatrix} = -\frac{2}{3}\frac{P_{AC}}{D} \begin{pmatrix} u_{Td}^{p} \\ u_{Tq}^{p} \\ 0 \\ 0 \end{pmatrix} - \frac{2}{3}\frac{Q_{AC}}{D} \begin{pmatrix} u_{Tq}^{p} \\ -u_{Td}^{p} \\ 0 \\ 0 \end{pmatrix}
\tag{2.42}
$$

where $D = -(u_{Td}^{p})^2 - (u_{Tq}^{p})^2$.

In order to extract the maximum achievable active power for a given reactive power according to (2.38), the parameters k_1 and k_2 are set as

$$
\begin{cases} k_1 = 1 \\ k_2 = 1 \end{cases}
\tag{2.43}
$$

On an MMC level, this operation mode implies the imposition of $\hat{i}_T^n = 0$ as well as $\phi_i^n = 0$. Defining p_{br}^{ku} and p_{br}^{kl} as the instantaneous powers for the upper and lower branches of the k-th phase-leg, respectively, the total phase-leg power equation Σp_{br}^{k} becomes

$$
\Sigma p_{br}^{k} = p_{br}^{ku} + p_{br}^{kl} = u_{UL} I_{circ0}^{k} - \frac{\hat{u}_V^p \hat{i}_T^p}{2} \cos\left(\phi_u^p - \phi_i^p\right) - \frac{\hat{u}_V^n \hat{i}_T^p}{2} \cos\left(\phi_u^n - \phi_i^p - \frac{2\pi(m-1)}{3}\right)
$$
$$
- \frac{\hat{u}_V^p \hat{i}_T^p}{2} \cos\left(2\omega t + \phi_u^p + \phi_i^p + \frac{2\pi(m-1)}{3}\right) - \frac{\hat{u}_V^n \hat{i}_T^p}{2} \cos\left(2\omega t + \phi_u^n + \phi_i^p\right) + \Sigma p_{cm}^{k}
\tag{2.44}
$$

It is clear that I_{circ0}^{k} should be controlled in a way that cancels the first three terms in steady state, implying an input/output active power equilibrium. This gives the reference value for the latter as

$$
I_{circ0}^{k*} = \frac{\hat{i}_T^p}{2u_{UL}} \left[\hat{u}_V^p \cos\left(\phi_u^p - \phi_i^p\right) + \hat{u}_V^n \cos\left(\phi_u^n - \phi_i^p - \frac{2\pi(m-1)}{3}\right) \right]
\tag{2.45}
$$

The fourth term in (2.44) appears naturally as an effect of the single-phase system nature. It oscillates with the second-order harmonic frequency. This negative sequence term is symmetrically shifted between the three converter phase-legs and has been already discussed in Section 2.3. It has been shown that it can be canceled by means of a respective intentional second-order harmonic imposition on the circulating current with an amplitude of $\hat{i}_{circ,2}^{k}$ and an angle of θ_2, which has led to (2.20). Since a symmetrical

AC quantity will be injected in the three phases, the DC-link will be unaffected. As discussed in Section 2.3, however, this imposed second harmonic will introduce some higher-order power terms, which will change the components of (2.44).

On the other hand, the fifth cross-product term in (2.44) is a common-mode power term, which does not cancel out throughout the phases and causes a pulsation of a second-order harmonic frequency during a network unbalance [17,50,103]. Interestingly, forcing the I_{circ0}^k to be perfectly constant by means of explicit control will transfer a constant power at the DC link even during asymmetric grid conditions. However, this term will have to be buffered within the converter leg causing an increase in the branch capacitor voltage ripple. Finally, Σp_{cm}^k is the instantaneous power due to a common-mode voltage injection. For a third-order harmonic imposition, which leads to an increase of the modulation index, the associated terms are oscillating and have zero average as obtained by

$$\Sigma p_{cm}^k = -\frac{\hat{u}_{cm}\hat{i}_T^p}{2} \left[\cos\left(2\omega t - \phi_i^p + \frac{2\pi(m-1)}{3} \right) + \cos\left(4\omega t + \phi_i^p - \frac{2\pi(m-1)}{3} \right) \right] \quad (2.46)$$

Another important remark is that each individual branch has a main power oscillation of fundamental frequency order, which are eliminated when summed within the same phase-leg since they are of opposite signs. However, the difference of the branch power components inside a phase leg is obtained as

$$\Delta p_{br}^k = p_{br}^{ku} - p_{br}^{kl} = \Delta p_{cm}^k + \frac{u_{UL}\hat{i}_T^p}{2} \cos\left(\omega t + \phi_i^p - \frac{2\pi(m-1)}{3} \right)$$
$$- 2I_{circ0}^k \left[\hat{u}_V^p \cos\left(\omega t + \phi_u^p - \frac{2\pi(m-1)}{3} \right) + \hat{u}_V^n \cos\left(\omega t + \phi_u^n + \frac{2\pi(m-1)}{3} \right) \right] \quad (2.47)$$

which exhibits the first harmonic order terms of positive and negative sequence. From (2.47) it is clear that there is no unbalance between the two branches of a phase leg due to a negative sequence voltage existence in steady state. For a u_{cm} with a third harmonic frequency, the associated term Δp_{cm}^k is also oscillating and given by

$$\Delta p_{cm}^k = -2\hat{u}_{cm}I_{circ0}^k \cos\left(3\omega t \right) \quad (2.48)$$

The typical waveforms for such a converter operation are depicted in Figure 2.12. For this simulation, a phase-to-ground fault of the first phase is considered with a severity of a total phase loss. The grid currents comprise the nominal positive sequence value. Each phase contributes to the DC-link with a different amount of current. However the instantaneous DC-link power p_{DC} remains constant, although the three-phase AC power p_{AC} oscillates at 100 Hz. As discussed, this operation mode and choice of common-mode power term elimination on the DC-link level will cause an increase of the branch capacitor voltage ripples, especially in the phase that is characterized by the voltage short-circuit.

The three-phase reactive power mean value Q_{AC} is controlled to be zero, but it also oscillates around this mean value with a second-order harmonic frequency due to the symmetric three-phase grid current injection.
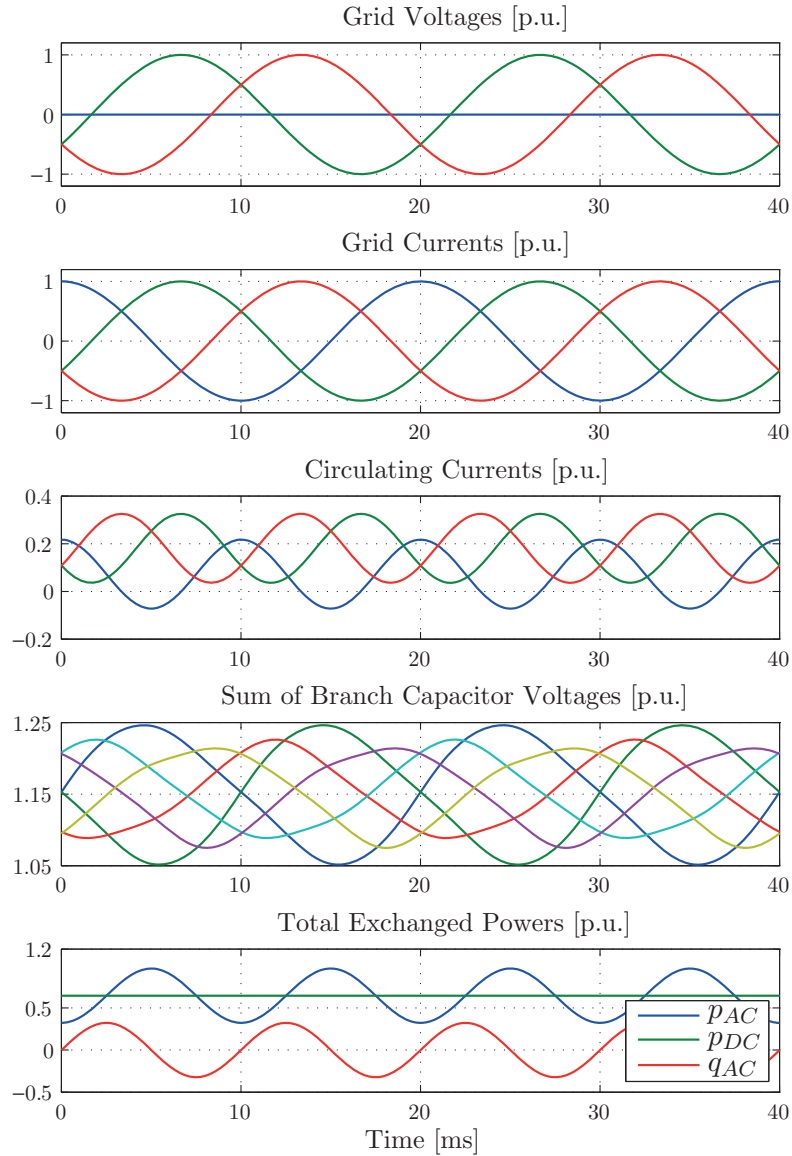

Figure 2.12: Waveforms for an operation of a Modular Multilevel Converter under a phase-to-ground fault in phase a. The grid currents are controlled to comprise only a positive sequence.

It is now interesting to observe how the branch energy variation ΔE evolves in function of the grid asymmetry for a given power factor, i.e., $Q_{AC} = 0$. The branch energy variation is an indication of the capacitive storage requirements in an MMC. The results are illustrated in Figure 2.13, both when a second harmonic in i^k_{circ} is used and when it is not. The grid asymmetry is expressed as the division of $\hat{u}^n_V$ with its maximum value

$\hat{u}^n_{V,max}$. Therefore, the unity corresponds to a full phase loss. In order to have a means of comparison, both branch variations are normalized with the minimum of variation without second harmonic injection ΔE^{no2nd}_{min}, i.e., with an asymmetry of zero. For each operating point, the maximum achievable active power is calculated so as not to exceed the maximum set grid current according to (2.38).
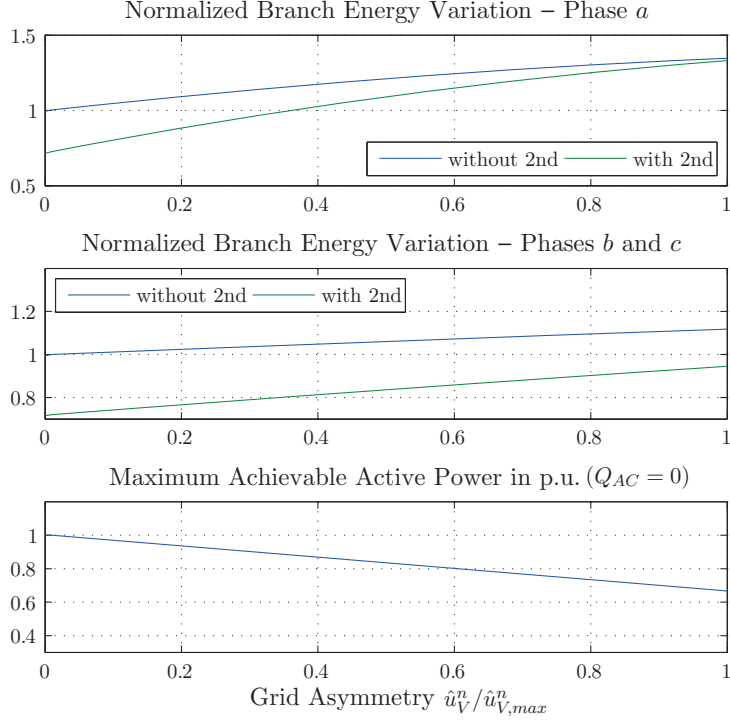
Figure 2.13: Evolution of branch energy variation and maximum achievable active power in function of the grid asymmetry for balanced grid current control with and without circulating current second harmonic injection. Reactive power has been set to zero and the branch energies are normalized with ΔE^{no2nd}_{min}.

It becomes evident that an increase in the negative sequence voltage component $\hat{u}^n_V$ causes a significant increase in the energy storage requirements. The second-order harmonic circulating current imposition according to the fourth term in (2.44) brings no significant benefit once the grid asymmetry becomes considerable. Therefore, a different choice for $\hat{i}^k_{circ,2}$ and θ_2 might prove to be better suited after a specific value of $\hat{u}^n_V$. It is also shown that phase a, which is experiencing the fault, exhibits a higher energy variation increase whereas phases b and c behave similarly and with a smaller increase.

2.6.2 Control for Power Oscillation Compensation with Current Limitation

The second studied case regards a mode of operation under grid unbalances, where the control aims to cancel either the active or the reactive power oscillations of the AC side. In order to achieve the latter, a set of reference values for the positive and negative sequence AC current components needs to be specified and controlled, accordingly [103,111-114].

On the MMC level, the existence of both sequences implies that $i_T^n \neq 0$ as well as $\phi_i^n \neq 0$ and results in a phase branch power sum of

$$
\Sigma p_{br}^k = p_{br}^{ku} + p_{br}^{kl} = u_{UL} I_{circ0}^k - \frac{\hat{u}_V^p \hat{i}_T^p}{2} \cos \left(\phi_i^p - \phi_u^p \right) - \frac{\hat{u}_V^n \hat{i}_T^n}{2} \cos \left(\phi_i^n - \phi_u^n \right)
$$
$$
- \frac{\hat{u}_V^p \hat{i}_T^n}{2} \cos \left(\phi_u^p - \phi_i^n + \frac{2\pi(m-1)}{3} \right) - \frac{\hat{u}_V^n \hat{i}_T^p}{2} \cos \left(\phi_u^n - \phi_i^p - \frac{2\pi(m-1)}{3} \right)
$$
$$
- \frac{\hat{u}_V^p \hat{i}_T^p}{2} \cos \left(2\omega t + \phi_u^p + \phi_i^p + \frac{2\pi(m-1)}{3} \right) - \frac{\hat{u}_V^n \hat{i}_T^n}{2} \cos \left(2\omega t + \phi_u^n + \phi_i^n - \frac{2\pi(m-1)}{3} \right)
$$
$$
- \frac{\hat{u}_V^p \hat{i}_T^n}{2} \cos \left(2\omega t + \phi_u^p + \phi_i^n \right) - \frac{\hat{u}_V^n \hat{i}_T^p}{2} \cos \left(2\omega t + \phi_u^n + \phi_i^p \right) + \Sigma p_{cm}^k \qquad (2.49)
$$

In a similar manner as before, I_{circ0}^k should now be controlled in a way that cancels the first five terms, so that no constant power components appear in the branch power equations, leading to the reference value of

$$
I_{circ0}^{k*} = \frac{\hat{i}_T^p}{2u_{UL}} \left[\hat{u}_V^p \cos \left(\phi_u^p - \phi_i^p \right) + \hat{u}_V^n \cos \left(\phi_u^n - \phi_i^p - \frac{2\pi(m-1)}{3} \right) \right]
$$
$$
+ \frac{\hat{i}_T^n}{2u_S} \left[\hat{u}_V^p \cos \left(\phi_u^p - \phi_i^n + \frac{2\pi(m-1)}{3} \right) + \hat{u}_V^n \cos \left(\phi_u^n - \phi_i^n \right) \right] \qquad (2.50)
$$

The sixth and seventh terms of (2.49) (negative and positive sequence, respectively) are symmetrically shifted between the phase legs and will therefore cancel out on the DC-link. In addition, they can be compensated for with two respective circulating current components of the same frequency. The last two cross-product terms are of common-mode nature and do not cancel themselves naturally. However, through a proper choice of the current references they can be eliminated as stated before. In such a case the imposed circulating current becomes as

$$
i_{circ}^k = I_{circ0}^k + \hat{i}_{circ,2a} \cos \left(2\omega t + \theta_a + \frac{2\pi(m-1)}{3} \right) + \hat{i}_{circ,2b} \cos \left(2\omega t + \theta_b - \frac{2\pi(m-1)}{3} \right)
$$
$$
(2.51)
$$

where

$$\hat{i}_{circ,2a} = \frac{\hat{u}_V^p \hat{i}_T^p}{2u_{UL}}, \quad \theta_a = \phi_u^p + \phi_i^p \tag{2.52}$$

$$\hat{i}_{circ,2b} = \frac{\hat{u}_V^n \hat{i}_T^n}{2u_{UL}}, \quad \theta_b = \phi_u^n + \phi_i^n \tag{2.53}$$

The difference of the branch power components inside a phase leg is now expressed by

$$\Delta p_{br}^k = p_{br}^{ku} - p_{br}^{kl} = \Delta p_{cm}^k + \frac{u_{UL}}{2}\left[\hat{i}_T^p \cos\left(\omega t + \phi_i^p - \frac{2\pi(m-1)}{3}\right)\right.$$
$$\left. + \hat{i}_T^n \cos\left(\omega t + \phi_i^n + \frac{2\pi(m-1)}{3}\right)\right] - 2I_{circ0}^k\left[\hat{u}_V^p \cos\left(\omega t + \phi_u^p - \frac{2\pi(m-1)}{3}\right)\right.$$
$$\left. + \hat{u}_V^n \cos\left(\omega t + \phi_u^n + \frac{2\pi(m-1)}{3}\right)\right] \tag{2.54}$$

Once again, the existence of negative sequence voltages and currents on the grid side does not create branch unbalances. Finally, it is noted that also in this case the terms Σp_{cm}^k and Δp_{cm}^k associated with a third harmonic injection are oscillating and have zero average, as shown below:

$$\Sigma p_{cm}^k = -\frac{\hat{u}_{cm}\hat{i}_T^p}{2}\left[\cos\left(2\omega t - \phi_i^p + \frac{2\pi(m-1)}{3}\right) + \cos\left(4\omega t + \phi_i^p - \frac{2\pi(m-1)}{3}\right)\right]$$
$$- \frac{\hat{u}_{cm}\hat{i}_T^n}{2}\left[\cos\left(2\omega t - \phi_i^n - \frac{2\pi(m-1)}{3}\right) + \cos\left(4\omega t + \phi_i^n + \frac{2\pi(m-1)}{3}\right)\right] \tag{2.55}$$

$$\Delta p_{cm}^k = -2\hat{u}_{cm}I_{circ0}^k \cos(3\omega t) \tag{2.56}$$

In the following, the two different choices for active or reactive power oscillation elimination during grid unbalanced conditions are investigated.

Active Power Oscillation Elimination

In order to compensate for the active power oscillating terms of (2.36), the amplitudes P_{c2} and P_{s2} are set to zero. The solution for the respective current references is then obtained as

$$\begin{pmatrix} i_{Td}^{p*} \\ i_{Tq}^{p*} \\ i_{Td}^{n*} \\ i_{Tq}^{n*} \end{pmatrix} = \frac{2}{3}\frac{P_{AC}}{D_1}\begin{pmatrix} u_{Td}^p \\ u_{Tq}^p \\ -u_{Td}^n \\ -u_{Tq}^n \end{pmatrix} + \frac{2}{3}\frac{Q_{AC}}{D_2}\begin{pmatrix} u_{Tq}^p \\ -u_{Td}^p \\ u_{Tq}^n \\ -u_{Td}^n \end{pmatrix} \tag{2.57}$$

where $D_1 = \left((u_{Td}^p)^2 + (u_{Tq}^p)^2\right) - \left((u_{Td}^n)^2 + (u_{Tq}^n)^2\right)$ and $D_2 = \left((u_{Td}^p)^2 + (u_{Tq}^p)^2\right) + \left((u_{Td}^n)^2 + (u_{Tq}^n)^2\right)$

In order to extract the maximum achievable active power for a given reactive power according to (2.38), the parameters k_1 and k_2 are now set as

$$\begin{cases} k_1 = \dfrac{(\hat{u}_V^p)^2}{(\hat{u}_V^p)^2 - (\hat{u}_V^n)^2} \\[3mm] k_2 = \dfrac{(\hat{u}_V^p)^2}{(\hat{u}_V^p)^2 + (\hat{u}_V^n)^2} \end{cases} \tag{2.58}$$
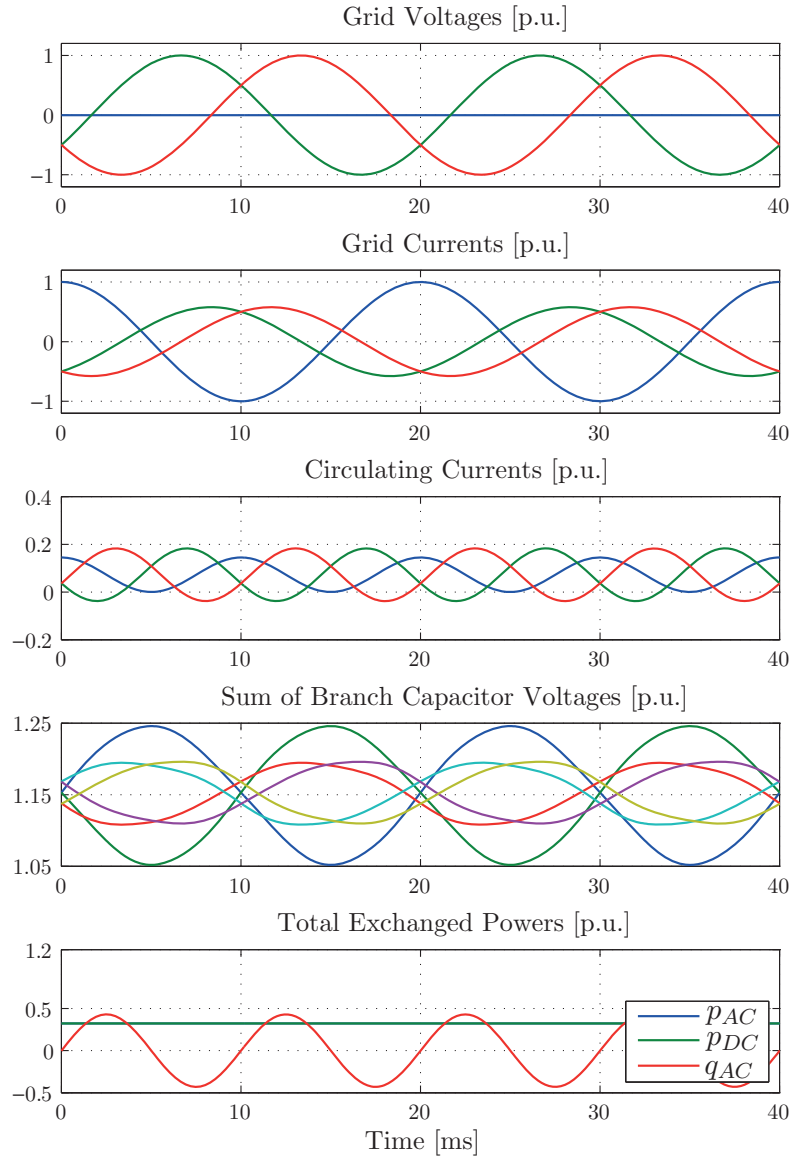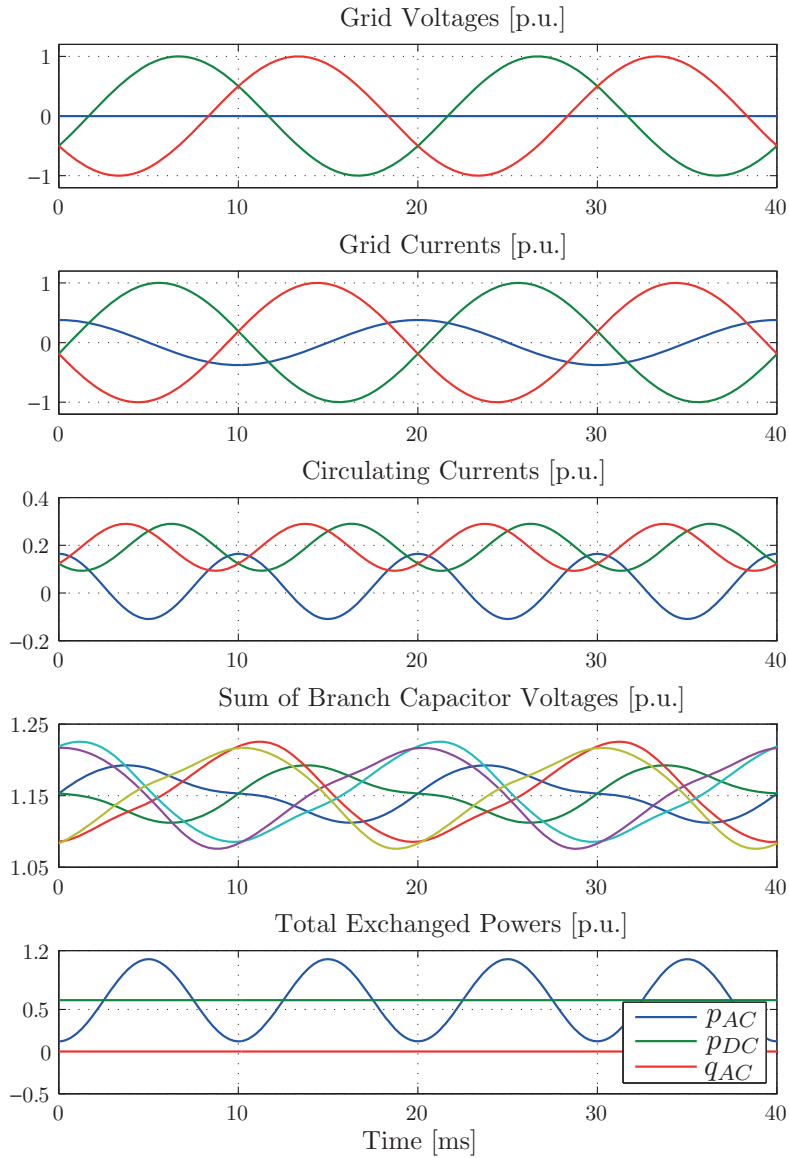

Figure 2.14: Waveforms for an operation of a Modular Multilevel Converter under a phase-to-ground fault in phase a. The grid currents are controlled in order to keep an oscillation-free three-phase active power.

The typical waveforms for such an operation are shown in Figure 2.14. Again a full loss of phase a is considered. The three-phase grid currents are not symmetrical. Similarly to the balanced current injection case, two second-order harmonic components are now imposed on the circulating current, in order to compensate for the sixth and seventh oscillating power terms of (2.49). It can be seen that all phases are now delivering the same amount of continuous current to the DC-link. The input and output instantaneous active powers p_{AC} and p_{DC} are identical, while no oscillations exist in either of them. However, the reactive power oscillations remain, since they cannot be compensated for with the current negative sequence injection strategy. The maximum current is drawn from the phase that is experiencing the fault, which causes the highest capacitor voltage ripple increase on this specific phase.
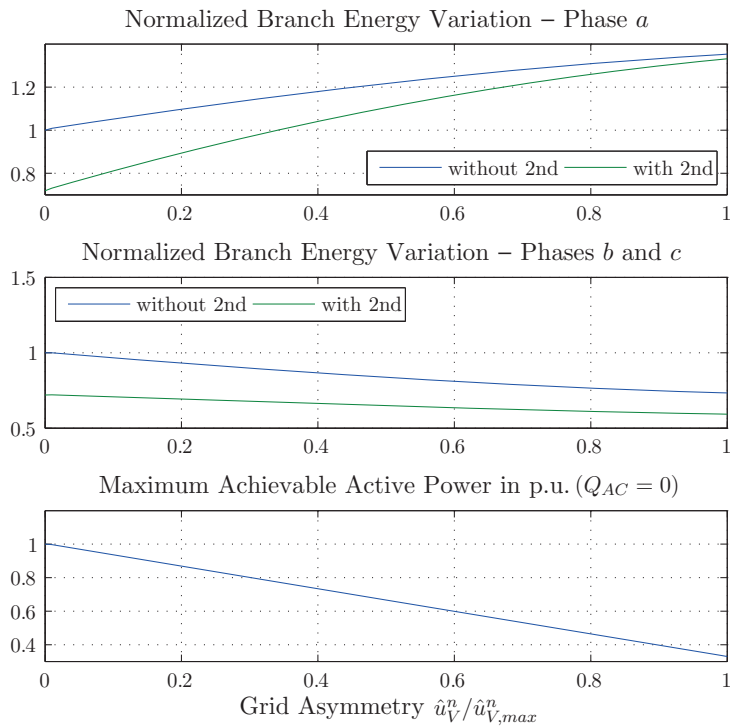
Figure 2.15: Evolution of branch energy variation and maximum achievable active power in function of the grid asymmetry for active power oscillation elimination control with and without circulating current second harmonic injection. Reactive power has been set to zero and the branch energies are normalized with ΔE_{min}^{no2nd}.

Similarly to the previous case, Figure 2.15 illustrates the impact of the grid unbalance on the MMC branch energy variation for $Q_{AC} = 0$. Once again phase a, where the grid fault occurs, experiences the highest branch energy variation increase. The two other phase in this case reveal a decrease in their branch energy variation and similar behavior between them. Finally, the second-order circulating current harmonic injection is studied. It is clear that the benefits of this injection are quite significant in balanced grid conditions, but the curves converge to almost the same value at the full phase loss. In both the cases

of balanced grid current control and active power oscillation elimination, the latter is due to the fact that the inherent fundamental frequency components dominate in the branch during the fault, compared to the second-order power oscillations.

Reactive Power Oscillation Elimination

In conventional three-phase converters, the active power oscillation elimination is generally preferred, since it implies a constant active power transfer on the DC-link side. As already discussed for the MMC, however, this can be achieved from the converter itself independently from the power form at the AC side. Therefore, the current references can be chosen so as to cancel the reactive power oscillating terms of (2.36) without affecting the DC-link. By setting to zero the amplitudes Q_{c2} and Q_{s2} in (2.36), the solution for the respective currents is given by

$$
\begin{pmatrix} i_{Td}^{p*} \\ i_{Tq}^{p*} \\ i_{Td}^{n*} \\ i_{Tq}^{n*} \end{pmatrix} = \frac{2}{3} \frac{P_{AC}}{D_1} \begin{pmatrix} u_{Td}^{p} \\ u_{Tq}^{p} \\ u_{Td}^{n} \\ u_{Tq}^{n} \end{pmatrix} + \frac{2}{3} \frac{Q_{AC}}{D_2} \begin{pmatrix} u_{Tq}^{p} \\ -u_{Td}^{p} \\ -u_{Tq}^{n} \\ u_{Td}^{n} \end{pmatrix}
\tag{2.59}
$$

where $D_1 = \left((u_{Td}^{p})^2 + (u_{Tq}^{p})^2 \right) + \left((u_{Td}^{n})^2 + (u_{Tq}^{n})^2 \right)$ and $D_2 = \left((u_{Td}^{p})^2 + (u_{Tq}^{p})^2 \right) - \left((u_{Td}^{n})^2 + (u_{Tq}^{n})^2 \right)$

In order to extract the maximum achievable active power for a given reactive power according to (2.38), the parameters k_1 and k_2 are now set as

$$
\begin{cases} k_1 = \dfrac{(\hat{u}_V^{p})^2}{(\hat{u}_V^{p})^2 + (\hat{u}_V^{n})^2} \\[3mm] k_2 = \dfrac{(\hat{u}_V^{p})^2}{(\hat{u}_V^{p})^2 - (\hat{u}_V^{n})^2} \end{cases}
\tag{2.60}
$$

Figure 2.16 depicts the typical waveforms for this operation mode. Compared to the active power oscillation elimination case, now two converter phases draw the maximum current, where an increase of the capacitor voltage ripples is observed. Each phase contributes with a different amount of circulating current to the DC-link power. The power p_{DC} is held constant irrespective of the oscillations observed in p_{AC}, and the reactive power oscillations have vanished due to the utilized current injection strategy.

Similarly to Figure 2.13 and Figure 2.15, Figure 2.17 reveals that in this case phases b and c are mostly affected by the fault regarding branch energy increase. On the contrary, phase a is characterized by an energy variation reduction. It is important to note that the branch energy increase is lower than the two previous studied cases. In addition, the second-order harmonic circulating current injection maintains its benefits throughout the

whole unbalance regime, since it keeps the energy variation below the value 1, which corresponds to the lowest variation in the case without harmonic injection.

Figure 2.16: Waveforms for an operation of a Modular Multilevel Converter under a phase-to-ground fault in phase a. The grid currents are controlled in order to keep an oscillation-free three-phase reactive power.

2.6.3 Comparison

It is now interesting to observe how the three different described strategies for the operation of an MMC during grid unbalances compare to one another. The two main comparison criteria regard the branch energy variation increase throughout the fault as well as the maximum power transfer.
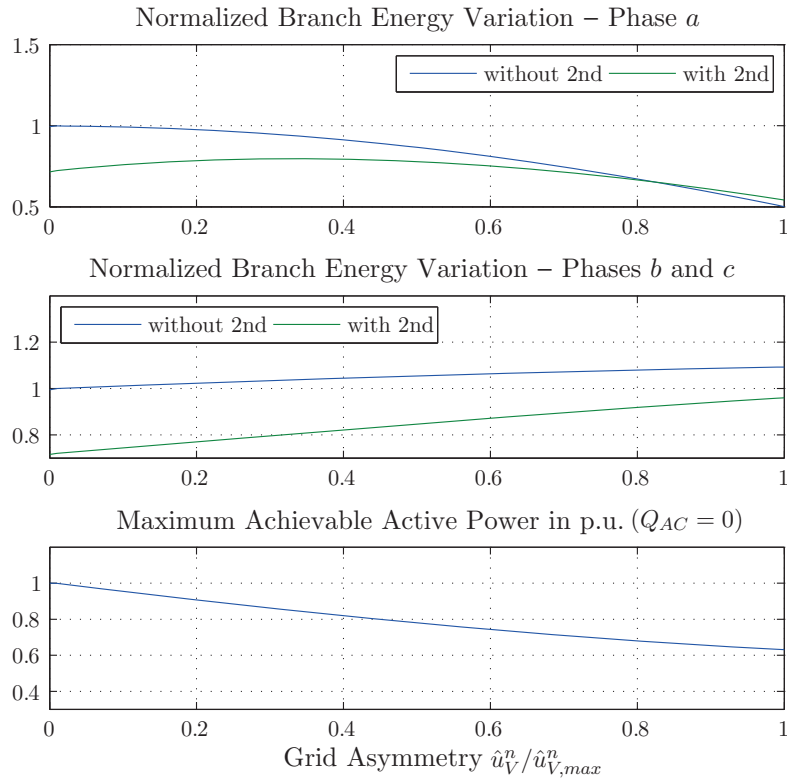
Figure 2.17: Evolution of branch energy variation and maximum achievable active power in function of the grid asymmetry for reactive power oscillation elimination control with and without circulating current second harmonic injection. Reactive power has been set to zero and the branch energies are normalized with ΔE_{min}^{no2nd}.

Initially, the branch energy variation in function of the grid asymmetry as well as the reactive power injection is studied. Figure 2.18-2.20 illustrate the results for the three aforementioned operation modes without and with second harmonic injection in the circulating current. As stated before, the grid asymmetry is expressed as the division of $\hat{u}_V^n$ with its maximum value $\hat{u}_{V,max}^n$. Therefore, the unity corresponds to a full phase loss. In order to have a means of comparison, both branch variations are again normalized with the minimum of variation without second harmonic ΔE_{min}^{no2nd}, i.e. with an asymmetry of zero and a purely active power transfer. Due to the inherent symmetry, the absolute value of reactive power $|Q_{AC}|$ is adequate for the analysis as the results are identical for capacitive or inductive operation.

From these surface figures, several important observations can be made. Initially, an increase in the negative sequence voltage component $\hat{u}_V^n$ causes a significant increase in the energy storage requirements, especially for values of $|Q_{AC}|$ close to zero and for the cases of balanced current injection as well as active power oscillation elimination. Another significant remark is that for pure reactive power transfer, the branch energy variation is high, even if no grid asymmetry exists for all the three cases. The second-order harmonic

51
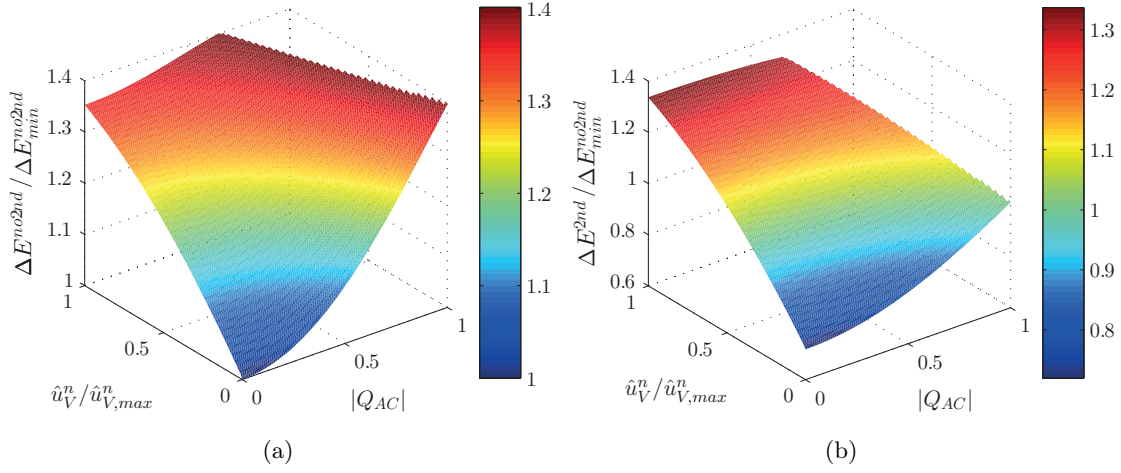
Figure 2.18: Branch energy variation for the case of symmetric grid current control in function of the injected reactive power $|Q_{AC}|$ and the asymmetry gravity, where 0 corresponds to a full phase voltage and 1 to a full phase loss: (a) without and (b) with 2nd harmonic circulating current injection.
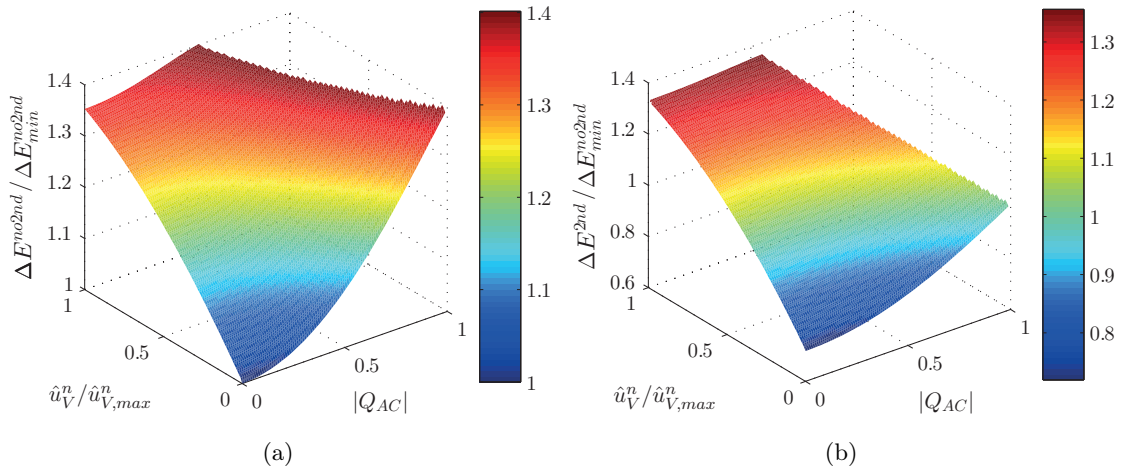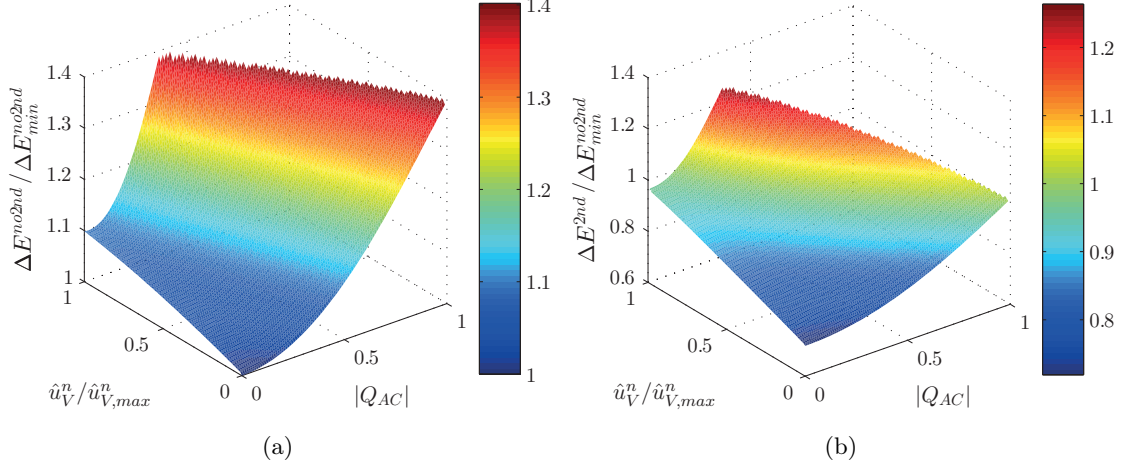

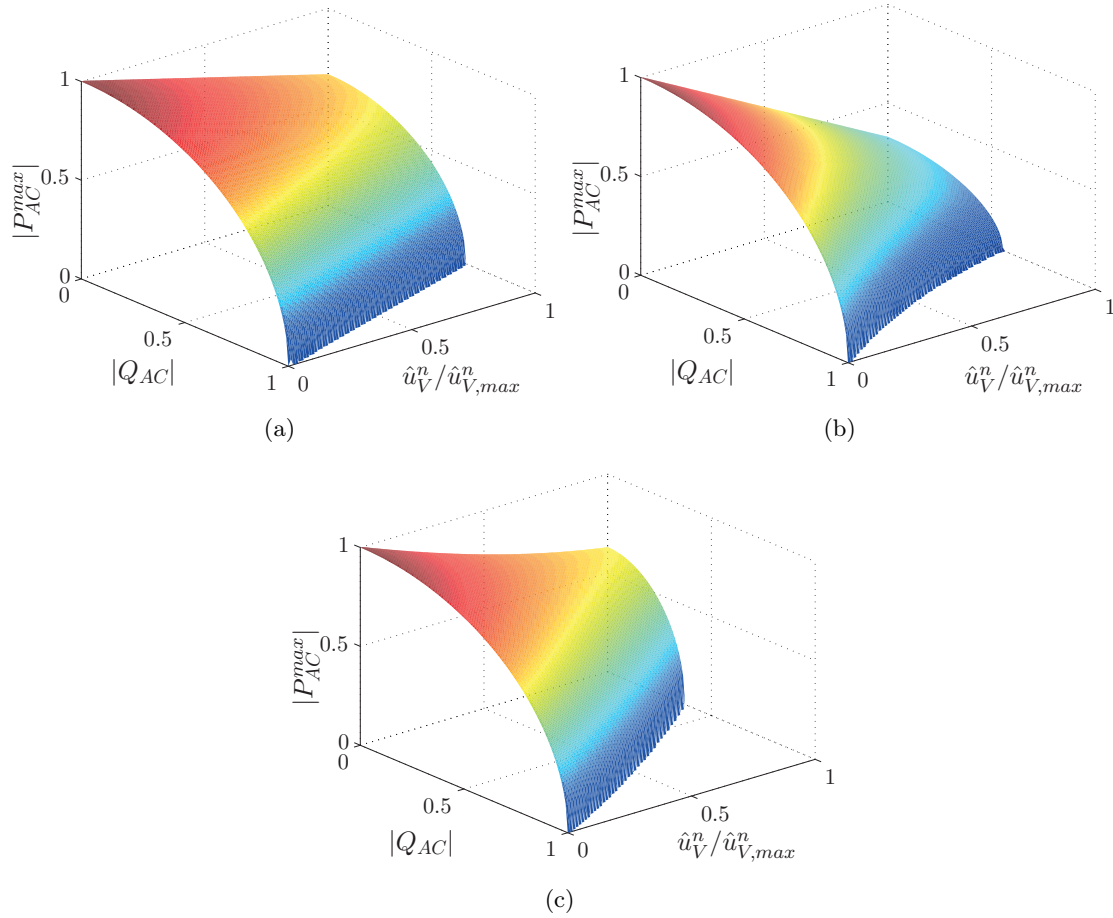Figure 2.19: Branch energy variation for the case of current control for active power oscillation elimination in function of the injected reactive power $|Q_{AC}|$ and the asymmetry gravity, where 0 corresponds to a full phase voltage and 1 to a full phase loss: (a) without and (b) with 2nd harmonic circulating current injection.

circulating current imposition according to the fourth term in (2.44) brings no significant benefit once the grid asymmetry becomes considerable in the cases of balanced current injection and active power oscillation reduction as well, where the results are similar.

On the other hand, the reactive power oscillation elimination method shows clear advantages over the two other methods under several operating points. Initially, the branch energy variation is not significantly affected by the fault for values of $|Q_{AC}|$ close to zero.

Moreover, the second-order harmonic injection is effective even under the most extreme case of purely reactive power and full phase loss.

Figure 2.20: Branch energy variation for the case of current control for reactive power oscillation elimination in function of the injected reactive power $|Q_{AC}|$ and the asymmetry gravity, where 0 corresponds to a full phase voltage and 1 to a full phase loss: (a) without and (b) with 2nd harmonic circulating current injection.

Figure 2.21 illustrates the maximum active power that can be achieved for the three studied cases in function of the grid asymmetry as well as the reactive power injection. Again due to the symmetry, the absolute value of $|P_{AC}^{max}|$ is considered. It is clear that the case of balanced current injection exhibits the highest power transfer of all three modes, as well as the wider range of operation. This is due to the fact that all three phases can be controlled to inject the rated current under all grid asymmetry and power factor values. The reactive power oscillation reduction mode shows a general advantage over the active power oscillation elimination, especially for low values of $|Q_{AC}|$. By exploring Figures 2.14 and 2.16, the latter can be attributed to the fact that the reactive power oscillation compensation mode forces two of the phases to inject the full current compared to the active power oscillation one. For values close to $|Q_{AC}| = 0$ and high grid asymmetries, however, the region of the active power oscillation compensation mode is slightly extended.

It can be concluded, though, that the reactive power oscillation compensation mode presents evident advantages over the active power oscillation elimination, both in terms of branch energy variation increase as well as maximum achievable active power. If the focus is laid on the branch energy variation, the reactive power oscillation compensation mode is also superior to the balanced current injection as well.

Figure 2.21: Maximum achievable active power in function of the injected reactive power $|Q_{AC}|$ and the asymmetry gravity, where 0 corresponds to a full phase voltage and 1 to a full phase loss for the three different grid current control strategies: (a) balanced grid currents, (b) active power oscillation compensation, (c) reactive power oscillation compensation.

2.6.4   Experimental Results

Several preliminary experimental tests have been carried out, in order to verify the developed theoretical investigations regarding the impact of grid asymmetries on the operation and design of Modular Multilevel Converters. The prototype of Figure 2.8 has been once again configured as a three-phase converter, connected to the grid through a variable transformer. In order to emulate a phase-to-ground fault with a severity of 1, i.e., a total phase loss, the converter phase a has been connected to the neutral point of the transformer's star connection. The converter is fed by a fixed DC source in parallel with a variable resistor, allowing the testing of active power flow in both directions, i.e., inverter and rectifier mode.

A decoupled double synchronous reference frame (DDSRF) algorithm [123] has been implemented for the grid voltage and current symmetrical component identification and synchronization with the grid positive sequence voltage. Two grid current control loops in a rotating reference frame allow an independent control of the positive and negative sequence grid current components. In addition, the circulating currents are controlled to bear a second-order harmonic for the reduction of the submodule capacitor voltage variations.

Figures 2.22-2.24 present the experimental results that correspond to the theoretical
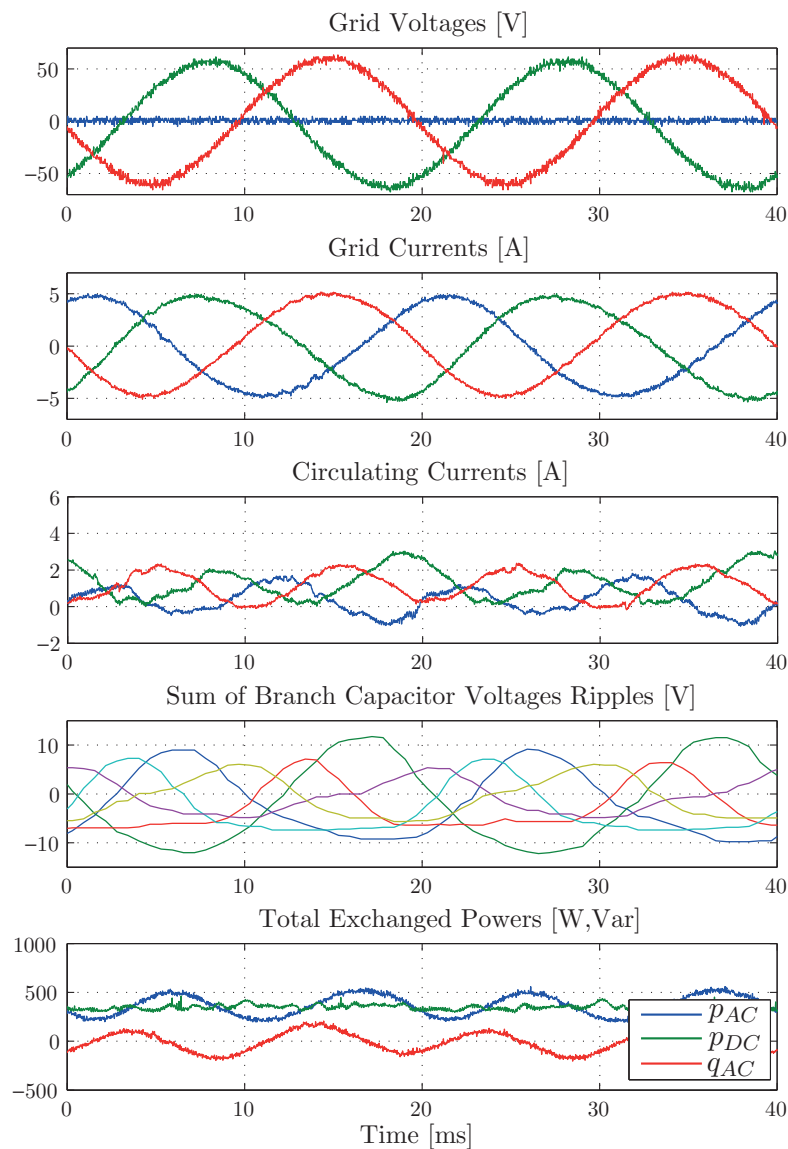
Figure 2.22: Experimental results for an operation of a Modular Multilevel Converter under a phase-to-ground fault in phase a. The grid currents are controlled to comprise only a positive sequence.

waveforms presented in Figures 2.12, 2.14 and 2.16, respectively. The maximum allowable grid current amplitude has been set to $i_T^{max} = 5$ A and the mean reactive power to Q_{AC} = 0 Var, calculating therefore the maximum transferred mean active power P_{AC} for all three cases according to these conditions.
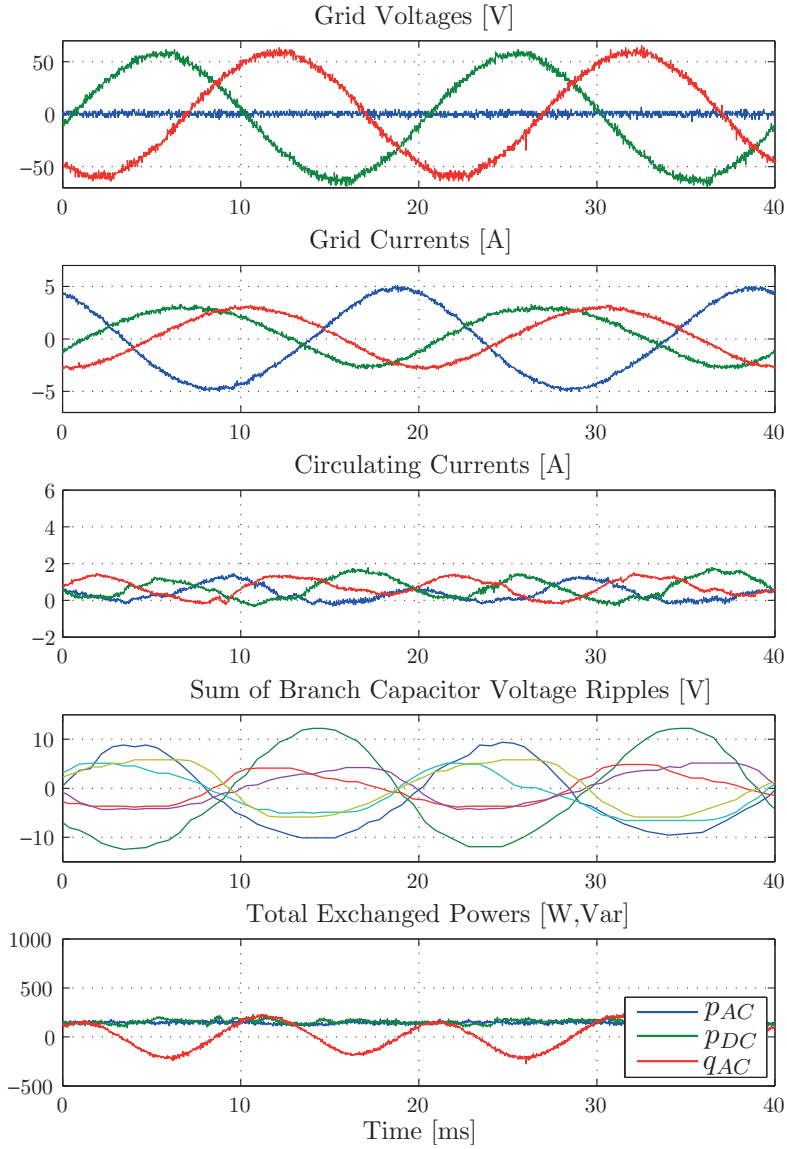
Figure 2.23: Experimental results for an operation of a Modular Multilevel Converter under a phase-to-ground fault in phase a. The grid currents are controlled in order to keep an oscillation-free three-phase active power.

The experimental results are in good agreement with the theoretical ones. The desired goals of the three different current control methods are validated, i.e., balanced three-phase positive sequence currents as well as negative sequence current injection for active and reactive power oscillation elimination. The fact that the largest active power transfer

is achieved by the first technique, followed with a small difference by the reactive power oscillation elimination one, is also verified. The active power oscillation elimination method is characterized by the smallest active power, due to the maximum amplitude injection by only one phase current. In all three cases, the converter is able to achieve a constant instantaneous DC-link power p_{DC}, proving the particularity of the MMC compared to conventional topologies.

The sums of the six branch capacitor voltage ripples are also depicted in the experimental figures for the sake of comparison. Once again theory is verified with the reactive power
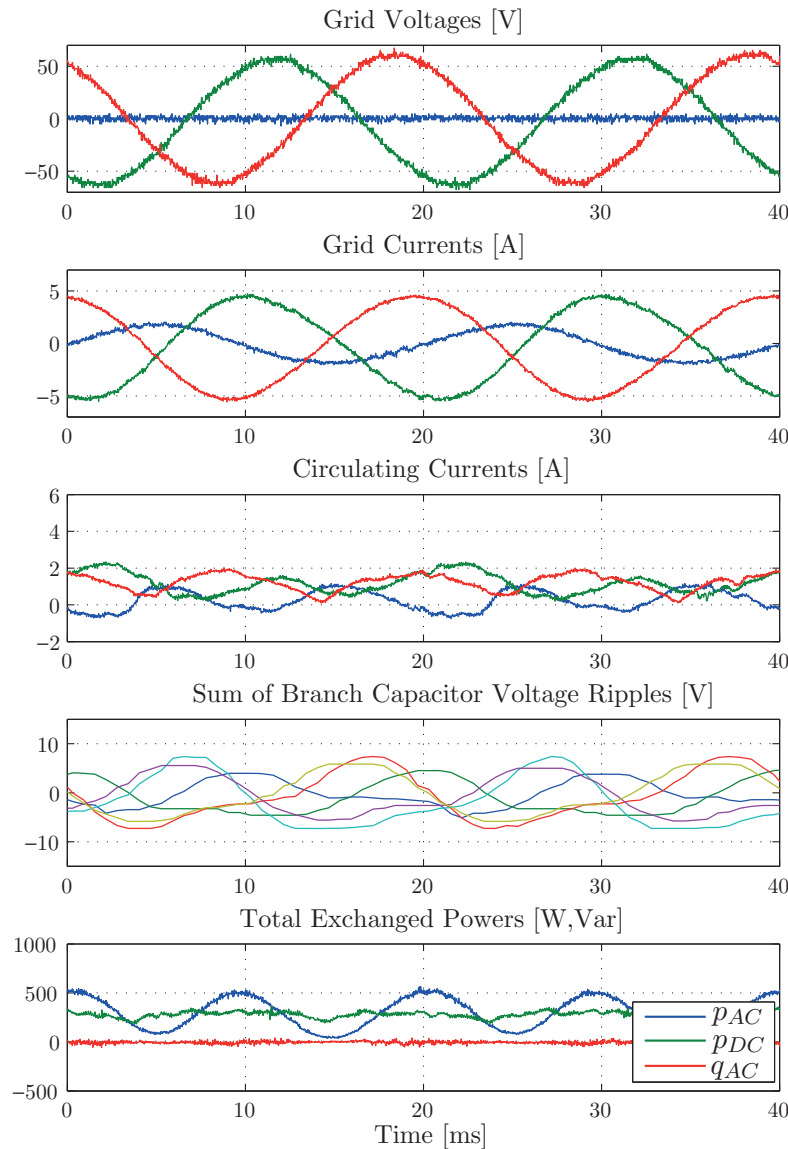
Figure 2.24: Experimental results for an operation of a Modular Multilevel Converter under a phase-to-ground fault in phase a. The grid currents are controlled in order to keep an oscillation-free three-phase reactive power.

oscillation elimination method outperforming the other two, i.e., being less affected in terms of branch energy variation increase. The balanced current injection and active power oscillation elimination methods present similar waveforms, where the largest voltage ripple increase is noticed in the phase experiencing the total phase loss.

It has to be noted that the presented results exhibit some differences compared to the theoretical ones. The main reason lays on the fact that due to existing noise in the measurement and control hardware, the theoretical bandwidth of the various designed control systems has not been reached without passing the stability limit. Nevertheless, it can be argued that the converter has been successfully operated under a severe phase loss and the main comparison goals between the three techniques have been adequately verified.

2.7   Conclusions

This chapter has provided the analytical expressions of the submodule capacitor voltage ripples in a Modular Multilevel Converter. The derivations have been made in a generalized manner. These equations reveal the harmonic content of the respective voltages. Therefore, they are beneficial for the design of the capacitive energy storage requirements.

Moreover, the knowledge of the capacitor voltage ripples is useful from a control point of view. Indeed, several control systems proposed in literature require the knowledge of the power pulsation in the MMC branches. In the so-called open-loop control schemes, the accurate voltage ripple evaluation can be directly used for the real-time modulation reference adjustment therefore capacitor voltage ripple compensation on a control level. On the other hand, closed-loop control schemes normally target at the explicit total capacitive phase-leg energy and energy difference between different MMC branches. In such a case, the low frequency components of the branch capacitor voltages have to be eliminated before fed to the respective regulators. On this level, the voltage ripple estimation can successfully substitute the use of software-based filters, which cause otherwise a decrease in the control loop bandwidth.

One of the major differences of MMC compared to conventional topologies is the ability to control independently the input with the output powers. This can be done by explicitly controlling both line and the so-called circulating currents in a decoupled manner. There are numerous possibilities for current control loop implementations and some have been presented in this chapter. The circulating currents also offer another degree of freedom for achieving further purposes, such as capacitor voltage ripple reduction. The latter leads evidently to a respective reduction of the submodule capacitance.

Regarding the operation of an MMC under grid unbalances, it is very important to point out the differences compared to other topologies. Indeed, the existence of three

independent capacitive legs implies a significant impact on the dimensioning of the components as well as the choice for positive and negative line current injection. Again, a proper circulating current use here can offer advantages, such as elimination of the common-mode second-order DC-link component when the line currents are controlled to comprise only a positive sequence, something which constitutes a main issue in traditional three-phase grid-connected converters.

3 Cascaded H-Bridge Converters with Integrated Battery Energy Storage

3.1 Introduction

This chapter investigates the three-phase star- and delta-configured Cascaded H-Bridge converters with embedded battery energy storage systems in terms of topology structure, dimensioning and control. Such converters can be used as application-specific energy storage units in medium/high voltage grids. In addition, they can be used as active front ends in Power Electronic Transformers-based architectures, such as the one proposed in Chapter 5 for the implementation of ultra-fast EV charging stations. The star-connected CHB-BESS converter case is illustrated in Figure 3.1a.

Initially, the submodule/battery interface problem is treated. The integration of battery energy storage elements within the CHB converter already poses a technical challenge for the design and control of the system. The CHB converter is implemented using standard full-bridges, as shown in Figure 3.1b. The main impediment for the direct interface of batteries is the fact that the converter submodules behave as individual single-phase rectifiers, thus buffering considerable power fluctuations of the grid second-order harmonic frequency.

In addition, this chapter investigates the ways to handle active power components for control and balancing purposes in such a CHB-BESS storage unit. The topology-specific degrees of freedom are exploited, both for the cases of star and delta converter configurations. In addition, control algorithms are developed and limitations are established. Potential grid asymmetries are taken into consideration through the utilization of symmetrical components. Several modes of operation are studied, such as independent load feeding, state of charge balancing as well as converter operation under grid faults.

It is noted that the following subscripts/superscripts are utilized throughout this chapter: $k \in \{a/ab, b/bc, c/ca\}$ referring to the studied branch of the CHB converter in star/delta configuration, and $i \in \{1, 2, .., N\}$ to the submodules of the respective branch.
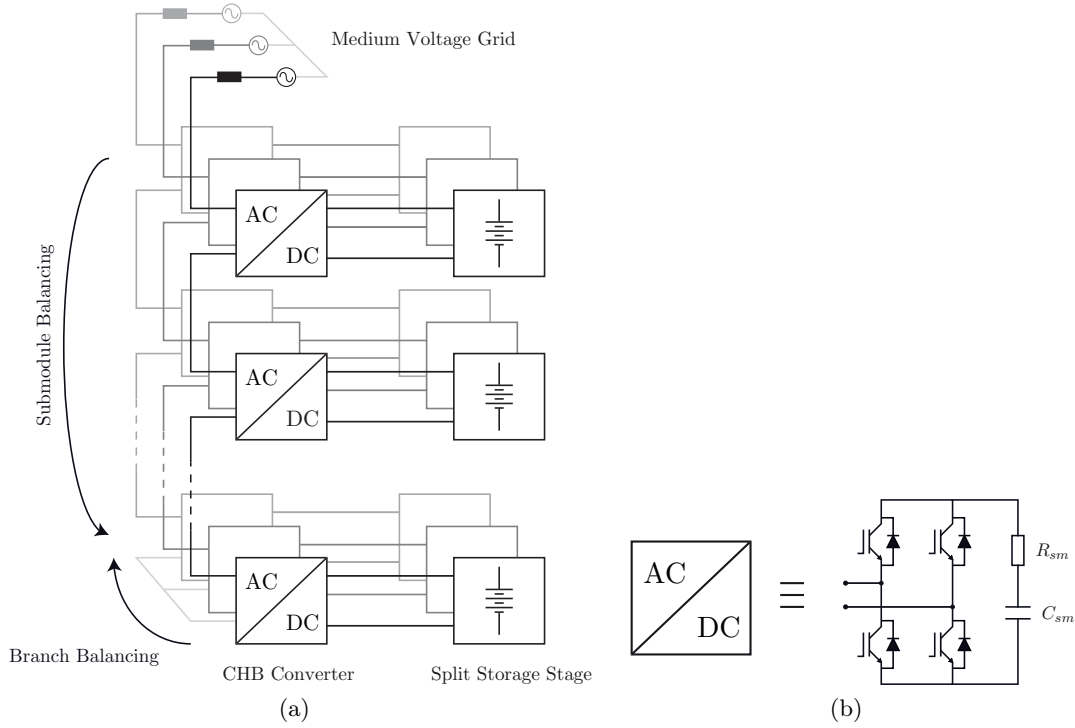
Figure 3.1: (a)The three-phase star-connected Cascaded H-Bridge Converter with integrated battery energy storage, (b) CHB converter submodule implementation.

3.2   Overview of Submodule-Battery Interface Solutions

The second-order current harmonic that appears at the submodule output is a result of the intrinsic pulsating power nature of any single-phase system. Considering u_k^i and i_k^i as the branch-side voltage and current of the ki-th submodule,

$$u_k^i = \hat{u}_k^i \cos(\omega t) \tag{3.1}$$

$$i_k^i = \hat{i}_k^i \cos(\omega t + \phi) \tag{3.2}$$

the instantaneous input-output power balance of the submodule gives

$$p_k^i = u_k^i i_k^i = \frac{1}{2}\hat{u}_k^i \hat{i}_k^i \cos(\phi) + \frac{1}{2}\hat{u}_k^i \hat{i}_k^i \cos(2\omega t + \phi) \tag{3.3}$$

The first constant term refers to the average power that is used to charge/discharge the battery. The second oscillating term, however, does not contribute to the average battery SoC. This component has a considerable peak-to-peak value, which can reach up to two times the grid current amplitude at a modulation index of unity.

The low frequency current component exhibits some disadvantages, e.g., increase of the inner battery resistive losses related to the resulting current *rms* value as well as periodic change of the battery behavior. Although such electrochemical investigations are not yet

widely available, it is believed to have a negative impact on the battery lifetime in the long run. Therefore and throughout this thesis work, it has been chosen to eliminate this second harmonic frequency on the submodule output level. In order to achieve this, several passive or active filtering solutions can be utilized.

Figure 3.2 illustrates three different possible ways to interface the BESS with the CHB submodule. For the sake of simplicity, the submodule full-bridge converter is modeled by means of a current source I_{sm}. In the first case, a resonant filter tuned at the second harmonic frequency combined with a low-pass filter for the additional switching harmonics is presented. The second case regards an additional nonisolated buck DC/DC converter in cascade with each submodule, acting as a controlled battery charger. Finally, the third case regards a nonisolated buck converter placed in parallel with the submodule and thus operating as an active filter. The latter is also done in conjunction with smaller passive filtering elements for the resulting submodule switching harmonics. The first case is referred to as direct passive interface (DPI), the second as indirect active interface (IAI), and the third one as active parallel interface (API).
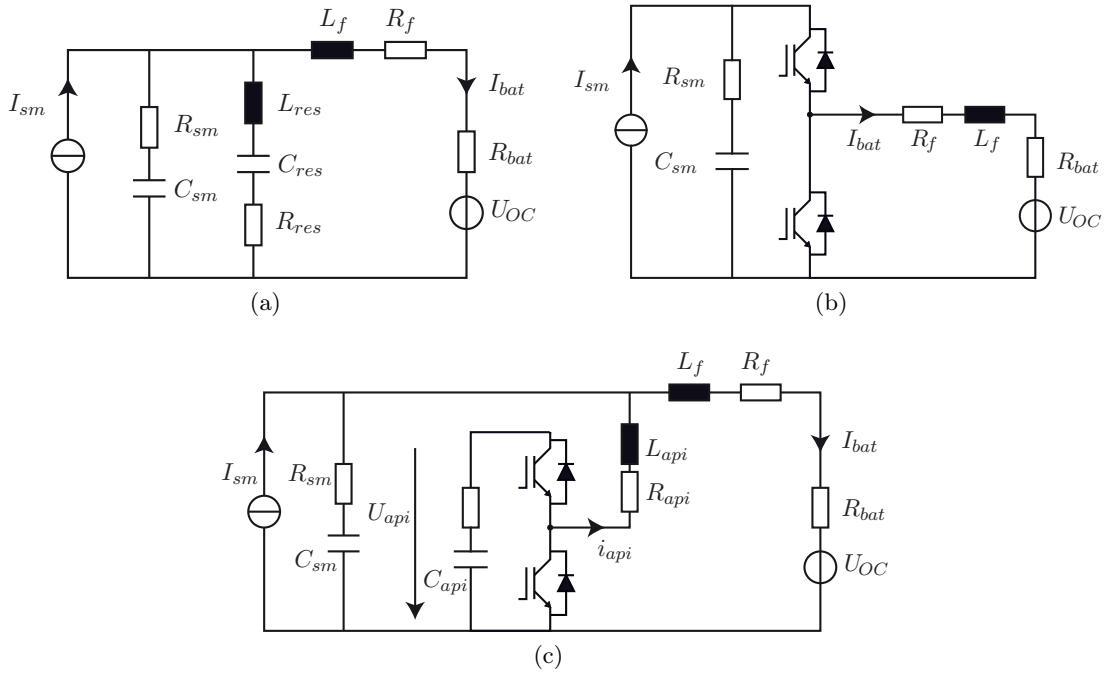
Figure 3.2: Possible interfaces between the CHB submodule and the integrated BESS utilizing: (a) a combination of resonant and low-pass filter (direct passive interface), (b) dedicated nonisolated DC/DC converter in cascade (indirect active interface), and (c) dedicated nonisolated DC/DC converter in parallel (active parallel interface).

In the next paragraphs, the three submodule/battery interfacing solutions are briefly discussed. For the dimensioning of the passive elements, a 10 % peak-to-peak battery current ripple is considered. Because of the difference in operating conditions of each

interfacing solution, the same submodule voltage U_{sm} and battery charging power is considered for all three cases. Finally, a 50 Hz three-phase grid frequency is assumed and the submodule switching frequency is set to 500 Hz.

Direct Passive Interface

The resonant filtering solution is the most straightforward implementation in terms of complexity and added components. It is used in a variety of applications, such as railway interties, i.e., the interconnection of the three-phase industrial grids with the single-phase railway supply commonly found in several European countries. It can be also found in the single-phase active front end converters for modern locomotives.

The model used for the design of the passive filter is illustrated in Figure 3.2a. The parasitic equivalent series resistance (ESR) is taken into consideration for all passive components. The electrical equivalent circuit of the battery depends on the utilized technology, having an impact on the filter design as well. For the scopes of this work, the battery pack has been simply modeled as a voltage source, representing the open-circuit voltage U_{OC}, in series with the respective internal resistance R_{bat}.

The filter transfer function is this case is given by (3.4), where the polynomials $n(s)$ and $d(s)$ are given in the bottom of the page.

$$G(s) = \frac{I_{bat}(s)}{I_{sm}(s)} = \frac{n(s)}{d(s)} \tag{3.4}$$

The advantage of using such a higher-order filter is that the utilized component values will be significantly lower. This, combined with the fact that the total grid charging power actually splits into dedicated levels, leads finally to the reduction of the size and cost of the filtering elements.

Figure 3.3 shows the typical waveforms for the case of the DPI utilization. The submodule

---

$$
\begin{aligned}
n(s) =\ & C_{res}L_{res}C_{sm}R_{sm}s^3 + \left[C_{res}\left(L_{res} + R_{res}C_{sm}R_{sm}\right)\right]s^2 \\
& + \left(R_{res}C_{res} + C_{sm}R_{sm}\right)s + 1 \\
d(s) =\ & L_f L_{res}C_{sm}C_{res}s^4 + \left[L_{res}C_{res}C_{sm}\left(R_{sm} + R_{bat} + R_f\right)\right. \\
& \left. + L_f C_{res}C_{sm}\left(R_{res} + R_{sm}\right)\right]s^3 \\
& + \left\{L_f\left(C_{sm} + C_{res}\right) + C_{res}\left[L_{res} + C_{sm}R_{res}\left(R_{sm} + R_f + R_{bat}\right)\right.\right. \\
& \left.\left. + C_{sm}R_{sm}\left(R_f + R_{bat}\right)\right]\right\}s^2 + \left[\left(C_{res} + C_{sm}\right)\left(R_f + R_{bat}\right) + C_{res}R_{res}\right. \\
& \left. + C_{sm}R_{sm}\right]s + 1
\end{aligned}
$$

current I_{sm} is switched with two times the submodule switching frequency f_{sw}, which is a result of a unipolar PWM scheme. It also comprises a strong second-order harmonic. The placed high-order filter is tuned at a resonance frequency of f_{res} in order to absorb the second-order harmonic of the grid frequency. It also attenuates significantly the switching-related ripple of I_{sm}.
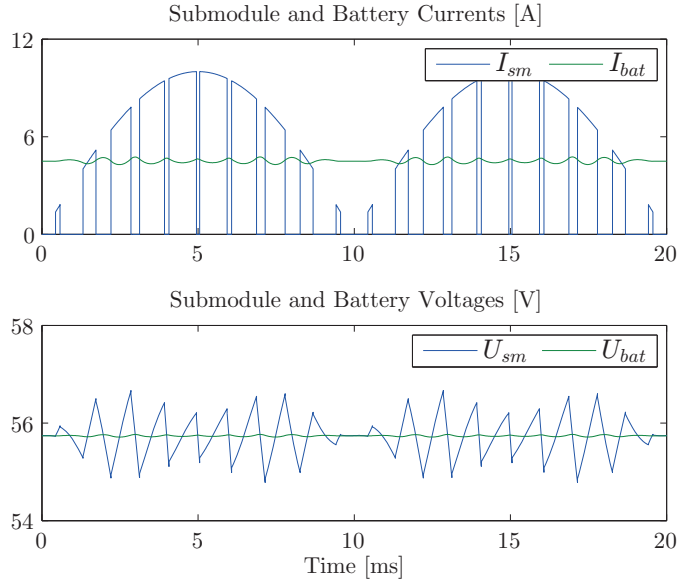
Figure 3.3: Main waveforms of the direct passive interface case for a resonance frequency of $f_{res} = 100$ Hz and a submodule switching frequency of $f_{sw}^{sm} = 500$ Hz.

The frequency response of the designed resonant and low-pass filter is shown in Figure 3.4 (upper) for different values of battery capacities. It is clear that the system is naturally well-damped at the two main observed undesirable resonant points in low battery capacities. This is due to the fact that in order to increase these values, the battery packs are placed in parallel leading to a reduction of the equivalent internal resistance. However for the same charging power, the battery resistive losses will be lower in higher capacitances, leading to an improved battery efficiency. This is additionally shown in Figure 3.4 (lower). The aforementioned observations and the respective trade-off have to be taken into account in the dimensioning process of the BESS, along with other typical parameters such as cost and battery lifetime due to deep discharge, in order to avoid unnecessary oversizing.

Indirect Active Interface

The IAI case refers to the placement of an additional power electronics-based conversion stage between the converter submodule and the battery. Compared to the DPI case, this means an increase on the system control hardware complexity but a decrease in the number of needed passive elements. Moreover, an additional degree of freedom for the control of the global system is offered, e.g., the submodule capacitor voltage can
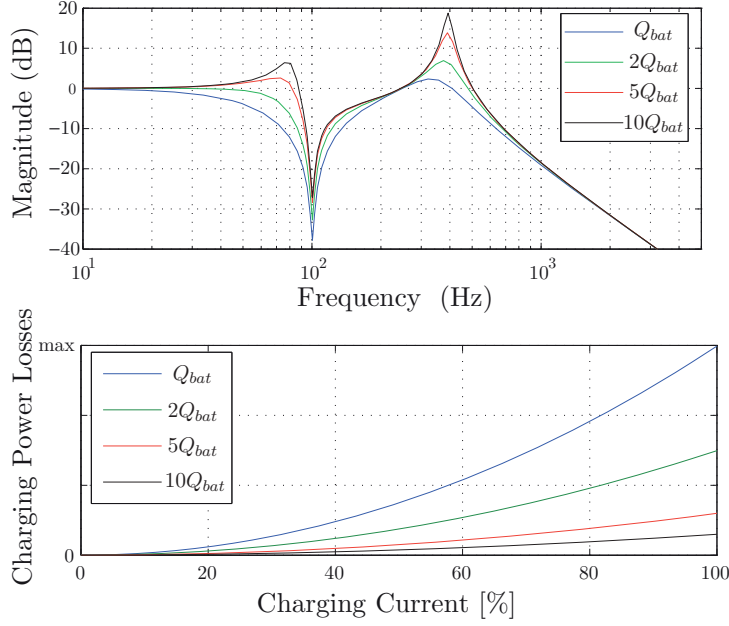
Figure 3.4: Frequency response of battery filter for different capacities (up), and graph illustrating the comparative evolution of battery losses for the same charging power (low) (the maximum value corresponds to the resulted losses from 100 % power at Q_{bat}).

be actively controlled from the battery side using the IAI. The latter will be further explained in Section 3.3 and will be used throughout this thesis work.

In order to calculate the required values of the submodule capacitances in the IAI case, the energy variation in the submodules is considered. This quantity, which is represented by ΔE_{sm} refers to the difference between the maximum and minimum energies inside the submodule and is calculated as follows:

$$\Delta E_{sm} = \frac{1}{2} C_{sm} \left[(U_{sm}^{max})^2 - (U_{sm}^{min})^2 \right] = \frac{1}{2} C_{sm} \underbrace{(U_{sm}^{max} + U_{sm}^{min})}_{2\overline{U}_{sm}} \underbrace{(U_{sm}^{max} - U_{sm}^{min})}_{U_{sm}^{p-p} = 2k_u \overline{U}_{sm}}$$

$$= 2 C_{sm} k_u \overline{U}_{sm}^2 \tag{3.5}$$

Therefore,

$$C_{sm} = \frac{\Delta E_{sm}}{2 k_u \overline{U}_{sm}^2} \tag{3.6}$$

The energy variation in one submodule can be approximated as being proportional to the energy variation in the whole converter branch, which is comprising N modules. Considering u_k and i_k as the converter voltage and current for the k-th branch respectively,

$$u_k = \hat{u}_k \cos(\omega t) \tag{3.7}$$

$$i_k = \hat{i}_k \cos(\omega t + \phi) \tag{3.8}$$

the branch power is calculated as

$$p_k = u_k i_k = \frac{1}{2}\hat{u}_k\hat{i}_k\cos(\phi) + \frac{1}{2}\hat{u}_k\hat{i}_k\cos(2\omega t + \phi) \tag{3.9}$$

Similarly to (3.3), the first constant term is in fact the active power that is transferred to the DC/DC converters. The second term causes the pulsation in the branch and its integral,

$$E_k = \frac{1}{2}\hat{u}_k\hat{i}_k\int\cos(2\omega t + \phi)dt = E_k^0 + \frac{\hat{u}_k\hat{i}_k}{4\omega}\sin(2\omega t + \phi) \tag{3.10}$$

gives finally the energy variation as

$$\Delta E_k = \frac{\hat{u}_k\hat{i}_k}{2\omega} \tag{3.11}$$

Finally and considering a symmetrical voltage operation of the converter submodules, the ripple is assumed to be divided equally, leading therefore to a submodule ripple of

$$\Delta E_{sm} = \frac{\Delta E_k}{N} \tag{3.12}$$

Substituting (3.12) in (3.6) gives finally the sizing equation of the submodule capacitors as follows in

$$C_{sm} = \frac{\hat{u}_k\hat{i}_k}{4\omega N k_u \overline{U}_{sm}^2} \tag{3.13}$$

The last component to be designed is the output filter inductor, which is given by (3.14) for a standard nonisolated buck DC/DC converter [115]:

$$L_f = \frac{(1-D)U_{bat}}{\Delta I_{bat}f_s} \tag{3.14}$$

where D refers to the converter duty cycle.

Figure 3.5 illustrates the main waveforms for the IAI case. The second-order power pulsating term is now buffered in the submodule capacitor. Therefore, the battery current will only feature the switching-related ripple of the buck converter. In order to maximize the efficiency, a duty cycle operation of close to 50 % has been considered for this case, therefore in this case half of the battery voltage is considered compared to the previous case of DPI.

It is noted that due to the switching frequency constraints in a high-power application, the inductor L_f has to be relatively large in order to limit the battery current ripple.
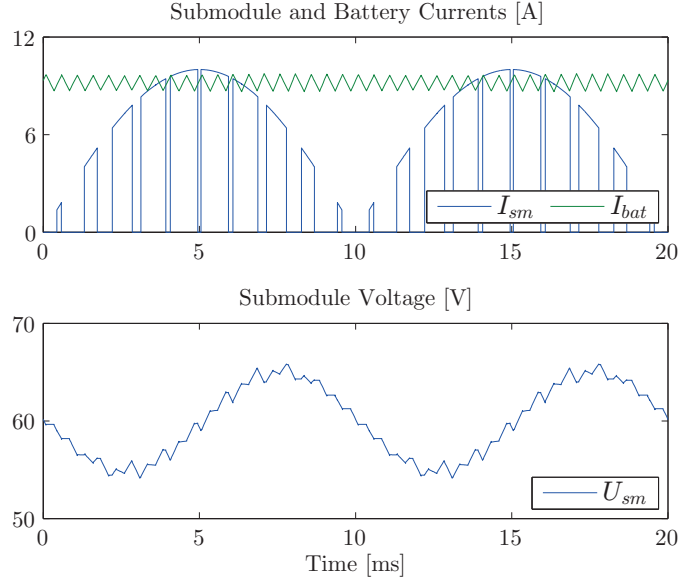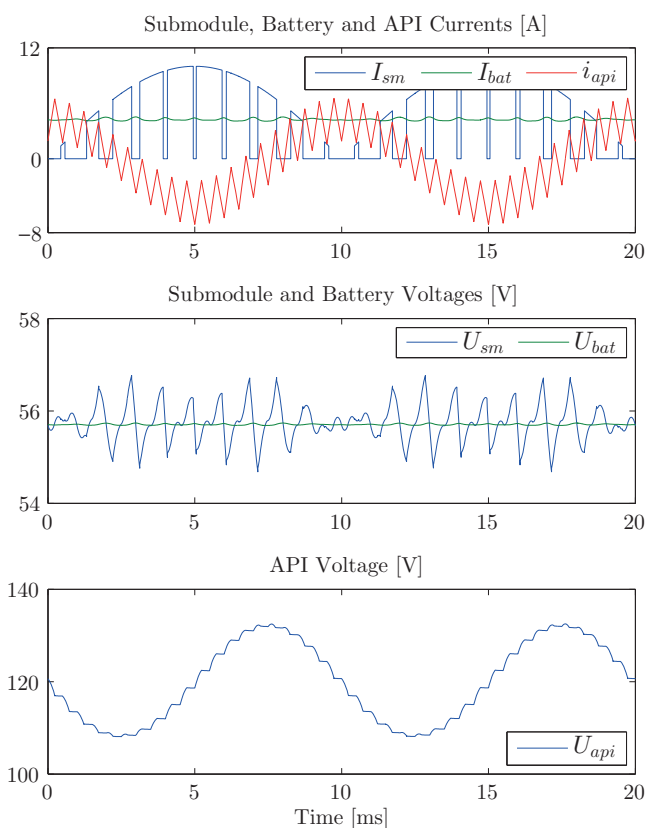
Figure 3.5: Main waveforms of the indirect active interface case for a submodule switching frequency of $f_{sw}^{sm} = 500$ Hz and IAI switching frequency of $f_{sw}^{iai} = 2$ kHz.

Active Parallel Interface

The dimensioning of the active parallel interface passive components is a combination of the two previous cases. The DPI case low-pass filter consisting of the elements C_{sm}, L_f is maintained to filter out the switching-related harmonics of the submodule and the additional converter as well. The two additional elements C_{api} and L_{api} are then designed according to the desired requirements. For the API capacitor, the low frequency energy pulsation is calculated as

$$E_{api} = \int U_{bat} i_{api} dt = \int U_{bat} \hat{i}_{api} \cos(2\omega t + \phi) dt = E_{api}^0 + \frac{U_{bat}\hat{i}_{api}}{2\omega} \sin(2\omega t + \phi) \quad (3.15)$$

which leads to an energy variation of

$$\Delta E_{api} = \frac{U_{bat}\hat{i}_{api}}{\omega} \quad (3.16)$$

The capacitance C_{api} is therefore given by

$$C_{api} = \frac{U_{bat}\hat{i}_{api}}{2\omega k_{\Delta u}\overline{U}_{api}^2} \quad (3.17)$$

Finally, the inductance value for L_{api} is calculated according to the admissible switching-related ripple over the average value of i_{api} and is therefore also given by (3.14).

68

The main waveforms for the API case are shown in Figure 3.6. The API acts as an active filter aiming at the elimination of the second-order submodule current harmonic. Similarly to the DPI case, the submodule voltage is imposed by the battery. The API capacitor C_{api} needs to be dimensioned so that its minimum voltage value U_{api}^{min} is always higher than the maximum submodule voltage U_{sm}^{max}, in order to achieve PWM operation. In addition, this voltage U_{api} has to be actively controlled to a desired average value $\overline{U}_{api}$, in order to compensate for losses and other non-idealities that would cause its divergence otherwise. As performed for the IAI case, the converter is chosen here to be operated with a duty cycle close to 50 %. In a real application this voltage would be preferably chosen close to the submodule one with an additional voltage margin for control reserve, in order to avoid using a capacitor and semiconductors with twice the blocking voltage.

Figure 3.6: Main waveforms of the active parallel interface case for a submodule switching frequency of $f_{sw}^{sm} = 500$ Hz and API switching frequency of $f_{sw}^{api} = 2$ kHz.

Discussion and Final CHB-BESS Topology Implementation

Some qualitative discussion can be now made regarding the three interface solutions. Table 3.1 shows the passive element dimensioning for each one of the aforementioned cases. The same battery charging power of approximately 230 W is considered for all cases and regards a low power laboratory prototype.

For the active-based solutions of IAI and API, a voltage variation factor of $k_u = 0.1$ has been used for the calculation of the necessary capacitances. It can be seen that the IAI needs considerably higher passive values than the API to achieve a desired low battery current ripple. In addition, the IAI semiconductors have to support all of the submodule current contrary to the API where only its AC part has to be provided. However and in order to be capable of achieving PWM operation, the API output capacitor minimum voltage has to be at least higher than the battery voltage (with an additional margin held for control reserve). The latter means higher capacitor and semiconductor blocking voltage requirement in the API case.

Table 3.1: Passive element requirements for all interfacing cases

Quantity	DPI	API	IAI
C_{sm}	1 mF		1.4 mF
L_f	0.5 mF		7.5 mH
C_{res}	2.3 mF	–	
L_{res}	1.1 mH	–	
C_{api}	–	0.28 mF	–
L_{api}	–	3.2 mH	–

In terms of control complexity, the DPI case implies the most straightforward implementation, since no additional control hardware components are needed. However, both the uncontrolled DPI and the controlled API cases feature the same disadvantage: the submodule-battery voltage dependency. The latter is not beneficial in cases where the submodules exhibit significant voltage differences because of SoC variations between the batteries. Only the IAI solution offers a complete decoupling between the submodule and the battery voltages.

The IAI control system is similar to the one of the API case and will be described in detail in Section 3.3. It is based on a typical cascaded outer voltage/inner current loop. The external PI-based loop aims at the stabilization of the capacitor DC-link voltage U_{sm} (or U_{api} accordingly) through a small active power extraction from the battery (or also the submodule in the API case), compensating for any imperfections that would cause its divergence otherwise. Moreover, the inner loop is responsible for regulating the converter current I_{bat} (i_{api} respectively). In the IAI case, I_{bat} is controlled to have a continuous average component, therefore a PI controller is sufficient. The API current, however, has to eliminate the second-order harmonic of the submodule current I_{sm}. Since the API current is expected to have a small continuous component (for the DC-link control) as well as an alternating component, a PI controller with an additional resonant term tuned at the second-order grid frequency harmonic offers the most straightforward solution. The feed-forward active filtering average current reference can be calculated using (3.3), since the grid current i_k^i is measured and the modulation reference u_k^i is a direct result of the grid current controller.

For a detailed comparison of the IAI and API cases, including efficiency considerations as well as passive component selection guidelines in the framework of a low voltage/power laboratory prototype, the reader is referred to [116]. In this thesis work, the indirect active interface concept has been finally chosen to be implemented, mainly due to its straightforward design as well as additional offered degree of freedom for complete power and voltage decoupling between the submodule capacitor and battery. Throughout the next sections, the control design is treated based on the IAI concept.

3.3 Voltage, Power and State of Charge Control Actions

In this section, the balancing control actions for CHB converters in star or delta connection will be discussed.

3.3.1 The Star-Configured Cascaded H-Bridge Converter Case

Initially, the control of the three-phase CHB with star connection is considered. This topology has been illustrated in Figure 3.1a.

Submodule Capacitor Voltage Balancing

One main issue regarding this specific topology is the balancing of the submodule capacitor voltages, especially when the fed loads are different but also due to the fact that the modeled capacitance and losses within the different submodules vary in practical systems. When using the extra conversion stage between the submodules and the batteries, this can be solved by controlling the individual voltages from the battery side through a typical cascaded outer voltage/inner current loop, similarly to the CHB converter-based photovoltaic unit of [117] and the supercapacitive MMC-based traction system of [118]. This paragraph deals with the dimensioning of the control system for the IAI, whose block diagram is given in Figure 3.7.

According to the notations of Figure 3.2b, the respective transfer functions for the current and voltage are given respectively as

$$G_S^U(s) = \frac{1}{sC_{sm}}, \quad G_S^I(s) = \frac{1}{sL_f + R_f} \tag{3.18}$$

The inner loop controls the average value of the battery current with the regulator $G_R^I(s)$ given by

$$G_R^I(s) = \frac{1 + sT_{nI}}{sT_{iI}} \tag{3.19}$$
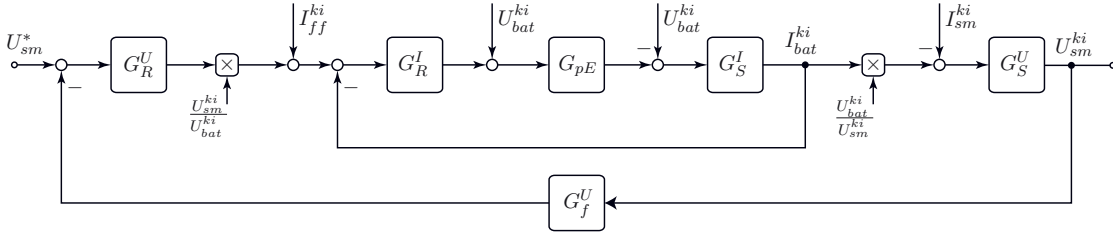
Figure 3.7: Cascaded voltage/current control loop for each of the indirect active interfaces.

The battery voltage is added to the output of the regulator for disturbance rejection purposes. The converter and control hardware non-linearities and delays are modeled by the small time constant T_{pE} according to the pseudo-continuous approach with the associated transfer function $G_{pE}(s)$ [106] as

$$G_{pE}(s) = \frac{K_{cm}}{1 + sT_{pE}} \tag{3.20}$$

where the transfer function gain $K_{cm} = U_{sm}$ in this case.

The external loop controls the submodule capacitor voltage U_{sm}^{ki} to its reference value U_{sm}^* through a PI controller $G_R^U(s)$:

$$G_R^U(s) = \frac{1 + sT_{nU}}{sT_{iU}} \tag{3.21}$$

A pre-calculated feed-forward current component $I_{ff}^{ki} = P_{bat}^{ki*}/U_{bat}^{ki}$ is added to the output of the regulator for faster response. The latter is based on the power demand of the battery, which is a result of the higher-level control functions. In this way, the contribution of the voltage regulator will correspond to a small amount of active power injection in order to compensate for the losses that would cause deviations of the capacitor voltage from its desired value. Since only the average value of the capacitor voltage can be controlled, a low-pass filter has to be added on the voltage measurement of U_{sm}^{ki} in order to reject the low-order harmonic frequency oscillations:

$$G_f^U(s) = \frac{1}{1 + sT_f} \tag{3.22}$$

The inner current loop is designed according to the magnitude optimum criterion. Therefore the regulator constants are given as:

$$T_{nI} = \frac{L_f}{R_f}, \quad T_{iI} = \frac{2T_{pE}}{R_f} \tag{3.23}$$

Since the submodule voltage is measured, it can be used for the second-order harmonic cancellation on a current control level. This is achieved by dividing the control output by

U_{sm} in order to finally obtain the required duty cycle.

Subsequently, an equivalent transfer function is considered for the closed-loop current control with a time constant of $T_{cl} = 2T_{pE}$, in order to design the external voltage loop. For the latter, the symmetric optimum criterion for systems with integral behavior is utilized. The gains are specified as

$$T_{nU} = 4(T_f + T_{cl}), \quad T_{iU} = \frac{8(T_f + T_{cl})^2}{C_{sm}} \tag{3.24}$$

Submodule Power Control

The power balancing problem regards the ability of the converter to absorb or inject different amounts of active power between the submodules or the branches. The latter implies that this can be divided in two different sub-problems, the submodule power control regarding the submodules within a given converter branch as well as the control between the independent converter branches, as depicted in Figure 3.1a.
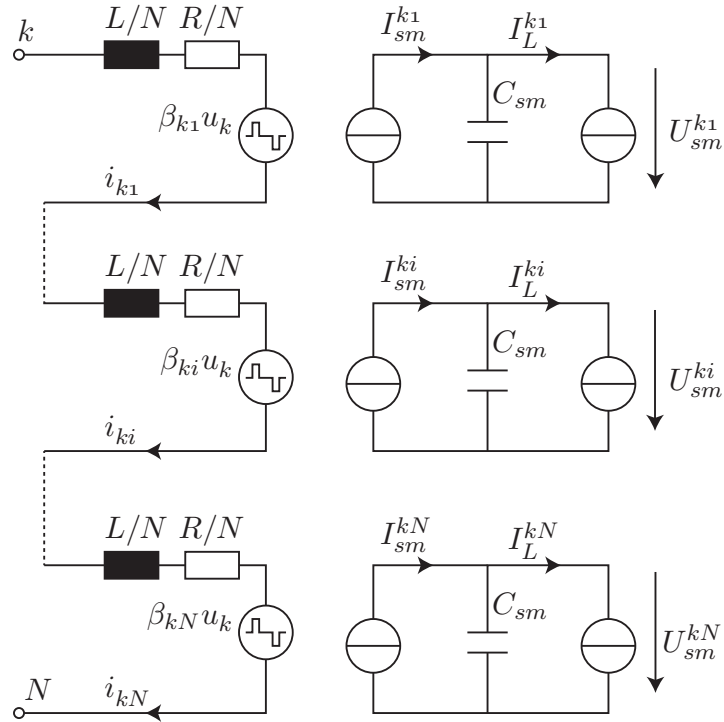
Figure 3.8: Equivalent circuit of a branch for decoupled power flow formulation.

In order to achieve individual submodule power control, the adaptation of the respective modulation references of each submodule has to take place. Figure 3.8 shows an equivalent circuit of one converter branch. The submodule outputs have been decoupled from their inputs. On the AC side, the same current flows through the equivalent voltages sources.

This means that in order to change the amount of absorbed or injected power flow by each DC side, the controlled AC submodule voltage is to be changed. The power ratio factor β_{ki} is therefore introduced for the analysis [119].

$$\beta_{ki} = \frac{\overline{U}_{sm}^{ki}\,\overline{I}_{sm}^{ki}}{\sum\limits_{i=1}^{N} \overline{U}_{sm}^{ki}\,\overline{I}_{sm}^{ki}} = \frac{P_{sm}^{ki}}{\sum\limits_{i=1}^{N} P_{sm}^{ki}} \quad \text{with} \quad \sum_{i=1}^{N} \beta_{ki} = 1. \tag{3.25}$$

By simply multiplying the global desired AC converter voltage u_k, which is the result of the line current control function, by the respective β_{ki}, the total branch active power can be distributed in a desired manner within the different submodules.
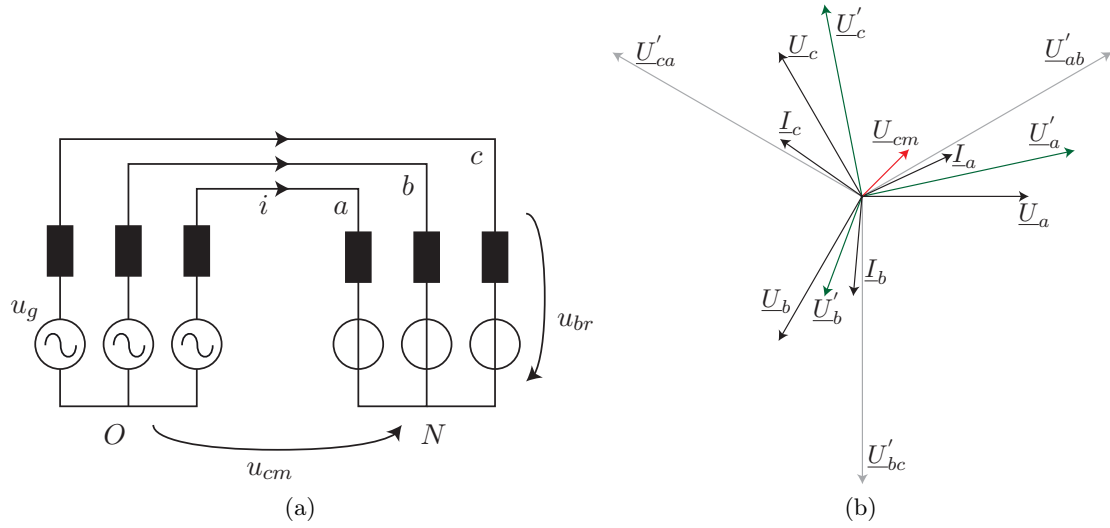
Figure 3.9: Star-connected CHB converter: (a) Definition of system voltages and currents, (b) definition of system voltage and current vectors, considering only positive sequences.

Branch Power Control

The case of independent branch power control is very important, since it generally implies the desire to handle different amounts of active power from each converter branch, without however disturbing the symmetry of the three-phase grid current. The degree of freedom to achieve this is to inject a specified common-mode voltage and has been introduced by [120]. In [66], the concept was explored for SoC balancing control. In this thesis work, the equations are generalized to account for grid unbalances and tailored for the application of the decoupling DC/DC conversion stage between the submodules and the batteries.

The idea is to specify the amplitude and angle of the common-mode voltage phasor $\underline{U}_{cm}$, which will affect the individual branch powers, but will keep the total three-phase

power flow unaffected. Therefore, the three-phase currents will remain balanced, since the line-to-line voltage will not change. The concept is illustrated in Figure 3.9. It is noted that in order to achieve a constant power term associated with the common-mode voltage, the latter should oscillate with the fundamental converter voltage frequency as well.

Similarly to Chapter 2, the three-phase grid quantities are modeled by means of symmetrical components, where the superscripts p and n denote the positive and negative sequences, respectively. The k-th converter branch voltage ($k = a, b, c$) can be written as

$$
\begin{aligned}
u_k =& \hat{u}^p \cos\left(\omega t + \phi_u^p - \frac{2\pi(m-1)}{3}\right) + \hat{u}^n \cos\left(\omega t + \phi_u^n + \frac{2\pi(m-1)}{3}\right) \\
& + \hat{u}_{cm} \cos\left(\omega t + \phi_{cm}\right)
\end{aligned}
\tag{3.26}
$$

where $m = 1, 2, 3$. For simplicity ϕ_u^p can be set to zero, if the control system is synchronized with the positive sequence voltage u^p. The k-th branch current can also be expressed through the use of the symmetrical components as

$$
i_k = \hat{i}^p \cos\left(\omega t + \phi_i^p - \frac{2\pi(m-1)}{3}\right) + \hat{i}^n \cos\left(\omega t + \phi_i^n + \frac{2\pi(m-1)}{3}\right)
\tag{3.27}
$$

The product of the voltage with the current in each converter branch gives the associated branch power components. Only the constant (P_{br}^k) and not the oscillating terms are of interest and are obtained for branches a and b as

$$
\begin{aligned}
P_{br}^a =& \frac{\hat{u}_{cm}\hat{i}^p}{2} \cos(\phi_{cm} - \phi_i^p) + \frac{\hat{u}_{cm}\hat{i}^n}{2} \cos(\phi_{cm} - \phi_i^n) + \frac{\hat{u}^p\hat{i}^n}{2} \cos\phi_i^n + \\
& + \frac{\hat{u}^n\hat{i}^p}{2} \cos(\phi_u^n - \phi_i^p) + \underbrace{\frac{\hat{u}^p\hat{i}^p}{2} \cos\phi_i^p + \frac{\hat{u}^n\hat{i}^n}{2} \cos(\phi_u^n - \phi_i^n)}_{\overline{P}_{3br}}
\end{aligned}
\tag{3.28}
$$

$$
\begin{aligned}
P_{br}^b =& \frac{\hat{u}_{cm}\hat{i}^p}{2} \cos(\phi_{cm} - \phi_i^p - \frac{4\pi}{3}) + \frac{\hat{u}_{cm}\hat{i}^n}{2} \cos(\phi_{cm} - \phi_i^n - \frac{2\pi}{3}) + \frac{\hat{u}^p\hat{i}^n}{2} \cos(\phi_i^n - \frac{2\pi}{3}) + \\
& + \frac{\hat{u}^n\hat{i}^p}{2} \cos(\phi_u^n - \phi_i^p - \frac{2\pi}{3}) + \underbrace{\frac{\hat{u}^p\hat{i}^p}{2} \cos\phi_i^p + \frac{\hat{u}^n\hat{i}^n}{2} \cos(\phi_u^n - \phi_i^n)}_{\overline{P}_{3br}}
\end{aligned}
\tag{3.29}
$$

The third branch forms an equation which is not independent, therefore it is adequate to solve the following system for the definition of u_{cm}:

$$
\begin{cases}
\underbrace{P_{br}^{a*} - \overline{P}_{3br} - \alpha_{1S}}_{\Delta P_{br}^a} = \hat{u}_{cm}\alpha_{2S} \cos\phi_{cm} + \hat{u}_{cm}\alpha_{3S} \sin\phi_{cm} \\
\underbrace{P_{br}^{b*} - \overline{P}_{3br} - \beta_{1S}}_{\Delta P_{br}^b} = \hat{u}_{cm}\beta_{2S} \cos\phi_{cm} + \hat{u}_{cm}\beta_{3S} \sin\phi_{cm}
\end{cases}
\tag{3.30}
$$

$$\alpha_{1S} = \frac{\hat{u}^p \hat{i}^n}{2} \cos \phi_i^n + \frac{\hat{u}^n \hat{i}^p}{2} \cos(\phi_u^n - \phi_i^p), \quad \alpha_{2S} = \frac{\hat{i}^p}{2} \cos \phi_i^p + \frac{\hat{i}^n}{2} \cos \phi_i^n, \quad \alpha_{3S} = \frac{\hat{i}^p}{2} \sin \phi_i^p + \frac{\hat{i}^n}{2} \sin \phi_i^n$$

$$\beta_{1S} = \frac{\hat{u}^p \hat{i}^n}{2} \cos(\phi_i^n - \frac{2\pi}{3}) + \frac{\hat{u}^n \hat{i}^p}{2} \cos(\phi_u^n - \phi_i^p - \frac{2\pi}{3}), \quad \beta_{2S} = \frac{\hat{i}^p}{2} \cos(\phi_i^p + \frac{4\pi}{3}) + \frac{\hat{i}^n}{2} \cos(\phi_i^n + \frac{2\pi}{3}),$$

$$\beta_{3S} = \frac{\hat{i}^p}{2} \sin(\phi_i^p + \frac{4\pi}{3}) + \frac{\hat{i}^n}{2} \sin(\phi_i^n + \frac{2\pi}{3})$$

The coefficients α_{1S-3S} and β_{1S-3S} are functions of the grid voltage and currents positive and negative sequence components and are given at the top of this page. The solution to the system is given similarly to [120] by

$$\phi_{cm} = \arctan\left(\frac{\Delta P_{br}^a \beta_{2S} - \Delta P_{br}^b \alpha_{2S}}{\Delta P_{br}^b \alpha_{3S} - \Delta P_{br}^a \beta_{3S}}\right), \quad \hat{u}_{cm} = \frac{\Delta P_{br}^a}{\alpha_{2S} \cos \phi_{cm} + \alpha_{3S} \sin \phi_{cm}} \quad (3.31)$$

The solution for the typical case of balanced converter voltages and currents (no negative sequence component), where obviously $\alpha_{1S} = \beta_{1S} = 0$, is given by

$$\phi_{cm} = \phi_i^p - \theta = \phi_i^p - \arctan\left[\frac{2\Delta P_{br}^b / \Delta P_{br}^a + 1}{\sqrt{3}}\right], \quad \hat{u}_{cm} = \frac{2\Delta P_{br}^a}{\hat{i}^p \cos \theta} \quad (3.32)$$

State of Charge Balancing

As already stated in the introduction, several battery technologies exhibit a flat curve of the voltage in function of their SoC. This means that a battery voltage balancing scheme would not be accurate, since two similar voltages do not necessarily imply similar SoCs. In time domain, the battery SoC evolution can be expressed by the integration of the current that flows into the battery divided by its nominal capacity:

$$SoC(t) = SoC(0) + \frac{100}{Q_{bat,n}} \int_0^t I_{bat} \cdot dt \quad (3.33)$$

When the control target is the balancing of the battery SoCs, the need of a closed-loop control algorithm is derived. In the studied case, two possible SoC unbalance directions exist: a) vertical (across the submodules of a branch), and b) horizontal (across the three converter branches). For the controller design, the system plants can be modeled by first-order transfer functions with integral behavior, based on (3.33). Since only the change rate of the SoCs is of interest for the control system, the initial value can be omitted. For the individual submodule SoC modeling, the following expression is gradually obtained,

$$SoC_{sm} = \frac{I_{bat}^{sm} \cdot 100}{s \cdot Q_{bat,n}^{sm}} = \frac{P_{bat}^{sm} \cdot 100}{s \cdot U_{bat,n}^{sm} Q_{bat,n}^{sm}} = \frac{P_{bat}^{sm} \cdot 100}{s \cdot E_{bat,n}^{sm}} \quad (3.34)$$

where $Q_{bat,n}^{sm}$ denotes the submodule battery nominal capacity and $U_{bat,n}^{sm}$ the respective nominal voltage. Similarly for the whole converter branch SoC, the following equation holds:

$$SoC_{br} = \frac{P_{bat}^{br} \cdot 100}{s \cdot E_{bat,n}^{br}} = \frac{P_{bat}^{br} \cdot 100}{s \cdot N E_{bat,n}^{sm}} \tag{3.35}$$

In both cases the SoC is a percentage (%), and the battery nominal energy $E_{bat,n}^{sm}$ is expressed in $(W \cdot s)$. The expressions of the submodule and branch SoCs in function of the submodule and branch powers, respectively, imply the fact that the latter can be directly used as control variables. Therefore, all degrees of freedom for achieving different amounts of active power on a submodule and branch level, and which have been discussed so far, can be utilized in a straightforward manner for the implementation of the control loops.

(a)

(b)
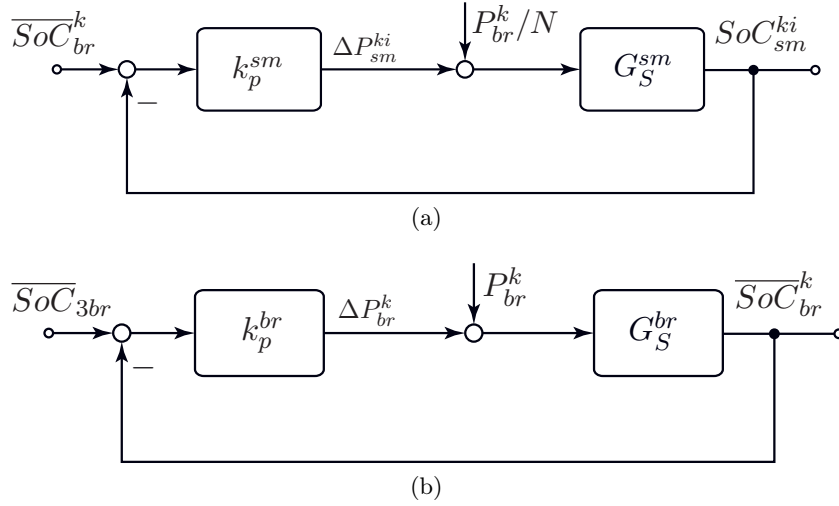
Figure 3.10: Block diagrams for (a) submodule and (b) branch balancing of battery State of Charges.

According to (3.34) and similarly to the active symmetrization concept presented in [121], the active powers to balance the state of charges can be calculated by means of a proportional control. The respective block diagrams for the branch and submodule SoC loops are illustrated in Figure 3.10. The branch SoC control forces the k-th branch mean SoC value $\overline{SoC}_{br}^{k}$ to follow the mean SoC value of all three branches $\overline{SoC}_{3br}$. These two quantities are defined as:

$$\overline{SoC}_{br}^{k} = \frac{1}{N} \sum_{i=1}^{N} SoC_{sm}^{ki} \tag{3.36}$$

$$\overline{SoC}_{3br} = \frac{\overline{SoC}_{br}^{a/ab} + \overline{SoC}_{br}^{b/bc} + \overline{SoC}_{br}^{c/ca}}{3} \tag{3.37}$$

The submodule SoC control forces accordingly the ki-th submodule SoC_{sm}^{ki} to follow the branch mean SoC value $\overline{SoC}_{br}^{k}$. The respective gains k_p^{br} and k_p^{sm} are given as a function of the desired rise times t_r^{sm}, t_r^{br} and the nominal battery energy storage $E_{bat,n}^{sm}$.

$$k_p^{sm} = \frac{E_{bat,n}^{sm}}{100 \cdot t_r^{sm}} \ln 9 \quad \text{and} \quad k_p^{br} = \frac{N E_{bat,n}^{sm}}{100 \cdot t_r^{br}} \ln 9 \tag{3.38}$$

From Figure 3.10, it can be seen that the branch or submodule power will consist of two terms: the main power contribution, which is common for all submodules/branches and does not contribute to the unbalance, as well as the balancing power term, which is the result of the closed-loop control. The total state of charge will be a result of both terms.

Figure 3.11 shows the step responses for the closed-loop control algorithm. It is evident that the rise times are set higher than a respective capacitor voltage balancing loop, as dictated by the significant difference in the system time constants.
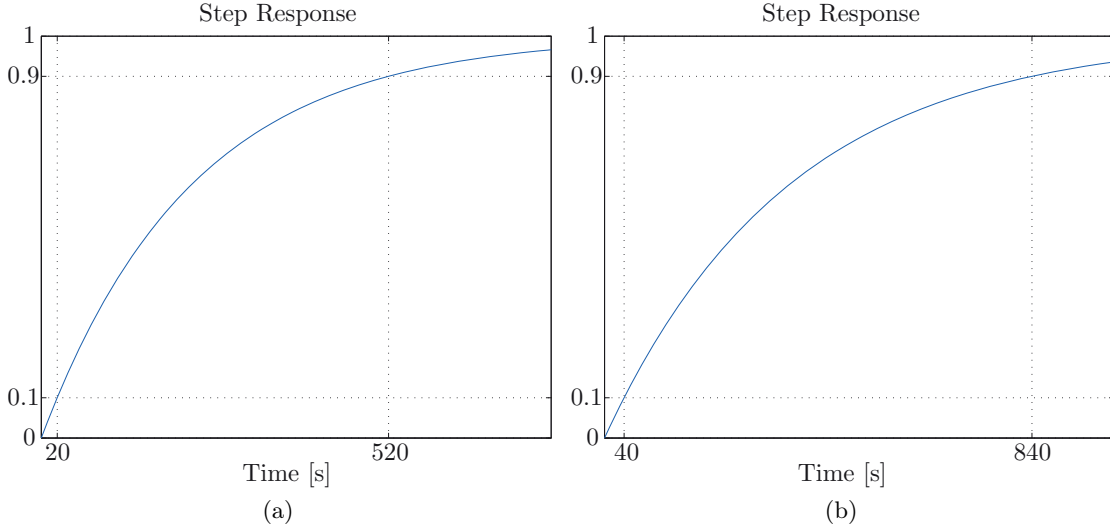
Figure 3.11: Step response of the closed-loop controllers for (a) branch SoC balancing with $t_r^{br} = 500$ s and (b) submodule SoC balancing with $t_r^{sm} = 800$ s.

Limitations on SoC Controller Gain Selection

Certain constraints exist regarding the choice for the SoC balancing controller gains. These are linked to the converter operation and rating. In this section, the respective limitations are established. It is noted that for sake of simplicity, only balanced grid conditions are assumed for this study.

Initially the limit for the branch balancing loop is examined. The amount of balancing power ΔP_{br}^{k} in the star-configured CHB converter is directly related to the maximum achievable injected common-mode voltage. The latter is a function of the dimensioned

branch blocking voltage u_{br}^{dim}, which is in turn related to the tolerated voltage variation in the submodule capacitors $k_{\Delta v} = U_{sm}^{max}/U_{sm}^{min}$ [75]. These can be expressed as:

$$u_{br}^{dim} \geq k_{\Delta v} \left(u_g^{max} + u_{cm}^{max} \right) \Leftrightarrow u_{cm}^{max} \leq \frac{Nu_{sm}^{dim}}{k_{\Delta v}} - u_g^{max} \Leftrightarrow \frac{2\Delta P_{br}^{max}}{\hat{i}^p \cos x} \leq \frac{Nu_{sm}^{dim}}{k_{\Delta v}} - u_g^{max} \Leftrightarrow$$

$$\Leftrightarrow \frac{2NE_{bat,n}^{sm}\Delta SoC_{br}^{max}\ln 9}{100 \cdot t_{r,S}^{br}} \leq \left(\frac{Nu_{sm}^{dim}}{k_{\Delta v}} - u_g^{max} \right) \hat{i}^p \cos x, \tag{3.39}$$

where $x = \arctan \left[\dfrac{2\left(\frac{\Delta SoC_{br}^{k+1}}{\Delta SoC_{br}^{k,max}} \right)+1}{\sqrt{3}} \right]$.

Taking branch a as a reference and assuming that the maximum SoC variations are shared between branches a and c with the same value and opposite signs, ΔSoC_{br}^{k+1} of branch b will be zero (since $\sum \Delta SoC_{br}^k = 0$). Therefore, x can be approximated as having the worst case value of $\arctan\left(1/\sqrt{3}\right) = \pi/6$. The latter leads to the definition of a minimum rise time $t_{r,S}^{br}$ of

$$t_{r,S}^{br} \geq \frac{4NE_{bat,n}^{sm}\Delta SoC_{br}^{max}k_{\Delta v}\ln 9}{100\sqrt{3}\hat{i}^p \left(Nu_{sm}^{dim} - k_{\Delta v}u_g^{max} \right)} \tag{3.40}$$

The result shows that the rise time is proportional to the battery energy and the tolerated maximum SoC error as expected. In addition, it is inversely proportional to the maximum current, i.e. in lower currents the maximum achievable balancing power is limited.

The constraint for the submodule SoC balancing control is related to overmodulation. The branch voltage is weighted with the desired amount of active power for each submodule, which is essentially the sum of the mean branch power P_{br}^k/N with the submodule balancing action ΔP_{sm}^{ki}. This can be expressed finally as

$$\beta_{ki}u_{br}^{max} \leq U_{sm}^{min} \Leftrightarrow \frac{\frac{P_{br}^k}{N} + \Delta P_{sm}^{max}}{P_{br}^k}u_{br}^{max} \leq U_{sm}^{min} \Leftrightarrow \left(\frac{1}{N} + \frac{2\Delta P_{sm}^{max}}{P_{br}^k} \right) \leq \frac{U_{sm}^{min}}{u_{br}^{max}}$$

$$\Leftrightarrow \Delta P_{sm}^{max} \leq P_{br}^k \left(\frac{U_{sm}^{min}}{u_{br}^{max}} - \frac{1}{N} \right) \overset{(3.38)}{\Leftrightarrow} \frac{E_{bat,n}^{sm}\Delta SoC_{sm}^{max}\ln 9}{100 \cdot t_{r,S}^{sm}} \leq \frac{P_{br}^k \left(NU_{sm}^{min} - u_{br}^{max} \right)}{Nu_{br}^{max}} \tag{3.41}$$

leading to a minimum rise time of

$$t_{r,S}^{sm} \geq \frac{Nu_{br}^{max}E_{bat,n}^{sm}\Delta SoC_{sm}^{max}\ln 9}{P_{br}^k \left(NU_{sm}^{min} - u_{br}^{max} \right)100} = \frac{Nu_{br}^{max}E_{bat,n}^{sm}\Delta SoC_{sm}^{max}\ln 9}{P_{br}^k \left[N(1-k_u)\overline{U}_{sm} - u_{br}^{max} \right]100} \tag{3.42}$$

where k_u is the allowed voltage ripple on the submodule capacitor voltage. Again in this case, the rise time has to be increased with an increase of the battery stored energy as

well as the maximum SoC error. In addition and with a higher amount of absorbed power P_{br}^k/N, a faster balancing can be achieved. Another way to avoid overmodulation is to control obviously the mean value of the submodule capacitor voltages $\overline{U}_{sm}$ at a higher value, which means however an increase in the required installed capacitive energy.

It is noted that the increase of common-mode voltage limits the amount of active power that can be absorbed or injected from each module. This means also that the branch balancing control loop has an effect on the module balancing one. It is implied that the submodule balancing loop should be designed with a lower bandwidth, leading therefore to $t_{r,S}^{br} < t_{r,S}^{sm}$. Finally and in order to achieve independence from the global current control, the relation $\sum \Delta P_{sm}^{ki} = 0$ should hold.

Finally, the established limitations can be utilized for an adaptive gain calculation in cases of operating point changes.

3.3.2   The Case of Delta-Configured Cascaded H-Bridge Converter

The aforementioned analysis can be also performed for the delta-connected Cascaded H-Bridge converter with integrated battery energy storage, which is depicted in Figure 3.12 There are, however, some differences that are to be taken into account during the design and control procedures. The delta connection implies the requirement of blocking the whole line-to-line voltage, which is larger by a factor of $\sqrt{3}$ compared to the star-connected
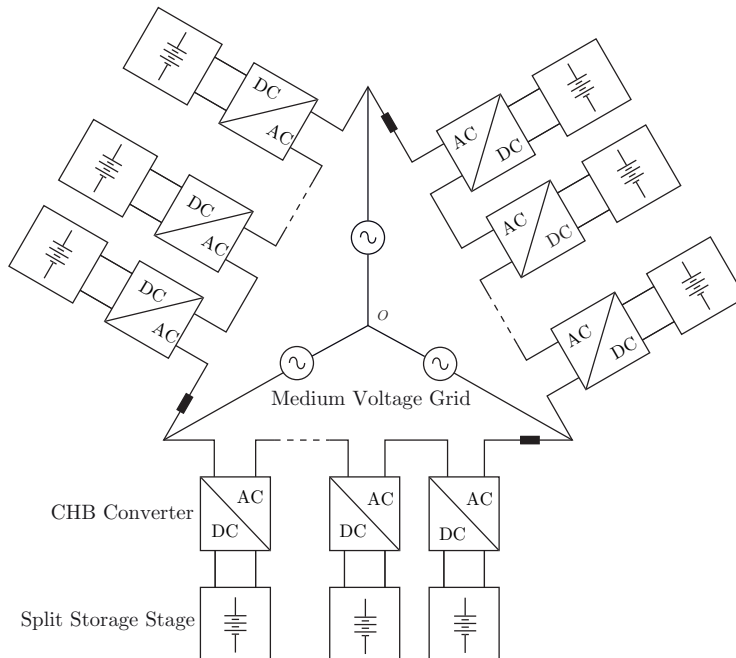
Figure 3.12: The three-phase delta-connected Cascaded H-Bridge converter with integrated battery energy storage.

case (if no common-mode voltage component is considered). However, the rated branch currents are decreased by the same factor. In addition and instead of a common-mode voltage injection, a circulating current can be added between the three converter branches without disturbing the grid phase currents. The latter can be used for branch balancing purposes in such a concept. Therefore, the delta connection can be considered as the *dual* converter case of the star-connected one.

Branch Balancing

Figure 3.13 illustrates the circulating current injection concept, which can be utilized to achieve independent branch power control without disturbing the three-phase grid current symmetry in the delta-connected CHB-BESS case. Similarly to the star configuration, i_{circ} has to oscillate with the fundamental frequency component to create the desired constant power terms.
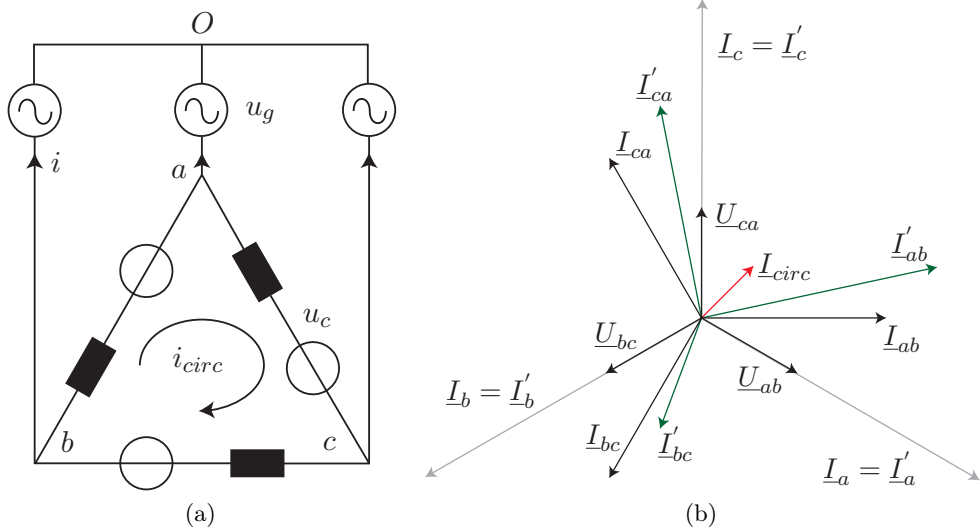
Figure 3.13: Delta-connected CHB converter: (a) Definition of system voltages and currents, (b) definition of system voltage and current vectors, considering only positive sequences.

In order to be consistent with the previous analysis, the phase voltages and currents will be considered for the definition of the circulating current component. Therefore the k-th branch voltage ($k = ab, bc, ca$) comprising positive and negative sequence components is now given as

$$u_k = \sqrt{3}\hat{u}^p \cos\left(\omega t + \phi_u^p - \frac{2\pi(m-1)}{3} + \frac{\pi}{6}\right) + \sqrt{3}\hat{u}^n \cos\left(\omega t + \phi_u^n + \frac{2\pi(m-1)}{3} - \frac{\pi}{6}\right)$$

(3.43)

and the respective branch currents as

$$i_k = \frac{\hat{i}^p}{\sqrt{3}} \cos\left(\omega t + \phi_i^p - \frac{2\pi(m-1)}{3} + \frac{\pi}{6}\right) + \frac{\hat{i}^n}{\sqrt{3}} \cos\left(\omega t + \phi_i^n + \frac{2\pi(m-1)}{3} - \frac{\pi}{6}\right) +$$
$$+ \hat{i}_{circ} \cos\left(\omega t + \phi_{circ}\right). \tag{3.44}$$

Assuming once again that $\phi_u^p = 0$, the constant branch power terms are given by

$$P_{br}^{ab} = \frac{\sqrt{3}}{2} \hat{u}^p \hat{i}_{circ} \cos(\phi_{circ} - \frac{\pi}{6}) + \frac{\sqrt{3}}{2} \hat{u}^n \hat{i}_{circ} \cos(\phi_{circ} - \phi_u^n + \frac{\pi}{6}) + \frac{\hat{u}^p \hat{i}^n}{2} \cos\left(\phi_i^n - \frac{\pi}{3}\right)$$
$$+ \frac{\hat{u}^n \hat{i}^p}{2} \cos\left(\phi_u^n - \phi_i^p - \frac{\pi}{3}\right) + \underbrace{\frac{\hat{u}^p \hat{i}^p}{2} \cos\phi_i^p + \frac{\hat{u}^n \hat{i}^n}{2} \cos\left(\phi_u^n - \phi_i^n\right)}_{\overline{P}_{3br}} \tag{3.45}$$

$$P_{br}^{bc} = \frac{\sqrt{3}}{2} \hat{u}^p \hat{i}_{circ} \cos(\phi_{circ} + \frac{\pi}{2}) + \frac{\sqrt{3}}{2} \hat{u}^n \hat{i}_{circ} \cos(\phi_{circ} - \phi_u^n - \frac{\pi}{2}) + \frac{\hat{u}^p \hat{i}^n}{2} \cos\left(\phi_i^n + \pi\right)$$
$$+ \frac{\hat{u}^n \hat{i}^p}{2} \cos\left(\phi_u^n - \phi_i^p + \pi\right) + \underbrace{\frac{\hat{u}^p \hat{i}^p}{2} \cos\phi_i^p + \frac{\hat{u}^n \hat{i}^n}{2} \cos\left(\phi_u^n - \phi_i^n\right)}_{\overline{P}_{3br}} \tag{3.46}$$

Again, the following system has to be solved in order to obtain the reference value for the injected circulating current component:

$$\begin{cases} \underbrace{P_{br}^{ab*} - \overline{P}_{3br} - \alpha_{1D}}_{\Delta P_{br}^{ab}} = \hat{i}_{circ}\alpha_{2D} \cos\phi_{circ} + \hat{i}_{circ}\alpha_{3D} \sin\phi_{circ} \\ \underbrace{P_{br}^{bc*} - \overline{P}_{3br} - \beta_{1D}}_{\Delta P_{br}^{bc}} = \hat{i}_{circ}\beta_{2D} \cos\phi_{circ} + \hat{i}_{circ}\beta_{3D} \sin\phi_{circ} \end{cases} \tag{3.47}$$

where the coefficients α_{1D-3D} and β_{1D-3D} are given at the bottom of the page. The solution to the system is obtained as

$$\phi_{circ} = \arctan\left(\frac{\Delta P_{br}^{ab}\beta_{2D} - \Delta P_{br}^{bc}\alpha_{2D}}{\Delta P_{br}^{bc}\alpha_{3D} - \Delta P_{br}^{ab}\beta_{3D}}\right), \quad \hat{i}_{circ} = \frac{\Delta P_{br}^{ab}}{\alpha_{2D} \cos\phi_{circ} + \alpha_{3D} \sin\phi_{circ}} \tag{3.48}$$

$$\alpha_{1D} = \frac{\hat{u}^p \hat{i}^n}{2} \cos\left(\phi_i^n - \frac{\pi}{3}\right) + \frac{\hat{u}^n \hat{i}^p}{2} \cos\left(\phi_u^n - \phi_i^p - \frac{\pi}{3}\right), \quad \alpha_{2D} = \frac{3}{4}\hat{u}^p + \frac{\sqrt{3}}{2}\hat{u}^n \cos\left(\phi_u^n - \frac{\pi}{6}\right),$$

$$\alpha_{3D} = \frac{\sqrt{3}}{4}\hat{u}^p + \frac{\sqrt{3}}{2}\hat{u}^n \sin\left(\phi_u^n - \frac{\pi}{6}\right)$$

$$\beta_{1D} = \frac{\hat{u}^p \hat{i}^n}{2} \cos\left(\phi_i^n + \pi\right) + \frac{\hat{u}^n \hat{i}^p}{2} \cos\left(\phi_u^n - \phi_i^p + \pi\right), \quad \beta_{2D} = -\frac{\sqrt{3}}{2}\hat{u}^n \sin\phi_u^n,$$

$$\beta_{3D} = -\frac{\sqrt{3}}{2}\hat{u}^p + \frac{\sqrt{3}}{2}\hat{u}^n \cos\phi_u^n$$

In the case where only balanced voltages and currents exist, the solution can be simplified to

$$\phi_{circ} = -\text{arccot} \left[\frac{2\Delta P_{br}^{ab}/\Delta P_{br}^{bc} + 1}{\sqrt{3}} \right], \quad \hat{i}_{circ} = \frac{2\Delta P_{br}^{ab}}{\sqrt{3}\hat{u}^p \cos\left(\phi_{circ} - \frac{\pi}{6}\right)} \tag{3.49}$$

Limitations on SoC Controller Gain Selection

In the case of the delta-connected CHB converter storage unit, it is the maximum semiconductor current rating i_{br}^{dim} which limits the amount of injected circulating current for individual branch power control. Following the same procedure as in the star-connected case, the respective constraint is obtained as

$$i_{br}^{dim} \geq \frac{\hat{i}^p}{\sqrt{3}} + i_{circ}^{max} \Leftrightarrow i_{circ}^{max} \leq i_{br}^{dim} - \frac{\hat{i}^p}{\sqrt{3}} \overset{(3.49)}{\Leftrightarrow} \frac{2\Delta P_{br}^{max}}{\sqrt{3}u_g^{max}\cos\left(y - \frac{\pi}{6}\right)} \leq i_{br}^{dim} - \frac{\hat{i}^p}{\sqrt{3}}$$

$$\overset{(3.38)}{\Leftrightarrow} \frac{2NE_{bat,n}^{mod}\Delta SoC_{br}^{max}\ln 9}{100 \cdot t_{r,D}^{br}} \leq \left(\sqrt{3}i_{br}^{dim} - \hat{i}^p\right)u_g^{max}\cos\left(y - \frac{\pi}{6}\right), \tag{3.50}$$

where in this case $y = -\text{arccot} \left[\dfrac{2\left(\frac{\Delta SoC_{br}^{k,max}}{\Delta SoC_{br}^{k+1}}\right)+1}{\sqrt{3}} \right]$.

With a similar approach as in the star-connected case, i.e. considering this time that the opposite values of the maximum SoC unbalances are shared between the consecutive branches ab and bc, the worst case value for y can be found as $-\text{arccot}\left(-1/\sqrt{3}\right) = \pi/3$. The latter finally leads to the definition of a minimum rise time $t_{r,D}^{br}$ of

$$t_{r,D}^{br} \geq \frac{4NE_{bat,n}^{sm}\Delta SoC_{br}^{max}\ln 9}{100\sqrt{3}u_g^{max}\left(\sqrt{3}i_{dim}^{br} - \hat{i}^p\right)} \tag{3.51}$$

As far as the submodule SoC balancing loop is concerned, it is not affected by the injection of the circulating current component. Hence, the minimum rise time is given as in the star-connected case,

$$t_{r,D}^{sm} \geq \frac{NE_{bat,n}^{sm}\Delta SoC_{sm}^{max}u_{br}^{max}\ln 9}{P_{br}\left(NU_{sm}^{min} - u_{br}^{max}\right)100} = \frac{NE_{bat,n}^{mod}\Delta SoC_{sm}^{max}u_{br}^{max}\ln 9}{P_{br}\left[N\left(1 - k_u\right)\overline{U}_{sm} - u_{br}^{max}\right]100} \tag{3.52}$$

Relation (3.42) is therefore valid for the rise time of the delta-configured storage unit as well. The different lies in the fact that u_{br}^{max} does not contain any common-mode voltage component for balancing purposes. However, the coupling between the two loops still exists due to the circulating current injection, which changes P_{br}^k/N among the three

branches. Once again, it is mentioned that the established limitations can be utilized for an adaptive gain calculation in cases of operating point changes, identically to the star-connected case.

3.3.3   Overall CHB-BESS Control System

By combining all the aforementioned concepts, the overall control block diagram of the CHB-BESS unit is given in Figure 3.14 together with all associated feedback variables and control signals. The blocks included in the dashed rectangles are executed either in the case of star- or delta-configured CHB converters.

The grid voltages u_{gk} and branch currents i_k are measured and used for the synchronization with the three-phase grid as well as vector current control in a rotating reference frame [122]. In the cases, where grid asymmetries are considered, a second identical current control loop is implemented for the negative sequence. The latter is done in conjunction with a proper algorithm for the symmetrical component identification and the synchronization with the three-phase asymmetric grid, such as the DDSRF-based PLL [123].

The control of the converter inner quantities is then split in two sub-problems, the voltage and power control. The former is handled by the dedicated cascaded outer voltage/inner current controllers for each indirect active interface. The power control is handled by the CHB converter submodule control through the different controllers that run in parallel or in cascade. The only communication requirement between the submodule and the IAI controllers comes through the feed-forward signals P^{ki*}, which are optional and are placed for quicker submodule voltage control during transients.

As it will be seen in the next section, the individual power control quantities ΔP_{sm}^{ki} and ΔP_{br}^k can either be used in open-loop or be fed by the external SoC controllers, according to the operation mode. The latter is based on the estimation of all battery SoC values, while performing the necessary calculations based on (3.36) and (3.37). Then, the proportional control actions based on Figure 3.10a and 3.10b give the necessary power control variables. The latter are then translated into either a necessary common-mode voltage (star unit) or circulating current (delta unit) components. For the star-connected CHB-BESS, the magnitude u_{cm}^* can be directly added to the branch voltage references, which are the result of the grid current control action. In the case of the delta-connected CHB-BESS, an additional proportional controller is sufficient to calculate the required amount (again denoted as u_{cm}^*) to be added to the modulation references for an effective circulating current injection. Finally, (3.25) is used on a submodule control level in order to change the global branch modulation reference according to the individual power demand (either in open-loop or in SoC balancing mode).
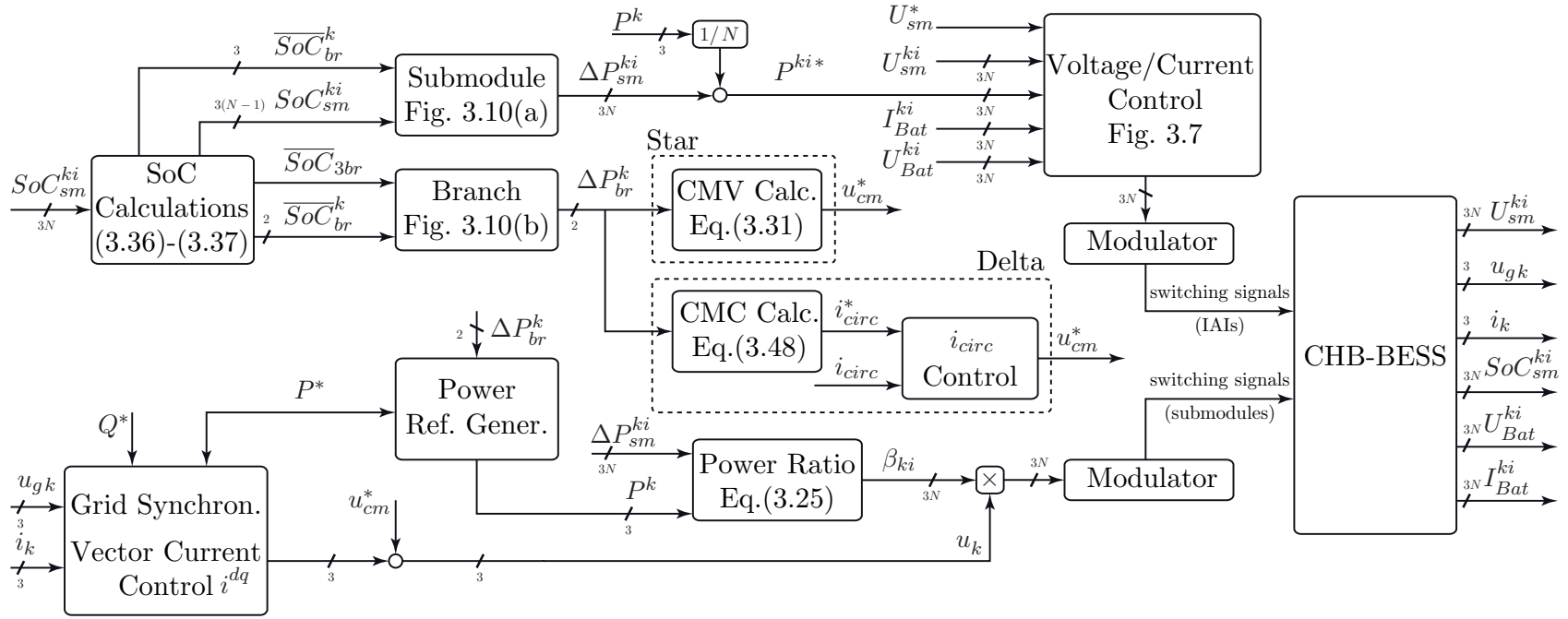
Figure 3.14: Overall system control block diagram for three-phase Cascaded H-Bridge converters with integrated split battery energy storage.

3.4   Modes of Operation and Performance Evaluation

Several modes of operation can be adopted for the CHB-based storage unit. This section describes the latter and presents simulation results for the performance evaluation of the described balancing concepts. The main parameters of the simulated converter are given in Table 3.2, according to an implemented down-scaled laboratory prototype.

Table 3.2: CHB-BESS Simulation/Down-Scaled Prototype Parameters

Quantity	Value	Comment
S_n	4.2 kVA	Nominal apparent power per branch
u_g	230 V	Grid rms phase voltage
N	8	Submodule number
C_{sm}	2.3 mF	Submodule capacitance
L_f	1 mH /140 μH	IAI filter inductance (simulation/experiment)
$U_{bat,n}^{sm}$	25.6 V	Nominal submodule battery voltage
$Q_{bat,n}^{sm}$	1.5 Ah	Nominal submodule battery capacity
$\overline{U}_{sm}$	50 V, 90 V	Average submodule voltage (star, delta)

3.4.1   Independent Load Feeding

The first operating mode regards an independent load feeding on the level of each submodule floating bus. An example where such a case might be needed regards the proposed ultra-fast charging station converter architecture that will be discussed in Chapter 5.

In this mode, the references for the converter branch and submodule powers ΔP_{br}^k and ΔP_{sm}^{ki} are fed in an open-loop fashion to the calculator of the common-mode voltage or circulating current for the cases of star and delta converter configurations, respectively. Therefore, the state of charge balancing controllers in Figure 3.14 are disabled. The results of such an asymmetric branch and submodule active power consumption are shown in Figure 3.15 for the star-connected CHB. The submodule capacitor voltages are controlled to the same mean value by the DC/DC converters, and the ripple varies according to the current demand. Each branch absorbs a different amount of active power, however, the three-phase currents are perfectly symmetric. For this test, the grid voltages have been considered balanced and the reactive power reference has been set to zero (unity power factor).

Similarly, Figure 3.16 illustrates the respective results of the delta-configured CHB converter. In this case, it is the branch currents that are not symmetric due to the circulating current injection for independent branch power control. However, the grid currents feature only a positive sequence component. The results in the two cases are identical, except from the fact that the capacitor voltages are controlled to a higher

average value, due to their need of blocking the whole line-to-line voltage. Therefore, the branch currents have smaller amplitudes to achieve the same amount of branch active power.

It is noted that the independent load feeding mode can be also used in conjunction with the state of charge balancing mode, as it will be seen in the context of the work described later in Chapter 5.
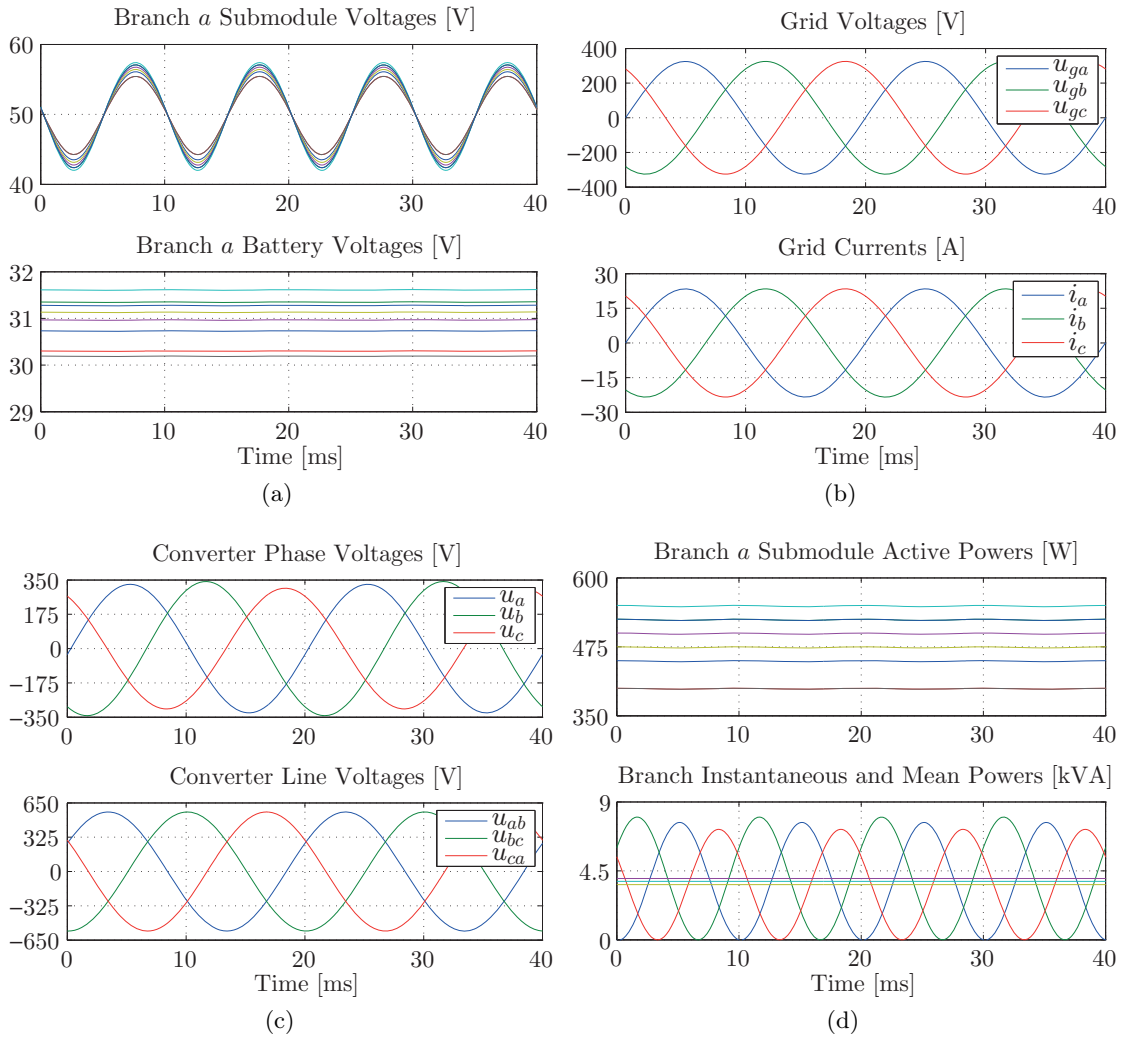
Figure 3.15: Simulation results of the individual submodule and branch battery charging mode for the star-connected CHB case: (a) Voltages on the submodule capacitors and batteries of branch a, (b) three-phase grid voltages and respective currents, (c) converter branch-to-neutral and branch-to-branch voltages, and (d) branch a submodule individual active powers and three-branch instantaneous and mean powers.
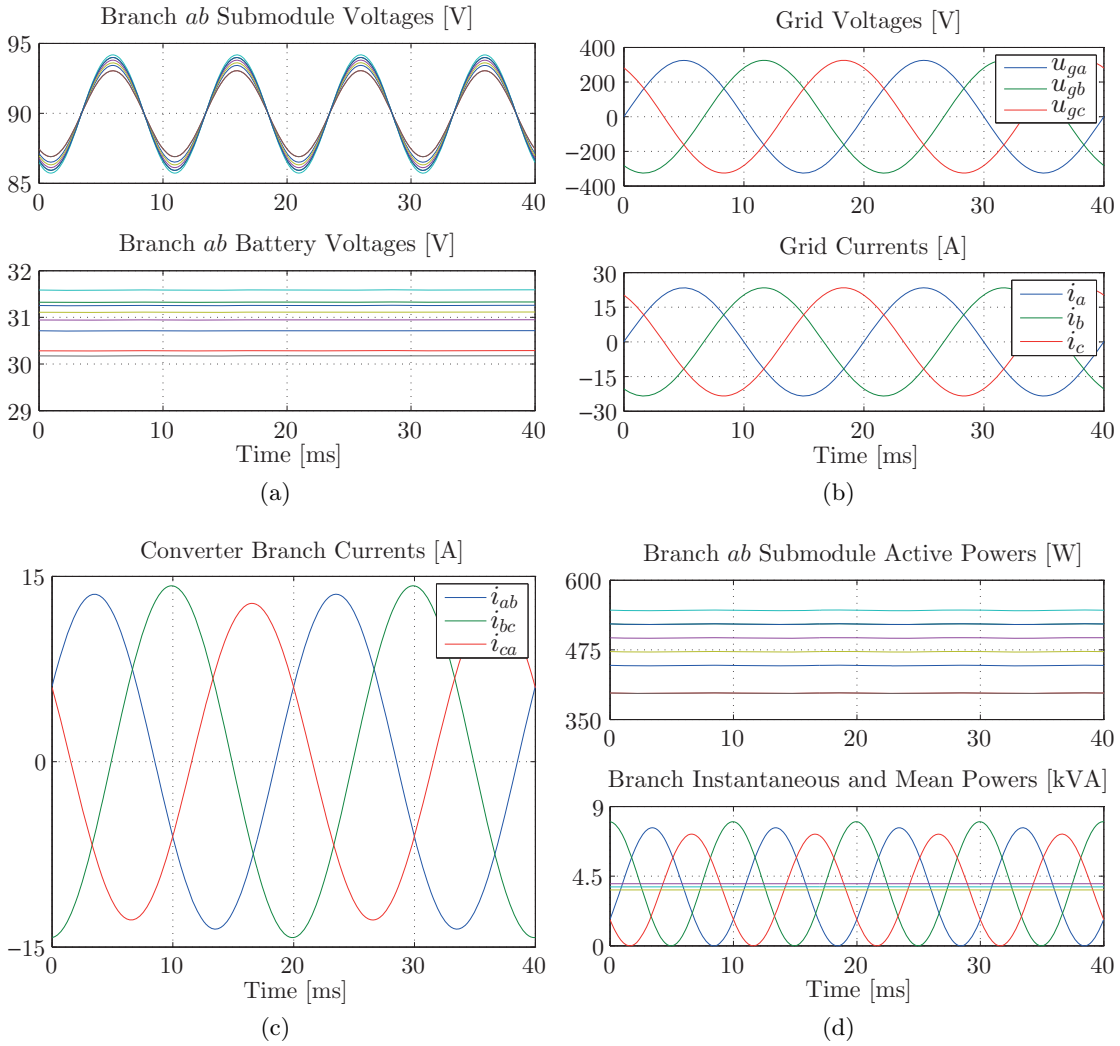
Figure 3.16: Simulation results of the individual submodule and branch battery charging mode for the delta-connected CHB case: (a) Voltages on the submodule capacitor and batteries of branch *ab*, (b) three-phase grid voltages and respective currents, (c) converter branch currents, and (d) branch *ab* submodule individual active powers and three-branch instantaneous and mean powers.

3.4.2 State of Charge Balancing

The second mode of operation regards the balancing action targeting on the battery State of Charges, which has been described in the previous section. In such a scenario, the proportional closed-loop controllers of Figure 3.14 are enabled and provide in turn the respective power references. The results of this simulation are shown in Figure 3.17 for the star-configured CHB-BESS case. All battery packs have been initialized with an arbitrary SoC. The convergence of the branch and submodule battery SoCs is clear throughout the consecutive charging and discharging operations of the storage unit. The

common-mode voltage is also fading out as the branch SoC deviation from the mean value tends asymptotically to zero. The unequal power distribution to the batteries for balancing purposes is clearly depicted on the battery currents. The branch SoC control has been clearly designed to be faster than the submodule balancing one, as explained in the previous section. Finally, the maximum common-mode voltage for the star case reaches the value of 35 V, which corresponds to almost 10% increase in the required branch blocking voltage.
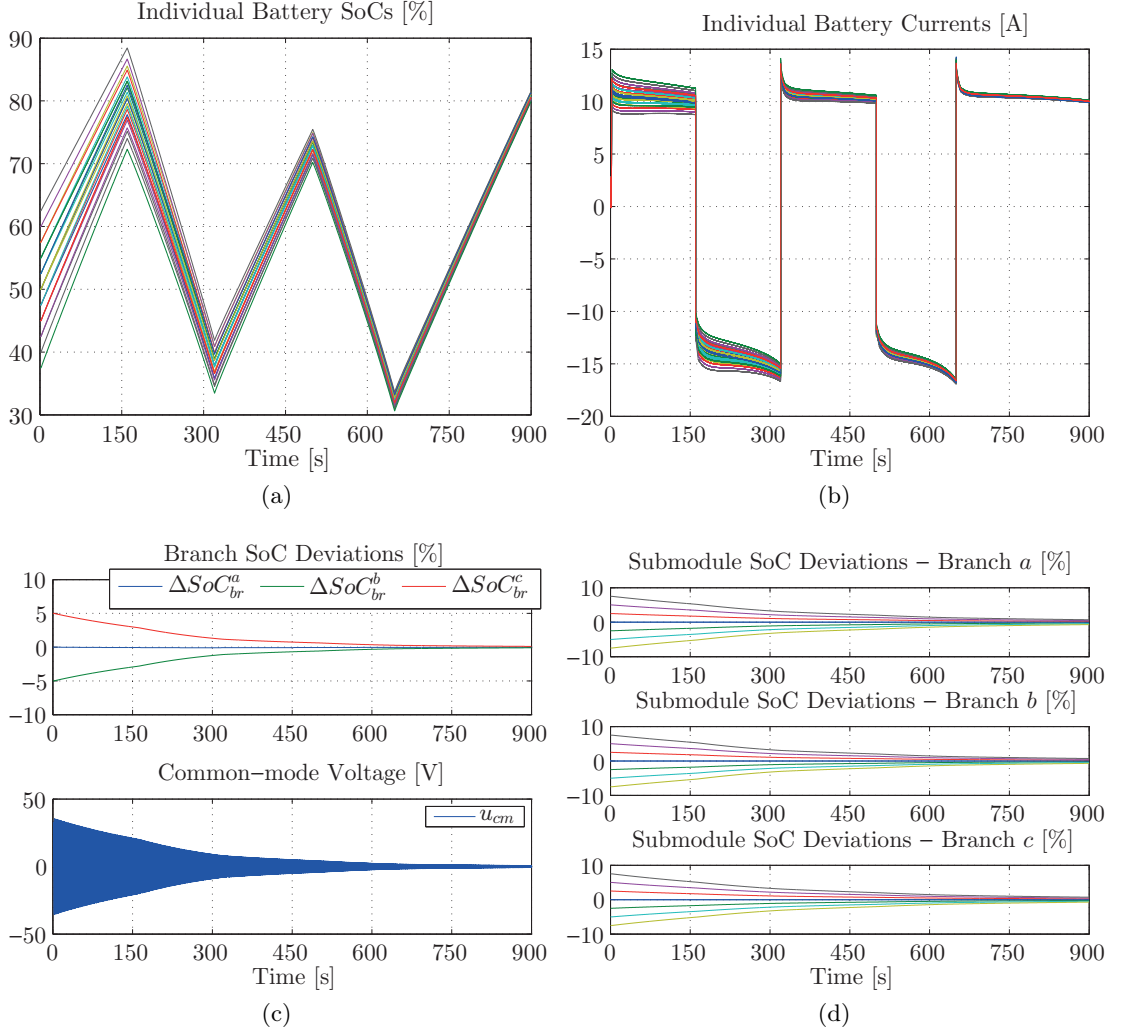
Figure 3.17: Simulation results for the star-configured storage unit: (a) Individual battery State of Charges and (b) respective battery currents during SoC balancing action, (c), (d) time-domain convergence of the submodule and branch SoC balancing regulators.

It is once again noted that in the presented concept of voltage control through the DC/DC conversion stage, the average submodule voltages can be kept constant throughout the whole balancing operation. This is an advantage over proposed concepts of direct submodule-battery interface [66,67] or even the presented DPI and API interfacing

methods. The latter imply an inevitable submodule voltage dependence on the battery State of Charge, which may lead to significant variations according to the utilized electrochemical technology.
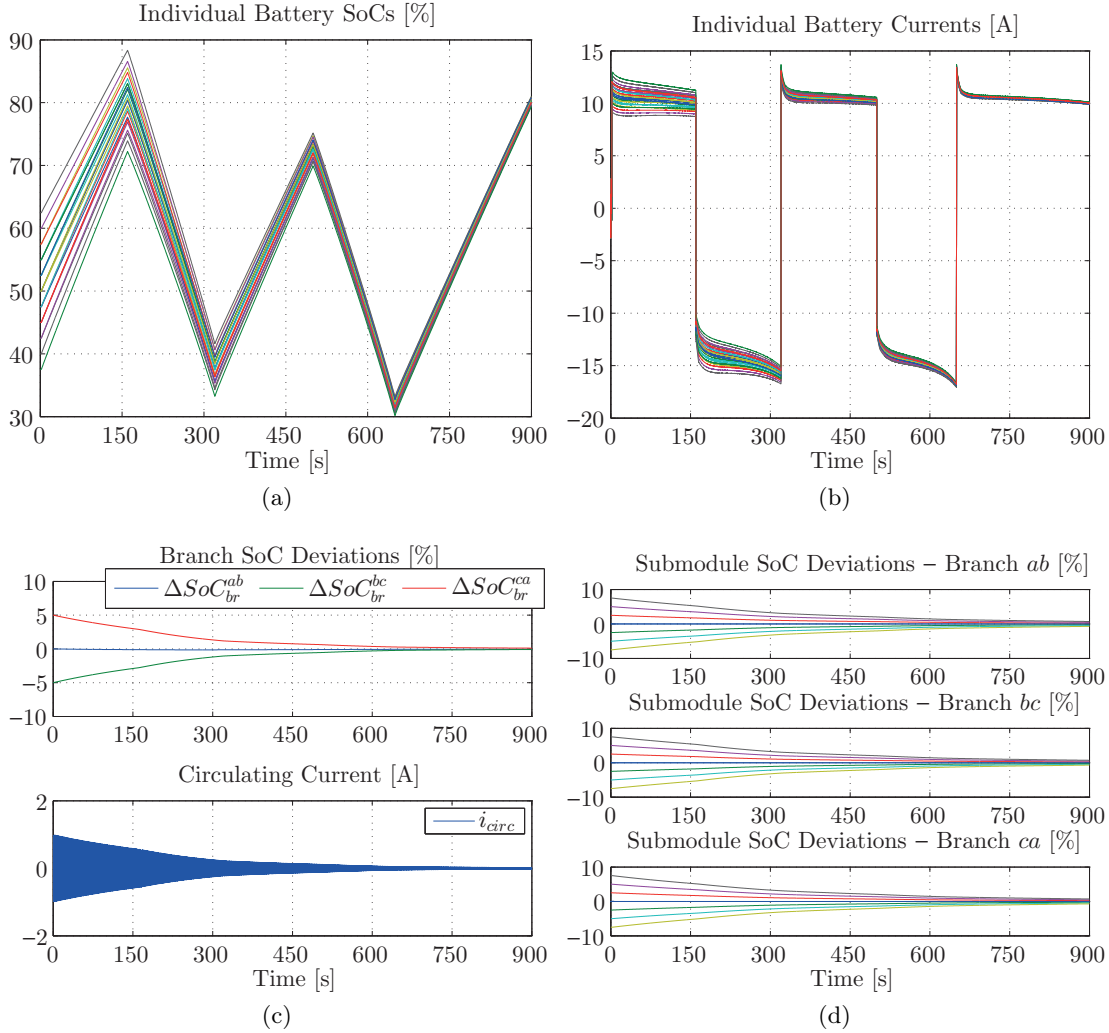
Figure 3.18: Simulation results for the delta-configured storage unit: (a) Individual battery State of Charges and (b) respective battery currents during converter balancing action, (c), (d) time-domain convergence of the submodule and branch State of Charge balancing regulators.

The same State of Charge balancing scenario has been applied for the CHB-BESS converter in delta configuration as well. The results are depicted in Figure 3.18. From a control point of view, the results are identical to the ones of Figure 3.17. This proves the validity of the control concept application on the delta-connected converter. The main difference is that in this case, the branch SoC deviations converge to the mean value due to a circulating current injection, contrary to the common-mode voltage in the star-connected converter. The maximum amount of injected circulating current reaches the value of

almost 1 A, which again corresponds to roughly a 10% of increase in the branch current rating. This is identical to the common-mode voltage injection case and proves once again the duality between the two converter configurations.

3.4.3   Operation under Grid Unbalances

As in any grid-connected converter case, the CHB-BESS unit is very likely to experience grid unbalances. This operating mode has been also considered for both converter configurations. In such a case, the control target is to keep symmetrical currents on the grid side, while achieving a constant power flow throughout the three different converter branches. In this way, the batteries will be always fed with the same currents and no SoC unbalances will occur due to the grid asymmetry.
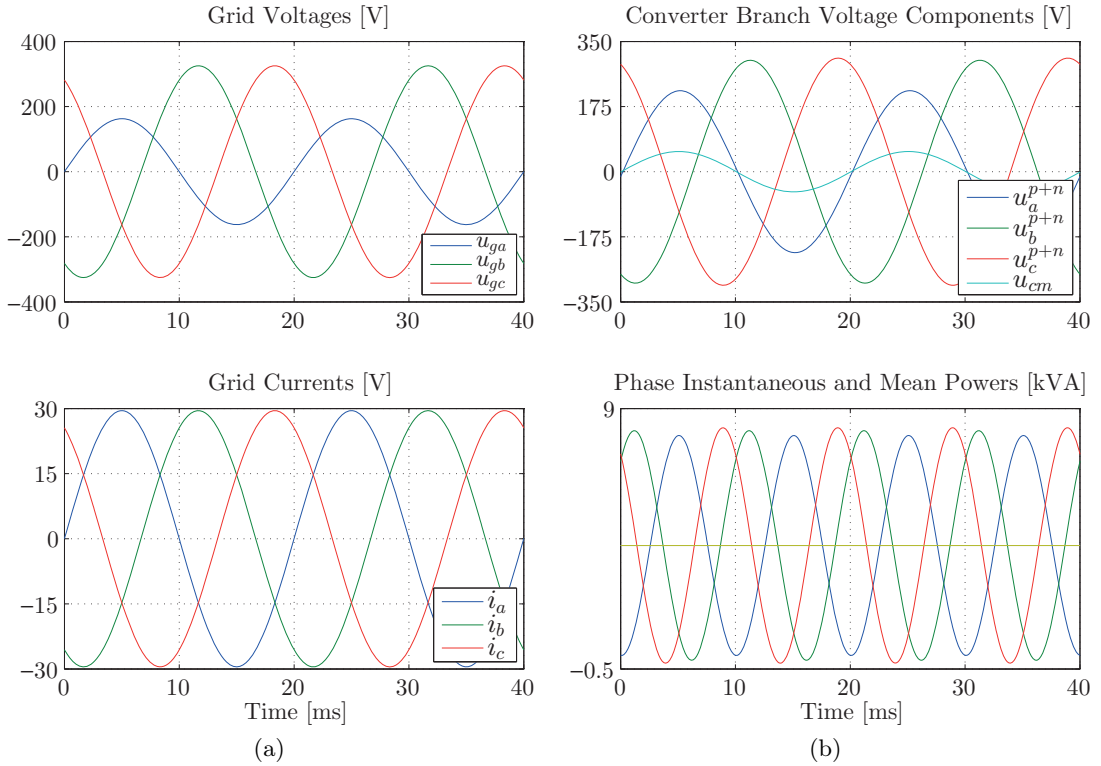
Figure 3.19: Simulation results from a battery charging mode under unbalanced grid conditions for the star-connected storage unit: (a) Three-phase grid voltages and respective currents (b), three-phase converter voltage components and instantaneous absorbed powers with their respective mean values.

In order to maintain three-phase balanced grid currents, the reference of the negative sequence current control loop is set to zero. The results for such an operation mode are illustrated in Figure 3.19 for the star-connected CHB-BESS unit. A phase-to-ground fault in phase a has been simulated. This results in unbalanced grid voltages. However

and due to the negative sequence current control, the three-phase currents comprise only positive-sequence components. This means that each phase cannot absorb the same power. Figure 3.19b shows that an appropriate choice of a common-mode voltage component u_{cm} in the star-connected case results in three-phase instantaneous powers that have the same mean value for the three branches. The solutions for the injected voltage component come from (3.31), where all positive and negative sequence components of the converter voltage are considered.

In order to verify the validity of (3.48) consisting of symmetrical components, the same operation test under unbalanced grid conditions has been performed for the delta-configured converter as well. Figure 3.20 shows the respective results with the ones already depicted in Figure 3.19. Once again, the system controllers are able to inject only positive sequence currents to the grid during a phase-to-ground fault, while the circulating current injection within the converter branches ensures an equal power flow to the batteries, having no consequence on the load demand.
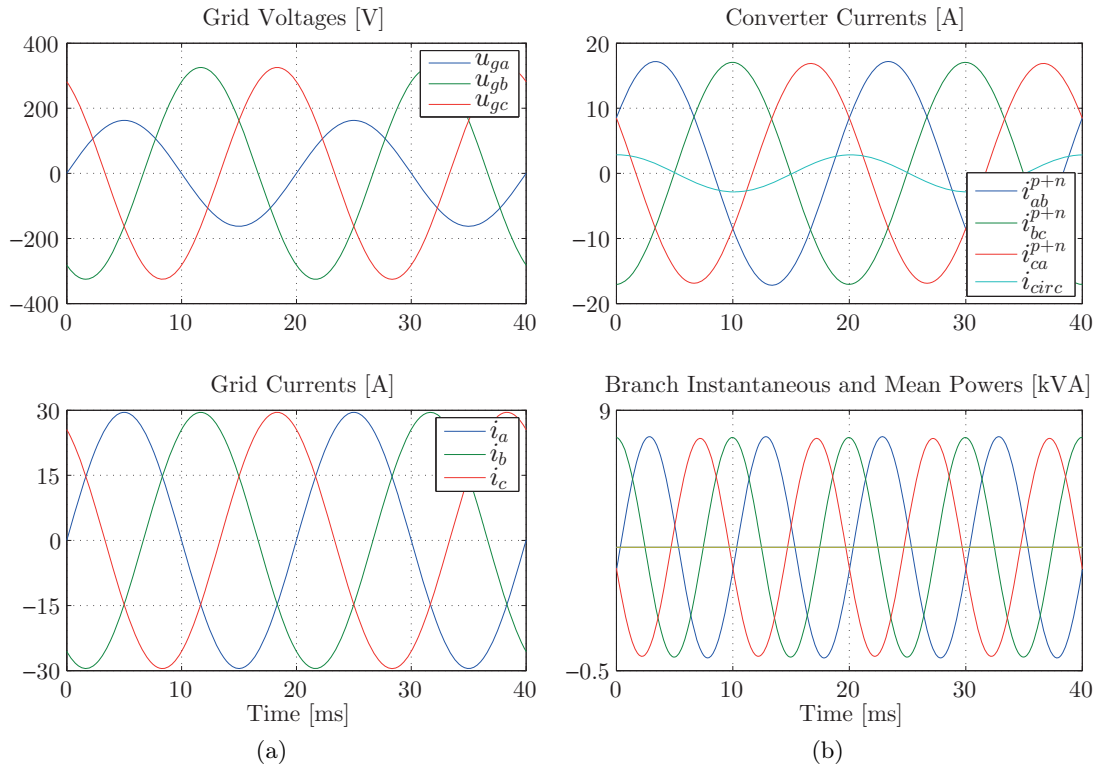
Figure 3.20: Simulation results from a battery charging mode under unbalanced grid conditions for the delta-connected storage unit: (a) Three-phase grid voltages and respective currents (b), three-phase converter current components and instantaneous absorbed powers with their respective mean values.

Individual Battery SoCs [%]

Individual Battery Currents [A]

Submodule SoC Deviations [%]

Branch SoC Deviations [%]

Circulating Current
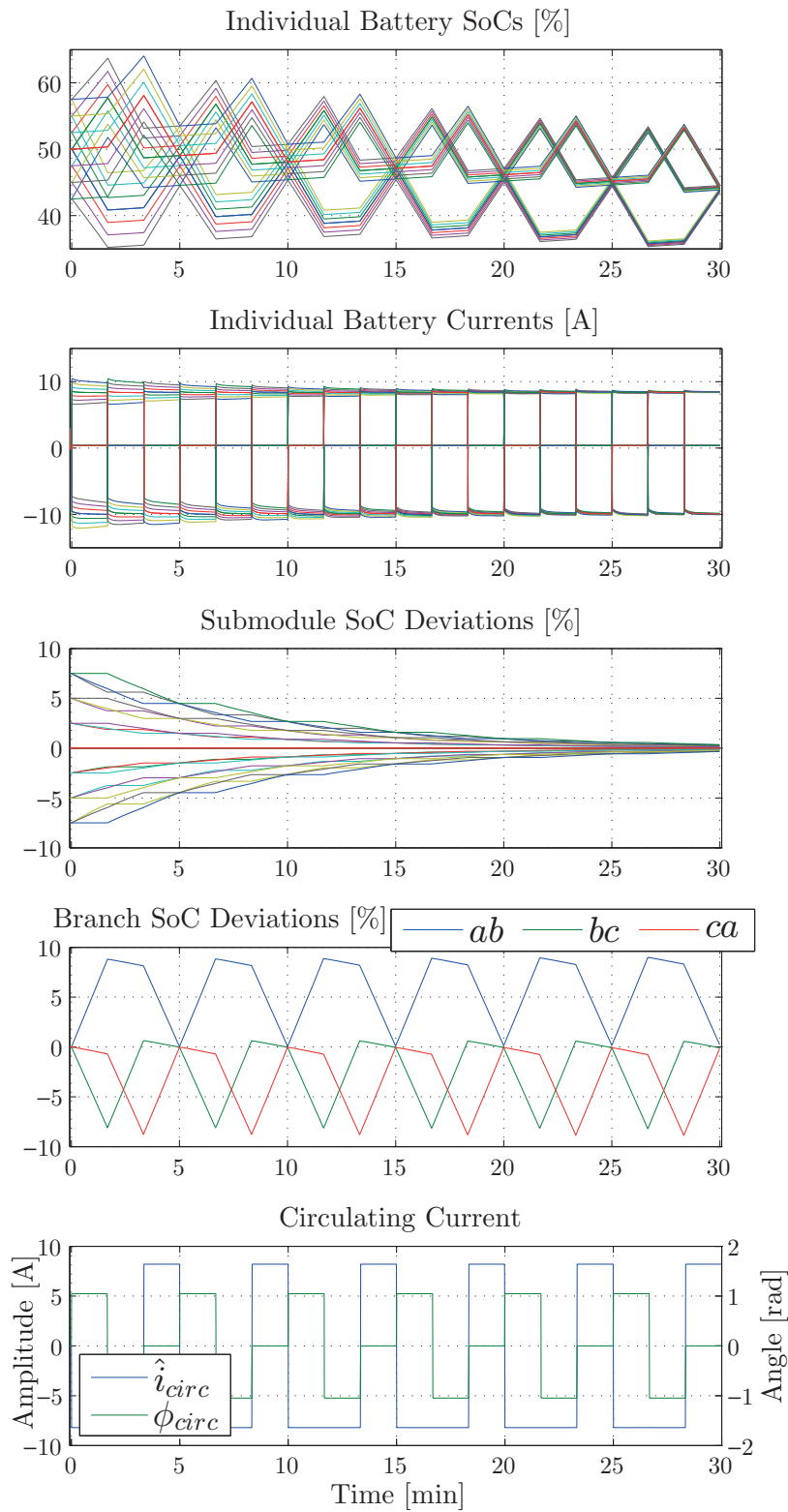
Figure 3.21: Time domain behavior of the delta-connected CHB converter in SoC self-balancing operation.

3.4.4   Self-Balancing Operation of the Delta-Configured CHB-BESS

The delta-configured CHB-BESS unit presents an additional attractive feature. Since the circulating current flows among the three connected branches, it can be used to balance the intermediate SoCs without affecting the grid currents and therefore the grid power. This leads to an additional operation mode, namely the self-balancing operation. Such an action is not possible in the star-connected CHB, where even if a common-mode voltage u_{cm} is imposed, a grid current is also needed to create the necessary three-branch flowing power.

The simulation results for the self-balancing operation of the delta-connected CHB-BESS are given in Figure 3.21. The circulating current injection is defined such as to sequentially discharge one branch and use the resulting power to charge its adjacent. At the end of the self-balancing mode, the submodule SoC deviations are converging to zero. It is noted that since only two branches are used at any time instant, this creates a periodical unbalance at the branch SoC values. The latter does not cause problems if the specified time intervals are always the same and are executed in a perfectly circular manner. This is also verified in Figure 3.21, where the branch SoC deviation value is zero at the end of this thirty-minute operating mode. For this test, the nominal submodule battery capacity has been set to $Q_{bat,b}^{sm} = 3$ Ah and the injected branch balancing active power is 2 kW.
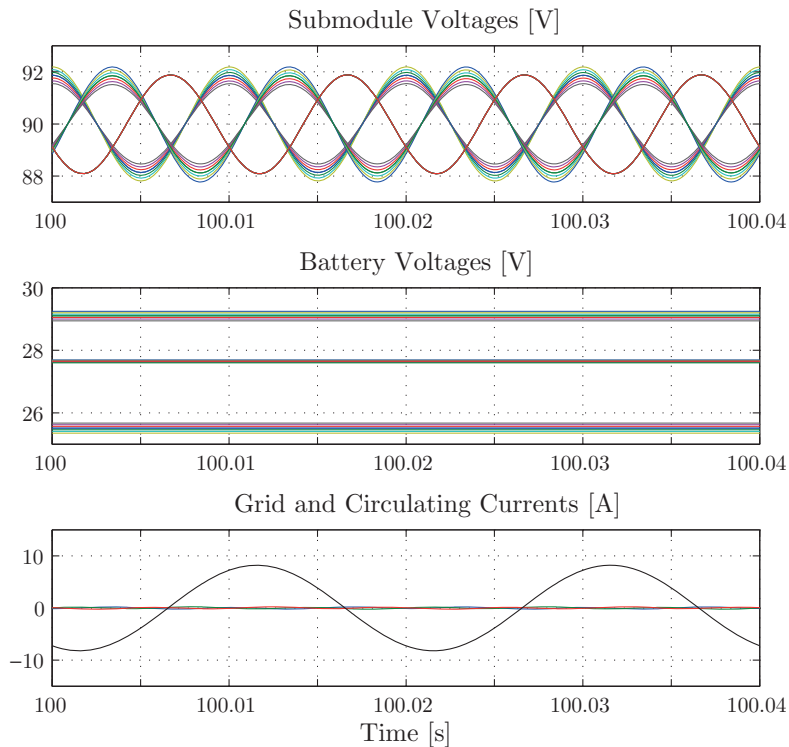
Figure 3.22: Detail of delta-connected CHB converter magnitudes during a discharge of branch *ab* and charging of branch *bc* in SoC self-balancing operation.

A detail of the inner converter magnitudes is given in Figure 3.22. During this time interval, branch *ab* is discharging into *bc*, whereas branch *ca* does not absorb or inject any power. The vertical SoC balancing controllers are in action, leading to a different submodule power values reflected in the different submodule capacitor voltage ripples. The battery voltages are significantly different due to their SoC variations, but the mean submodule voltages are the same. Finally, only a circulating current exists flowing among the three branches, since the grid currents are controlled to be zero.

3.5 Experimental Tests

A reduced-scale prototype has been implemented, in order to test experimentally the basic functionalities of the studied system. A single phase-leg of 4 kVA nominal power has been designed and constructed so far, which consists of eight submodules with split battery energy storage systems. The latter is an extension of the prototype presented in Section 2.5. Further details about the design of the main parts and its operation are also given in the Appendix A. This is illustrated in Figure 3.23.
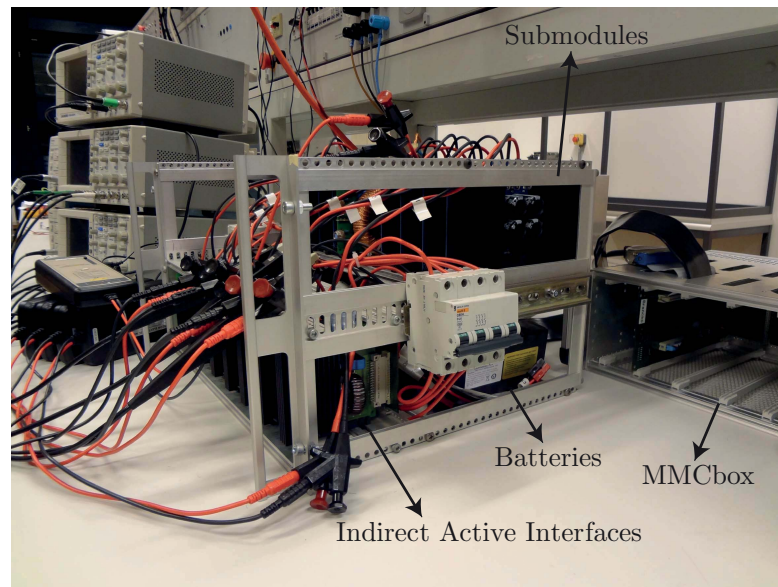
Figure 3.23: The Modular Multilevel Converter phase leg with integrated BESS.

Figure 3.24 shows the results for a split storage stage discharge. The 17-level high-resolution converter waveform leads to a very smooth sinusoidal grid current waveform. Since the measurements are performed through a digital oscilloscope, only the four upper submodule capacitor voltages and split battery currents are depicted because of the channel number limitation. The voltages are very well balanced due to the IAI cascaded voltage/current control. The battery current waveforms coincide as well and contain only the switching-related ripple.
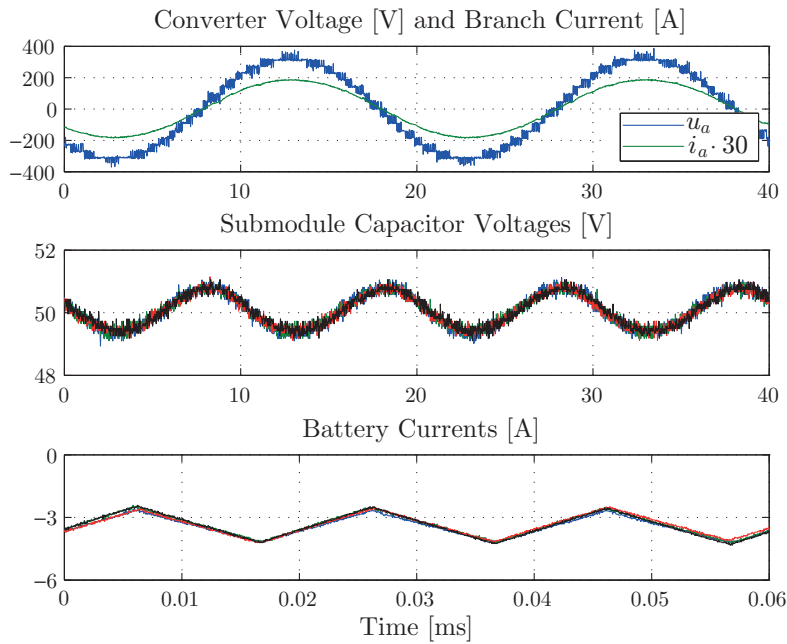
Figure 3.24: Experimental results for a discharging procedure of the batteries.

3.6 Conclusions

This chapter investigated the three-phase Cascaded H-Bridge converter with integrated split battery energy storage in either star or delta configurations. The indirect active interface seems to be a straightforward solution for the integration of storage elements to the converter submodules. The latter offers a practical power decoupling, preventing the single-phase submodule power pulsating elements from flowing into the batteries. In addition, an extra degree of freedom for the control of a global system is at hand due to the existence of actively controlled power electronic devices. Therefore, it has been used for achieving submodule capacitor voltage balancing from the battery side.

By formulating a power control problem rather than a voltage control one, the battery state of charges can be modeled in a straightforward manner as well as controlled in all possible directions of unbalances. It is very important to target directly at the battery SoC, since several battery technologies exhibit flat curve dependency of the voltage in function of the SoC. The designed control loop proportional gains are subject to constraints that concern the safe operation of the converter. The latter have been analytically established.

The most important outcome is the fact that the developed generalized methods can be extended and tailored for the control of any type of Modular Multilevel Converter topology, where a submodule enhancement with energy storage elements is desired. This is shown in the next chapter of this thesis.

4 DC/AC Modular Multilevel Converters with Integrated BESS

4.1 Introduction

Extending the developed concepts of the previous chapter, this chapter performs a similar analysis for the case of the DC/AC Modular Multilevel Converter with integrated split battery energy storage systems. This converter structure features a common DC-link, keeping therefore the properties of an AC/DC converter. The batteries are now enhancing the converter's active power capability, rather than giving it the character of an application-specific storage unit as in the case of the CHB. Applications of such a system include HVDC lines, active front ends for medium voltage drives or railway interties, as well as AC/DC converters coupled on a energy source level, where the batteries will provide load leveling services because of the fluctuating power source nature.

Initially, a brief overview of the submodule-battery interface solutions is given similarly to the previous chapter. Eventually the chosen interface regards the nonisolated DC/DC converter in cascade with the submodule, keeping a consistency with what has been utilized in the CHB case as well. A thorough analysis of the different operating modes that can be encountered in the MMC with integrated split BESS (MMC-BESS) case is performed. Again, the individual power control in all unbalance directions is discussed, namely submodule, phase, as well as the now appearing case of the two branches of the same phase leg. The SoC control problem is also treated and the limitations of the proportional regulator gains are derived analytically. Moreover, the operation of such a storage unit under grid asymmetries is investigated and solutions are offered.

The three-phase Modular Multilevel Converter with integrated BESS is illustrated in Figure 4.1. It comprises three parallel-connected phase legs. Each leg consists of two branches, where the midpoint is connected to the AC side handling an amount of active as well as reactive powers, respectively. Each submodule is equipped with a storage element, which serves as an active power port. This is in contrast with the typical MMC case described in Chapter 2, where the average active power in the capacitors should

equal zero. In addition, the phase legs are connected to a common DC-link, which can be considered as an additional active power flow port in the studied system. In a typical MMC case the submodule is implemented by means of a half-bridge. This implies that each branch cannot provide negative voltages.
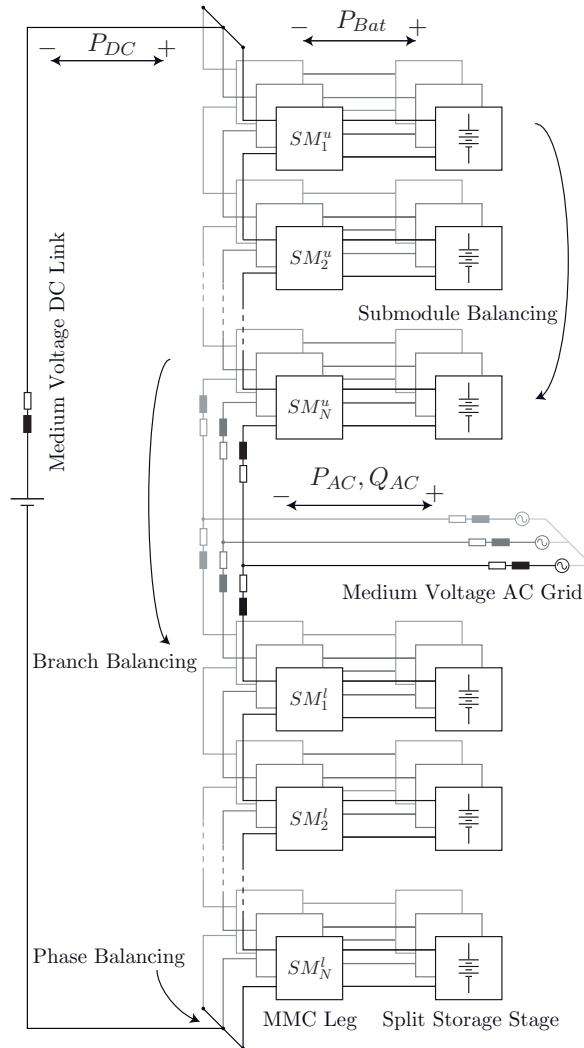
Figure 4.1: Modular Multilevel Converter with integrated battery energy storage elements.

4.2   Overview of Submodule-Battery Interface Solutions

Similarly to the CHB-BESS case described in the previous chapter, the submodule-battery interface impediment arises in the MMC-BESS case as well. Each capacitive phase leg exhibits a single-phase nature. Therefore, low frequency power components have to be buffered within the branch capacitors.

In the CHB-BESS case the submodule current consists of a DC component plus a

superimposed AC component of the grid second-order frequency harmonic, as shown in (3.3). However and as shown in Section 2.3, the MMC submodule dominant buffered frequency is the one of the grid. Moreover, several other frequencies appear in the submodule capacitors, according to whether a third-order common-mode voltage or second-order circulating current harmonic injections take place for modulation index increase or capacitor voltage ripple reduction, respectively.

In any case, the oscillating terms do not contribute to the average battery SoCs and are therefore chosen to be eliminated for the scopes of this work for the reasons that were mentioned in the previous chapter. In the following, the suitability of the CHB-BESS interfacing concepts, previously presented in Section 3.2, is discussed for the MMC-BESS case together with an additional control-based solution.

The DPI, IAI, and API Cases

The indirect active interface as well as the active parallel interface concepts, which have been described in the previous chapter, can be equally applied in the case of the MMC as well. The passive converter elements can be also designed according to the considerations made in Chapters 2 and 3. The main difference lies on the harmonic content of the submodule current in the MMC case, which can bear different components than only a second-order harmonic in the CHB. A proper estimation of the low-frequency submodule current components, such as the one described in Section 2.3, can be used as reference for the current controller in the API case similarly with the CHB-BESS case.

In the case of the DPI, however, the solution of a resonant filter is not straightforward. In contrast with the CHB converter,the MMC branch capacitors comprise their main ripple component at the line frequency. As a result, the branch modules have to buffer fluctuations of 50 Hz in the studied case. In addition, a significant second-harmonic component, making the design of the filtering elements more challenging. As already discussed in Chapter 2, the second-order frequency component can be compensated for through the introduction of suitable circulating currents [12,124], see (2.20). The effective removal of the second-order harmonic component makes it possible to introduce a passive resonant filter as in the case of CHB, which will be tuned at the main line frequency of 50 Hz. The design procedure is the same with the one described in the respective section of Chapter 3. Even in such a case, however, the second-order circulating current injection and a possible third-harmonic common-mode voltage for modulation index increase give rise to power terms of other frequencies as well, which have to be attenuated by the additional low-pass filtering elements making their chosen values inevitably higher.

The existence of the common-mode voltages in conjunction with the circulating currents in an MMC offer an additional submodule-interfacing concept based purely on the choice of converter control. The latter is discussed in the following.

Branch Power Frequency-Shifting (BPFS) in a Modular Multilevel Converter

In [62], a method for operating Modular Multilevel Converters at low output frequencies has been proposed. The main impediment in such a case regards the inversely proportional relation between the line current frequency and the branch capacitor voltage ripple. In order to reduce the large low-order harmonics in the capacitor currents, the branch power can be shifted towards a desired frequency by adding a common-mode voltage and respective circulating current components. A control system for implementing such a method has been shown by the authors of [56].

Normally such an action is employed in the low frequency range, i.e., during the startup phase of a motor drive. In the studied MMC-BESS case, such a mode could be utilized for the fixed grid frequency of 50 Hz as well. By doing so, the capacitor current frequency can be increased, leading to a significant reduction of the passive filtering elements between the submodule and the battery. According to [56] and following the notation utilized in Chapter 2, the higher frequency injected common-mode voltage u_{cm} as well as k-th phase-leg circulating current i_{circ}^k are obtained as

$$u_{cm} = U_{cm} + \hat{u}_{cm}\cos(\omega_{cm}t) \tag{4.1}$$

$$i_{circ}^k = I_{circ0}^k + \hat{i}_{circ}^k\cos(\omega_{cm}t) \tag{4.2}$$

where

$$U_{cm} = -\frac{\hat{u}_V}{4\cos\phi}\cos\left(3\omega t + \phi\right) \tag{4.3}$$

$$I_{circ0}^k = \frac{\varepsilon}{U_S}\left(u_{Vk}i_{Tk} + U_{cm}i_{Tk}\right) \tag{4.4}$$

$$\hat{i}_{circ}^k = \frac{1}{\hat{u}_{cm}}\left(\frac{1}{2}U_S i_{Tk} - 2u_{Vk}I_{circ0}^k - 2U_{cm}I_{circ0}^k\right) \tag{4.5}$$

Compared to [56], the factor ε has been added for the calculation of the continuous circulating current part I_{circ0}^k in (4.4). This factor controls the amount of active power that is distributed between the AC and DC sides as well as the split batteries. It will be explained throughout the next paragraphs.

Figure 4.2 depicts switching-averaged simulation results of such a concept in comparison with a plain DC circulating current control as well as a second-order harmonic injection. Only a lowpass filter of $C_{sm} = 1$ mF and $L_f = 0.5$ mH is utilized, such as the one depicted in Figure 3.2a but without the resonant part. It is clear that without this specific control mode, the battery current will feature severe low-order oscillations due to the intrinsic single-phase system power pulsation. Even if a second-order harmonic is utilized on the circulating current, the passive filter is not capable of adequately attenuating the battery current ripple. In the BPFS mode, however, the injected common-mode voltage

and circulating current components of $\omega_{cm} = 2000\pi$ shift the capacitor current towards around 1 kHz, which can be filtered out easily without the need for large passive elements.
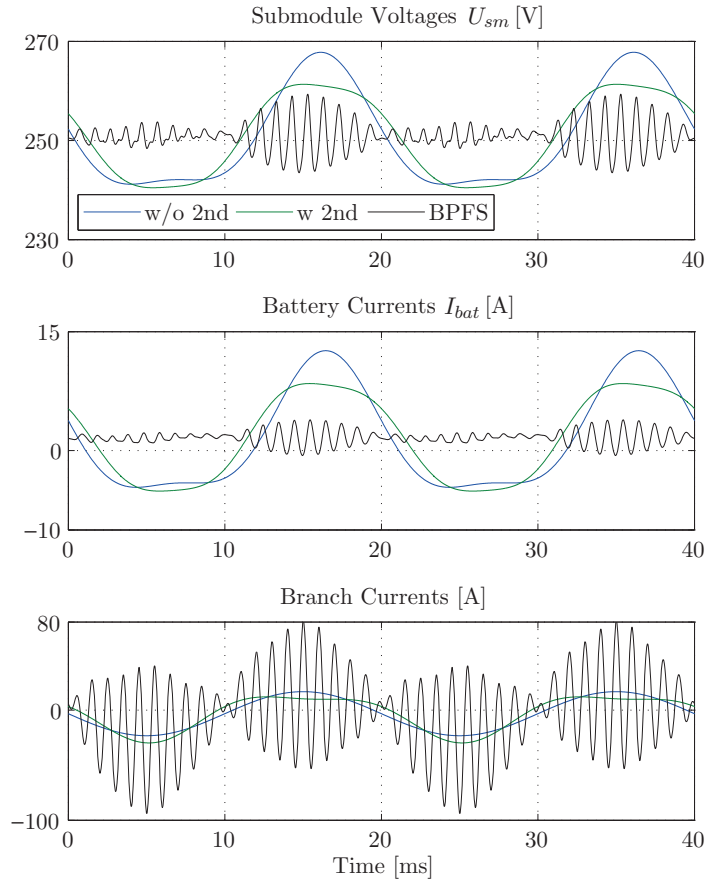
Figure 4.2: Switching-averaged simulation results for a direct submodule-battery interface using only a low-pass filter consisting of C_{sm}, L_f. The plain DC circulating current and the second-order harmonic injection are compared to the branch power frequency-shifting (BPFS) mode (battery charging power of 345 W).

However, this method brings along certain significant disadvantages, which have to be considered. The most important regards the existence of high frequency/amplitude common-mode voltages, something which poses additional insulation requirements on a transformer connection level. Moreover for transformerless approaches, such an action might not be acceptable by the grid standards. A solution would then be to use a common-mode voltage filter, which would also change the line impedances and might possibly not be acceptable by transmission line owners/operators.

From a MMC perspective, another disadvantage concerns the injection of extra high circulating currents inside the converter branches. This leads eventually to an apparent oversizing of the power electronic components. Equation (4.5) reveals that the amplitude of high frequency circulating current is inversely proportional to the chosen common-mode voltage. In fact, such a chosen operation can lead to up four times the necessary

installed switching power than the normal MMC operation [26]. Finally, the effect of very low switching frequency per device is lost, if all the output voltage range is to be used, as each submodule has to switch twice per common-mode voltage period [62]. The circulating current imposed frequency is also limited by the maximum achievable control loop bandwidth.

To conclude, although possible, it is not advisable to use the BPFS method for such a utility application.

Final MMC-BESS Topology Implementation

Similarly to the CHB-BESS case, the IAI is chosen as a power electronics-based active solution for the MMC-BESS as well. The final implementation of the respective blocks of Figure 4.1 is therefore shown in Figure 4.3.

(a) (b)
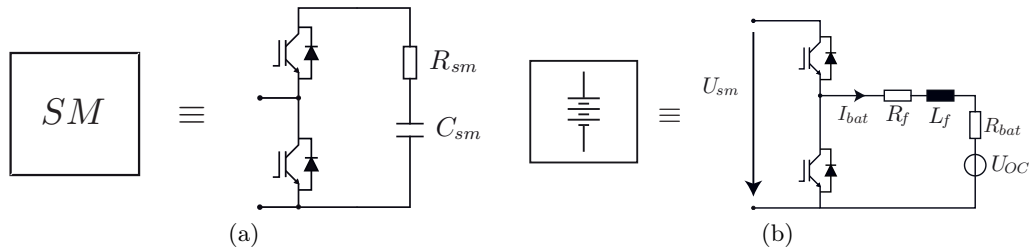
Figure 4.3: Implementation of the (a) MMC submodule and (b) the split storage stage based on the indirect active interface.
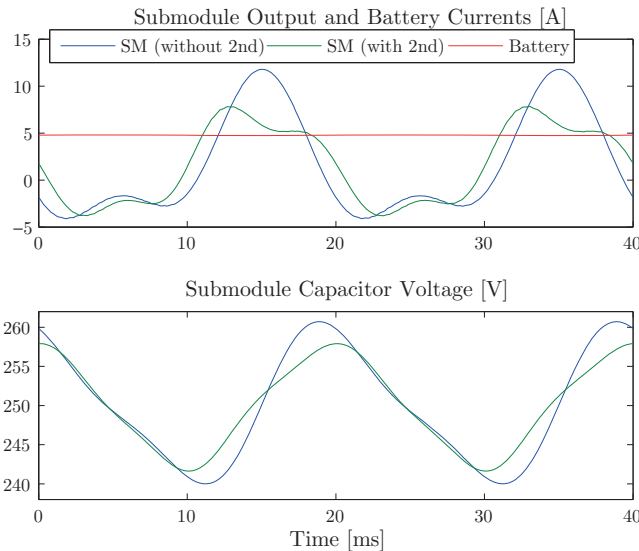
Figure 4.4: Average submodule output and battery currents as well as submodule capacitor voltage with and without second-order harmonic injection in the circulating current for voltage ripple reduction.

The effective power decoupling is illustrated in Figure 4.4. The average submodule output current is depicted together with the respective average battery current, both for the case of pure DC circulating current as well as second-order harmonic injection. The battery current is the same for both cases, even though the harmonic content of the submodule output current is different. The low-frequency power is buffered in the submodule capacitor as in the typical MMC operation highlighted in Chapter 2. The battery current ripple, however, will be limited to the switching harmonics generated by the buck converter, which are now related to the switching frequency, the filter inductance L_f, as well as the output/input voltage ratio.

4.3 Operating Modes of an MMC-BESS

In Figure 4.5, a simplified scheme of one converter leg defining all necessary magnitudes is presented. This is evidently very similar to Figure 2.1a presented in Chapter 2. The common link-related magnitudes are DC quantities and are therefore denoted with capital letters as U_S and I_S, respectively. Similarly to the two previous chapters, the following subscripts/superscripts are also utilized here: $k \in \{a, b, c\}$ referring to the studied phase, $j \in \{u, l\}$ to the upper/lower branches of the same phase-leg, and $i \in \{1, 2, .., N\}$ to the submodules of the respective branch.

Figure 4.5: Multi-phase Modular Multilevel Converter with integrated BESS.

The generalized form of the so-called circulating current on a per phase level is also repeated here as

$$i_{circ}^k = \underbrace{I_{circ0}^k}_{I_S/3} + \sum_{n=1}^{\infty} \hat{i}_{circ,n}^k \cos(n\omega t + \theta_n) \tag{4.6}$$

Assuming that the branch impedances are symmetrical and therefore the line current splits equally between the upper and lower branches of the same phase leg, the branch currents i_j^k are equally defined as

$$i_u^k = \frac{i_{Tk}}{2} + i_{circ}^k, \qquad i_l^k = -\frac{i_{Tk}}{2} + i_{circ}^k \tag{4.7}$$

4.3.1   Submodule Capacitor Voltage Balancing

Similarly to the CHB-BESS case, factors such as losses, practical variations between the submodule capacitances as well as different battery power demands can lead to divergence from the desired submodule capacitor voltages. Therefore, an individual control of these voltages should take place. This problem will be treated as in the CHB-BESS storage unit, i.e., by means of an active voltage control of the indirect active interface between the submodules and the split storage systems. Figure 4.6 illustrates the block diagram of the cascaded outer voltage/inner current control loops, which evidently very similar to the one of Figure 3.7. The only difference lies in the notation, using now the additional superscript j referring to the respective upper or lower branch of the same MMC phase leg.
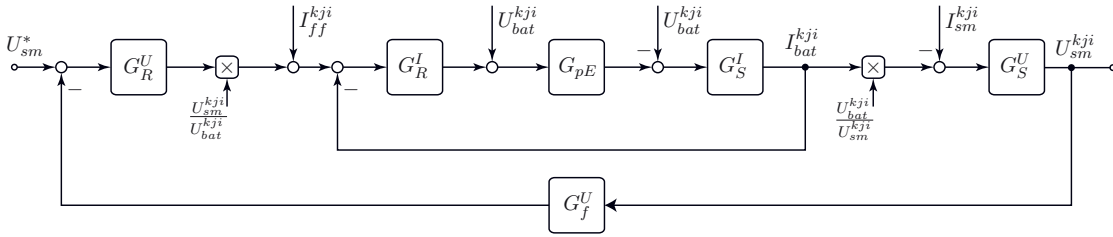
Figure 4.6: Cascaded voltage/current control loop for each of the indirect active interfaces.

The dimensioning procedure of the voltage and current controllers G_S^U and G_S^I is exactly the same with the one described for the CHB-BESS case in Section 3.3. Thus, it will not be repeated here. It is noted that the voltage measurement filter G_f^U in this case has to be tuned at a lower frequency compared to the CHB-BESS due to the line frequency component dominating the capacitor voltage ripple.

4.3.2 Operation Modes

By exploring Figure 4.1, the definition of power flows is at hand. The converter can exchange a specific amount of mean active and reactive power P_{AC} and Q_{AC} with the three-phase grid, respectively. A fraction of the average active power P_{AC} is exchanged with the DC-link P_{DC} and the rest will be exchanged with the three-phase BESS (P_{bat}). Evidently the following relation holds:

$$P_{AC} = P_{DC} - P_{Bat} \tag{4.8}$$

The sign of each power component reveals its direction, considering as positive the one defined by the respective signs of Figure 4.1 or equivalently by the current arrows in Figure 4.5. An explicit decoupled line and circulating current control implies the ability to regulate independently the average DC power from the AC one, as it has been discussed in Chapter 2. By defining as ε the ratio P_{DC}/P_{AC}, (4.8) can be written as

$$P_{AC} = \varepsilon P_{AC} - P_{Bat} \Leftrightarrow P_{Bat} = P_{AC}(\varepsilon - 1) \tag{4.9}$$

Defining the quantities P_{AC}^k, P_{DC}^k and P_{Bat}^k, (4.9) is valid on a per-phase level, accordingly. The DC part of the circulating current I_{circ0}^k cannot be used to charge/discharge the batteries, as it is physically transferred to the DC-link. The latter can be expressed by

$$I_{circ0}^k = \frac{P_{DC}^k}{U_S} = \frac{\varepsilon P_{AC}^k}{U_S} \tag{4.10}$$

The AC part of the branch current, however, multiplied with the branch voltage, transfers the continuous power at the output of the submodules. According to the aforementioned considerations, six different operation modes can be distinguished:

Rectifier Operation ($P_{AC} < 0$):

- Mode I: $P_{AC} = P_{DC} \Rightarrow P_{Bat} = 0$ (idle)

- Mode II: $|P_{AC}| > |P_{DC}| \Rightarrow P_{Bat} > 0$ (charging)

- Mode III: $|P_{AC}| < |P_{DC}| \Rightarrow P_{Bat} < 0$ (discharging)

Inverter Operation ($P_{AC} > 0$):

- Mode IV: $|P_{AC}| < |P_{DC}| \Rightarrow P_{Bat} > 0$ (charging)

- Mode V: $|P_{AC}| > |P_{DC}| \Rightarrow P_{Bat} < 0$ (discharging)

- Mode VI: $P_{AC} = P_{DC} \Rightarrow P_{Bat} = 0$ (idle)

It is noted that due to the considerations made in Chapter 2 for the DC/AC MMC operating under unbalanced grid conditions, the instantaneous DC-link active power can be forced to be equal to the average one even during such asymmetries. Therefore, $p_{DC} = P_{DC}$ can be considered for the three-phase DC/AC MMC-BESS at all times.

In Modes I and VI the storage system is not used at all, which corresponds to a typical MMC case. Figure 4.7 shows the simulation results for the different operation modes of the MMC-BESS unit. The results correspond to a switching-averaged model, where all the closed-loop controllers are in action. The parameters are given in Table 4.1. They resemble the down-scaled laboratory prototype characteristics, with the exception of augmented nominal power which has been used to decrease the rise times of the SoC balancing algorithms explained throughout the next sections. The integrated battery energy storage system behaves according to the load demand and the power flow direction. Therefore, it will charge or discharge, in order to meet the active power balance condition of (4.8). Moreover, it is clear that the average battery current contains a purely continuous component. In addition, the submodule voltage is not affected by the respective variations of the battery voltage. It is noted that the figures depicting the submodule and battery magnitudes consist of 24 waveforms each, which perfectly coincide due to their symmetric operation.

Table 4.1: MMC-BESS Simulation Parameters

Quantity	Value	Comment
S_n	20 kVA	Nominal grid power
$\tilde{u}_T$	230 V	Grid rms phase voltage
N	4	Submodules/branch
$U_{bat,n}^{sm}$	76.8 V	Nominal battery voltage
$Q_{bat,n}^{sm}$	1.5 Ah	Nominal battery capacity
C_{sm}	2.3 mF	Submodule capacitance
U_S	800 V	DC-link voltage
L, R	2.3 mH, 0.2 Ω	Branch inductance/resistance
L_T, R_T	4 mH, 0.5 Ω	Grid inductance/resistance

Up to now, an ideal condition of balanced SoC operation and power consumption between the submodules, branches and phases of the Modular Multilevel Converter was considered. However, different factors can lead to divergence of the battery SoCs, as in the case of the CHB-BESS. Throughout the next sections, the respective balancing control problems will be identified and solved by means of topology-specific degree of freedom exploitation.
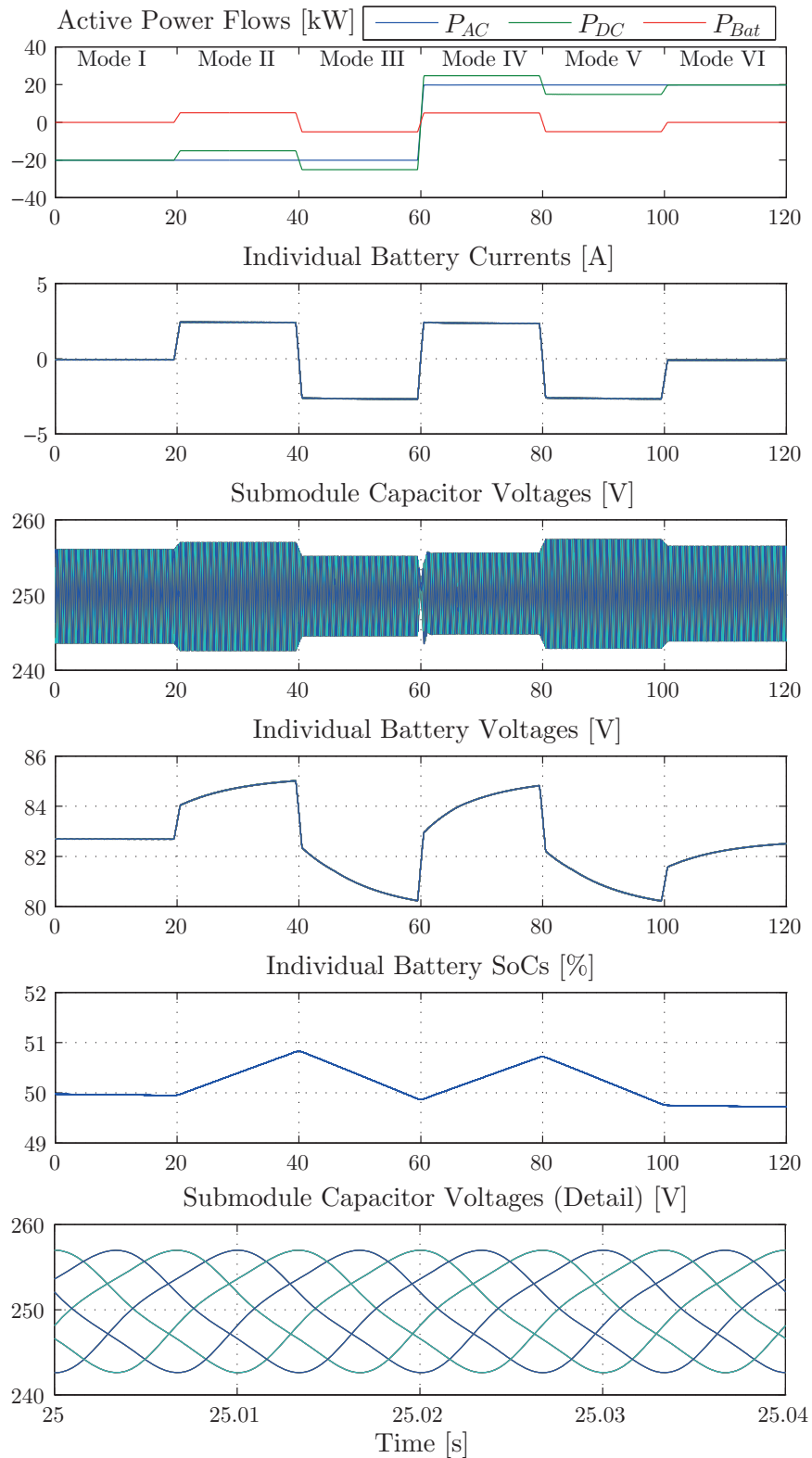
Figure 4.7: Simulation results of an MMC-BESS unit for a hypothetical power profile, exploiting all possible operation modes.

4.4 Individual Power Control

The individual power control problem is similar to the CHB-BESS problem with the exception of the third unbalance direction between the branches of the same phase leg. The common points are briefly rediscussed for the sake of completeness.

4.4.1 Submodule Power Control

The term individual submodule power control once again refers to the capability of absorbing or injecting different amounts of active power between the submodules of a converter branch. Similarly to Figure 3.8, the equivalent circuit of one MMC branch is now illustrated in Figure 4.8. An adaptation of the modulation reference for each submodule by the factor β_{kji} allows different amounts of absorbed or injected power by each DC side:

$$\beta_{kji} = \frac{\overline{U}_{sm}^{kji}\overline{I}_{sm}^{kji}}{\sum\limits_{i=1}^{N} \overline{U}_{sm}^{kji}\overline{I}_{sm}^{kji}} = \frac{P_{sm}^{kji}}{\sum\limits_{i=1}^{N} P_{sm}^{kji}} \quad \text{with} \quad \sum\limits_{i=1}^{N} \beta_{kji} = 1. \tag{4.11}$$

In this case, the desired PWM-controlled branch voltage u_j^k is a result of the high-level line and circulating current controllers, such as the ones described in Chapter 2.
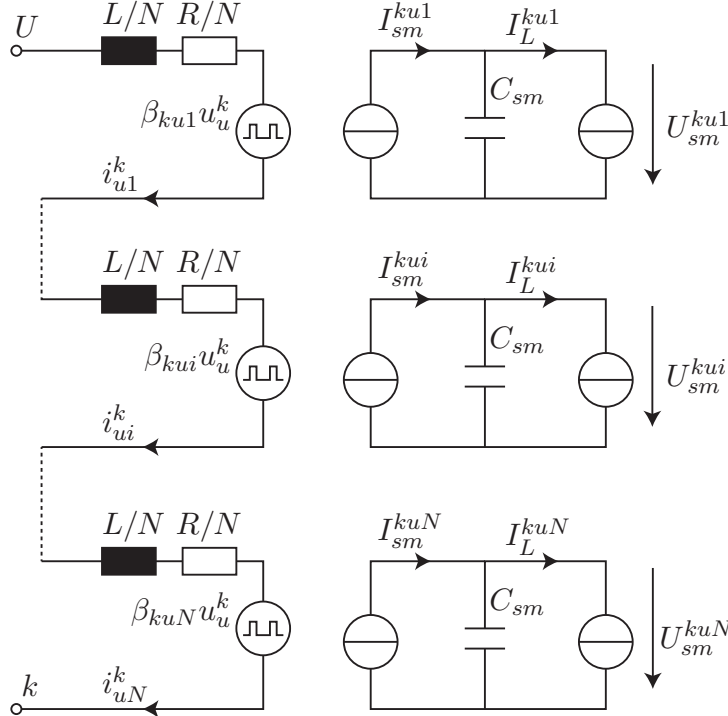
Figure 4.8: Equivalent circuit for a decoupled power flow formulation, taking the upper (u) branch of the k-th converter phase as an example.

4.4.2 Phase Power Control

The case of phase power control implies the ability to handle different amounts of active power components from each converter phase without affecting the three-phase grid currents. Similarly to the CHB converter with star configuration, the MMC offers the possibility of freely choosing the common-mode voltage u_{cm}, which is shown in Figure 4.5. Such an action enables the circulation of power within the converter phases, while keeping the total three-phase power transfer unaffected.

The three-phase voltage and current quantities are once again modeled by means of symmetrical components, where the superscripts p and n denote the positive and negative sequences, respectively. In order to achieve a constant power term associated with the common-mode voltage, the latter has to oscillate with the fundamental converter frequency. The k-th converter phase voltage can be written as

$$u_k = \hat{u}_V^p \cos\left(\omega t + \phi_u^p - \frac{2\pi(m-1)}{3}\right) + \hat{u}_V^n \cos\left(\omega t + \phi_u^n + \frac{2\pi(m-1)}{3}\right)$$
$$+ \hat{u}_{cm} \cos\left(\omega t + \phi_{cm}\right) \tag{4.12}$$

where $m = 1, 2, 3$. The quantity ϕ_u^p can be set to zero, assuming that the control system is synchronized with the positive sequence voltage u_V^p. The k-th phase current can also be expressed through the use of the symmetrical components as

$$i_{Tk} = \hat{i}_T^p \cos\left(\omega t + \phi_i^p - \frac{2\pi(m-1)}{3}\right) + \hat{i}_T^n \cos\left(\omega t + \phi_i^n + \frac{2\pi(m-1)}{3}\right) \tag{4.13}$$

The product of the voltage with the current in each converter phase gives the associated phase power components. The constant terms P_{ph}^k are obtained for phases a and b as

$$P_{ph}^a = \underbrace{U_S I_{circ0}^a}_{P_{DC}^a} - \frac{\hat{u}_{cm}\hat{i}_T^p}{2}\cos(\phi_{cm} - \phi_i^p) - \frac{\hat{u}_{cm}\hat{i}_T^n}{2}\cos(\phi_{cm} - \phi_i^n) - \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos\phi_i^n$$
$$- \frac{\hat{u}_V^n\hat{i}_T^p}{2}\cos(\phi_u^n - \phi_i^p) - \underbrace{\frac{\hat{u}_V^p\hat{i}_T^p}{2}\cos\phi_i^p - \frac{\hat{u}_V^n\hat{i}_V^n}{2}\cos(\phi_u^n - \phi_i^n)}_{\overline{P}_{3ph}} \tag{4.14}$$

$$P_{ph}^b = \underbrace{U_S I_{circ0}^b}_{P_{DC}^b} - \frac{\hat{u}_{cm}\hat{i}_T^p}{2}\cos(\phi_{cm} - \phi_i^p - \frac{4\pi}{3}) - \frac{\hat{u}_{cm}\hat{i}_T^n}{2}\cos(\phi_{cm} - \phi_i^n - \frac{2\pi}{3})$$
$$- \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos(\phi_i^n - \frac{2\pi}{3}) - \frac{\hat{u}_V^n\hat{i}^p}{2}\cos(\phi_u^n - \phi_i^p - \frac{2\pi}{3})$$
$$- \underbrace{\frac{\hat{u}_V^p\hat{i}_T^p}{2}\cos\phi_i^p - \frac{\hat{u}_V^n\hat{i}_T^n}{2}\cos(\phi_u^n - \phi_i^n)}_{\overline{P}_{3ph}} \tag{4.15}$$

For the definition of u_{cm} the two expressions are adequate, since the third phase is not forming an independent equation:

$$
\begin{cases}
\underbrace{P_{Bat}^a - P_{ph}^{a*} - \alpha_1}_{\Delta P_{ph}^a} = \hat{u}_{cm}\alpha_2 \cos\phi_{cm} + \hat{u}_{cm}\alpha_3 \sin\phi_{cm} \\[4mm]
\underbrace{P_{Bat}^b - P_{ph}^{b*} - \beta_1}_{\Delta P_{ph}^b} = \hat{u}_{cm}\beta_2 \cos\phi_{cm} + \hat{u}_{cm}\beta_3 \sin\phi_{cm}
\end{cases}
\tag{4.16}
$$

The coefficients α_{1-3} and β_{1-3} are functions of the phase voltage and current positive and negative sequence components and are given at the bottom of the page. The solution to the system is given by

$$
\phi_{cm} = \arctan\left(\frac{\Delta P_{ph}^a\beta_{2S} - \Delta P_{ph}^b\alpha_{2S}}{\Delta P_{ph}^b\alpha_{3S} - \Delta P_{ph}^a\beta_{3S}}\right), \quad \hat{u}_{cm} = \frac{\Delta P_{ph}^a}{\alpha_{2S}\cos\phi_{cm} + \alpha_{3S}\sin\phi_{cm}} \tag{4.17}
$$

For a balanced three-phase system, where no negative sequence component exists and therefore $\alpha_1 = \beta_1 = 0$, the solution becomes

$$
\phi_{cm} = \phi_i^p - \theta = \phi_i^p - \arctan\left[\frac{2\Delta P_{ph}^b/\Delta P_{ph}^a + 1}{\sqrt{3}}\right], \quad \hat{u}_{cm} = -\frac{2\Delta P_{ph}^a}{\hat{i}^p\cos\theta} \tag{4.18}
$$

The above expressions are similar to the CHB-BESS case in star configuration.

4.4.3 Branch Power Control

Contrary to the CHB-BESS unit, a third balancing direction exists in the MMC case. It regards the two branches within the same phase leg, which is also shown in Figure 4.1. A power transfer between the two branches should take place, without however disturbing neither the AC or the DC sides. Such an action is possible through the injection of a circulating current component with a fundamental frequency and the same angle with the phase voltage [51,58]. Considering only a positive sequence component for the converter voltages, the constant power difference between the two branches of the same k-th phase

---

$$
\alpha_1 = \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos\phi_i^n + \frac{\hat{u}_V^n\hat{i}_T^p}{2}\cos(\phi_u^n - \phi_i^p), \quad \alpha_2 = \frac{\hat{i}_T^p}{2}\cos\phi_i^p + \frac{\hat{i}_T^n}{2}\cos\phi_i^n, \quad \alpha_3 = \frac{\hat{i}_T^p}{2}\sin\phi_i^p + \frac{\hat{i}_T^n}{2}\sin\phi_i^n
$$

$$
\beta_1 = \frac{\hat{u}_V^p\hat{i}_T^n}{2}\cos(\phi_i^n - \frac{2\pi}{3}) + \frac{\hat{u}_V^n\hat{i}_T^p}{2}\cos(\phi_u^n - \phi_i^p - \frac{2\pi}{3}), \quad \beta_2 = \frac{\hat{i}_T^p}{2}\cos(\phi_i^p + \frac{4\pi}{3}) + \frac{\hat{i}_T^n}{2}\cos(\phi_i^n + \frac{2\pi}{3}),
$$

$$
\beta_3 = \frac{\hat{i}_T^p}{2}\sin(\phi_i^p + \frac{4\pi}{3}) + \frac{\hat{i}_T^n}{2}\sin(\phi_i^n + \frac{2\pi}{3})
$$

leg will then become as follows:

$$\Delta P_{br}^k = -\hat{i}_{bal}^k \hat{u}_V - \hat{i}_{bal}^k \hat{u}_{cm} \cos\phi_{cm} = -\hat{i}_{bal}^k \left(\hat{u}_V + \hat{u}_{cm} \cos\phi_{cm}\right) \tag{4.19}$$

Therefore for a given amount of power difference ΔP_{br}^k between the branches of the same phase leg, a circulating current amplitude is associated as

$$\hat{i}_{bal}^k = -\frac{\Delta P_{br}^k}{\left(\hat{u}_V + \hat{u}_{cm} \cos\phi_{cm}\right)} \tag{4.20}$$

This action implies that if different amounts of balancing powers are needed within the three phase legs, different AC circulating currents will be injected and therefore the DC-link current will no longer be a pure DC. This is something not acceptable when used for a SoC balancing control, given the fact that the time that the injection lasts will be in the order of minutes, due to the high battery time constant. Therefore and according to [58], for each phase-leg circulating current injection, a respective injection in the other two phases should take place. The other two components will be orthogonal to the phase voltages, in order to deliver only reactive power to the legs. In addition, their amplitude should be chosen, so as to cancel out between the three-phases and not cause any AC components to the DC-link. The final branch balancing circulating currents can be therefore chosen as:

$$\begin{pmatrix} i_{bal}^a \\ i_{bal}^b \\ i_{bal}^c \end{pmatrix} = \begin{pmatrix} \cos\omega t & -\frac{1}{\sqrt{3}}\sin\omega t & \frac{1}{\sqrt{3}}\sin\omega t \\ \frac{1}{\sqrt{3}}\sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) & -\frac{1}{\sqrt{3}}\sin(\omega t - \frac{2\pi}{3}) \\ -\frac{1}{\sqrt{3}}\sin(\omega t + \frac{2\pi}{3}) & \frac{1}{\sqrt{3}}\sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{pmatrix} \begin{pmatrix} \hat{i}_{bal}^a \\ \hat{i}_{bal}^b \\ \hat{i}_{bal}^c \end{pmatrix} \tag{4.21}$$

4.4.4 Operation Under Grid Unbalances

When a voltage unbalance occurs in the three-phase AC side and the currents are controlled to be perfectly symmetrical (negative sequence-free), each phase cannot provide the same amount of active power. Similarly to what has been discussed for the CHB-BESS case, this would mean that the batteries can no longer be charged or discharged with the same rate, something that would cause an unbalance in the battery SoCs in the MMC case as well. In order to avoid this, a common-mode voltage injection can take place with the objective of keeping a constant power flow throughout the three converter phase legs. It is noted that a grid unbalance does not affect the power distribution between the branches of the same phase leg as shown in Section 2.6.

The simulation results for such a scenario are illustrated in Figure 4.9. Initially the system is operating in symmetrical conditions and each phase absorbs the same amount of active power. At t = 20 ms, a phase-to-ground fault takes place with a severity of
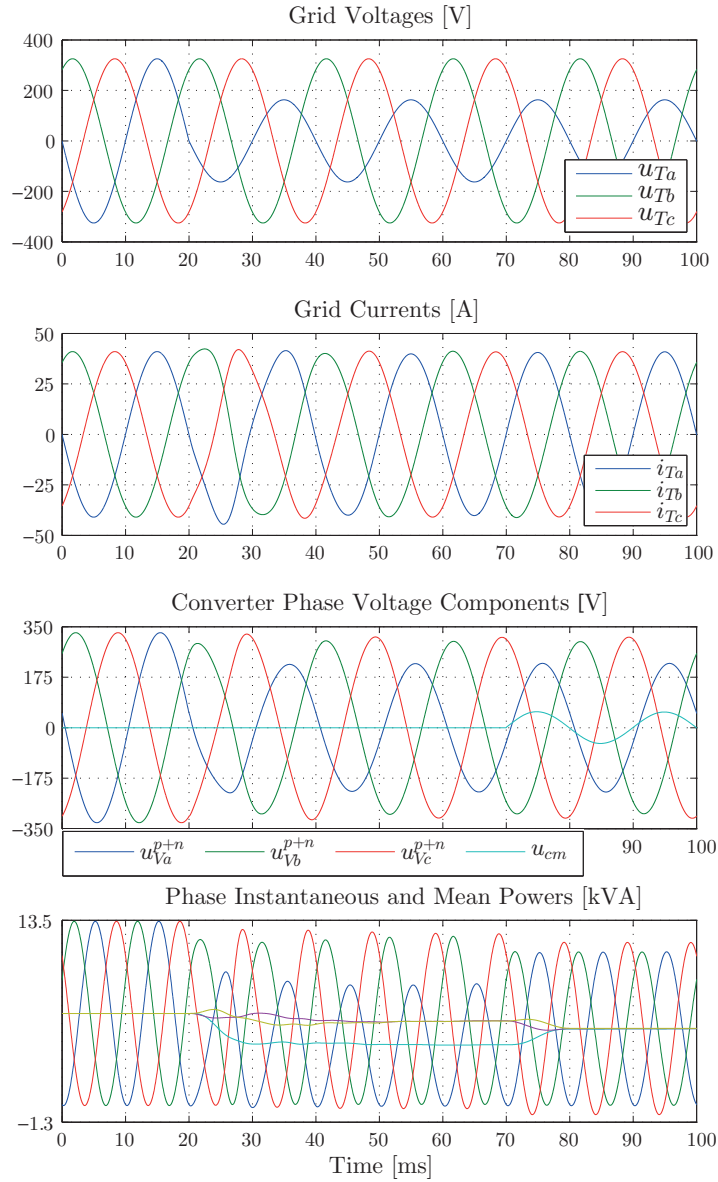
Figure 4.9: Simulation results from a battery charging mode under unbalanced grid conditions for the MMC-BESS case: Three-phase grid voltages and respective currents, converter phase components as well as instantaneous absorbed powers with their respective mean values.

50% phase loss. The three-phase currents are controlled to be perfectly symmetrical through the use of two control loops in the rotating reference frame, in conjunction with a DDSRF algorithm for symmetrical component identification and synchronization with the three-phase unbalanced network [123]. When no common-mode voltage component is used, the three-phases obviously deliver different amounts of mean active powers. At t = 70 ms, the injection of u_{cm} takes place according to (4.17), making the three-phase delivered powers to the branches converge.

It is noted that such an action is preferable when the target is to avoid the SoC unbalance within the phases. However, the DC-link power in such a case remains unaffected and obviously reduced because of the network asymmetry. Alternatively, it can be chosen to use the BESS of a certain phase to cover a DC power demand, when the AC grid cannot support it during a faulty condition.

4.5 State of Charge Balancing

When the target is the state of charge balancing of the different battery packs, the concepts developed in the previous paragraph can be utilized for achieving this in a closed-loop manner. Therefore, the explicit transfer functions relating the SoC with the amount of charging/discharging power need to be derived as in the case of the CHB-BESS. The difference is that now the third possible branch SoC unbalance direction has to be considered as well. It has been shown that the SoCs can be modeled as first-order systems with integral behavior. Assuming a submodule battery nominal capacity of $Q_{bat,n}^{sm}$ and nominal voltage of $U_{bat,n}^{sm}$, the respective transfer function is obtained

$$SoC_{sm} = \frac{I_{bat}^{sm} \cdot 100}{s \cdot Q_{bat,n}^{sm}} = \frac{P_{bat}^{sm} \cdot 100}{s \cdot U_{bat,n}^{sm} Q_{bat,n}^{sm}} = \frac{P_{bat}^{sm} \cdot 100}{s \cdot E_{bat,n}^{sm}} \tag{4.22}$$

For the whole MMC phase leg, the following expression is derived, accordingly:

$$SoC_{ph} = \frac{P_{bat}^{ph} \cdot 100}{s \cdot E_{bat,n}^{ph}} = \frac{P_{bat}^{ph} \cdot 100}{s \cdot 2N E_{bat,n}^{sm}} \tag{4.23}$$

Finally, the branch unbalance direction implies the definition of the branch SoC as

$$SoC_{br} = \frac{P_{bat}^{br} \cdot 100}{s \cdot E_{bat,n}^{br}} = \frac{P_{bat}^{br} \cdot 100}{s \cdot N E_{bat,n}^{sm}} \tag{4.24}$$

In all three cases the SoC is a percentage (%), and the battery nominal energy $E_{bat,n}^{sm}$ is expressed in $(W \cdot s)$.

The required active powers of the state of charge balancing can be once again calculated utilizing a proportional controller. Figure 4.10 presents the block diagrams used for the control system design. The submodule SoC controller forces the kji-th submodule SoC_{sm}^{kji} follow the mean SoC value $\overline{SoC}_{br}^{kj}$ of the kj-th branch. Similarly, the phase SoC controller forces the mean SoC value $\overline{SoC}_{ph}^{k}$ of the k-th phase follow the mean SoC value $\overline{SoC}_{3ph}$ of all three phases. Finally, the branch balancing controller ensures that both branch mean SoC values $\overline{SoC}_{br}^{kj}$ of the same phase leg converge. The aforementioned quantities are therefore defined as follows:

$$\overline{SoC}_{br}^{kj} = \frac{1}{N} \sum_{i=1}^{N} SoC_{sm}^{kji} \tag{4.25}$$

$$\overline{SoC}_{ph}^{k} = \frac{\overline{SoC}_{br}^{ku} + \overline{SoC}_{br}^{kl}}{2} \tag{4.26}$$

$$\overline{SoC}_{3ph} = \frac{\overline{SoC}_{ph}^{a} + \overline{SoC}_{ph}^{b} + \overline{SoC}_{ph}^{c}}{3} \tag{4.27}$$

By setting the desired rise times t_r^{sm}, t_r^{ph}, t_r^{br} for the closed-loop control system, the respective proportional gains k_p^{sm}, k_p^{ph}, and k_p^{br} are calculated as a function of the nominal submodule battery energy storage $E_{bat,n}^{sm}$, which represents the plant time constant:

$$k_p^{sm} = \frac{E_{bat,n}^{sm}}{100 \cdot t_r^{sm}} \ln 9, \quad k_p^{ph} = \frac{2N E_{bat,n}^{sm}}{100 \cdot t_r^{ph}} \ln 9 \quad \text{and} \quad k_p^{br} = \frac{N E_{bat,n}^{sm}}{100 \cdot t_r^{br}} \ln 9 \tag{4.28}$$

(a)

(b)

(c)
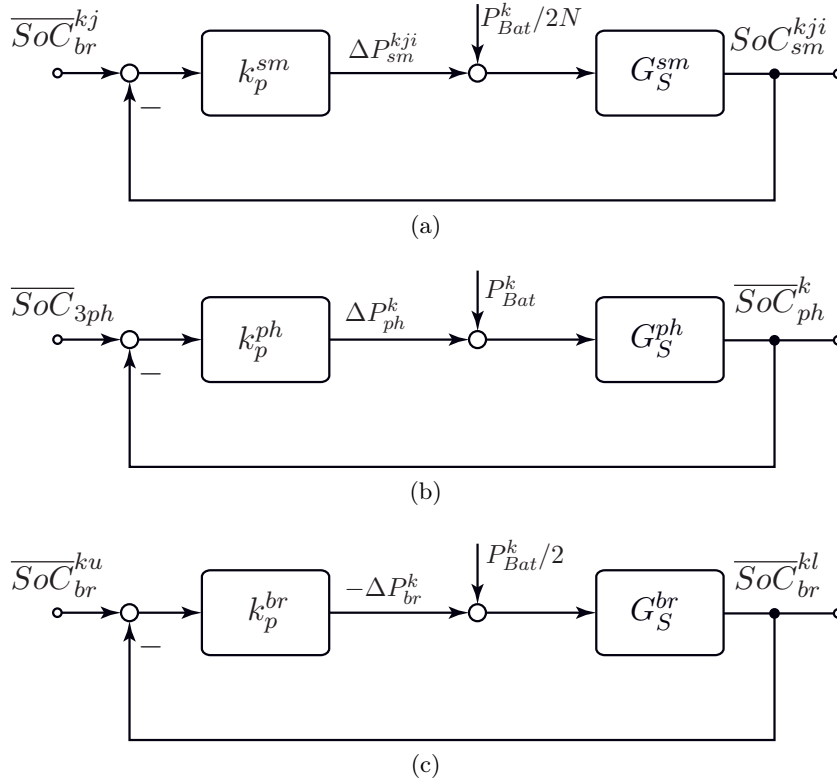
Figure 4.10: Block diagrams for (a) submodule, (b) phase, and (c) branch balancing of battery state of charges.

Figure 4.10 reveals that the submodule, phase and branch powers will consist of two terms: the main power contribution, which is common for all submodules/phases/branches and does not contribute to the unbalance, as well as the balancing power term, which is the result of the closed-loop control. The total state of charge will be a result of both terms.

It is noted that the sum of all balancing terms in all three directions will have to be zero, in order not to affect the global power transfer. Finally, the rise times are set higher than a respective capacitor voltage balancing loop, as dictated by the significant difference in the system time constants.

4.5.1 Limitations on Gain Selection

The SoC balancing controller gains have to follow certain constraints, which are linked to the operation and ratings of the converter, similarly to the CHB-BESS case. These limitations are established in this paragraph. For sake of simplicity, only balanced grid conditions are assumed.

Initially, the phase balancing loop is examined. The maximum achievable common-mode voltage defines the amount of balancing power ΔP_{ph}^{max} that can be utilized for the balancing. Similarly to the CHB-BESS case, this limitation is directly related to the dimensioned branch blocking voltage u_{br}^{dim}, where the tolerated submodule capacitor voltage variation $k_{\Delta v}$ has to be taken into account. This can be expressed as

$$u_{br}^{dim} \geq k_{\Delta v} \left(U_S/2 + u_T^{max} + u_{cm}^{max}\right) \overset{(4.18)}{\Leftrightarrow} \frac{2\Delta P_{ph}^{max}}{\hat{i}_T^p \cos x} \leq \frac{N u_{sm}^{dim}}{k_{\Delta v}} - U_S/2 - u_T^{max}$$

$$\overset{(4.28)}{\Leftrightarrow} \frac{4 N E_{bat,n}^{sm} \Delta SoC_{ph}^{max} \ln 9}{100 \cdot t_r^{ph}} \leq \left(\frac{N u_{sm}^{dim}}{k_{\Delta v}} - U_S/2 - u_T^{max}\right) \hat{i}_T^p \cos x,$$

$$x = \arctan \left[\frac{2\left(\frac{\Delta SoC_{ph}^{k+1}}{\Delta SoC_{ph}^{k,max}}\right) + 1}{\sqrt{3}}\right] \tag{4.29}$$

Taking phase a as a reference and assuming that the maximum SoC variations are shared between phases a and c with the same value and opposite signs, ΔSoC_{ph}^{k+1} of phase b will be zero (since $\sum \Delta SoC_{ph}^{k} = 0$). Therefore, x can be approximated as having the worst case value of $\arctan\left(1/\sqrt{3}\right) = \pi/6$. The latter leads to the definition of a minimum rise time t_r^{ph} of

$$t_r^{ph} \geq \frac{8 N E_{bat,n}^{sm} \Delta SoC_{ph}^{max} k_{\Delta v} \ln 9}{100\sqrt{3}\hat{i}_T^p \left[N u_{sm}^{dim} - k_{\Delta v}\left(U_S/2 + u_T^{max}\right)\right]} \tag{4.30}$$

In addition, each branch cannot provide negative voltages. That means that a second constraint should be posed regarding the minimum branch voltage value, which should not fall below zero. This is formulated as follows

$$\frac{U_S}{2} - u_T^{max} - u_{cm}^{max} \geq 0 \Leftrightarrow \Leftrightarrow u_{cm}^{max} \leq \frac{U_S}{2} - u_T^{max}$$

115

$$\Leftrightarrow \frac{8NE_{bat,n}^{sm}\Delta SoC_{ph}^{max}\ln 9}{100\sqrt{3}\hat{i}_T^p t_r^{ph}} \leq U_S/2 - u_T^{max} \tag{4.31}$$

giving therefore the second limitation as

$$t_r^{ph} \geq \frac{8NE_{bat,n}^{sm}\Delta SoC_{\mathrm{ph}}^{\max}\ln 9}{100\sqrt{3}\hat{i}_T^p\left(U_S/2 - u_T^{max}\right)} \tag{4.32}$$

Therefore, the rise time is proportional to the battery nominal energy as well as the tolerated maximum SoC error. However, it is inversely proportional to the maximum current, which means that the maximum achievable balancing power is limited in lower currents.

The constraint for the submodule SoC balancing control is related to overmodulation. The branch voltage is weighted with the ratio factor β_{kji}, which is related to the sum of the submodule mean power $P_{Bat}^k/2N$ with the respective balancing action ΔP_{sm}^{kji}, as shown in Figure 4.10a. This can be finally expressed as

$$\beta_{kji}u_{br}^{max} \leq U_{sm}^{min} \Leftrightarrow \frac{\frac{P_{Bat}^k}{2N} + \Delta P_{sm}^{max}}{\frac{P_{Bat}^k}{2}}u_{br}^{max} \leq U_{sm}^{min} \Leftrightarrow \left(\frac{1}{N} + \frac{2\Delta P_{sm}^{max}}{P_{Bat}^k}\right) \leq \frac{U_{sm}^{min}}{u_{br}^{max}}$$

$$\Leftrightarrow \Delta P_{sm}^{max} \leq \frac{P_{Bat}^k}{2}\left(\frac{U_{sm}^{min}}{u_{br}^{max}} - \frac{1}{N}\right) \overset{(4.28)}{\Leftrightarrow} \frac{E_{bat,n}^{sm}\Delta SoC_{sm}^{max}\ln 9}{100\cdot t_r^{sm}} \leq \frac{P_{Bat}^k\left(NU_{sm}^{min} - u_{br}^{max}\right)}{2Nu_{br}^{max}} \tag{4.33}$$

leading to a minimum rise time of

$$t_r^{sm} \geq \frac{2Nu_{br}^{max}E_{bat,n}^{sm}\Delta SoC_{sm}^{max}\ln 9}{P_{Bat}^k\left(NU_{sm}^{min} - u_{br}^{max}\right)100} = \frac{2Nu_{br}^{max}E_{bat,n}^{sm}\Delta SoC_{\mathrm{sm}}^{max}\ln 9}{P_{Bat}^k\left[N\left(1 - k_u\right)\overline{U}_{sm} - u_{br}^{max}\right]100} \tag{4.34}$$

where k_u is the allowed voltage ripple on the submodule capacitor voltage and $u_{br}^{max} = U_S/2 + u_T^{max} + u_{cm}^{max}$.

In this case, a faster balancing can be achieved with a higher amount of absorbed submodule power $P_{Bat}^k/2N$. Another way to avoid overmodulation is to control the mean value of the submodule capacitor voltages $\overline{U}_{sm}$ at a higher value, which means however an increase in the required installed capacitive energy.

Finally, the limitation of the branch SoC balancing loop should be established. Since it regards a circulating current injection, it is limited by the respective rating of the semiconductors in the converter branches. Considering all different components, the

branch current can be expressed as

$$
i_{br} = \frac{\hat{i}_T^p}{2}\cos(\omega t + \phi_i^p) + \frac{I_S}{3} + \hat{i}_{circ,2}\cos(2\omega t + \phi_i^p) + \hat{i}_{bal}^k \cos\omega t + \frac{1}{\sqrt{3}}\left(\hat{i}_{bal}^{k+2} - \hat{i}_{bal}^{k+1}\right)\sin\omega t \tag{4.35}
$$

Considering the worst case, i.e. that all three phases are experiencing the maximum SoC error between their upper and lower branches, the following inequality should hold for the dimensioned branch current:

$$
\begin{aligned}
i_{br}^{dim} \geq \hat{i}_T^p &\left(\frac{1}{2}\cos(\omega t + \phi_i^p) + \frac{\varepsilon}{4}\cos\phi_i^p + \frac{1}{4}\cos(2\omega t + \phi_i^p)\right) \\
&+ \frac{NE_{bat,n}^{sm}\ln 9}{100\cdot t_r^{br}}\left[\frac{\Delta SoC_{br}^{k,max}}{(\hat{u}_V + \hat{u}_{cm}\cos\phi_{cm})}\cos\omega t\right. \\
&+ \frac{1}{\sqrt{3}}\left.\left(\frac{\Delta SoC_{br}^{k+2,max}}{\left(\hat{u}_V + \hat{u}_{cm}\cos\left(\phi_{cm} - \frac{2\pi}{3}\right)\right)} - \frac{\Delta SoC_{br}^{k+1,max}}{\left(\hat{u}_V + \hat{u}_{cm}\cos\left(\phi_{cm} + \frac{2\pi}{3}\right)\right)}\right)\sin\omega t\right] \tag{4.36}
\end{aligned}
$$

It is clear that the phase balancing SoC loop is interacting with the branch balancing one through the appeared injection of the common mode voltage component u_{cm}. In addition the ratio ε, which defines the value of I_{circ0}, has an impact on the branch current peak value. A generalized analytical solution is therefore not straightforward. Instead, a numerical evaluation can be performed in order to specify the minimum rise time of the loop. The respective equation is obtained as

$$
t_{br} \geq \max\left\{\frac{\frac{NE_{bat,n}^{sm}\ln 9}{100}\left[\text{par}1\cos\omega t + \frac{1}{\sqrt{3}}\text{par}2\sin\omega t\right]}{i_{br}^{dim} - \hat{i}_T^p\left(\frac{1}{2}\cos(\omega t + \phi_i^p) + \frac{\varepsilon}{4}\cos\phi_i^p + \frac{1}{4}\cos(2\omega t + \phi_i^p)\right)}\right\} \tag{4.37}
$$

where $\text{par}1 = \frac{\Delta SoC_{br}^{k,max}}{(\hat{u}_V + \hat{u}_{cm}\cos\phi_{cm})}$, $\text{par}2 = \left(\frac{\Delta SoC_{br}^{k+2,max}}{\left(\hat{u}_V + \hat{u}_{cm}\cos\left(\phi_{cm} - \frac{2\pi}{3}\right)\right)} - \frac{\Delta SoC_{br}^{k+1,max}}{\left(\hat{u}_V + \hat{u}_{cm}\cos\left(\phi_{cm} + \frac{2\pi}{3}\right)\right)}\right)$

Some remarks can be therefore made. Relation (4.34) reveals that a common-mode voltage increase limits the amount of active power that can be absorbed or injected from each submodule for balancing purposes. Moreover, the branch average power $P_{Bat}^k/2$ is a function of the current angle ϕ_i^p as well as the power ΔP_{ph}^k needed for the phase SoC balancing. This is a constraint, which should be also taken into account during the design process. In general, the phase balancing control loop has an effect on the submodule balancing one, implying that the latter should be chosen with a lower bandwidth, leading therefore to $t_r^{ph} < t_r^{sm}$. Moreover and in order to achieve independence from the global current control as well as power transfer, the relations $\sum \Delta P_{ph}^k = \sum \Delta P_{sm}^{kji} = 0$ should hold. This can be also guaranteed through the use of $(N-1)$ controllers/branch for the submodule as well as 2 controllers for the phase SoC balancing loops.

Finally, it is noted that the established limitations in (4.32) and (4.34) can be utilized for adaptive gain calculation in cases of operating point changes, as already mentioned for (4.37).

4.5.2 Overall MMC-BESS Control System and Simulation Results

The final overall system control block diagram of the MMC-BESS system is illustrated in Figure 4.11. All different utilized control systems and variables are depicted according to the considerations made throughout the previous sections. The control system is obviously similar to what has been illustrated in Figure 3.14 for the CHB-BESS case.

Once again, the three-phase grid voltages and currents are measured and used for grid synchronization as well as line current control in a rotating reference frame. On this level, the DDSRF [123] together with two current loops for positive and negative sequences is used for handling the control during grid asymmetries.

The factor ε defines the power amount splitting between AC and DC sides and the integrated converter BESS. The reference generator gives therefore the desired values for the phase-leg battery power P_{Bat}^k as well as circulating current, which will ensure DC power control as well as capacitor voltage ripple reduction through optional intended second-order harmonic components, as described in Chapter 2.

The voltage control of the submodule capacitors is treated from the battery side through the individual cascaded outer voltage/inner current controllers. On the other hand, the SoC unbalances are handled in the submodule, phase and branch directions. The submodule SoC control is based on the independent submodule power control and is implemented by adjusting the power ratio of (4.11). The phase SoC control is implemented by the injection of the common-mode voltage quantity u_{cm}^* which can be added directly to the line controller outcome. Finally, the branch SoC control is performed by the balancing circulating current injection i_{bal}^k together with the associated matrix components for achieving pure continuous DC-link current. This are added to the respective outcome of the power-based reference generator. It is noted that the SoC balancing controllers will not have any contribution to the system once the batteries are perfectly balanced, as already assumed for the results of Figure 4.7.
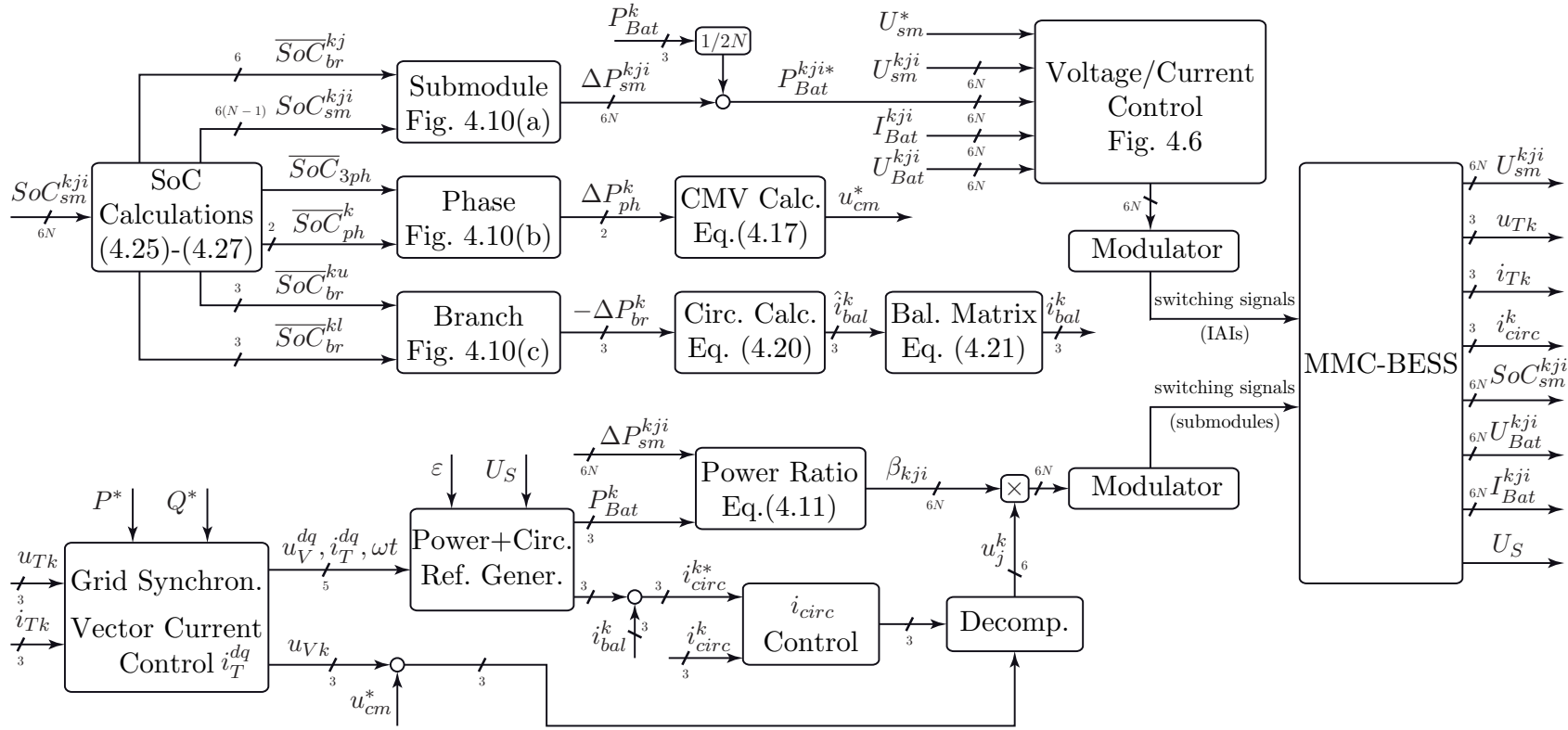
Figure 4.11: Overall system control block diagram for three-phase Modular Multilevel Converters with integrated split battery energy storage.

The proposed SoC balancing control strategy has been tested in simulations and the results are shown in Figure 4.12. All battery packs have been initialized with an arbitrary SoC and the maximum difference reaches up to 22.5%. A battery charging procedure until t = 250 s is followed by a respective discharging. The convergence of the submodule, phase and branch SoCs is evident. The common-mode voltage as well as the balancing circulating currents are also fading out as the respective phase and branch SoC deviations tend asymptotically to zero. The unequal power distribution to the batteries for balancing purposes is depicted on the battery currents of Figure 4.12a. In Figure 4.12d, it is shown
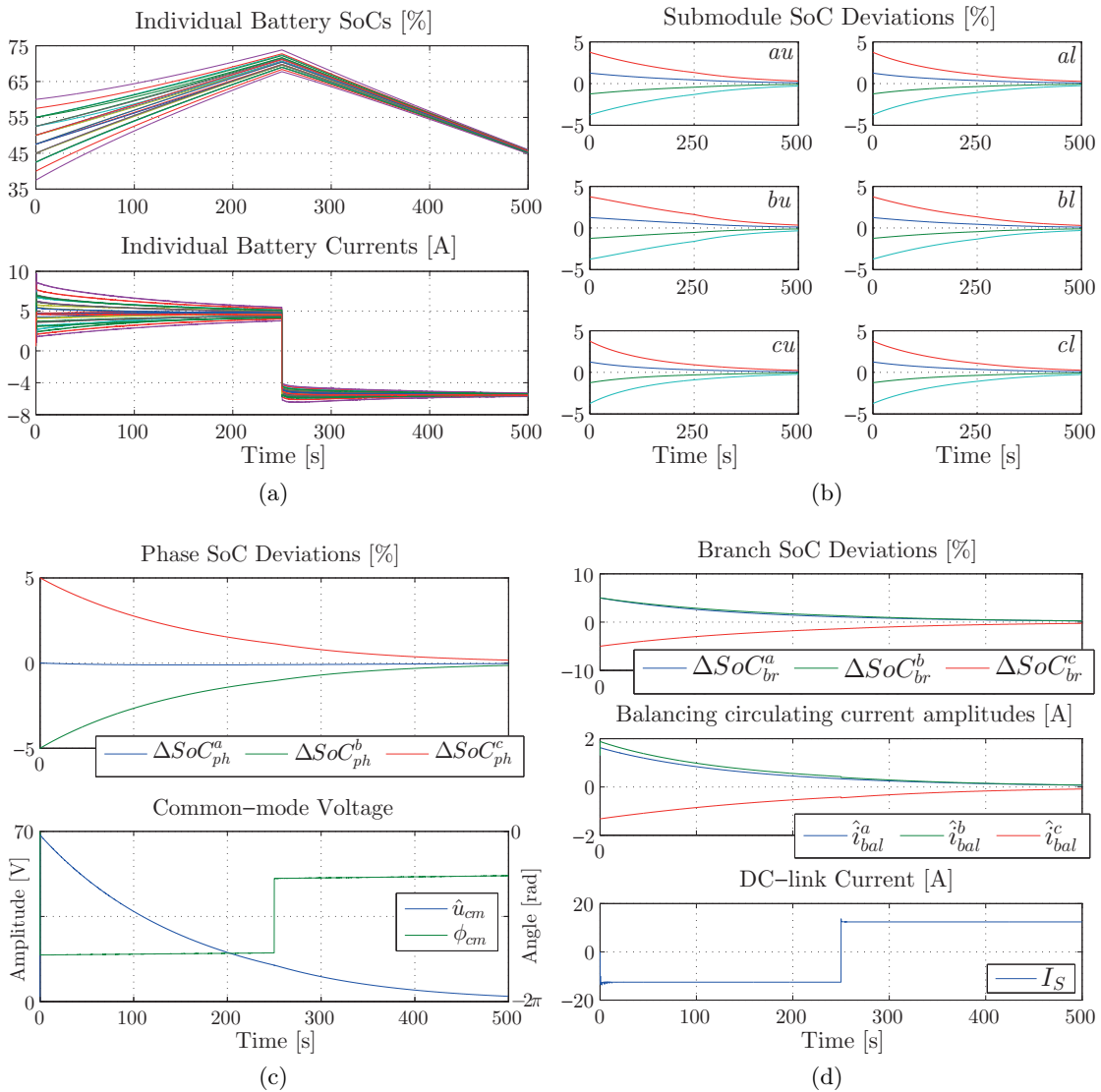
Figure 4.12: Simulation results for the MMC-BESS unit: (a) Individual battery state of charges and respective currents during converter balancing action, (b), (c), (d) Time-domain convergence of the submodule, phase and branch SoC balancing regulators. Closed-loop rise times have been set to $t_r^{sm} = 400$ s, $t_r^{ph} = 300$ s and $t_r^{br} = 350$ s.

that the DC-link current will not be affected by the branch balancing circulating currents, due to the respective reactive injection in the other two phases. Therefore, it will bear only a DC component.

Similarly to the CHB-BESS case, the average submodule voltages are also kept constant throughout the balancing operation in the MMC-BESS as well. This proves a beneficial voltage decoupling between the battery and the submodule, which cannot be achieved with the DPI, API or BPFS interfacing methods.

4.6 Experimental Results

The same reduced-scale prototype used for the experimental validation of the CHB-BESS converter, which has been illustrated in Figure 3.23 has been reconfigured towards its exploration as an MMC-BESS topology.

For the performed test, the phase leg is connected to a fixed voltage source on the DC-link side and to an inductive/resistive passive load on the AC side. The circuit configuration is shown in Figure 4.13 along with the main system parameters. Figure 4.14 illustrates the resulted magnitudes of the upper branch. The circulating current is controlled to comprise an almost zero DC component, therefore most of the power will be delivered to the load by the batteries. This corresponds to operating Mode V, as explained in Section 4.3. The carriers of the submodule modulators are phase-shifted in order to obtain the five-level voltage waveform u_u. Finally, the submodule capacitor voltages are perfectly balanced due to their active control from the battery side through the IAIs.
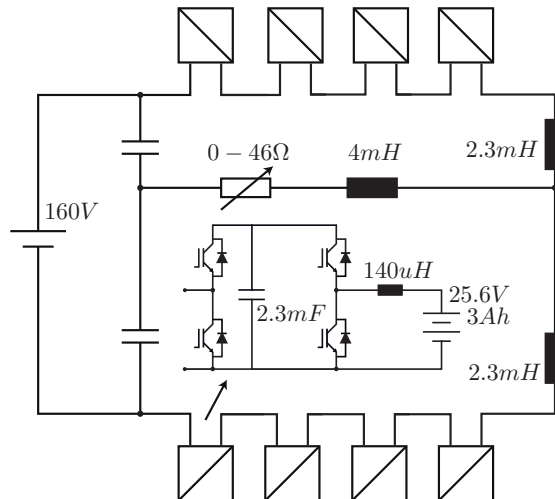
Figure 4.13: Schematic of the experimental setup circuit configuration (MMC-BESS).

A detail of the battery currents and voltages is depicted in Figure 4.15. The currents contain only the switching-related ripple but no low frequency components. The difference of the battery voltages according to their state of charge has no effect on the upper branch

121
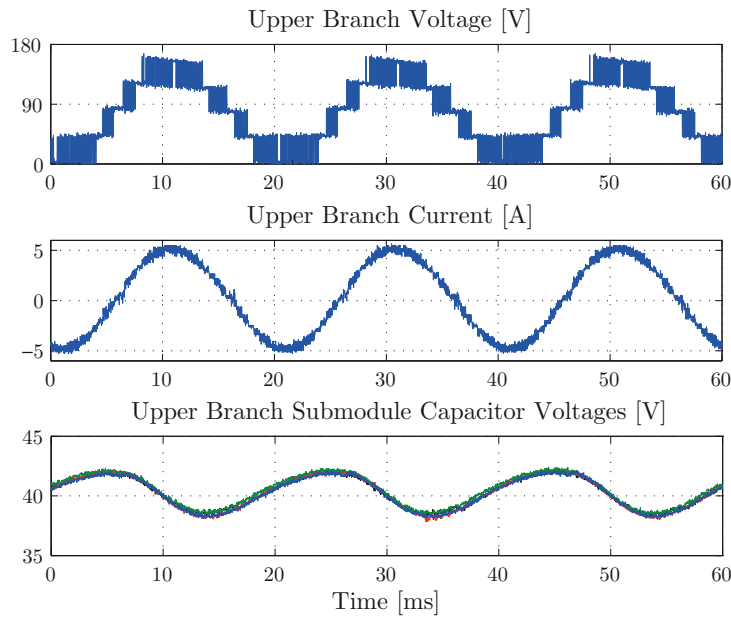
Figure 4.14: Experimental results for a discharging procedure of the batteries in inverting operation, corresponding to Mode V: Upper branch quantities.
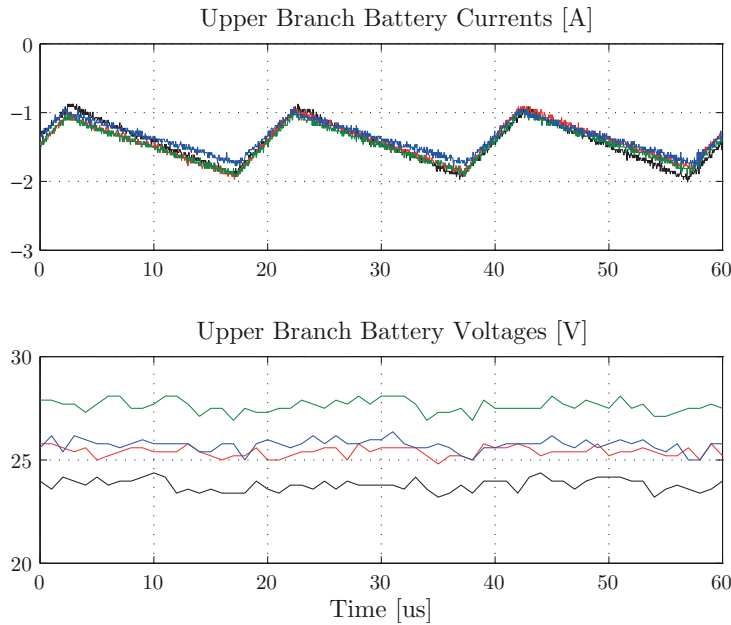
Figure 4.15: Experimental results for a discharging procedure of the batteries in inverting operation, corresponding to Mode V: Battery magnitudes.

voltage waveform, which is an advantage of their decoupling from the submodules. In this test, the same battery current reference is set for all IAIs. This implies a different amount of injected power due to the respective difference of the battery voltages. The latter is handled effectively by the individual submodule power control. It is noted that larger

active power differences between the submodules would lead to more visible differences on their capacitor voltage ripples, due to the different respective current variations.

4.7 Conclusion

This chapter has investigated the operation of a Modular Multilevel Converter-based storage unit with split accumulation. Compared to the CHB-BESS unit, the system control features similarities. It can be characterized, however, as slightly more complicated due to the existence of more available power flows and operating modes. The same method to control the battery SoCs has been applied successfully. In the MMC case, the third unbalance direction between the two branches of the same phase leg has been also treated.

Once again it can be concluded that the proposed methods can be applied to any type of Modular Multilevel Converter with integrated split BESS by making the necessary modifications. These include the IAI concept utilization for submodule capacitor voltage control, leaving the independent power control handle all possible SoC unbalance directions, as well as the specific degree of freedom utilization for symmetrizing the three-phase power during unbalanced grid operation.

5 Power Electronic Transformer-based Ultra-Fast EV Charging Station

5.1 Introduction

This chapter introduces and analyzes a topology for the implementation of an ultra-fast charging station for electric vehicles on the medium voltage level. Figure 5.1 shows a conventional converter architecture for such an application. It utilizes a common DC voltage bus, which is interfaced to the AC medium voltage grid through a step-down low frequency transformer and an AC/DC converter. Additional DC/DC conversion stages are used for interfacing intermediate battery energy storage systems as well as the EV battery, which is to be charged [89]. In other cases, other storage means are proposed as well, such as flywheels and supercapacitors [90]. The storage stage plays the role of a power buffer, reducing thus the influence of the charging station on the distribution grid.
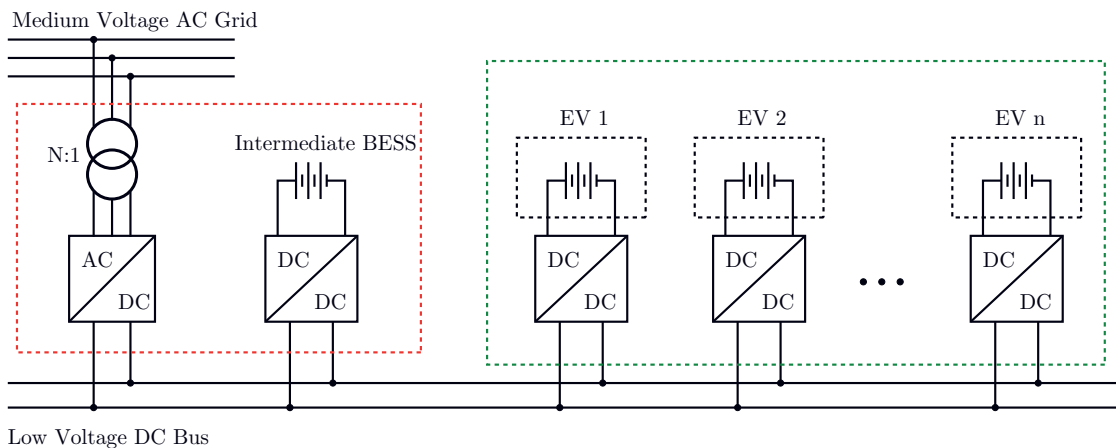
Figure 5.1: Conventional EV ultra-fast charging station architecture, utilizing a common DC bus with additional battery energy storage system buffers.

A simplified scheme of the proposed ultra-fast charging architecture is illustrated in Figure 5.2. The diagram part that is enclosed within the red rectangle corresponds to the respective one in Figure 5.1. The low frequency step-down transformer has been

eliminated, leading to a direct coupling of the active front end stage to the medium voltage grid. The intermediate BESS stage is also integrated into the same conversion structure. The EV battery isolation requirements are now shifted towards the medium frequency range. As depicted in Figure 5.2, it is desirable to acquire a multiport concept, where several vehicles can be charged simultaneously by means of isolated DC/DC converters, leading therefore to a realization of an ultra-fast charging station utilizing a single converter structure.
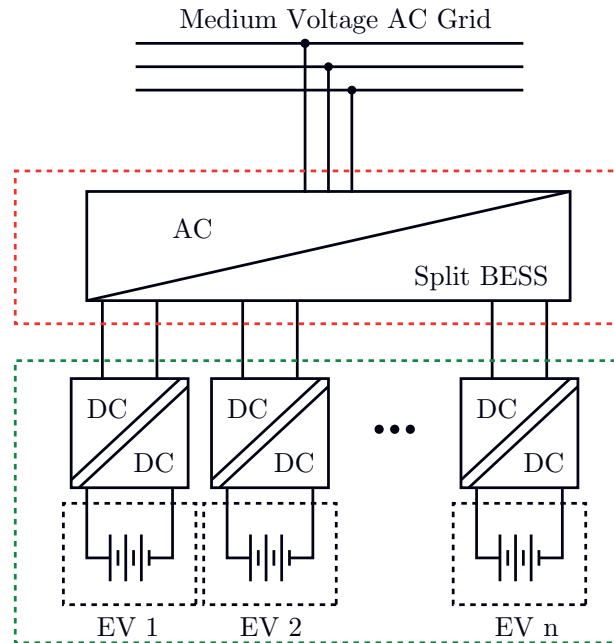
Figure 5.2: Proposed EV ultra-fast charging station architecture, utilizing a multiport power converter with integrated split battery energy storage.

For the implementation of the transformerless medium voltage AC grid coupling, the choice of a multilevel converter topology offers a straightforward solution. Similarly to what has been described in the two previous chapters, the CHB converter offers the additional advantages of: a) a modular design and b) the existence of low voltage dedicated DC buses for the interfacing of the intermediate BESS.

The CHB converter modularity also facilitates the converter configuration into a versatile multiport structure. This is shown in Figure 5.3, where the proposed modular versatile PET-based multiport EV charging station is illustrated in detail. It consists of three conversion stages: a) the transformerless active front end (CHB converter), b) the stationary batteries with the associated interface solution (split storage stage), as well as the medium frequency transformer-based DC/DC converters (isolation stage). The three-phase Cascaded H-Bridge converter can be utilized either in star or in delta configurations.

As in any modular PET application, the medium frequency transformer-based DC/DC converters are connected in parallel. In this case such an action achieves the needed high

output currents as well as meeting the EV battery galvanic isolation standards. The multiport concept is achieved by selecting several different submodule configurations on a parallel-connection level.
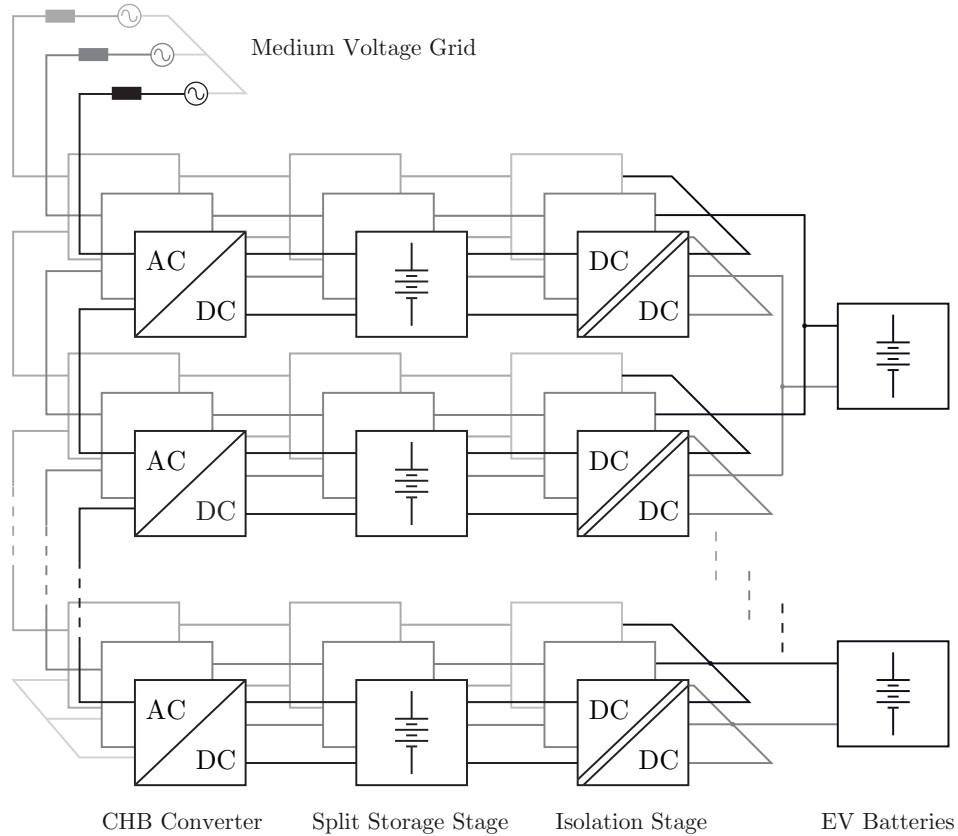
Figure 5.3: Proposed detailed converter architecture for ultra-fast charging of electric vehicles, based on a star-configured Cascaded H-Bridge converter with integrated battery energy storage and isolated DC/DC converters.

It is noted that the cascaded H-bridge active front end stage gives a significant degree of freedom for choosing the number of submodules feeding each charging port. Hence, a parallel connection of the isolated modules between different phases gives the additional advantage of maintaining the symmetry of the three-phase grid currents during the EV charging without the need for common-mode voltage/circulating current injection. Finally, it is evident that the global system architecture is bidirectional in terms of power flow. Therefore, it can also provide ancillary services, such as STATCOM operation as well as frequency control and active power support through a Buffer-to-Grid (B2G) concept.

The CHB-BESS storage unit and its associated control functions have been already described in detail in Chapter 3, they will therefore not be repeated here. Throughout the next paragraphs the focus will be laid on the choice of the isolated stage topology and control as well as the global EV charging station operation.

5.2 Dual Half-Bridge-based Isolation Stage

The power interface between the CHB converter with integrated storage and the EV battery should fulfill three basic requirements: (a) very low charging current ripple, (b) current and voltage control capability, and (c) galvanic isolation. Apart from the international standards, the latter is also imposed by the fact that the converter outputs have to be connected in parallel, in order to achieve the high charging current. Soft switching capability is an additional desirable feature, since it implies the possibility to increase the switching frequency without significantly affecting the global system losses. Finally, the converter should be able to operate in a wide output voltage range with an acceptable efficiency. This is again due to the existence of different types of available EV battery packs.

Initially, the straightforward solution of the full-bridge phase-shift controlled PWM converter has been considered for the implementation of the PET isolation stage. However, several drawbacks of such a topology were highlighted, such as unequal thermal stress of the two primary converter legs, as well as incapability of bidirectional power flow without additional external circuitry. The reader is referred to Appendix C for an analysis and current control of the specific converter.

On the other hand, the DHB converter presented in [125,126] exhibits significant advantages and features all aforementioned requirements. In addition, it offers the ability of transferring power from the EV battery to the grid, i.e., Vehicle-to-Grid (V2G) operation. This section therefore analyzes the DHB converter topology in the framework of the proposed charging station.

5.2.1 DHB Converter Analysis for Input-Output Voltage Variations

The studied topology is illustrated in Figure 5.4a. It consists of two half-bridges with dividing capacitors, coupled through an MF transformer. The primary converter is of voltage-source nature and is connected to the CHB submodule in the studied application. The secondary converter is of current-source nature due to the placement of the inductive element L_o and is finally connected to the EV battery. Figure 5.4b illustrates the equivalent converter circuit referred to the primary side. The transformer has been substituted by its leakage inductance L_σ. In addition, two resistive elements have been added, namely R_{eq} and R'_o, representing the input modeled voltage source (U_{eq}) and the output inductor ($L'o$) and EV battery inner resistances, respectively.

The main waveforms of a DHB converter are shown in Figure 5.5. The operating principle of the DHB lies in the shifting of the transformer secondary voltage u_{sec} in regard to the primary voltage u_{pri} by a phase-shift δ. In this way, a specific amount of active power is transferred between the two transformer sides by means of the leakage inductance L_σ.

(a)

(b)
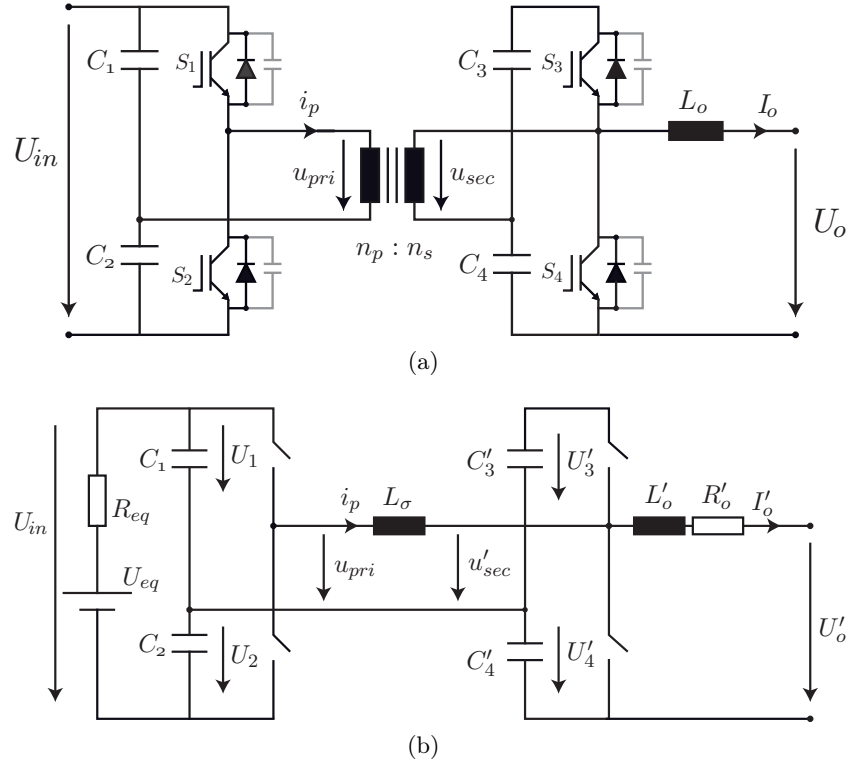
Figure 5.4: (a) The dual half-bridge topology with current-fed output bridge, (b) primary referred dual half-bridge equivalent electrical circuit.

Soft-Switching Operation

The converter offers natural zero voltage switching (ZVS) transitions for the turn-on of all devices. In order to achieve the same conditions during the turn-off instants as well, snubber capacitors can be added to the circuit, as illustrated in Figure 5.4a. Works such as [127,128] have shown that the duty cycle D of the two half-bridges can be also used as a degree of freedom for extending the ZVS region as well as minimizing the transformer *rms* current value. The ZVS conditions can be ensured for any loading conditions when the ratio of $U_o'/(DU_{in})$ is almost unity, where U_o' is the primary-referred output voltage. In the studied system, both U_{in} and U_o are experiencing significant variations. At the input, U_{in} is buffering the low-order harmonic oscillation of double the grid frequency, which is the result of the intrinsic single-phase submodule nature. At the output, U_o is also varying according to the battery SoC as well as the EV battery type. In practical cases, the duty cycle change is limited within a specific range, since it implies a different charge level of the four dividing capacitors C_{1-4}.

The authors of [129] are modeling the second-order harmonic frequency of U_{in} and maintain ZVS in a wide operating range, but the investigated case regards fixed duty cycle and U_o. In the UFCEV system, a duty cycle control is preferable due to the varying U_o and therefore an extension of the analysis is needed. For the extraction of the soft

switching conditions, the knowledge of the transformer and output inductor currents i_p and I_o at the switching instants is needed. Such equations can be found in literature for boost converter mode [128,129], but are also derived and given here following the buck-mode conventions of Figure 5.4 and for the sake of completeness.
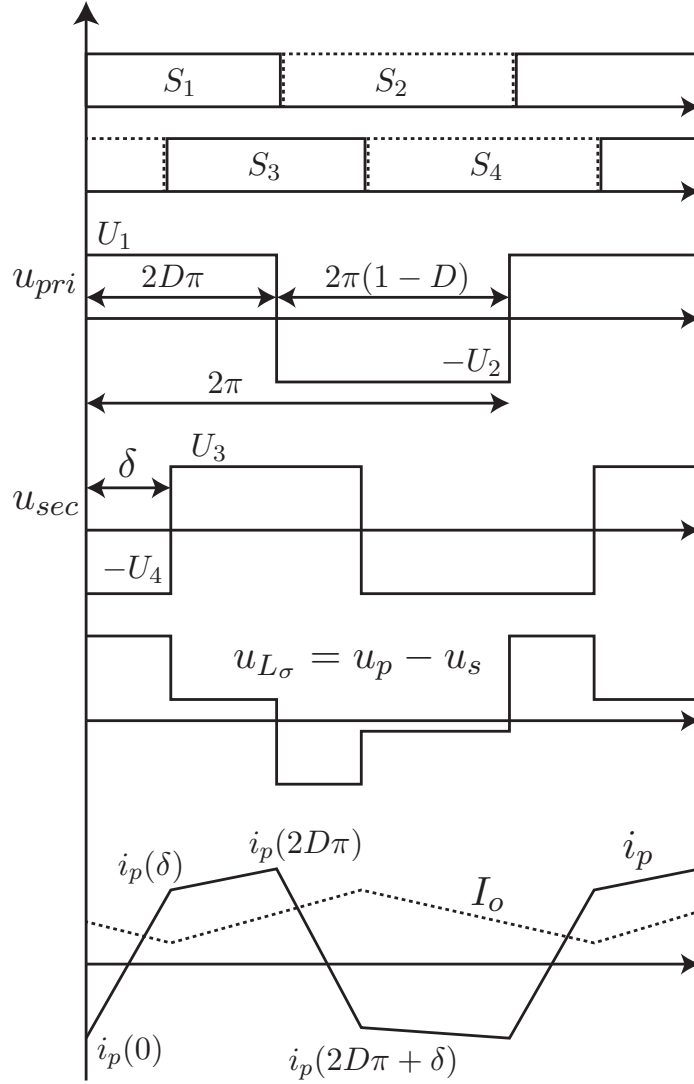
Figure 5.5: Main operation waveforms of a DHB converter.

Defining an allowable ripple factor time variable of the input voltage U_{in} as k_r, the four capacitor voltages U_{1-4} can be expressed as

$$
\begin{aligned}
U_1 &= (1 - D)k_r U_{in} \\
U_2 &= D k_r U_{in} \\
U_3 &= \frac{1 - D}{D} U_o \\
U_4 &= U_o
\end{aligned}
\tag{5.1}
$$

By referring the circuit to the primary, as shown in Figure 5.4b, the instantaneous transformer current is given by the four following equations

$$
\begin{aligned}
i_p(\omega_s t) &= i_p(0) + \frac{U_1 + U_4'}{\omega_s L_\sigma}(\omega_s t), \quad 0 \leq \omega_s t < \delta \\
i_p(\omega_s t) &= i_p(\delta) + \frac{U_1 - U_3'}{\omega_s L_\sigma}(\omega_s t - \delta), \quad \delta \leq \omega_s t < 2D\pi \\
i_p(\omega_s t) &= i_p(2D\pi) - \frac{U_2 + U_3'}{\omega_s L_\sigma}(\omega_s t - 2D\pi), \quad 2D\pi \leq \omega_s t < 2D\pi + \delta \\
i_p(\omega_s t) &= i_p(2D\pi + \delta) - \frac{-U_2 + U_4'}{\omega_s L_\sigma}(\omega_s t - 2D\pi - \delta), \quad 2D\pi + \delta \leq \omega_s t < 2\pi
\end{aligned}
\tag{5.2}
$$

where ω_s denotes the angular switching frequency.

By combining (5.1)-(5.2) as well as equating the average transformer current to zero during a period of operation, the transformer current values at the four consecutive switching instants marked in Figure 5.5 are obtained after some manipulations by

$$
\begin{aligned}
i_1 &= K\left\{k_r\pi D\,(D-1) + \frac{U_o'}{U_{in}}\pi\left(1 - D - \frac{\delta}{\pi}\right)\right\} \\
i_2 &= K\left\{k_r\,(D-1)\,(\pi D - \delta) + \frac{U_o'}{U_{in}}\pi\,(1-D)\right\} \\
i_3 &= K\left\{k_r\pi D\,(1-D) + \frac{U_o'}{U_{in}}\,(D-1)\left(\pi - \frac{\delta}{D}\right)\right\} \\
i_4 &= K\left\{k_r\pi D\left(1 - D - \frac{\delta}{\pi}\right) + \frac{U_o'}{U_{in}}\pi\,(1-D)\right\}
\end{aligned}
\tag{5.3}
$$

where $K = U_{in}/(\omega_s L_\sigma)$ and $U_o' = nU_o$, $n = n_p/n_s$.

For $\delta < \min\{2D\pi, 2(1-D)\pi\}$ and $0 < D < 1$, the average active power transfer is calculated as

$$
P_o = \frac{1}{2\pi}\int_0^{2\pi} u_{pri} \cdot i_{pri} \cdot d(\omega_s t) = \frac{k_r U_{in} n U_o \delta}{4\pi\omega_s L_\sigma}\left[4\pi\,(1-D) - \frac{\delta}{D}\right]
\tag{5.4}
$$

leading to an average output current of

$$
\overline{I_o} = \frac{P_o}{U_o} = \frac{k_r U_{in} n\delta}{4\pi\omega_s L_\sigma}\left[4\pi\,(1-D) - \frac{\delta}{D}\right]
\tag{5.5}
$$

By defining the peak-to-peak inductor current ripple as

$$
\Delta I_o = \frac{2\pi\,(1-D)\,U_o}{\omega_s L_o}
\tag{5.6}
$$

the following soft switching conditions are derived for the respective switches turn-on:

$$S_1 : i_1 < 0, \ S_3 : i_2 > I_o^{'min}, \ S_2 : i_3 > 0, \ S_4 : I_o^{'max} > i_4 \tag{5.7}$$

where $I_o^{'min} = \left(\overline{I_o} - \Delta I_o/2 \right)/n$, $I_o^{'max} = \left(\overline{I_o} + \Delta I_o/2 \right)/n$.

Since both U_{in} and U_o are varying, it is beneficial to present a graph of the phase-shift δ in function of the voltage ratio U_o'/U_{in}. The investigated system parameters are given in Table 5.1 and regard a down-scaled laboratory prototype, which aims at testing of the basic control and modulation functions of the proposed ultra-fast charger. Figure 5.6 shows that an acceptable change in the duty cycle can cover practically all load conditions, providing ZVS for all switches. The latter can be achieved by detecting the converter operating point in real-time and choosing the respective duty cycle value.

Table 5.1: DHB Simulation/Down-Scaled Prototype Parameters

Quantity	Value	Comment
U_{in}	50±10% V	Input voltage (submodule)
U_o	19-31 V	Output voltage (EV battery)
n_p/n_s	1	Transformer ratio
C_{1-4}	2.7 mF	Capacitance
L_σ	1.5 μH	Transformer leakage inductance
L_o	15 μH	Filter inductance
R_o	0.1 Ω	Filter/battery resistance
f_s	50 kHz	Switching frequency
δ_n	$\pi/6$ rad	Nominal phase-shift angle

As stated in [128], the output current ripple provides the ZVS conditions for the secondary switches in light load operation. Therefore, there is a trade-off in the inductance value choice between switching and conduction losses. Certain loads, such as EV batteries, are not to be fed with high ripples. In the studied UFCEV system this can be achieved by interleaving the converter outputs, while maintaining the ZVS conditions for each module. Otherwise, additional passive filtering elements are needed to achieve load current ripple suppression [129].

5.2.2   Current Control of a Dual Half-Bridge

The ultra-fast battery charging is typically limited by its internal electrochemical processes and can be therefore executed up to a point of about 80% of its state of charge. During this period, a constant current has to be provided to the battery. This implies the need for an accurate control method derivation at the output of the parallel-connected dual half-bridges.
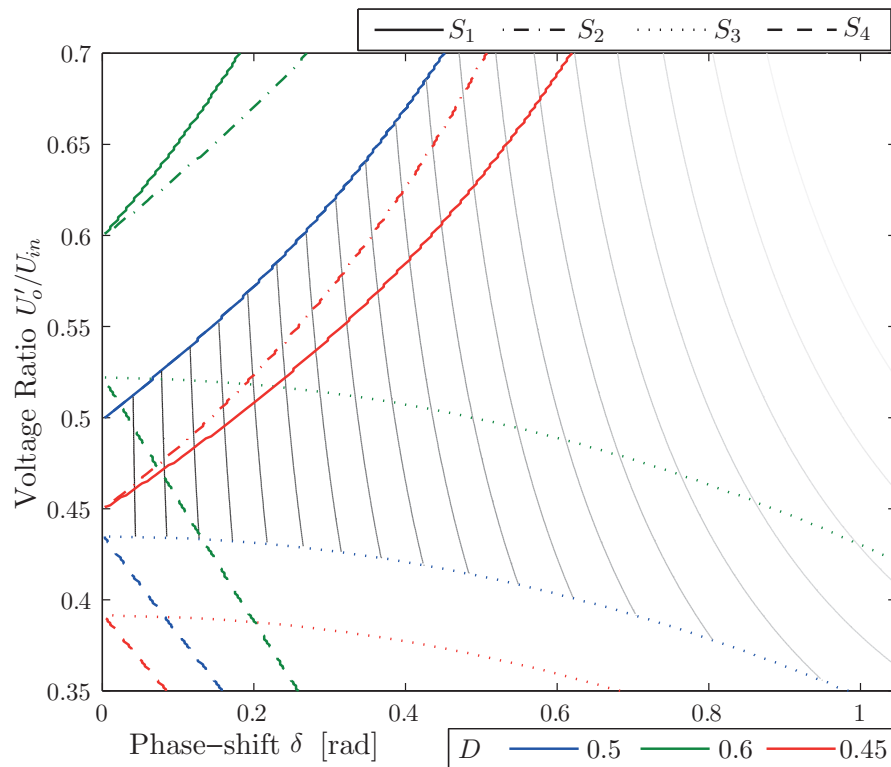
Figure 5.6: ZVS regions of the DHB converter in regards with the output/input voltage ratio. The effect of duty cycle change is visible. The contour lines are representing constant power in the case of $D = 0.5$. Output inductance value is set to $L_o = 10\ \mu$H.

In this chapter a discrete-time control method is proposed, whose design is based on convex optimization. The basic idea is to minimize the absolute error between the open-loop system transfer function and a desired one through the use of nonparametric system models [130,131]. The optimization problem is also subject to appropriate constraints, in order to ensure the closed-loop system stability and desired dynamic performance. Throughout this section, the design process for the studied system is described and analyzed.

Nonparametric Model Derivation

The dual half-bridge converter exhibits non-linearities and dynamics of high order, due to the existence of several passive elements. The required nonparametric model of the single-input single-output (SISO) system, considering the phase-shift δ as input and the current I_o as output, can be derived from a duty-cycle dependent analytical average system model, such as by modifying the one given by [129,132]. Since the output current switching-related ripple is high, a low-pass filter is required on a control algorithm level. Thus, the output is defined finally as I_o^f, in order to account for the latter as well. By linearizing it around several operating points, a family of desired models can be derived.

133

The analytical model of the studied system is given in Appendix D.

Alternatively, the nonparametric model of the system can be found by using an identification process. In order to do so, the system is excited by means of a specific signal, e.g., pseudo random binary sequence (PRBS) and the outputs are observed [133]. The system frequency response for a i-th operating point is then identified as

$$G_i(j\omega) = \frac{\mathscr{F}(I_{o,i}^f)}{\mathscr{F}(\delta_i)} \tag{5.8}$$

where $\mathscr{F}$ represents the Fourier transform. The same procedure can be repeated for m operating points leading to a family $\mathscr{G}$ of nonparametric models

$$\mathscr{G} = \{G_i(j\omega); i = 1, ..., m; \omega \in \mathbb{R}\} \tag{5.9}$$

The aforementioned concept has been followed for this work. The down-scaled system, whose parameters are given in Table 5.1, has been identified by means of simulations for five operating points: 1) $D = 0.5$, $U_o = 25$, $\delta = \pi/6$ (G_1), 2) $D = 0.4$, $U_o = 19$, $\delta = \pi/6$ (G_2), 3) $D = 0.6$, $U_o = 31$, $\delta = \pi/6$ (G_3), 4) $D = 0.6$, $U_o = 28$, $\delta = \pi/16$ (G_4), 5) $D = 0.45$, $U_o = 22$, $\delta = \pi/16$ (G_5).
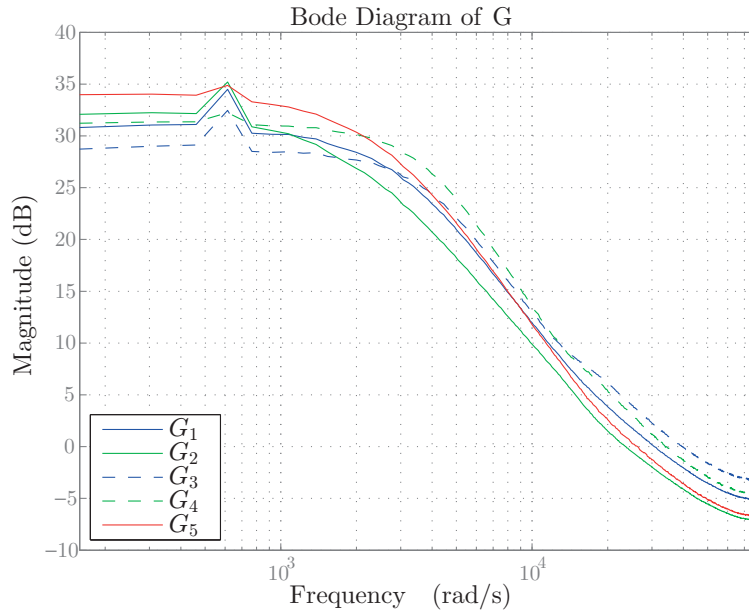
Figure 5.7: Identified nonparametric system models for $R_o = 0.1$ Ω.

Figure 5.7 shows the bode diagrams for the nonparametric models of the studied system. The behavior of the latter does not change significantly in regard to operating conditions. A resonance exists at double the grid frequency, which is a result of the single-phase power pulsation. This sets an additional requirement for the control system design, which

regards the decoupling of the second-order input current harmonic (submodule) from the output (EV battery).

Controller Class

In order to form the open-loop transfer function of the system to be controlled, the class of the controller needs to be determined. From the curves in Figure 5.7 it can be judged that a PI-controller is sufficient for controlling the system with a very good dynamic performance. However, the 100-Hz component also has to be compensated for. The latter can be achieved by adding a resonant term to the controller, tuned at this desired frequency. The overall controller transfer function in z-domain is obtained as [134]

$$K(z, \rho) = \frac{\rho_1 + \rho_2 z^{-1}}{1 - z^{-1}} + \rho_3 \frac{b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{5.10}$$

The second term represents a discrete-time resonant controller, where ω_h is the desired frequency and $\zeta = 3/\omega_h$ the damping ratio. The coefficients a_{1-2} and b_{1-2} are determined by

$$b_1 = 1 - \alpha \left(\beta + \frac{\zeta \omega_h}{\omega_b} \eta \right), \ \ b_2 = \alpha^2 + \alpha \left(\frac{\zeta \omega_h}{\omega_b} \eta - \beta \right)$$
$$\alpha_1 = -2\alpha\beta, \ \ \alpha_2 = \alpha^2 \tag{5.11}$$

where $\omega_b = \omega_h \sqrt{1 - \zeta^2}$ for $\zeta < 1$, $\alpha = e^{-\zeta \omega_h T_s}$, $\beta = \cos(\omega_b T_s)$, $\eta = \sin(\omega_b T_s)$ and T_s denotes the controller sampling time, which is set to 100 μs.

The open-loop system transfer function of the i-th operating point therefore becomes $L_i(j\omega, \rho) = K(j\omega, \rho)G_i(j\omega)$, leading to a respective family $\mathscr{L}$ of open-loop functions

$$\mathscr{L} = \{L_i(j\omega); i = 1, ..., m; \omega \in \mathbb{R}\} \tag{5.12}$$

Optimization-based Loop Shaping

The loop shaping of (5.12) is performed through an optimization procedure. In order to achieve this, the following cost function should be minimized [130,131],

$$\min_{\rho} \sum_{i=1}^{m} \|L_i(\rho) - L_D\|^2 \tag{5.13}$$

which is the square second norm of the errors between the open-loop transfer function of the system $L_i(j\omega, \rho)$ with a desired one L_D for all systems $i = 1,...,m$. The latter is chosen according to the system requirements, i.e., as the addition of an integral and a

resonant terms:

$$L_D(s) = \frac{\omega_{c1}}{s} + \frac{\omega_{c2}}{s^2 + 2\zeta\omega_h s + \omega_h^2} \tag{5.14}$$

For this thesis the values have been set to $\omega_{c1} = 1e3$ and $\omega_{c2} = 40e3$ rad/s, respectively.

The optimization problem is subject to several constraints, which aim at ensuring the stability as well as dynamic performance of the controller [130,131]. The resulting problem is a semi-infinite problem (SIP) including infinite number of constraints and finite number of states. In order to simplify it, only a finite number of frequency points are taken, e.g. in the interval $[0\ \omega_{max}]$. This transforms the problem to a semi-definite problem (SDP), which can be solved utilizing standard respective solvers.

By choosing N linearly-spaced frequencies within the range of $[0\ \omega_{max}] \in \mathbb{R}$, an approximation of the quadratic objective function can be carried out as [130,131]

$$\sum_{i=1}^{m} \|L_i(\rho) - L_D\|^2 \approx \sum_{i=1}^{m}\sum_{k=1}^{N} \|L_i(j\omega_k, \rho) - L_D(j\omega_k)\|_F \tag{5.15}$$

where $\|.\|_F$ denotes the Frobenius norm. Therefore, the following optimization problem is finally deduced:

$$\min_{\rho} \sum_{i=1}^{m}\sum_{k=1}^{N} \|L_i(j\omega_k, \rho) - L_D(j\omega_k)\|_F \tag{5.16}$$

subject to the respectively modified discrete linear constraints.

The aforementioned technique has been applied only for the case of the identified model G_1 of the rated system. The results of the numerical procedure are: $\rho_1 = 0.0132$, $\rho_2 =$ -0.0106 and $\rho_3 = 0.0217$.

For more information on the formulation of constraints as well as several applications of this control method on power electronics systems, the reader is referred to works such as [130,131,134,135].

Control Design Validation and DHB Parallel Connection

The effectiveness of the power decoupling for the input and output currents is demonstrated by the simulation results of Figure 5.8. Initially, the system is controlled only by means of the PI-controller. The output current features a significant 100-Hz component, which should not be absorbed by the EV battery. At $t = 20$ ms, the resonant term is activated and almost eliminates the output current oscillation by changing the amplitude and phase of the respective harmonic in the transformer phase-shift δ.

The Cascaded H-Bridge active front end stage gives a significant degree of freedom for choosing the number of submodules feeding each charging port. Except from the resonant controllers, which compensate for the second harmonic locally on the level of each DHB, a parallel connection between different phases is at hand which permits a further reduction. An additional advantage of interconnecting isolated modules from the three-phases comes from the fact that the symmetry of the three-phase currents can be maintained during the EV ultra-fast charging without the need for common-mode voltage injection [68].
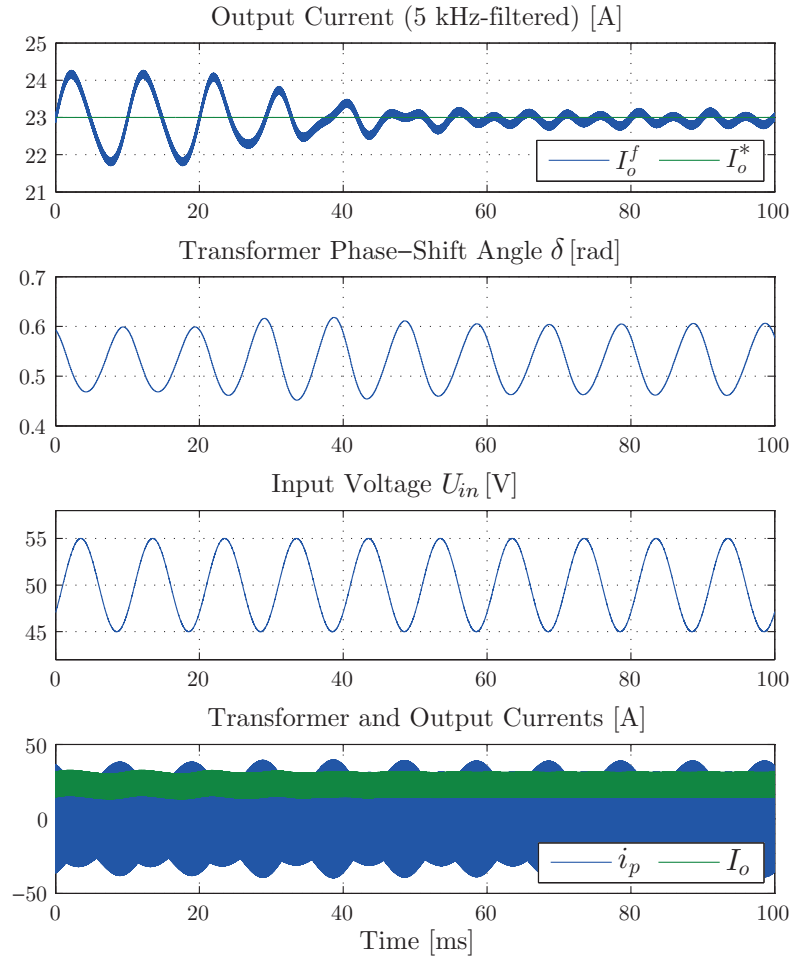
Figure 5.8: Simulation results of the resonant controller activation.

A simulation model consisting of six parallel-connected dual half-bridge modules has been also built and tested. The connection takes place as two submodules/phase, as for the upper charging port illustrated in Figure 5.3. By interleaving the outputs, a number of six converters with a duty cycle of $D = 0.5$ lead to a perfect switching ripple compensation. The simulation results for a reference step change are illustrated in Figure 5.9. The EV battery current reference $I_o^{\Sigma *}$ is equally split between the individually current-controlled DHBs. The controller presents a good dynamic performance. The worst-case scenario has been simulated in terms of input voltage ripple, i.e., that even after the transient the grid

power is kept constant and the excess is charging the stationary submodule batteries. The second harmonic resonance is slightly excited during the transient but it is compensated by the resonant term. Higher resonant control gains might damp the resonance more rapidly, but are not preferred since the latter could lead to implementation issues and the control speed is not the main issue in such an application.
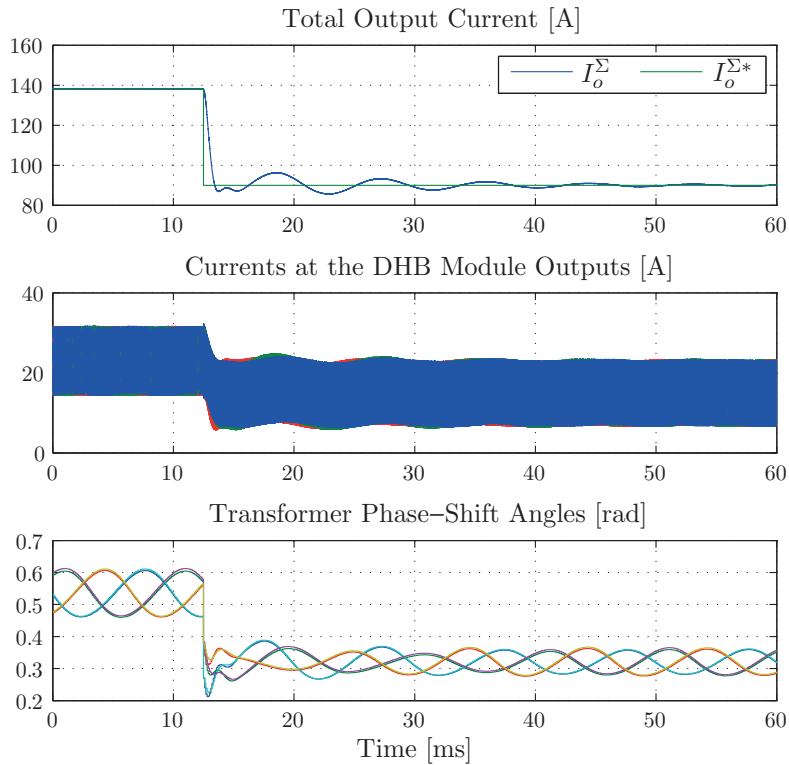
Figure 5.9: Simulation results of the six parallel-connected closed-loop controlled DHB modules during a current reference step change.

Current Control in Low Output Resistance Case

So far, the system has been assumed to have a resistance of $R_o = 0.1$ Ω at its output, considering both the battery and inner inductance resistances. In a high current application, however, the output resistance is expected to be minimized both for efficiency purposes and because of the parallel-connection of EV battery strings which achieves higher capacities. In this paragraph, the analysis is performed once again for an operating scenario of $R_o = 100$ mΩ. The identification procedure is repeated for the same system operating points G_{1-6}. From Figure 5.10 it can be observed that a significant undesired resonance exists due to the high-order of the system and the interaction of its passive elements. This is further complicated by the fact that the resonance is depending on the

duty cycle value and is characterized by the following relation:

$$\omega_{res} = D\sqrt{\frac{2}{L_o C}} \tag{5.17}$$
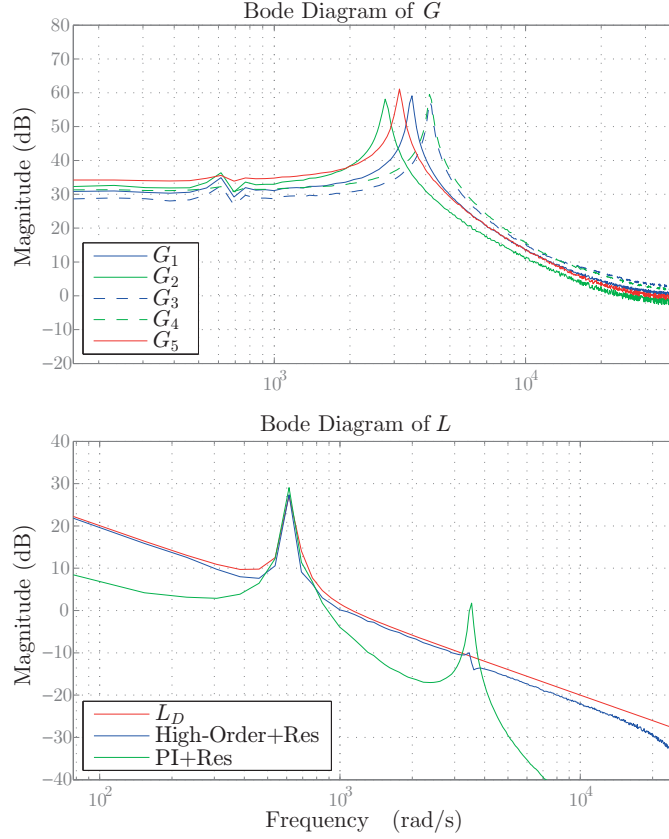
Figure 5.10: Identified nonparametric system models for the case of low output resistance $R_o = 1\ m\Omega$ (upper figure), and the respective results of the loop shaping optimization procedure (lower figure).

This poses difficulties in the control system design. A conventional PI-controller can only compensate for the dominant plant pole and is not capable of adequately attenuating the resonance. The solution to the latter comes through the design of a high-order controller. The transfer function of the 3rd-order controller augmented with a resonant term is given in z-domain by

$$K(z, \rho) = \frac{\rho_1 + \rho_2 z^{-1} + \rho_3 z^{-2} + \rho_4 z^{-3}}{1 - z^{-1}}$$
$$+ \rho_5 \frac{b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{5.18}$$

The results of the optimization-based loop shaping of the rated system G_1 are also shown

139

in Figure 5.10. It is clear that the PI-controller is not capable of following the reference curve L_D and attenuating the resonance, whereas the 3rd-order controller can provide the desired transfer function. The results of the optimization procedure give: $\rho_1 = 0.0092$, $\rho_2 = -0.0033$, $\rho_3 = -0.0162$, $\rho_4 = 0.0131$, and $\rho_5 = 0.0187$.

A current reference step change has been simulated and the results are depicted in Figure 5.11. The control system provides a good dynamic performance. The undesired system resonance is visible during the transient as a superimposed component on the second-order harmonic, which is also slightly excited without having a significant impact and is quickly compensated by the resonant term.
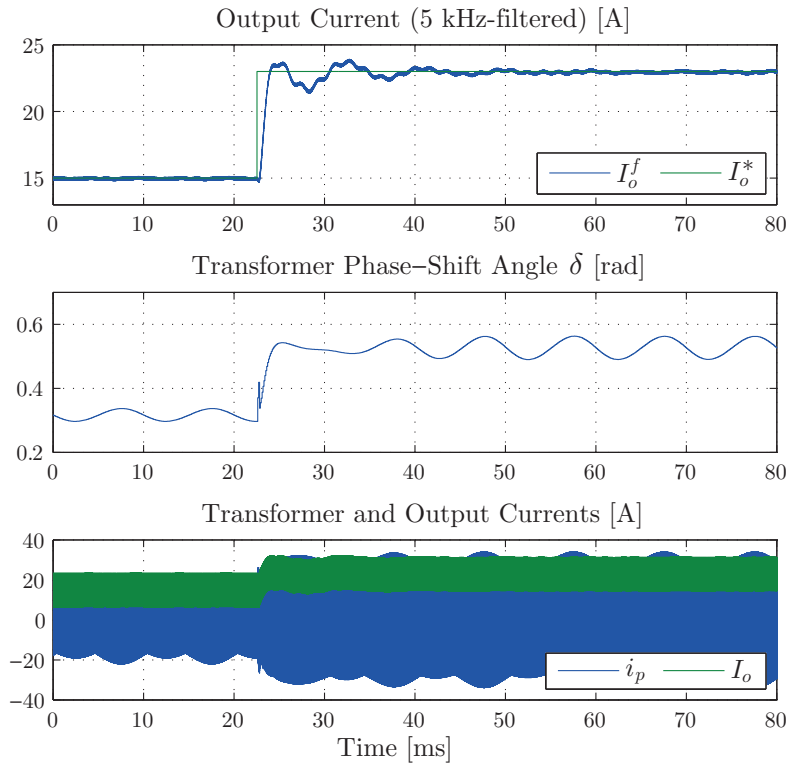
Figure 5.11: Simulation results of the low output resistance closed-loop controlled system during a current reference step change.

5.2.3 Experimental Tests

A down-scaled laboratory prototype has been developed for the verification of the afore-mentioned concepts. The system parameters are the ones given in Table 5.1. A number of four dual half-bridges have been built, which are backplane-connected and integrated into a standard rack. The hardware and software development elements of the converters are also explained in Appendix A. The implemented setup is illustrated in Figure 5.12.

Figure 5.12: The experimental setup of the dual half-bridge-based isolation stage.

The initial experimental tests, which have been carried out, do not consider the second-order harmonic of the input current. The EV battery is emulated by a variable voltage source. Since the latter cannot absorb any power, a variable resistance is placed in parallel.

Figure 5.13 shows the basic circuit waveforms for one DHB module under different operating point conditions. More specifically, the two phase-shifted transformer voltages u_{pri} and u_{sec} are depicted along with the transformer (i_p) and output (I_o) currents. The input voltage U_{in} is provided by a fixed voltage source and is set to 50 V.

In a second step, all four modules are tested in a series-input/output-parallel configuration, i.e., a single voltage source of 200 V feeds their series-connected inputs. The common output is set to $U_o = 25.6$ V, which refers to the battery nominal voltage. The results of this test are shown in Figure 5.15. Since the output inductances are low the individual ripples are high, something which allows ZVS conditions at light loads as mentioned before. However and due to the interleaving of four channels with 0.5 duty cycle each, the total battery current I_{Bat} is completely ripple-free without the use of additional passive elements.
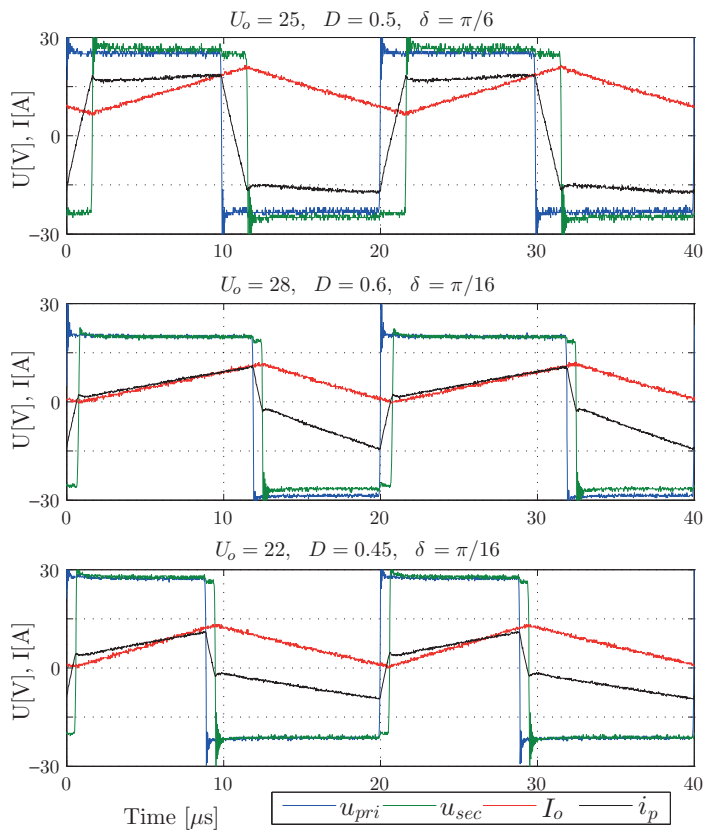
Figure 5.13: Experimental results for one DHB module in several operating points of different output voltage U_o, duty cycle D and phase-shift δ.
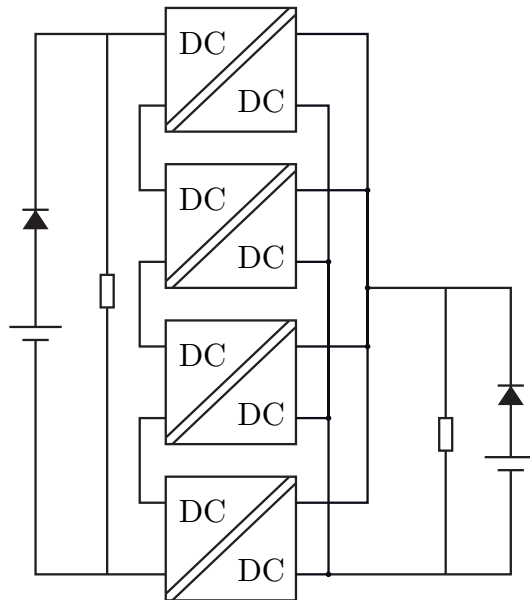
Figure 5.14: Schematic of the experimental setup circuit configuration (DHBs).
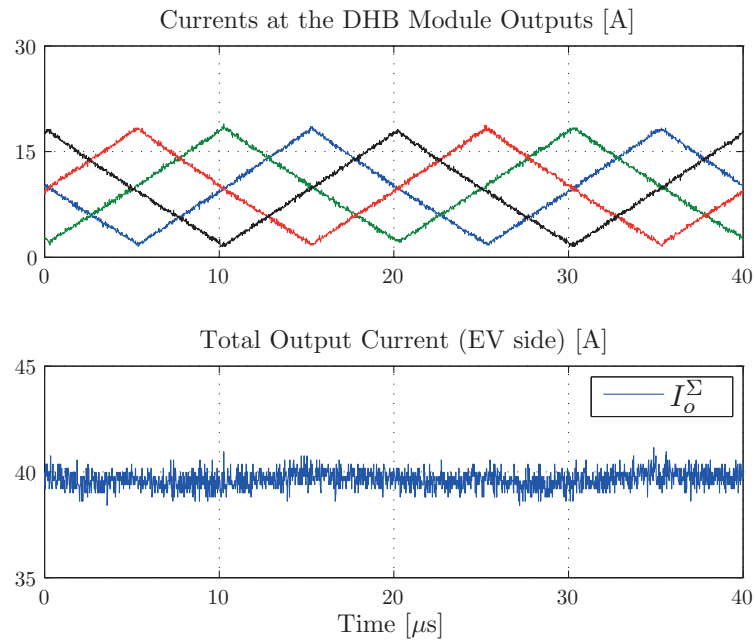
Figure 5.15: Experimental results for the parallel connection of the four DHB modules.
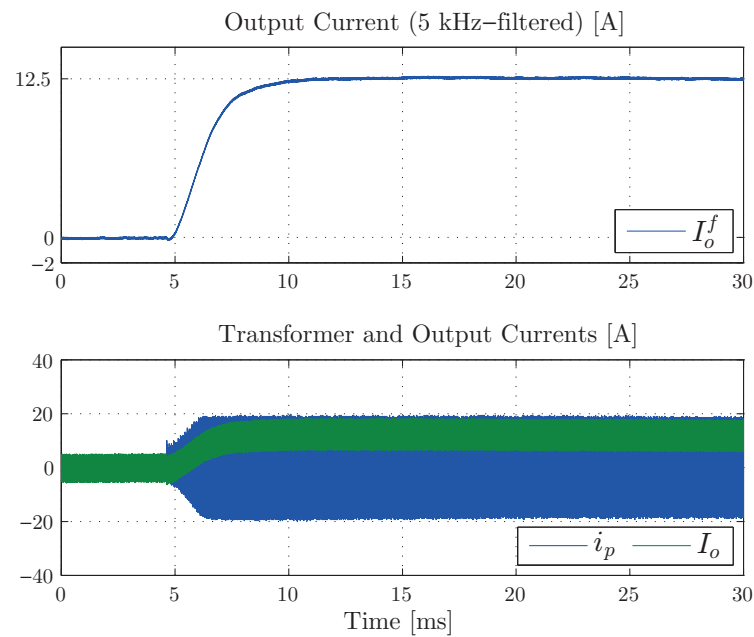
Figure 5.16: Experimental results for a reference step change from 0 to 12.5 A.

Finally, Figure 5.16 validates the closed-loop control design for one DHB module. At $t \approx$ 5 ms, an output current reference step change takes place from 0 to 12.5 A. The average value of the output current gradually reaches the new desired value without exhibiting any overshoot and without steady state errors, as it has been posed in the control design requirements. Furthermore, no saturation of the transformer current is observed.

143

5.3 Global Charging Station System Control

The overall three-phase PET-based system of Figure 5.2 from grid to EV batteries is now treated. The implementation of a whole conversion chain is depicted in Figure 5.17. The CHB converter submodule is implemented by means of a full-bridge. The IAI concept is used to interface the submodule to the battery energy storage buffer, in order to prevent the second-order DC-link current harmonic from flowing into the latter, as having been explained throughout Chapters 3 and 4. The dual half-bridge finally completes the whole conversion chain.

It is noted that the superscript/subscript $k \in \{a, b, c\}$ (star) or $\{ab, bc, ca\}$ (delta) refers to the k-th CHB converter branch and $i \in \{1, ..., N\}$ to the i-th submodule of the respective branch. According to the active power direction illustrated in Figure 5.17, the following relation holds for the ik-th conversion chain:

$$P_{EV}^{ki} = P_{sm}^{ki} - P_{bat}^{ki} = \left(\frac{P^k}{N} + \Delta P_{sm}^{ki} \right) - P_{bat}^{ki} \tag{5.19}$$

The proposed global control system is illustrated in Figure 5.18, together with all associated feedback variables and control signals. This is very similar to what has been shown in Figure 3.14 for the CHB-BESS case. The main difference regards the addition of the current control block for the isolation stage. The blocks included in dashed rectangles are executed either in the case of star- or delta-configured CHB converters. Moreover, the feed-forward power component for the IAI current control now consists of the additional term P_{EV}^{ki}, which fulfills the power equation of (5.19).
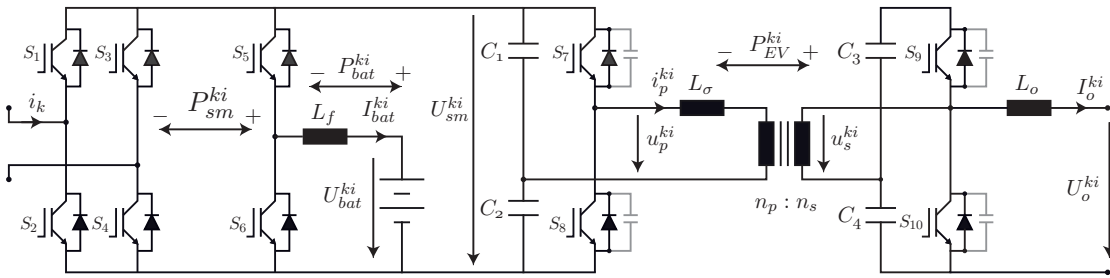
Figure 5.17: Implementation of a whole conversion chain for the proposed topology.
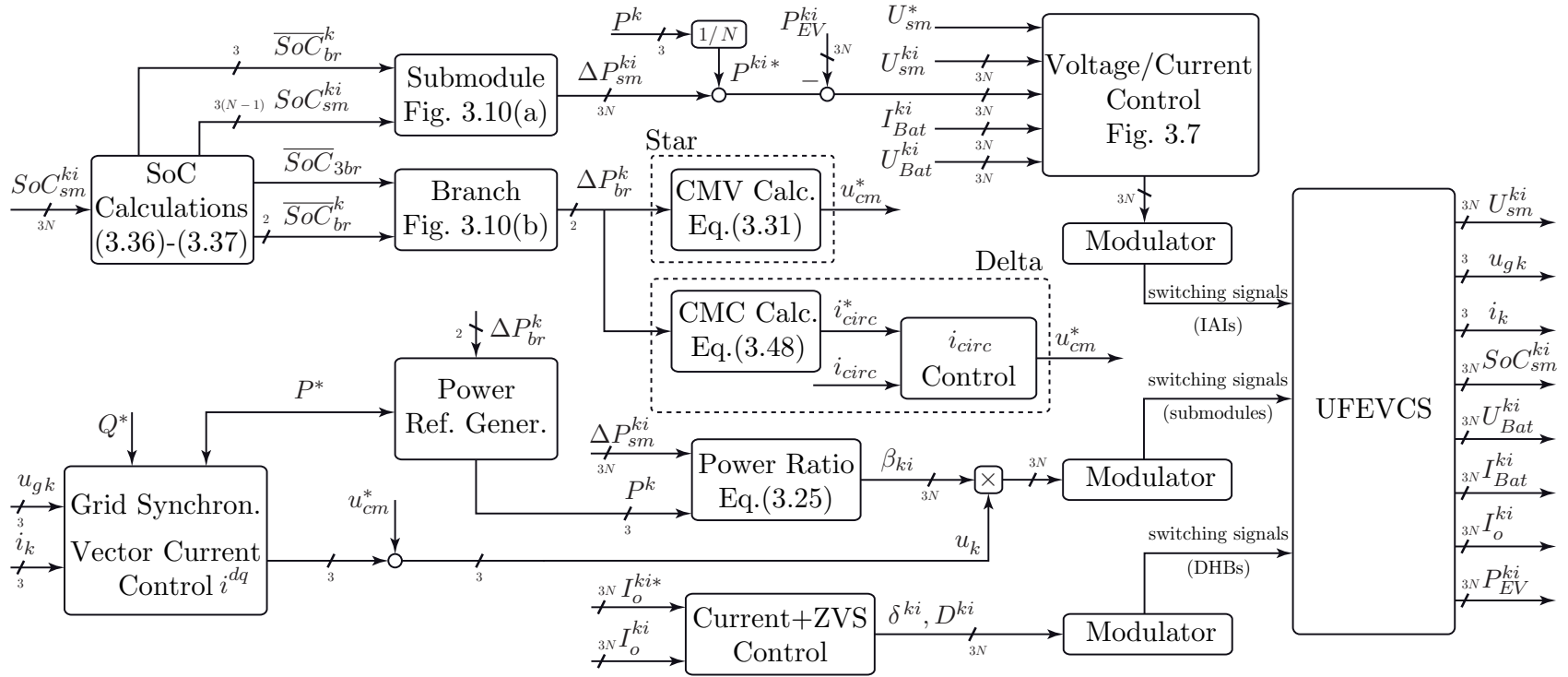
Figure 5.18: Overall ultra-fast EV charging station system control block diagram.

5.3.1   Simulation Model and Results

In order to verify the effectiveness of the proposed control system, a simulation model of the whole PET-based EV charging station has been built. Since the PWM effects are of no significant interest compared to the evolution of magnitudes with high time constants, the switching-averaged power converter models have been considered for all conversion stages. For the DHB converters the utilized model, which neglects the AC transformer quantities, is derived in Appendix D. The details for the parameters of the studied system as well as the charging station configuration are given in Table 5.2. A diagram of the considered PET-based ultra-fast EV charging station configuration is also illustrated in Figure 5.19.

Table 5.2: UFEVCS Simulation/Down-Scaled Prototype Parameters

Quantity	Value	Comment
N	6+2	Submodules/branch (w. redundancy)
N_{ch}	4	Charging ports (6 submodules each)
$\tilde{u}_{gk}$	140 V	Grid rms phase voltage
$U_{bat,n}^{ki}$	25.6 V	Nominal battery voltage
$Q_{bat,n}^{ki}$	3 Ah	Nominal submodule battery capacity
C_{1-4}	2.7 mF	Submodule/DHB capacitance
U_{sm}^{ki}	50±10% V	Submodule voltage (star-CHB)
L_f	1 mH	IAI filter inductance
U_o^{ki}	19-31 V	DHB output voltage (EV battery)
$Q_{EV,n}^{1-3}$	20 Ah	Nominal EV battery capacity
$n_p : n_s$	1	DHB transformer ratio
L_σ	1.5 μH	DHB transformer leakage inductance
L_o	15 μH	DHB filter inductance
δ_n	$\pi/6$ rad	DHB nominal phase-shift angle

Figure 5.20 shows the simulation results for the different operating modes of the converter architecture utilizing a hypothetical power profile. In Mode I, the converter behaves as an ultra-fast EV charger. It is assumed that the three out of four EV charging ports are used, whereas the fourth is in idle mode. The three EVs arrive at the station with a time difference of one minute and are charged within ten minutes each. The three ports charging the EVs will cause a discharge to the stationary intermediate batteries, whereas the fourth port will be charging the respective storage stage. In Mode II, the DHBs are not operating and the converter structure extracts active power from the grid, in order to recharge the power buffers. Accordingly, in Mode III the charging station provides active power to the grid by discharging the intermediate batteries. Finally in Mode IV, no active power is exchanged with the grid or the EVs and the CHB converter operates with its well known functionality of a STATCOM. At the end of the power profile, all battery SoCs are practically the same, due to the SoC balancing controllers that are in action throughout the whole converter operation.
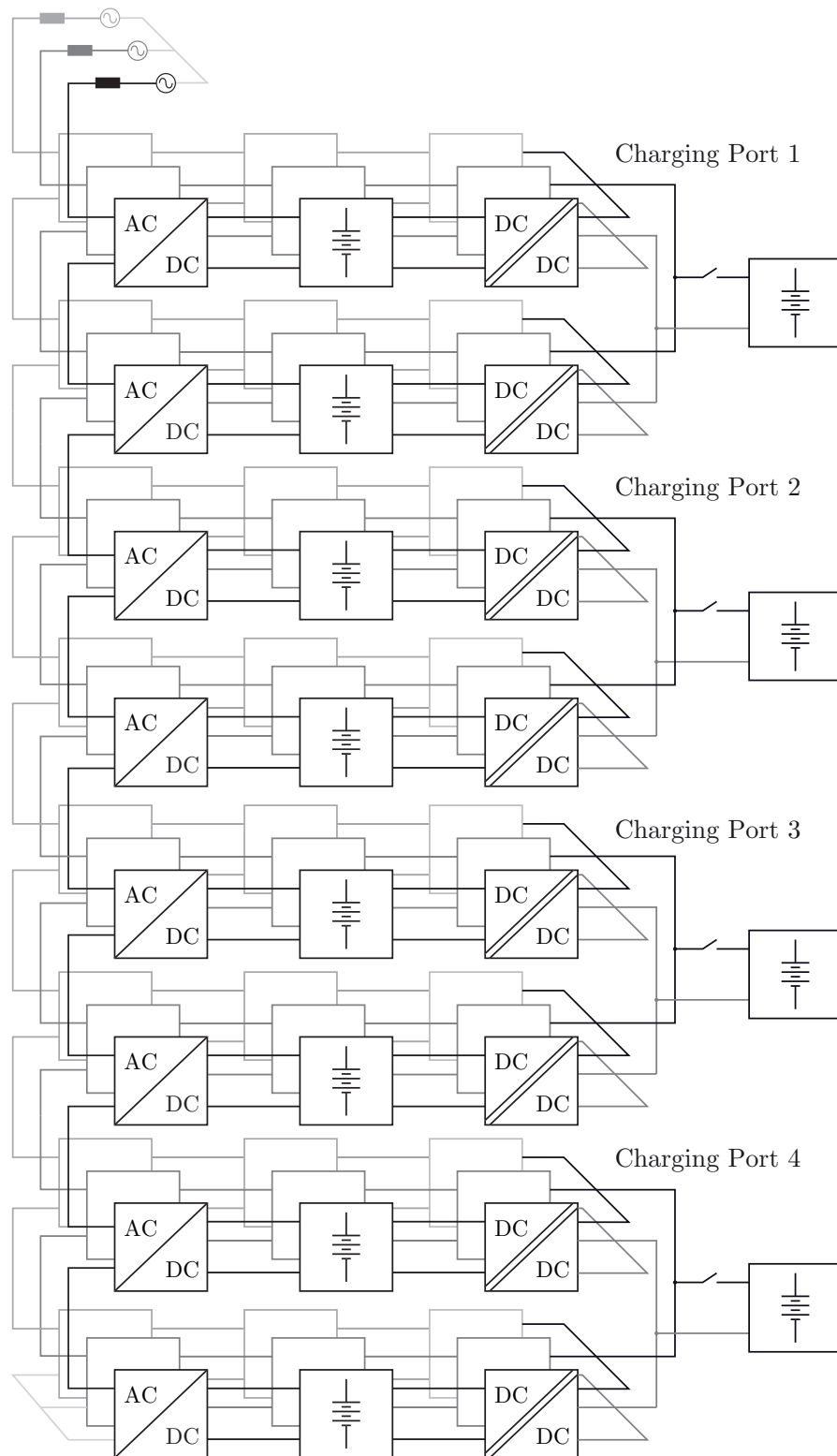
Figure 5.19: The considered simulation model for the PET-based ultra-fast EV charging station.
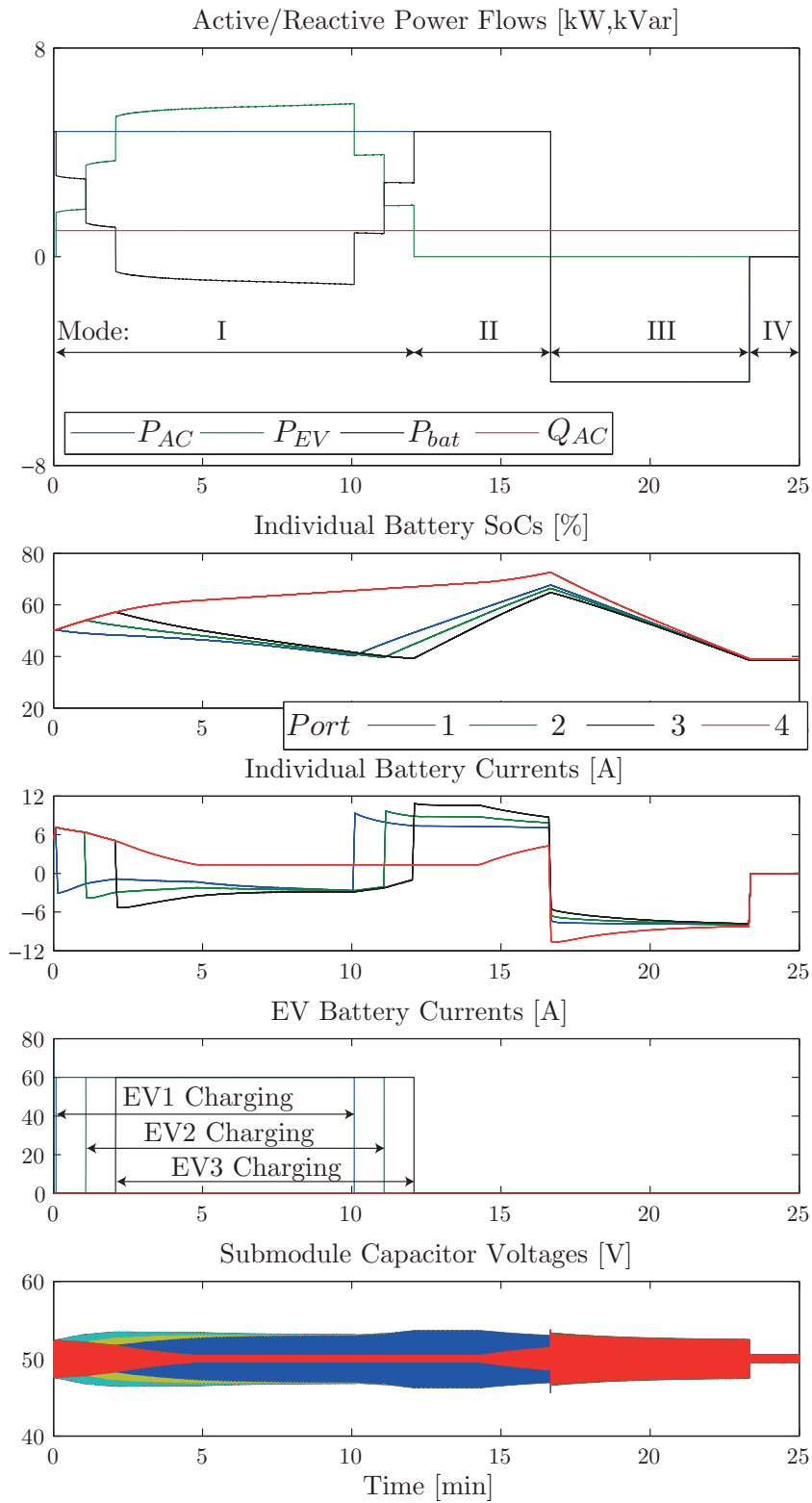
Figure 5.20: Simulation results of the PET-based charging station for a hypothetical power profile, exploiting all operation modes.
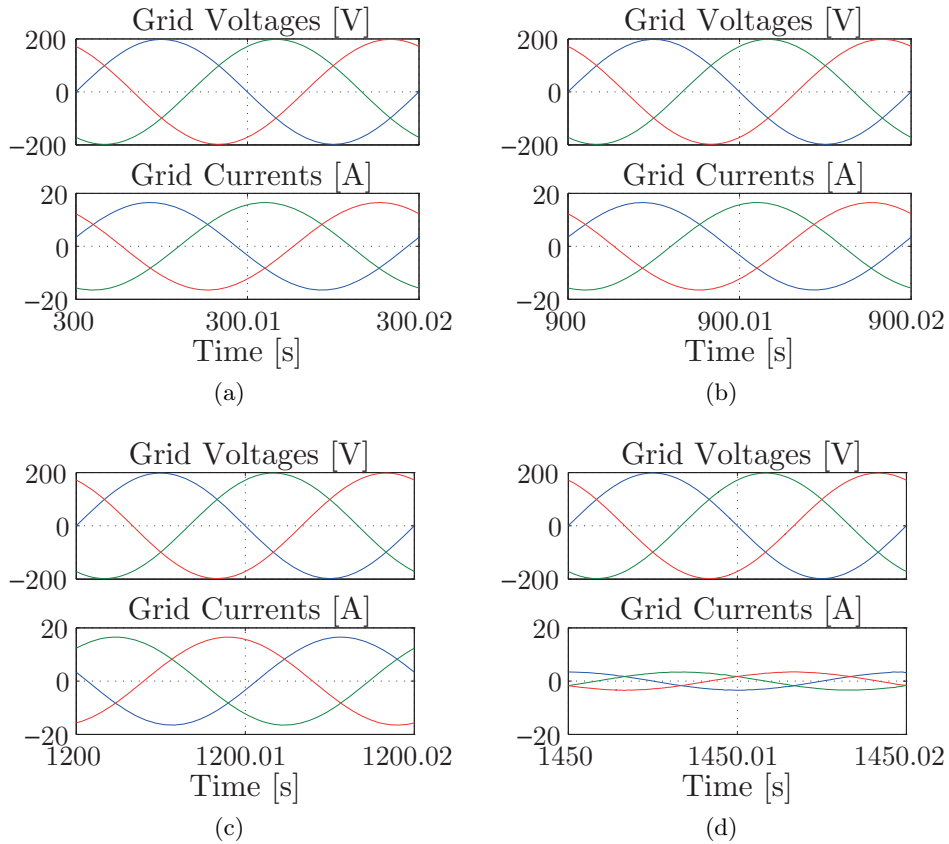
Figure 5.21: Detailed versions of the three-phase grid voltage and current quantities for: (a) Mode I, (b) Mode II, (c) Mode III and (d) Mode IV corresponding to Figure 5.20.

Figure 5.21 shows some details of the three-phase grid voltage and current quantities for different operation modes. It is clear that the control system is capable of keeping the current symmetry unaffected, even during asymmetric load conditions, e.g., when not all EV charging ports are in use and some intermediate batteries are charging while others are discharging. The active power evolution of the four different charging ports is illustrated in Fig. 5.22. It is clear that the submodule SoC balancing power ΔP_{sm} plays a major role in the asymmetric power distribution between the stationary batteries. For example, if a charging port is not used, the grid power fed to it will be minimal, ensuring a small SoC variation in the respective batteries. On the other hand, the ports that need a larger amount of charging power will absorb more grid power leading to a need for less power coming from the stationary batteries.

The effect of the gain-scheduling controller for the vertical SoC balancing action, which is based in equations (3.38) and (3.42) is depicted in Figure 5.23. It is clear than when the SoC deviation exceeds a predefined value, the rise time of the closed-loop control system increases. This leads to a respective decrease of the control gain k_p^{sm} in order to avoid saturation of the control action, which would cause submodule overmodulation in this

149
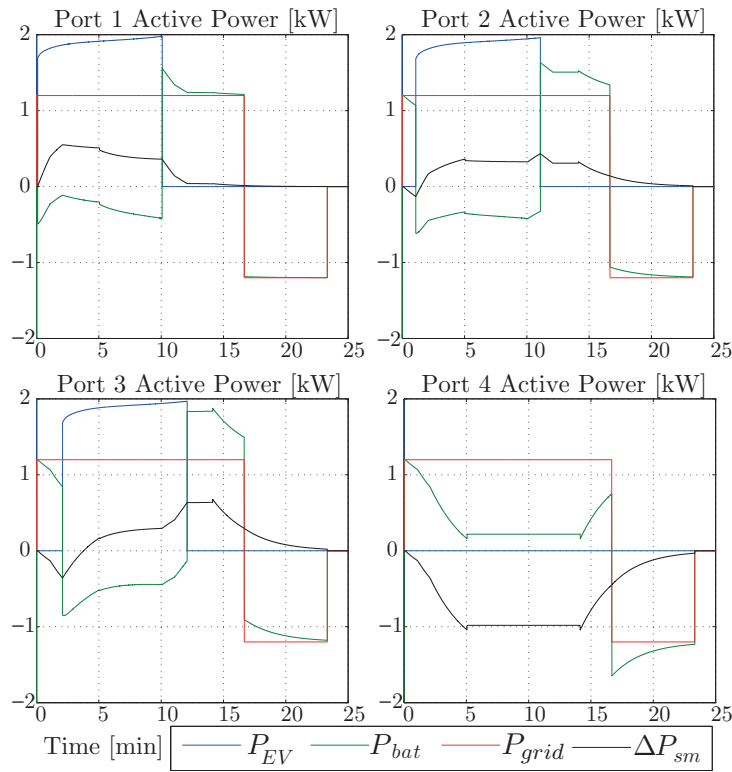
Figure 5.22: Simulation results for the active power distribution within the four charging ports.
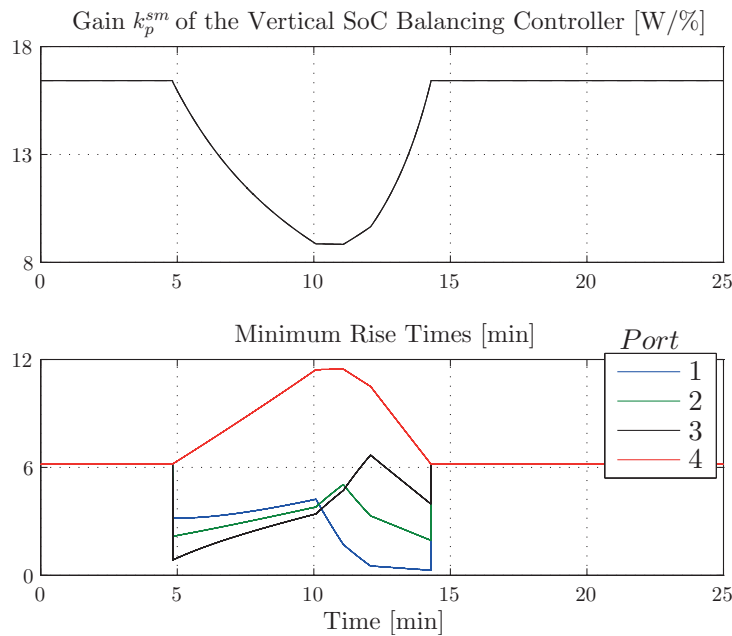
Figure 5.23: Gain scheduling control behavior of the vertical SoC balancing controller.

case. It is once again mentioned that the gain k_p^{sm} has to be the same for all submodules of a branch, in order to ensure that $\Sigma \Delta P_{sm}^{ki} = 0$ and that the grid current controller is not affected.

5.4 Conclusion

This chapter has presented a novel multiport Power Electronic Transformer-based concept for the realization of multifunctional medium voltage ultra-fast EV charging stations. Among the numerous isolated converter topologies, the dual half-bridge converter seems to be a reasonable choice. The DHB converter analysis of the converter has revealed that with a change of the primary and secondary converter duty cycle an extension of the soft-switching region in wide input and output voltage variations can take place. The current control has been designed using nonparametric models, overcoming the challenges posed by the high-order and system nonlinearities.

A global system control structure has been described, which is capable of handling all different power flow directions as well as capacitor voltage and battery SoC unbalances. The operating modes of the system have been presented and simulated, verifying the versatility of the introduced converter structure.

6 Conclusions and Future Research

6.1 Summary and Contributions

Modular Multilevel Converters are undoubtedly expected to play a major role in future large-scale medium- and high-voltage networks. Indeed, features such as a modular design, network friendliness through the injection of currents with very low harmonic contents, redundancy, as well as easy voltage and power scalability, imply evident offered advantages compared to the conventional power conversion concepts. It is no wonder that during the last five years a tremendous academic and industrial interest has been observed in this field. All this comes with a price to pay, i.e., the complexity in terms of physical system behavior, control system design, global hardware and software implementation, as well as arising reliability issues. Even though numerous literature has been appearing, there are many unanswered questions and challenges, as well as constant initiations of novel research directions.

6.1.1 DC/AC Modular Multilevel Converters

This thesis has tried to identify and tackle some of such issues related with the operation and control of such MMC structures. In the field of the DC/AC MMC, which is the most frequently encountered and studied topology, two main aspects have been investigated in Chapter 2.

The first one regards the accurate capacitor voltage ripple estimation without strong assumptions, especially when it comes to taking into consideration the converter branch passive elements. Such an estimation is initially beneficial for converter dimensioning purposes. Indeed, one of the key components of an MMC is the submodule capacitor, which has to buffer low frequency power components, contrary to traditional topologies featuring a central DC-link capacitive filter. This can be probably considered as the main disadvantage of such a topology, since such an element adds cost and volume to the system, and should be therefore chosen in a sensible manner. By knowing exactly the amount

of energy that needs to be stored within a period of operation, such a task becomes straightforward. In addition, the equivalent branch capacitor voltage ripple estimation can be used to ameliorate several of the different control systems proposed in the literature for the inner dynamics of a DC/AC MMC. For the so-called 'open-loop' control schemes, the voltage ripple knowledge is the core of the control system implementation, where the latter needs to be compensated for in real-time through the normalization of the branch modulation references. On the other hand, capacitor voltage closed-loop control schemes can also benefit in the sense of avoiding the use of excessive software filtering for the intrinsic low frequency oscillating components of the phase-leg total and branch difference voltage quantities.

The second aspect of Chapter 2 regards the impact of grid asymmetries on the operation and design of DC/AC grid-connected MMCs. Indeed, the topology specificities, such as the circulating current existence as well as the capacitive nature of the converter phase legs make its analysis different than conventional topologies. With the late research on converters during grid unbalances using symmetrical components, it has been proven possible to control the system without tripping during a system fault and using different techniques to achieve different desired results, such as symmetric grid current injection and active or reactive power oscillation elimination. This thesis has tailored and compared the aforementioned well-established concepts for the case of an MMC. It has been shown that such a converter is able to provide a constant DC-link power during grid unbalances in all three cases, unlike other topologies. However, this has an impact in the dimensioning of the required capacitive storage that will inevitably increase due to the additional low frequency oscillations buffering. If a maximum power transfer is preferred, the balanced current injection is the evident choice. However, the reactive power oscillation canceling offers the best performance in terms of branch energy variation increase while keeping the DC-link power constant and seems therefore a very useful solution. The latter has been also proven to benefit from a second-order harmonic circulating current injection throughout the whole regime of phase loss severity.

Chapter 2 has also documented in a simple and comprehensive illustrative manner the natural charge level mechanism of the branch capacitor voltages, which allows to freely choose the average stored energy. The decoupled line and circulating current control is at this moment a very clear concept used by many researchers. On this level, this thesis has proposed an extension of the fictive axis emulation concept for the implementation of a vector line current control scheme for two-phase MMCs that could be used in three-/single-phase back-to-back railway interties.

6.1.2 Modular Multilevel Converters with Integrated Split BESS

The second axis of this thesis has been the integration of BESS elements into the submodules of Modular Multilevel Converter topologies as well as the global system

operating modes analysis and control. Although an emerging topic, the idea of split energy storage arises interesting questions and technical challenges that need to be handled and evaluated.

In Chapters 3 and 4, three different MMC structures with integrated split BESS have been investigated, i.e. the Cascaded H-Bridge converter in either star or delta configurations as well as the DC/AC Modular Multilevel Converter. Once again, it has to be noted that these topologies should not be considered as competitive regarding their use as application-specific storage units. Instead, there might be cases where a system active power enhancement is needed without, however, changing the conversion character of each topology. For example the CHB-BESS can be either used as an energy storage system interface on its own in the medium- or high-voltage range, providing also its well-established STATCOM services. It can be also used as an active front end stage for power electronic transformers, where additional storage element ports are needed to buffer the extracted instantaneous grid active power. The latter has been shown in the proposed converter architecture of Chapter 5. On the other hand, the DC/AC MMC can be used in HVDC systems where the intermittent nature of energy sources benefits from the use of energy storage devices. In addition, future medium voltage DC networks and active front ends of electric drives or back-to-back railway interties might be needing enhancement through active power source addition. In these cases, the converter remains an DC/AC conversion structure but with embedded storage capability, which benefits from the split storage concept instead of utilizing additional converters for the BESS interface. It is noted, therefore, that in this sense all members of the MMC family illustrated in Figure 1.2 are worth being investigated as Modular Multilevel Converters with integrated split BESS.

For the scopes of this thesis, it has been chosen to eliminate the low-frequency submodule current components on a battery level. The nonisolated buck converter concept between the submodule and the battery has been employed. Moreover, one important contribution of this thesis regards the development of a global hierarchized control method, which is applicable to any MMC topology with integrated split BESS by performing only minor topology-specific modifications. More specifically, it has been proposed to use the submodule/battery IAI concept to control the submodule capacitors, leaving the remaining degrees of freedom for handling the active power flows independently in all possible directions. The latter can be used for the battery SoC balancing, which is essential in cases where a flat curve of the latter in relation to the battery voltage is observed.

All possible operating modes of each of the studied converter topologies have been established, including the necessary control actions under asymmetric grid conditions. It has been also shown that the delta-connected CHB-BESS unit offers an attractive additional operating mode, namely the self-balancing, which permits the SoC convergence without affecting the power grid.

6.1.3   Multiport PET-based Ultra-Fast EV Charging Station Architecture

In the framework of a given application, i.e., the ultra-fast charging of electric vehicles, the concept of power electronic transformers with integrated split battery energy storage has been proposed and investigated as well. A novel versatile PET-based multiport converter architecture has been presented in Chapter 5 as an alternative to the low frequency transformer-based EV charging station with intermediate stationary battery storage buffers and high-power chargers.

The key element of any PET system is evidently the isolated MF-based DC/DC converter. One can choose among a huge number of available topologies with different operating characteristics. For the considered application the main requirements regard a very low charging current ripple, EV battery side current and voltage control capability as well as soft switching over a wide range of input and output voltage variations. Bidirectional power flow is also favorable in cases where a V2G operation is foreseen. The Dual Half-Bridge topology has been chosen since it features minimum number of active devices as well as an input voltage-source behavior (submodule side) in conjunction with a current-source type output (EV battery side). The soft switching regions in function of the input-output voltage variations have been identified. It has been shown that a reasonable adjustment of the converter duty cycle can extend the ZVS regime to almost all loading conditions. In addition, the converter output inductance can be minimized, leading to an extension of the ZVS range for the secondary half-bridge without, however, sacrificing the EV battery current ripple since the interleaving of the several parallel-connected DHB modules is at hand.

Another technical challenge associated with the DHB topology has been tackled in Chapter 5. The latter concerns the output current control, commonly used during a constant current charging technique for an EV battery. This method is also expected to be used in cases of ultra-fast charges, where a maximum of 80% of the SoC is allowed to be reached before significant nonlinearities begin to take place in the inner electrochemical processes. The DHB has several passive elements leading to a high-order nonlinear system with associated resonances. In addition, the inherent second-order submodule capacitor voltage harmonic will be reflected in the EV battery current, if no appropriate further actions are taken.

A transparent control design method based on nonparametric models extracted through system identification has been followed. By executing such a procedure for several operating points, a family of such models can be derived. Once defining an appropriate controller, an optimization procedure minimizes the error between the open-loop control transfer function and a desired one, defining therefore the utilized controller gains. One of the main advantages of this method regards the lack of need for analytical model derivation and linearization. In addition and if executed for the experimental system

itself, the identification procedure takes into consideration all real-time system delays and non-ideal behaviors. Moreover, any controller order type can be specified and designed, accordingly. In the proposed system, the second-order harmonic has been eliminated by adding a resonant term to the controller, keeping the EV battery current unaffected. An enhancement of this effect is also at hand by interconnecting DHB modules from different phases on the level of each port, taking advantage of a natural second-order harmonic canceling due to the three-phase system symmetry. Finally, the undesired resonance due to the system passive element interactions has been overcome through the design of a high-order controller, which offers more degrees of freedom for adequately attenuating it, compared to a simple PI control design.

A final contribution of Chapter 5 regards the proposal of a global control system for the developed multiport UFEVCS, which proves the feasibility of such an implementation and the capability of handling all different port active power demands, the resulting SoC unbalances as well as further ancillary services providing, such as voltage support through reactive power control and B2G covering of active power demand.

It can be concluded that the proposed PET is appealing for the implementation of future ultra-fast EV charging infrastructures, where the focus is laid on system compactness due to the lack of excessive filtering and low frequency transformers (CHB converter and MF isolation stage, respectively) as well as equal power split between the different isolating converters without the need of additional high-power chargers.

6.2 Proposals for Future Research

Even after the end of a thesis work, several new challenges, questions and stimulating ideas arise. Indeed, based on the concepts developed in this thesis, several future research directions can be proposed. Especially when it comes to high-power conversion, the experimental validation utilizing a reduced scale prototype is only performed in order to carry out a proof of concept when it comes to the control part. Therefore, the real-scale implementation issues cannot be tackled.

Towards such direction, one of the interesting topics for research regards the investigation of the insulation requirements of the interface converter components and battery storage elements in MMC converters. Indeed, due to the different potentials of the converter submodules in respect to the ground, parasitic capacitances and common-mode currents appear causing EMI and oscillating behavior issues. This might put an additional constraint in the appropriate choice of a battery/submodule power interface, e.g., having to consider isolated converter topologies as well.

In a similar topic, the optimized MF power transformer design for the proposed UFEVCS is probably the most essential direction, since it constitutes the core element of the

PET-based system. The respective Chapter 5 has focused on the control of such a complex multiport system and has therefore not dealt with the design considerations using real-scale data. Therefore, it will be particularly interesting to address the topic of efficiency comparison between the conventional and proposed converter architectures, especially given the number of three cascaded conversion stages (submodule/IAI/DHB) in the whole chain of Figure 5.17.

In order to verify the proposed control method applicability, different MMC topologies can be considered, accordingly. These include the three/three-phase direct AC/AC converter of Figure 1.2e, the Hexverter of Figure 1.2f etc. For the sake of completeness, it is noted that preliminary results already exist regarding the single/three-phase direct AC/AC converter topology illustrated in Figure 6.1, but have not been included in this thesis report. The latter is a structure that can be primarily utilized for railway interties or similar applications, as mentioned in the introduction of this report.
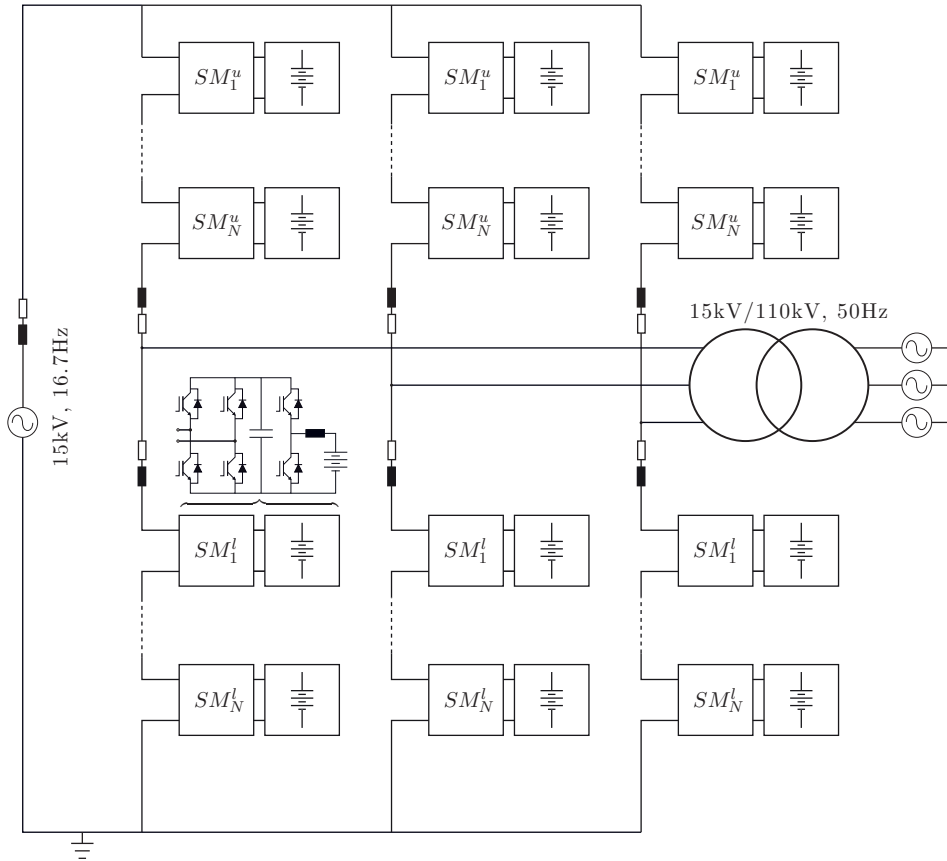
Figure 6.1: Single/Three-Phase direct AC/AC Modular Multilevel Converter with integrated battery energy storage for railway interties.

On an experimental level, the next step is to test the whole PET-based multiport converter architecture, i.e., the CHB-BESS-based active front end together with the implemented DHB modules, which have been only tested separately so far.

Finally and given the large number of hardware elements, studies on the failure rates and reliability of such power conversion structures with integrated battery energy storage are of great importance, in association with fault management techniques and implementations of redundancy schemes.

A Prototype Development

This section briefly describes the design and development principles of the various down-scaled laboratory setup components used for the experimental validation of several concepts presented in this thesis. The prototype design has been focused on the versatility of the implementation, which facilitates the reconfiguration towards the examination of several modular multilevel converter topologies, including isolated DC/DC converters as well as converters with integrated storage elements.

A.1   Power Part

Submodule and Branch Current Measurement

A modular rack-based design has been followed for all developments. The first multiphase prototype version without integrated energy storage components has been illustrated in Figure 2.8. Each rack constitutes a phase leg consisting of eight submodules, a branch current measurement board as well as the two branch inductances. The basic submodule printed circuit board (PCB) is depicted in Figure A.1a. It has been designed to comprise four power switches, giving the user the option to switch between a half- or full-bridge implementation (see Figure 1.1b). The latest submodule version is realized using power MOSFETs, contrary to the first version consisting of IGBTs. In addition, the submodules provide measurements for their capacitor voltages, which are also integrated on the same board. The backplanes of the rack-mounted boards carry all gate signals, power supplies as well as measurements through a Serial Peripheral Interface (SPI) bus. The submodule design was already existing as a result of a Master Project [136].

The branch current measurement board is depicted in Figure A.1b. It has been designed in a versatile manner, so as to provide two different measurement options, either an on-board A/D conversion and SPI communication through the backplane, or an independently processed measurement through the converter dedicated measurement system for increased bandwidth. The latter is better highlighted in the next section on the description of

the control platform. In addition, this card offers a branch overcurrent detection analog circuit, in order to ensure the converter protection.

(a)   (b)
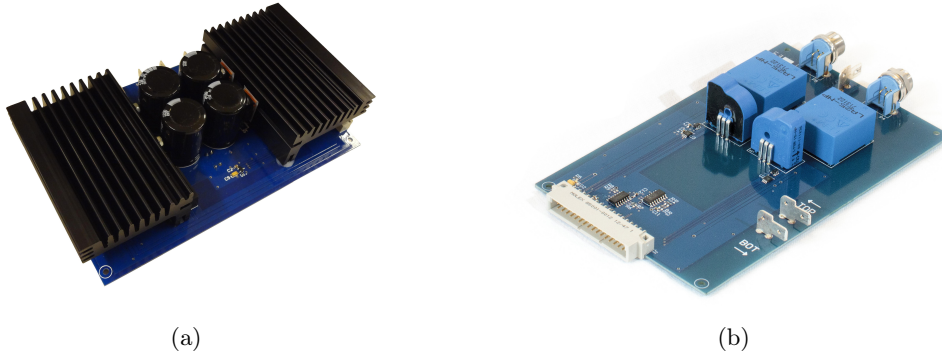
Figure A.1: (a) The MMC prototype submodule and (b) the branch current measurement board.

Indirect Active Interface and Battery Module

For the scopes of the current thesis, the IAI interface solution (nonisolated buck converter) has been implemented (see Figure 3.2b). It comprises a MOSFET-based half-bridge with a filter inductor, which is illustrated in Figure A.2a. Measurements of the battery current and voltage are also provided by the board. The same concept as the MMC submodules has been followed, where the IAIs are mounted in a rack, whose backplanes carry all gate signals, SPI measurements and power supplies.

(a)   (b)
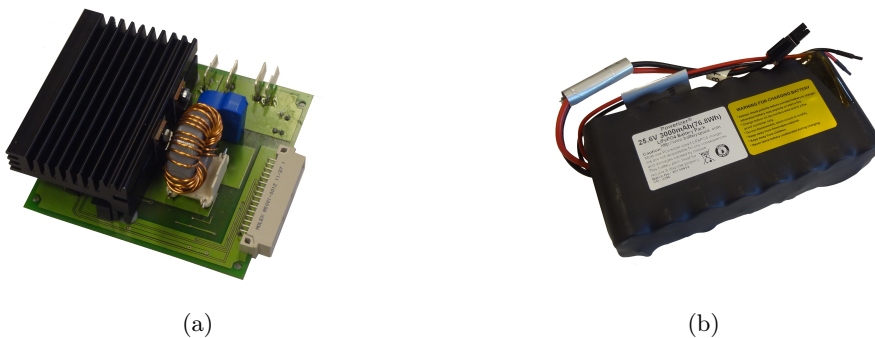
Figure A.2: (a) The indirect active interface and (b) the utilized LiFePO$_4$ battery module.

The batteries are also placed in the same rack. The utilized packs are of LiFePO$_4$ 25.6V/3Ah technology commonly used for e-bikes [137]. The embedded BMS of each pack protects the battery from short-circuits, under- and over-voltages. However, it does

not provide cell-balancing functions or estimation for the State of Charge of the pack. Therefore, the purpose of the prototype at this point is to test the basic control/modulation functions and operating modes rather than implementing the SoC balancing algorithms developed in this thesis. The implemented MMC phase leg has been illustrated in Figure 3.23.

Dual Half-Bridge Module and MF Transformer

In the framework of the proposed PET-based multiport UFEVCS topology, the chosen dual half-bridge-based isolation stage topology has been also realized. The implemented DHB module is shown in Figure A.3 and corresponds to the circuit schematic of Figure 5.4a. It features two half-bridges for the primary and secondary converter side, whose realization is based on MOSFETs as in the submodule and IAI cases. For the implementation of the four splitting capacitors, high-current aluminium electrolytic technology by EPCOS has been utilized. The transformers are constructed using ETD49 cores once again by EPCOS and the windings consist of Litz wire. The achieved leakage inductances L_σ vary between 1.5 and 1.9 μH.
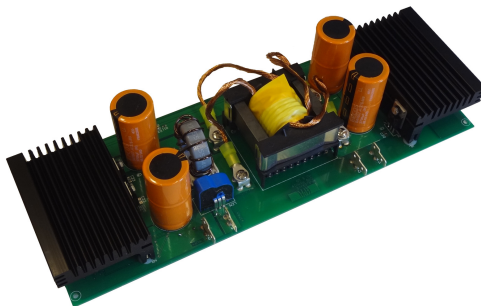
Figure A.3: The implemented dual half-bridge module.

Again, one PCB per module has been designed and the whole system is integrated in a standard rack, as it has been shown in Figure 5.12. Similarly to the submodule and BESS stage a backplane is used, carrying all gate signals, SPI measurements and power supplies. The voltage and current outputs of each DHB module are sensed for control as well as security purposes. Additional technical characteristics on the choice of components and the MF transformer design, which has been based on the considerations made in [138], can be found in [139].

A.2 Control Part

Given the system complexity and the large number of required I/Os, only customized commercial solutions can be considered for the control part of such a prototype. The latter together with the fact that such systems can become very expensive put significant constraints on the choice for control hardware. Therefore, the Laboratory of Industrial Electronics at EPFL has decided to build its own control platform for the evaluation of several different already completed and ongoing research projects. The developed custom hardware platform, namely the 'MMCbox', whose design and features resemble the one of [140], is illustrated in Figure A.4 and is still undergoing changes and updates.
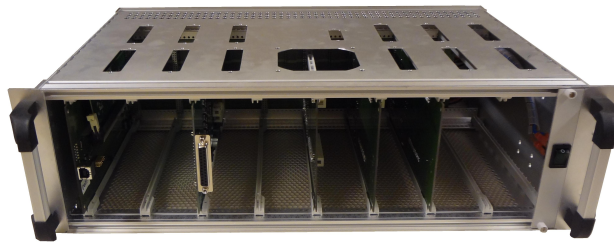
Figure A.4: The control platform (MMCbox).

The control part implementation together with the associated power parts are illustrated in the simplified block diagram of Figure A.5. In the following, the functionalities of the main system blocks are explained. For a more detailed description of the hardware design and implementation of the 'MMCbox', the reader is referred to [141].

High-level Control and Communication

All different control hardware components are connected to a backplane. The communication between the various control units is performed through a nonmultiplexed parallel asynchronous bus, namely the external interface (XINTF). The supervision is carried out by a central floating point microcontroller unit (MCU) based on the TI TMS320C28346 Delfino, which is programmed in C/C++.

The MCU executes all higher level control functions by receiving the system voltage and current measurements, which are processed in an Field-Programmable Gate Array (FPGA)-based board (see Measurement FPGA), as well as the inner converter measurements, such as submodule capacitor voltages, integrated BESS voltages/currents, and DHB output voltages/currents (see Control FPGA). All different operating modes of the converter, including submodule capacitor charging/discharging, steady state operation as well as fault mode, are handled through a state machine implemented in the MCU. The latter is then sending information about the auxiliary relays states as well as calculated modulation references to the low-level slave controllers that are explained right after.

Finally, the Delfino motherboard communicates in real-time with the control PC by means of a serial UART to USB interface.
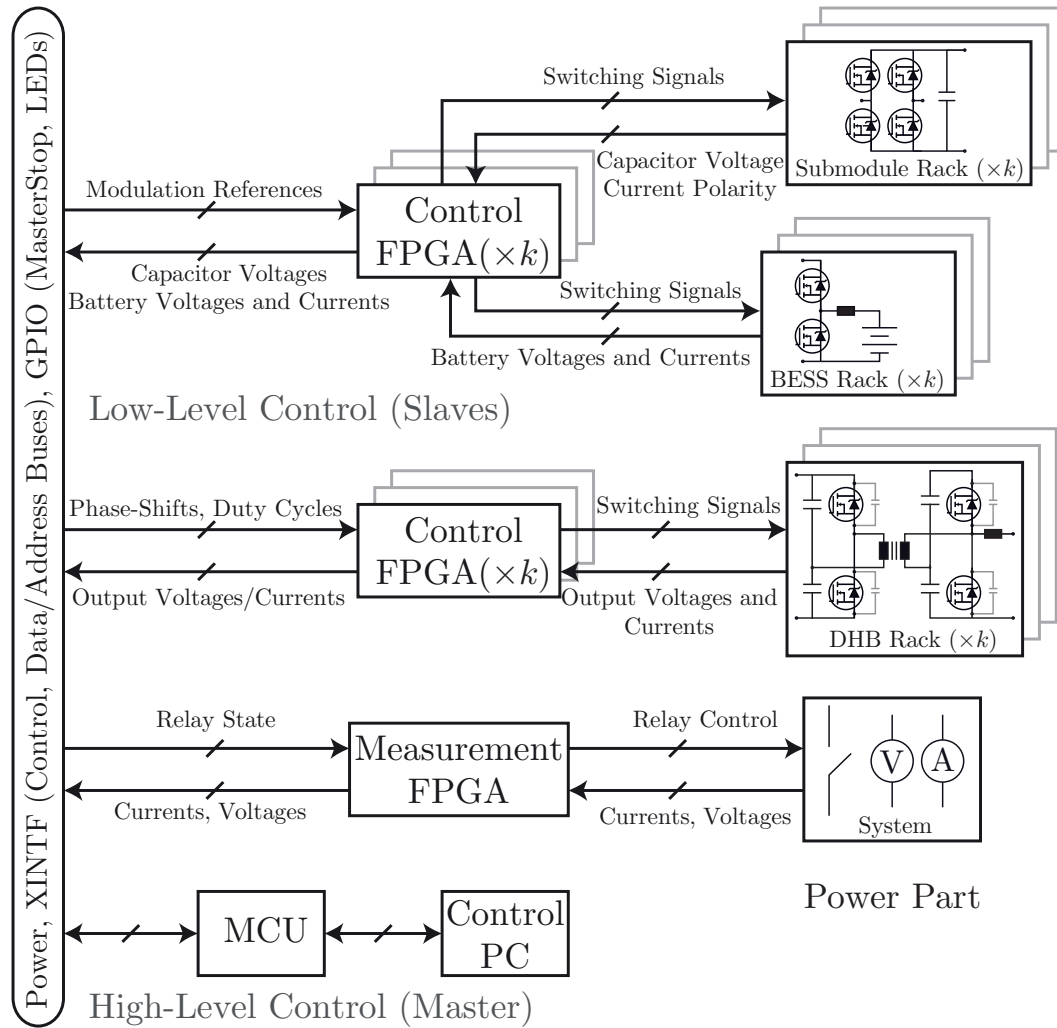
Figure A.5: Generalized simplified scheme of the proposed implemented MMC control platform functionality.

Control FPGA

The localized lower level modulation functions are carried out in dedicated VHDL-programmed FPGA control boards. Each of these boards corresponds to one phase leg, thus following a modularized concept. The FPGAs receive data regarding the calculated modulation references from the microcontroller. They are also responsible for retrieving the capacitor voltage and branch current polarity from the converter branches as well as the battery currents and voltages from the integrated BESS stage.

It is noted that three different submodule capacitor balancing concepts have been im-

plemented. The first concept regards a sorting algorithm in conjunction with an active selection process dynamically distributing the gate control signals to the switches [3]. The second case is based on individual voltage feedback control loops that act on the duty cycles of each submodule [41]. Finally, the third method is based on the proposals of this thesis work and is dedicated to the integrated BESS case, i.e., the active submodule voltage control from the battery side through the IAI utilization.

The Control FPGAs are also in charge of ensuring converter protection, in cases where overvalues are detected. A common error signal, namely the 'Master Stop' acts accordingly in order to remove all gating signals from the converter switches.

The main hardware part of the described PCB is an Actel (M1)A3P10001 FPGA. A 50-pin and a 40-pin connectors are used for the communication with the MMC and the BESS backplanes of each phase leg, respectively. Level shifters for 3.3V to 5V conversion are also utilized. Finally, a static random-access memory SRAM of 4MB has been foreseen for data logging, although the latter has not been yet implemented.

An identical board is utilized for the control of the DHB-based isolation stage. The measured output voltages and currents are also communicated to the MCU for the execution of the control that defines the converter phase-shifts and duty cycles. With this information, the required switching signals are generated.

Measurement FPGA

An additional FPGA-based board has been designed for the retrieval of system-related measurements, such as DC-link/grid voltages and branch currents. The PCB supports a maximum number of twelve simultaneous measurements. It features an anti-aliasing filter (AAF) before feeding the LEM transducer-based measurements to dedicated A/D converters at 100 ksamples/s. The FPGA implements low-pass filters, before sending the digital data to the MCU for processing. Similarly to the Control FPGA, the Measurement FPGA also offers the possibility to store data in a 256MB synchronous dynamic random-access memory (SDRAM) for post-processing purposes, although the latter has not yet been implemented.

It is noted that even if the branch current measurement PCB offeres a full A/D current conversion and SPI communication to the Control FPGA, a second LEM-based branch current measurement is available in the system through the Measurement FPGA, in order to achieve a higher bandwidth.

The Measurement FPGA is also responsible for the control of the relays used for converter pre-charging/discharging operations through respective resistors, as well connection/disconnection from the grid.

B Branch Energy Variations of an MMC under Grid Unbalances

In this section, the analytical expressions of the branch energies for the case of a DC/AC MMC operating under unbalanced grid conditions are provided, without and with a second-order harmonic imposition on the circulating current. They have been utilized for the analysis of the grid unbalance impact on the energy variations and capacitive energy storage requirements in Chapter 2. It is noted that a third-order harmonic common-mode voltage injection is considered for an increase of the converter modulation index as

$$u_{cm} = \hat{u}_{cm} \cos\left(3\omega t\right) \tag{B.1}$$

For the MMC phase a, the result for the upper and lower arms when the circulating current is controlled to comprise only a continuous component is given by

$$E_{no2nd}^{au} = \Sigma E_{br}^0 + A_{u_S}^\omega - A_{circ0}^\omega - A_p^{2\omega} - A_n^{2\omega} - A_{cm}^{2\omega} - A_{cm}^{3\omega} - A_{cm}^{4\omega} \tag{B.2}$$

$$E_{no2nd}^{al} = \Sigma E_{br}^0 - A_{u_S}^\omega + A_{circ0}^\omega - A_p^{2\omega} - A_n^{2\omega} - A_{cm}^{2\omega} + A_{cm}^{3\omega} - A_{cm}^{4\omega} \tag{B.3}$$

The constant terms are identical in the two branches of the same phase leg and can either be of common-mode (same signs) or differential-mode (opposite signs) nature. They are obtained as

$$A_{u_S}^\omega = \frac{u_S}{4\omega} \left[\hat{i}_T^p \sin\left(\omega t + \phi_i^p\right) + \hat{i}_T^n \sin\left(\omega t + \phi_i^n\right) \right]$$

$$A_{circ0}^\omega = \frac{I_{circ0}^a}{\omega} \left[\hat{u}_V^p \sin\left(\omega t + \phi_u^p\right) + \hat{u}_V^n \sin\left(\omega t + \phi_u^n\right) \right]$$

$$A_p^{2\omega} = \frac{\hat{u}_V^p}{8\omega} \left[\hat{i}_T^p \sin\left(2\omega t + \phi_u^p + \phi_i^p\right) + \hat{i}_T^n \sin\left(2\omega t + \phi_u^p + \phi_i^n\right) \right]$$

$$A_n^{2\omega} = \frac{\hat{u}_V^n}{8\omega} \left[\hat{i}_T^p \sin\left(2\omega t + \phi_u^n + \phi_i^p\right) + \hat{i}_T^n \sin\left(2\omega t + \phi_u^n + \phi_i^n\right) \right]$$

$$A_{cm}^{2\omega} = \frac{\hat{u}_{cm}}{8\omega} \left[\hat{i}_T^p \sin\left(2\omega t - \phi_i^p\right) + \hat{i}_T^n \sin\left(2\omega t - \phi_i^n\right) \right]$$

Appendix B. Branch Energy Variations of an MMC under Grid Unbalances

$$A_{cm}^{3\omega} = \frac{\hat{u}_{cm}}{16\omega} \left[\hat{i}_T^p \sin\left(4\omega t + \phi_i^p\right) + \hat{i}_T^n \sin\left(4\omega t + \phi_i^n\right) \right]$$

$$A_{cm}^{4\omega} = \frac{\hat{u}_{cm} I_{circ0}^a}{3\omega} \sin\left(3\omega t\right)$$

It can be seen that the dominant components are of first- and second-order harmonic frequencies and both due to the voltage and current positive and negative sequences. The common-mode voltage injection causes terms oscillating at the third- and fourth-harmonic frequencies.

In the case where a second-order circulating current injection takes place for the compensation of the respective power oscillating terms according to (2.51)-(2.53), the branch energies are modified. They are now expressed by

$$E_{2nd}^{au} = \Sigma E_{br}^0 + A_{u_S}^\omega - A_{circ0}^\omega - A_{circ,2}^{\omega,p} - A_{circ,2}^{\omega,n} - A_{pn}^{2\omega} - A_{circ,2}^{3\omega,p} - A_{circ,2}^{3\omega,n}$$
$$- A_{cm}^\omega - A_{cm}^{2\omega} - A_{cm}^{3\omega} - A_{cm}^{4\omega} - A_{cm}^{5\omega} \tag{B.4}$$

$$E_{2nd}^{au} = \Sigma E_{br}^0 - A_{u_S}^\omega + A_{circ0}^\omega + A_{circ,2}^{\omega,p} + A_{circ,2}^{\omega,n} - A_{pn}^{2\omega} + A_{circ,2}^{3\omega,p} + A_{circ,2}^{3\omega,n}$$
$$+ A_{cm}^\omega - A_{cm}^{2\omega} + A_{cm}^{3\omega} - A_{cm}^{4\omega} + A_{cm}^{5\omega} \tag{B.5}$$

with the respective constants

$$A_{u_S}^\omega = \frac{u_S}{4\omega} \left[\hat{i}_T^p \sin\left(\omega t + \phi_i^p\right) + \hat{i}_T^n \sin\left(\omega t + \phi_i^n\right) \right]$$

$$A_{circ0}^\omega = \frac{I_{circ0}^a}{\omega} \left[\hat{u}_V^p \sin\left(\omega t + \phi_u^p\right) + \hat{u}_V^n \sin\left(\omega t + \phi_u^n\right) \right]$$

$$A_{circ,2}^{\omega,p} = \frac{\hat{u}_V^p}{2\omega} \left[\hat{i}_{circ,2a} \sin\left(\omega t - \phi_u^p + \theta_a\right) + \hat{i}_{circ,2b} \sin\left(\omega t - \phi_u^p + \theta_b\right) \right]$$

$$A_{circ,2}^{\omega,n} = \frac{\hat{u}_V^n}{2\omega} \left[\hat{i}_{circ,2a} \sin\left(\omega t - \phi_u^n + \theta_a\right) + \hat{i}_{circ,2b} \sin\left(\omega t - \phi_u^n + \theta_b\right) \right]$$

$$A_{pn}^{2\omega} = \frac{1}{8\omega} \left[\hat{u}_V^p \hat{i}_T^n \sin\left(2\omega t + \phi_u^p + \phi_i^n\right) + \hat{u}_V^n \hat{i}_T^p \sin\left(2\omega t + \phi_u^n + \phi_i^p\right) \right]$$

$$A_{circ,2}^{3\omega,p} = \frac{\hat{u}_V^p}{6\omega} \left[\hat{i}_{circ,2a} \sin\left(3\omega t + \phi_u^p + \theta_a\right) + \hat{i}_{circ,2b} \sin\left(3\omega t + \phi_u^p + \theta_b\right) \right]$$

$$A_{circ,2}^{3\omega,n} = \frac{\hat{u}_V^n}{6\omega} \left[\hat{i}_{circ,2a} \sin\left(3\omega t + \phi_u^n + \theta_a\right) + \hat{i}_{circ,2b} \sin\left(3\omega t + \phi_u^n + \theta_b\right) \right]$$

$$A_{cm}^\omega = \frac{\hat{u}_{cm}}{2\omega} \left[\hat{i}_{circ,2a} \sin\left(\omega t - \theta_a\right) + \hat{i}_{circ,2b} \sin\left(\omega t - \theta_b\right) \right]$$

$$A_{cm}^{2\omega} = \frac{\hat{u}_{cm}}{8\omega} \left[\hat{i}_T^p \sin\left(2\omega t - \phi_i^p\right) + \hat{i}_T^n \sin\left(2\omega t - \phi_i^n\right) \right]$$

$$A_{cm}^{3\omega} = \frac{\hat{u}_{cm} I_{circ0}^a}{3\omega} \sin\left(3\omega t\right)$$

$$A_{cm}^{4\omega} = \frac{\hat{u}_{cm}}{16\omega} \left[\hat{i}_T^p \sin\left(4\omega t + \phi_i^p\right) + \hat{i}_T^n \sin\left(4\omega t + \phi_i^n\right) \right]$$

$$A_{cm}^{5\omega} = \frac{\hat{u}_{cm}}{10\omega} \left[\hat{i}_{circ,2a} \sin\left(5\omega t + \theta_a\right) + \hat{i}_{circ,2b} \sin\left(5\omega t + \theta_b\right) \right]$$

It can be now seen that the the second-order harmonic frequencies that are not of common-mode nature between the three phases have been eliminated. However, the circulating current harmonic imposition gives rise to an energy term of the third harmonic frequency. In addition, the third-order common-mode voltage injection leads to oscillating frequencies between the fundamental and up to a fifth.

In both considered cases, the expressions for phases b and c are derived in a similar manner and are not provided here.

C Phase-Shift Controlled Full-Bridge-based Isolation Stage

Figure C.1a depicts a topology, which is suitable for the proposed PET-based ultra-fast charging station architecture of Chapter 5. The principle of operation and properties of the full-bridge phase-shift controlled isolated PWM converter have been widely discussed in literature [142] and are also summarized here for sake of completeness. The implementation of a relative phase-shift between the primary legs and a sufficient switching dead-time within the same leg ensure zero voltage switching for all four switches of the primary H-Bridge. In order to gain the same property during turn-off, snubber capacitors can be

(a)

(b)
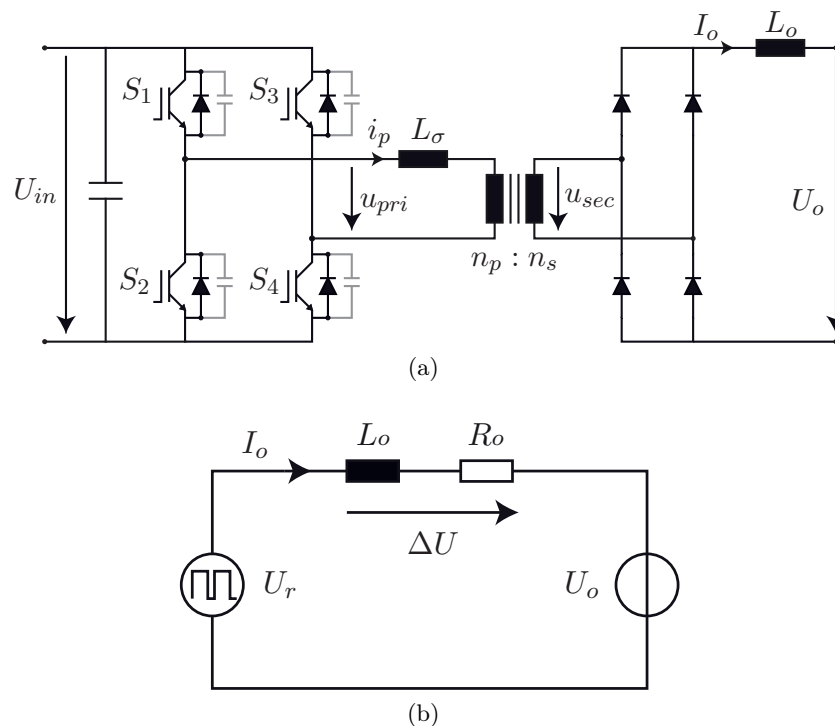
Figure C.1: (a) Full-bridge phase-shift controlled ZVS isolated PWM converter, (b) Output equivalent electrical circuit for current control design.

used in the circuit as well. The phase-shift leads to an asymmetric utilization and thermal behavior of these legs. The mechanism by which the zero voltage switching mechanism is achieved is different for the two legs of the primary full-bridge.

For the two lagging switches S_4 and S_2 the ZVS is provided by the resonance between the transformer leakage inductance L_σ as well as the snubber and parasitic capacitances, which are denoted by C_S, C_{IGBT} and C_{TR} respectively (parasitics refer to the IGBTs and transformer). This provides a sinusoidal voltage across the switch capacitances that reaches a maximum at one fourth of the resonant frequency period. Therefore, the dead-time between S_4 and S_2 has to be set to [142]

$$\delta t_{lag} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L\sigma(C_S + C_{IGBT} + C_{TR})} \tag{C.1}$$

in order to ensure that there is sufficient time to charge and discharge the capacitances at the maximum possible load range.

The ZVS condition for S_4 and S_2 depends on the load level of the converter. For light loads, the current through L_σ when S_4 and S_2 are turned-off may not be enough to turn-on the anti-parallel diodes. In such a low load, however, the conduction losses are significantly lower, which may compensate in an acceptable manner for the existence of switching losses.

For the leading switches S_1 and S_3, ZVS is provided by a different mechanism. Before S_1 is turned-off, the current in the primary is reaching its peak value. The aforementioned current is the filter inductor current reflected to the primary. When S_1 is turned-off, the energy available to charge the output capacitance of S_1 and discharge the output capacitance of S_3 is the energy stored in L_σ as well as the output filter inductor L_o. This energy in the output filter inductor is available because the filter inductor current does not freewheel through the rectifier until the voltage across the secondary has fallen to zero. Since the energy in the filter inductor is large compared to the energy stored in the switch capacitances in the primary, the charging of the switches can be approximated by a linear charging with a constant current. Consequently, the dead time δt_{lead} required between the turn off of S_1 and turn on of S_3 can be determined from the following equation [142]:

$$\delta t_{lead} = \frac{(4C_{IGBT} + C_S + C_{TR})U_{in}}{I_o^{max}} \tag{C.2}$$

A final parameter that plays a key role in the ZVS conditions is the output current ripple ΔI_o. The latter is influenced by the output filter inductor L_o, the switching frequency f_s as well as the converter equivalent duty cycle D_{eq}. The quantity D_{eq} is not to be confused with the actual switching duty cycle, which is set to 50% in this case. Moreover, with an interleaving of the different isolated converters, each DC/DC stage can operate at a higher ripple. Therefore, a further reduction of L_o is possible, in function of course of the

number of stages that are utilized for each EV charger.

The ZVS for S_1 and S_3 can be achieved even at light loads because the respective anti-parallel diodes can always be turned-on by the energy stored in the output filter inductance. However, ZVS for S_2 and S_4 can only be achieved for a load current above a critical value. Summarizing the above, this limitation for the load current is expressed by [142]:

$$I_o > \frac{n_p}{n_s} I_{crit} - \frac{\Delta I_o}{2} + \frac{U_o}{L_o}(1 - D_{eq})\frac{1}{2f_s} \tag{C.3}$$

In the above, ΔI_o is the output current ripple at each converter stage, which is obtained from

$$\Delta I_o = \frac{\frac{n_s}{n_p}U_{in} - U_o}{2L_o}\frac{D_{eq}}{f_s} \tag{C.4}$$

as well as I_{crit} is the critical current, for which ZVS is achieved for the lagging converter leg switches S_4 and S_2 [142]:

$$I_{crit} = \sqrt{\frac{2}{L_\sigma}\left(\frac{4}{3}C_{IGBT} + \frac{1}{2}(C_S + C_{TR})\right)U_{in}^2} \tag{C.5}$$

Figure C.2 shows the resulted waveforms for a number of 13 parallel-connected isolated DC/DC converters, operating with a switching frequency of $f_s = 10$ kHz at 250 kW of output power. The output EV battery charging current has an average value of 500 A with an almost negligible ripple, whereas each converter stage tolerates a bigger ripple. The typical primary transformer voltage and current are also depicted, which result from the phase-shifted PWM operation. The number of parallel-connected converters corresponds to the analysis performed in [69].

C.1 EV Current Control

The modeling of the full-bridge phase-shift controlled isolated PWM converter has already been presented in literature using small and large signal analysis and aiming for output voltage regulation, both in continuous and discontinuous conduction modes (CCM and DCM respectively). In the studied application, an output current regulation is also needed, for example during the first phase of a constant current constant voltage (CC-CV) fast-charge characteristic or when a pulse-controlled charging process is performed. The behavior of the converter resembles the standard half-bridge buck DC/DC converter.

Figure C.1b shows the equivalent electrical diagram of a single isolated converter output connected to the EV battery. The internal resistance R_o of the filter inductor is also
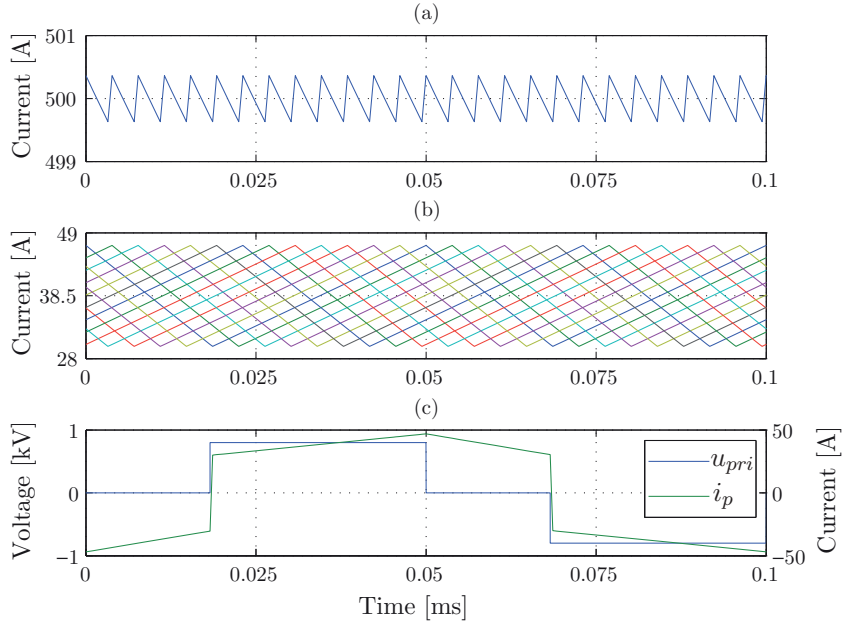
Figure C.2: Typical waveforms of 13 parallel-connected isolated DC/DC converter with interleaved operation during one cycle of 10 kHz switching frequency: (a) EV battery charging current, (b) Individual output currents of the 13 converter channels, and (c) Primary transformer voltage and current of the first DC/DC isolated converter.

considered. The following equation (C.6) can be formulated in average,

$$I_o = \frac{\Delta U}{sL_o + R_o} = \frac{MU_{in} - U_o}{sL_o + R_o} \tag{C.6}$$

where M denotes the conversion ratio as defined in [115]. The above equation (C.6) shows that an explicit control with high bandwidth is at hand, by adjusting the voltage drop ΔU across the filter inductor L_o.

It is important to relate the conversion ratio M with the converter duty cycle D_{eq}, in order to effectively interpret the outcome of the closed-loop controller. Following the same analysis as proposed in [115], this function can be extracted for the cases of CCM and DCM as

$$M = \begin{cases} \dfrac{n_s}{n_p} D_{eq} & \text{for } \text{CCM} \\[2ex] \dfrac{n_s}{n_p} \dfrac{1}{(Kn_p)/(D_{eq}^2 n_s U_{in}) + 1} & \text{for } \text{DCM} \end{cases} \tag{C.7}$$

where $K = 2L_o i_o f_s$.

Finally, it is noted that there is a main difference between the nonisolated with the isolated DC/DC buck-derived topologies in the definition of their duty cycles. The phase-shift

controlled PWM converter experiences an effective duty cycle, which has to do with the loss due to the linear charging and discharging of the leakage inductor current [143]. The effective duty cycle is quantified as

$$D_{eff} = D_{eq} - \Delta D_{eq} = D_{eq} - \left(\frac{2L_\sigma}{U_{in}T_s} \frac{n_s}{n_p} \left(2I_o - \frac{U_o}{L_o} D'_{eq} \frac{T_s}{2} \right) \right) \tag{C.8}$$

where $D'_{eq} = 1 - D_{eq}$.

Figure C.3 shows the results of the closed-loop system performance. The EV battery voltage U_{EV} is measured and used as a disturbance rejection feed-forward signal. Three different modes are tested. Only the principle of operation and the accurate reference tracking throughout the whole application range are of interest, since the time-scale values do not correspond to a real case. In the starting up mode, a ramped increase of the current leads to a smoother initialization of the converter control and EV charging process. The second mode regards a typical constant current battery feeding, normally up to a SoC of 80 %. This is normally followed by the final constant voltage phase, which is not considered here. Finally, the third mode regards a pulsed charging technique, where small rest periods throughout the charging procedure allow the stabilization of the battery electrochemical processes.
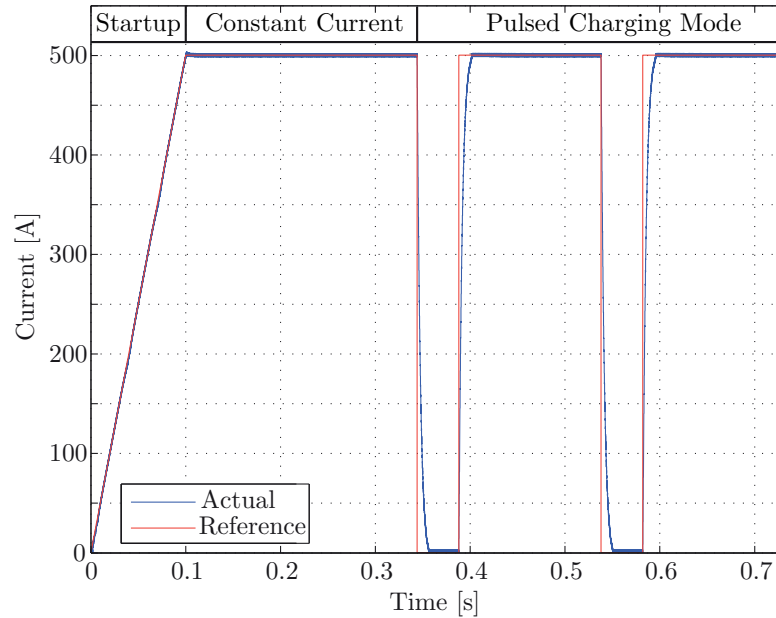
Figure C.3: Results of a controlled EV battery current for three different modes of operation.

C.2   Topology-Related Issues

The converter of Figure C.1a can only transfer power to the EV batteries. However, it might be beneficial in several cases to support the grid from the EV side, leading to the so-called Vehicle-to-Grid (V2G) concept. If the secondary converter is implemented utilizing active switches, such an operation is possible. However, this implies that in reversed power transfer, the secondary bridge would connect in series the two inductors L_o and L_σ, leading to unacceptable spikes. An additional issue regards the forward operation as well, where the transformer leakage inductance interacts with the rectifier stage diode capacitances causing voltage oscillation stresses. Therefore and in any case, additional external passive or active circuitry is required, both for oscillation clamping and bidirectional converter operation. Two solutions are depicted in Figure C.4. The first one is based on a passive RCD clamping circuit with a dissipative resistor. The second more elegant one replaces the resistor with an energy recycling baby buck converter [144].
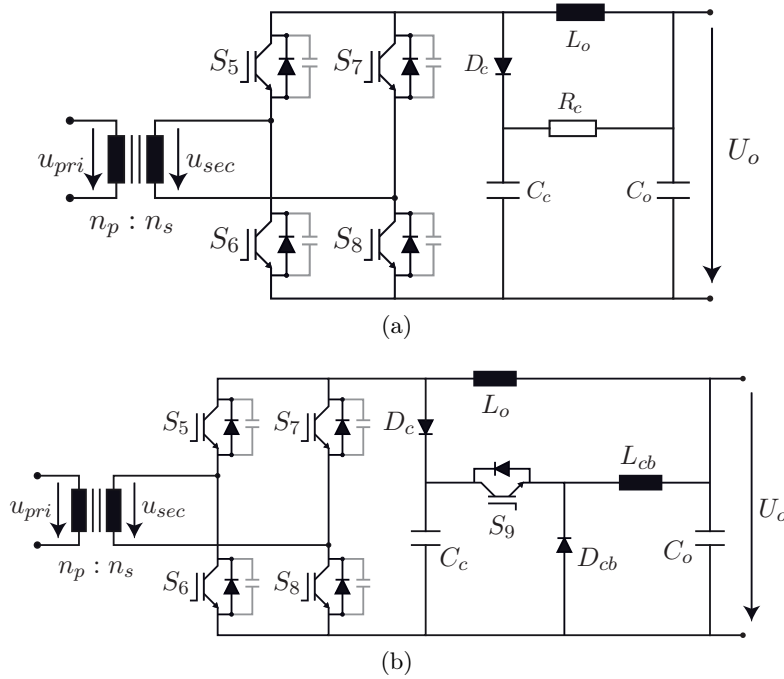
Figure C.4: Solutions for achieving bi-directional operation with a phase-shift controlled isolated PWM converter, (a) utilizing a passive clamp snubber with a resistance (b) replacing the resistance with a baby buck converter.

D DHB Average Linearized Model

The duty cycle-dependent linearized average state space model of the dual half-bridge converter is derived here with the buck-mode conventions of Figure 5.4. The model of [129,132] is augmented with the filtered output current I_o^f and linearized using small variations.

The circuit is referred to the transformer primary according to Figure 5.4b. By denoting the sum of voltages across the capacitors C_{1-2} and C_{3-4} as U_{12} and U'_{34}, respectively, the differential equations that describe mathematically the dual half-bridge converter are obtained as follows:

$$
\begin{cases}
\dfrac{dI'_o}{dt} = -\dfrac{U'_o}{L'_o} - \dfrac{R'_o}{L'_o}I'_o + \dfrac{DU'_{34}}{L'_o} \\[2mm]
\dfrac{dU_{12}}{dt} = -\dfrac{2}{CR_{eq}}U_{12} + \dfrac{\delta\left[\delta + 4\pi D\left(D-1\right)\right]}{2\pi\omega_s C_1 L_\sigma}U'_{34} + \dfrac{2}{CR_{eq}}U_{eq} \\[2mm]
\dfrac{dU'_{34}}{dt} = -\dfrac{2D}{C'}I'_o - \dfrac{\delta\left[\delta + 4\pi D\left(D-1\right)\right]}{2\pi\omega_s C'_3 L_\sigma}U_{12} \\[2mm]
I'^f_o = \dfrac{1}{T_f}I'_o - \dfrac{1}{T_f}I'^f_o
\end{cases}
\tag{D.1}
$$

with T_f being the time constant of the first-order current measurement filter.

The first and fourth equations of (D.1) are linear but the second and third exhibit nonlinearities. Therefore and in order to design a linear control system, such as a PI controller, these equations have to be linearized. The linearization can be performed through the introduction of small variations around an operating point, such as the nominal one. It is noted that when introducing small variations for nonlinear equations, even the linear ones have to be expressed as such in order to keep a consistency in the mathematical symbols and manipulations.

It is reminded that the small variations of a nonlinear function of one variable expressed

as

$$y = f(x) \tag{D.2}$$

around the nominal operating point P_0 are approximated by

$$y = y_0 + \Delta y \cong f(x_0) + \left.\frac{\partial f}{\partial x}\right|_0 \Delta x \Leftrightarrow \Delta y = \left.\frac{\partial f}{\partial x}\right|_0 \Delta x \tag{D.3}$$

Similarly, a nonlinear function of m variables

$$y = f(x_1, x_2, ..., x_m) \tag{D.4}$$

can be linearized using the expression

$$y = y_0 + \Delta y \cong f(x_1^0, x_2^0, ..., x_m^0) + \left.\frac{\partial f}{\partial x_1}\right|_0 \Delta x_1 + \left.\frac{\partial f}{\partial x_2}\right|_0 \Delta x_2 + ... + \left.\frac{\partial f}{\partial x_m}\right|_0 \Delta x_m$$
$$\Leftrightarrow \Delta y = \left.\frac{\partial f}{\partial x_1}\right|_0 \Delta x_1 + \left.\frac{\partial f}{\partial x_2}\right|_0 \Delta x_2 + ... + \left.\frac{\partial f}{\partial x_m}\right|_0 \Delta x_m \tag{D.5}$$

For the product of two variables x_1 and x_2

$$y = x_1 \cdot x_2 \tag{D.6}$$

the small variations give

$$\Delta y = \left.\frac{\partial(x_1 \cdot x_2)}{\partial x_1}\right|_0 \Delta x_1 + \left.\frac{\partial(x_1 \cdot x_2)}{\partial x_2}\right|_0 \Delta x_2 = x_2^0 \Delta x_1 + x_1^0 \Delta x_2 \tag{D.7}$$

where x_1^0, x_2^0 are the values of the respective variables x_1, x_2 at the specific operating point.

Finally, for a quotient of two variables x_1 and x_2

$$y = \frac{x_1}{x_2} \tag{D.8}$$

the small variations give

$$\Delta y = \left.\frac{\partial(x_1/x_2)}{\partial x_1}\right|_0 \Delta x_1 + \left.\frac{\partial(x_1/x_2)}{\partial x_2}\right|_0 \Delta x_2 = \frac{1}{x_2^0}\Delta x_1 - \frac{y_0}{x_2^0}\Delta x_2 \tag{D.9}$$

In the studied case, the state vector ia defined as $x = \left[\Delta I_o' \ \Delta U_{12} \ \Delta U_{34}' \ \Delta I_o'^f\right]^T$, and the input vector as $u = [\Delta U_o' \ \Delta \delta \ \Delta U_{eq}]^T$. After applying the aforementioned relations to (D.1), the linearized dynamics of the converter result in a state-space representation form

as

$$\dot{x} = Ax + Bu$$
$$y = Cx \tag{D.10}$$

where

$$A = \begin{pmatrix} -\frac{R'_o}{L'_o} & 0 & \frac{D}{L'_o} & 0 \\ 0 & -\frac{2}{CR_{eq}} & \frac{\delta[\delta+4\pi D(D-1)]}{2\pi\omega_s C_1 L_\sigma} & 0 \\ -\frac{2D}{C} & -\frac{\delta[\delta+4\pi D(D-1)]}{2\pi\omega_s C'_3 L_\sigma} & 0 & 0 \\ \frac{1}{T_f} & 0 & 0 & -\frac{1}{T_f} \end{pmatrix}$$
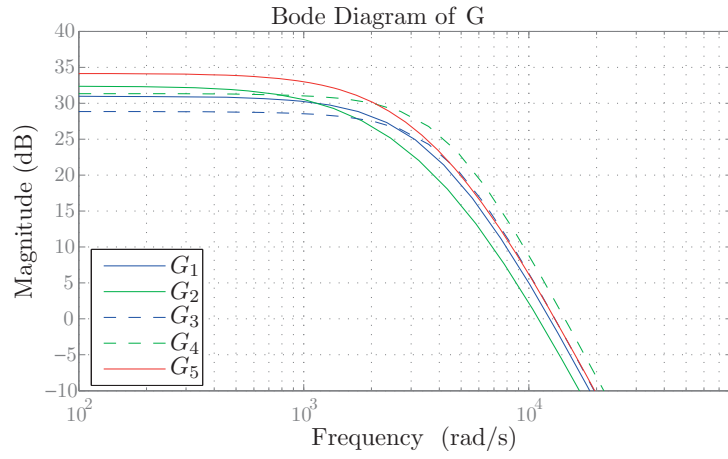
(a)
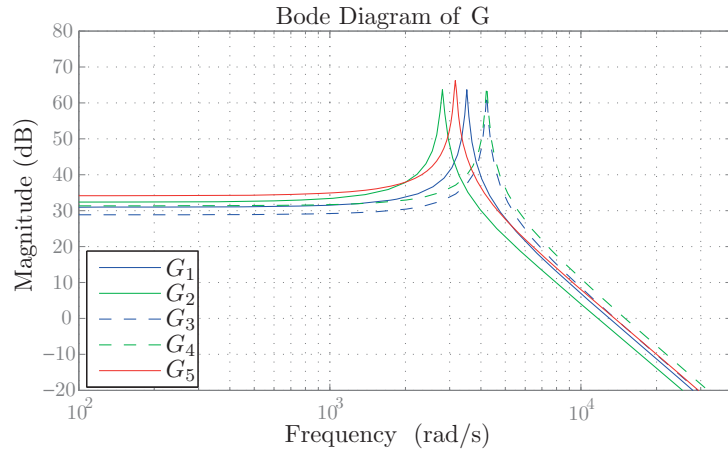
(b)

Figure D.1: Dual half-bridge bode diagrams based on the linearized average analytical model for the cases of (a) high output resistance (R_o=100 mΩ) and (b) low output resistance (R_o=1 mΩ).

$$B = \begin{pmatrix} -\frac{1}{L'_o} & 0 & 0 \\ 0 & \frac{DU_o[2\delta+4\pi D(D-1)]}{2\pi\omega_s C_1 L_\sigma} & \frac{2}{CR_{eq}} \\ 0 & \frac{-U_{eq}[2\delta+4\pi D(D-1)]}{2\pi\omega_s C'_3 L_\sigma} & 0 \\ 0 & 0 & 0 \end{pmatrix}$$

$$C = \begin{pmatrix} 0 & 0 & 0 & 1 \end{pmatrix}$$

It is noted that the superscripts 0 have been omitted for the sake of simplicity. The aforementioned state-space model can be numerically converted into a transfer function from $\Delta\delta$ to I'^f_o and used for the control design. Drawing the Bode plots with such a model yields similar results with the identification procedure results presented in Figure 5.7 and Figure 5.10 of Chapter 5, as illustrated in Figure D.1.

List of Figures

List of Tables

Bibliography

[1] R. Marquardt. Stromrichterschaltungen mit verteilten energiespeichern, Offenlegungsschrift DE 1010331A1, 2002.

[2] R. Marquardt, A. Lesnicar, and J. Hildinger. Modulares Stromrichterkonzept für Netzkupplungsanwendungen bei hohen Spannungen. In *ETG-Fachtagung*, Bad Nauheim, Germany, 2002.

[3] A. Lesnicar and R. Marquardt. A new modular voltage source inverter topology. In *Proc. of the 10th European Conference on Power Electronics and Applications (EPE)*, Toulouse, France, Sept. 2-4, 2003.

[4] R. Baker and L. Bannister. Electric power converter, Patent US 3867643, 1975.

[5] F.Z. Peng, J.-S. Lai, J.W. McKeever, and J. VanCoevering. A multilevel voltage-source inverter with separate DC sources for static VAr generation. *IEEE Transactions on Industry Applications*, 32(5):pp. 1130–1138, Sep./Oct. 1996.

[6] L.M. Tolbert, F.Z. Peng, and T.G. Habetler. Multilevel converters for large electric drives. *IEEE Transactions on Industry Applications*, 35(1):36–44, Jan.-Feb. 1999.

[7] A. Rufer, N. Schibli, and Ch. Briguet. A Direct Coupled 4-Quadrant Multilevel Converter for 16 2/3 Hz Traction Systems. In *Proc. of the IEEE Conference on Power Electronics and Variable Speed Drives (PEVD)*, Nottingham, UK, Sept. 1996.

[8] J. Ainsworth, D. Trainer, and P. Fitz. Multilevel converter, Patent GB 2294821A, 1996.

[9] M. Hiller, D. Krug, R. Sommer, and S. Rohner. A new highly modular medium voltage converter topology for industrial drive applications. In *Proc. of the 13th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Sept. 8-10, 2009.

[10] R. Marquardt. Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications. In *Proc. of the International Power Electronics Conference (IPEC)*, pp. 502-507, June 21-24, 2010.

Bibliography

[11] E. Solas, G. Abad, J.A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac. Modular Multilevel Converter With Different Submodule Concepts–Part I: Capacitor Voltage Balancing Method. *IEEE Transactions on Industrial Electronics*, 60(10):4525–4535, Oct. 2013.

[12] M. Winkelnkemper, A. Korn, and P. Steimer. A modular direct converter for transformerless rail interties. In *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 562-567, July 4-7, 2010.

[13] M. Vasiladiotis, S. Kenzelmann, N. Cherix, and A. Rufer. Power and DC link voltage control considerations for indirect AC/AC Modular Multilevel Converters. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Aug. 30 - Sept. 1, 2011.

[14] M. Glinka and R. Marquardt. A New AC/AC Multilevel Converter Family. *IEEE Transactions on Industrial Electronics*, 52(3):662–669, June 2005.

[15] M.A. Pérez, J.R. Rodríguez, E.J. José, and F. Kammerer. Predictive Control of AC-AC Modular Multilevel Converters. *IEEE Transactions on Industrial Electronics*, 59(7):2832–2839, July 2012.

[16] S. Allebrod, R. Hamerski, and R. Marquardt. New transformerless, scalable Modular Multilevel Converters for HVDC-transmission. In *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 174-179, June 15-19, 2008.

[17] M. Saeedifard and R. Iravani. Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System. *IEEE Transactions on Power Delivery*, 25(4):2903–2912, Oct. 2010.

[18] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li. Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems. *IEEE Transactions on Power Delivery*, 28(1):483–490, Jan. 2013.

[19] Q. Song, W. Liu, X. Li, H. Rao, S. Yu, and L. Li. A Steady-State Analysis Method for A Modular Multilevel Converter. *IEEE Transactions on Power Electronics*, 28(8):3702–3713, Aug. 2013.

[20] M. Hagiwara, K. Nishimura, and H. Akagi. A Medium-Voltage Motor Drive with a Modular Multilevel PWM Inverter. *IEEE Transactions on Power Electronics*, 25(7):1786–1799, July 2010.

[21] L. Ängquist, A. Haider, H.-P. Nee, and H. Jiang. Open-loop Approach to Control a Modular Multilevel Frequency Converter. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Aug. 30 - Sept. 1, 2011.

[22] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi. A single-phase to three-phase direct AC/AC modular multilevel cascade converter based on double-star bridge-cells (MMCC-DSBC). In *Proc. of the 1st International Future Energy Electronics Conference (IFEEC)*, pp. 476-481, Nov. 3-6, 2013.

[23] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F. Canales, and Y.R. de Novaes. A versatile DC-DC Converter for Energy Collection and Distribution using the Modular Multilevel Converter. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Aug. 30 - Sept. 1, 2011.

[24] S. Kenzelmann. *Modular DC/DC Converter for DC Distribution and Collection Networks*. PhD thesis, EPFL, Switzerland, 2012.

[25] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y.R. de Novaes. Isolated DC/DC Structure based on Modular Multilevel Converter. *IEEE Transactions on Power Electronics*, PP(99):1–1, 2014.

[26] A.J. Korn, M. Winkelnkemper, P. Steimer, and J.W. Kolar. Direct Modular Multi-Level Converter for gearless low-speed drives. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-7, Aug. 30-Sept. 1, 2011.

[27] L. Baruschka and A. Mertens. A New Three-Phase AC/AC Modular Multilevel Converter with Six Branches in Hexagonal Configuration. *IEEE Transactions on Industry Applications*, 49(3):1400–1410, May-June 2013.

[28] F. Kammerer, J. Kolb, and M. Braun. A novel cascaded vector control scheme for the Modular Multilevel Matrix Converter. In *Proc. of the 37th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 1097 - 1102, Nov. 7-10, 2011.

[29] W. Kawamura and H. Akagi. Control of the modular multilevel cascade converter based on triple-star bridge-cells (MMCC-TSBC) for motor drives. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3506-3513, Sept. 15-20, 2012.

[30] W. Kawamura, M. Hagiwara, and H. Akagi. Control and Experiment of a Modular Multilevel Cascade Converter Based on Triple-Star Bridge Cells (MMCC-TSBC). *IEEE Transactions on Industry Applications*, PP(99):1–1, 2014.

[31] M.M.C. Merlin, T.C. Green, P.D. Mitcheson, and D.R. Trainer. The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability. *IEEE Transactions on Power Delivery*, 29(1):310–317, Feb. 2014.

[32] K. Wang, Y. Li, Z. Zheng, and L. Xu. Voltage Balancing and Fluctuation-Suppression Methods of Floating Capacitors in a New Modular Multilevel Converter. *IEEE Transactions on Industrial Electronics*, 60(5):1943 – 1954, May 2013.

Bibliography

[33] H. Akagi. Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC). *IEEE Transactions on Power Electronics*, 26(11):3119–3130, Nov. 2001.

[34] S. Rohner, S. Bernet, M. Hiller, and R. Sommer. Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters. *IEEE Transactions on Industrial Electronics*, 57(8):3482–3494, Aug. 2010.

[35] Q. Tu, Z. Xu, and L. Xu. Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters. *IEEE Transactions on Power Delivery*, 26(3):2009–2017, July 2011.

[36] D. Siemaszko. Fast Sorting Method for Balancing Capacitor Voltages in Modular Multilevel Converters. *IEEE Transactions on Power Electronics*, PP(99):1–1, 2014.

[37] A. Hassanpoor, S. Norrga, H.-P. Nee, and L. Ängquist. Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application. In *Proc. of the 38th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 388-393,Oct. 25-28, 2012.

[38] A. Hassanpoor, L. Ängquist, S. Norrga, K. Ilves, and H.-P. Nee. Tolerance Band Modulation Methods for Modular Multilevel Converters. *IEEE Transactions on Power Electronics*, PP(99):1–1, 2014.

[39] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee. Predictive Sorting Algorithm for Modular Multilevel Converters Minimizing the Spread in the Submodule Capacitor Voltages. *IEEE Transactions on Power Electronics*, PP(99):1–1, 2014.

[40] J. Qin and M. Saeedifard. Reduced Switching-Frequency Voltage-Balancing Strategies for Modular Multilevel HVDC Converters. *IEEE Transactions on Power Delivery*, 28(4):2403–2410, Oct. 2013.

[41] M. Hagiwara and H. Akagi. PWM control and experiment of modular multilevel converters. In *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 154-161, June 15-19, 2008.

[42] Nikolaus Schibli. *Symmetrical Multilevel Converters with Two Quadrant DC-DC Feeding.* PhD thesis, EPFL, Switzerland, 2000.

[43] H. Akagi, S. Inoue, and T. Yoshii. Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration. *IEEE Transactions on Industry Applications*, 43(4):1041–1049, July-Aug. 2007.

[44] G. Konstantinou and V. Agelidis. Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques. In *Proc. of the 4th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pp. 3399 - 3404, May 25-27, 2009.

194

[45] Q. Tu and Z. Xu. Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter. *IEEE Transactions on Power Delivery*, 26(1):298–306, Jan. 2011.

[46] G. Konstantinou, M. Ciobotaru, and V. Agelidis. Selective harmonic elimination pulse-width modulation of modular multilevel converters. *IET Power Electronics*, 6(1):96–107, Jan. 2013.

[47] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee. A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency. *IEEE Transactions on Power Electronics*, 27(8):3482–3494, Aug. 2012.

[48] L. Ängquist, A.Antonopoulos, S. Norrga, and H.-P. Nee. Arm-current-based control of modular multilevel converters. In *Proc. of the 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Sept. 2-6, 2013.

[49] N. Cherix, M. Vasiladiotis, and A. Rufer. Functional Modeling and Energetic Macroscopic Representation of Modular Multilevel Converters. In *Proc. of the 15th International Power Electronics and Motion Control Conference (EPE-PEMC)*, pp. 1-8, Sept. 4-6, 2012.

[50] Q. Tu, Z. Xu, Y. Chang, and L. Guan. Suppressing DC Voltage Ripples of MMC-HVDC Under Unbalanced Grid Conditions. *IEEE Transactions on Power Delivery*, 27(3):1332–1338, July 2012.

[51] A. Antonopoulos, L. Ängquist, and H.-P. Nee. On dynamics and voltage control of the Modular Multilevel Converter. In *Proc. of the 13th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Sept. 8-10, 2009.

[52] M.A. Pérez and J. Rodríguez. Generalized modeling and simulation of a modular multilevel converter. In *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 1863-1868, June 27-30, 2011.

[53] S. Rohner, J. Weber, and S. Bernet. Continuous model of Modular Multilevel Converter with experimental verification. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4021-4028, Sept. 17-22, 2011.

[54] M. Hagiwara and H. Akagi. Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters. *IEEE Transactions on Power Electronics*, 24(24):1737–1746, July 2009.

[55] M. Hagiwara, R. Maeda, and H. Akagi. Control and Analysis of the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC). *IEEE Transactions on Power Electronics*, 26(6):1649–1658, June 2011.

[56] J. Kolb, F. Kammerer, and M. Braun. Straight forward vector control of the Modular Multilevel Converter for feeding three-phase machines over their complete

frequency range. In *Proc. of the 37th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 1596-1601, Nov. 7-10, 2011.

[57] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzandé, J.-C. Vannier, and M. Molinas. An Energy-Based Controller for HVDC Modular Multilevel Converter in Decoupled Double Synchronous Reference Frame for Voltage Oscillation Reduction. *IEEE Transactions on Industrial Electronics*, 60(6):2360–2371, June 2013.

[58] P. Munch, D. Gorges, M. Izak, and S. Liu. Integrated current control, energy control and energy balancing of Modular Multilevel Converters. In *Proc. of the 36th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 150-155, Nov. 7-10, 2010.

[59] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.P. Nee. Open-Loop Control of Modular Multilevel Converters Using Estimation of Stored Energy. *IEEE Transactions on Industry Applications*, 47(6):2516–2524, Nov.-Dec. 2011.

[60] L. Harnefors, A. Antonopoulos, S. Norrga, L. Ängquist, and H.-P. Nee. Dynamic Analysis of Modular Multilevel Converters. *IEEE Transactions on Industrial Electronics*, 60(7):2526–2537, July 2013.

[61] X. Li, W. Liu, Q. Song, H. Rao, and S. Xu. An enhanced MMC topology with DC fault ride-through capability. In *Proc. of the 39th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 6382-6188, Nov. 10-13, 2013.

[62] A. Korn, M. Winkelnkemper, and P. Steimer. Low output frequency operation of the Modular Multi-Level Converter. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3993-3997, Sept. 12-16, 2010.

[63] M. Guan and Z. Xu. Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions. *IEEE Transactions on Power Electronics*, 27(12):4858–4867, Dec. 2012.

[64] G. Bergna, J. Suul, E. Berne, P. Egrot, P. Lefranc, J. Vannier, and M. Molinas. Mitigating DC-side power oscillations and negative sequence load currents in Modular Multilevel Converters under unbalanced faults- first approach using resonant PI. In *Proc. of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp. 537-542, 25-28 Oct., 2012.

[65] C. Blanc. *Modeling of a Vanadium Redox Flow Battery Electricity Storage System*. PhD thesis, EPFL, Switzerland, 2009.

[66] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura. State-of-Charge (SOC)-Balancing Control of a Battery Energy Storage System Based on a Cascade PWM Converter. *IEEE Transactions on Power Electronics*, 24(6):1628–1636, June 2009.

[67] L. Maharjan, T. Yamagishi, and H. Akagi. Active-Power Control of Individual Converter Cells for a Battery Energy Storage System Based on a Multilevel Cascaded PWM Converter. *IEEE Transactions on Power Electronics*, 27(3):1099–1107, March 2012.

[68] M. Vasiladiotis and A. Rufer. Balancing control actions for cascaded H-bridge converters with integrated battery energy storage. In *Proc. of the 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Sept. 2-6, 2013.

[69] M. Vasiladiotis, A. Rufer, and A. Béguin. Modular converter architecture for medium voltage ultra fast EV charging stations: Global system considerations. In *Proc. of the IEEE International Electric Vehicle Conference (IEVC)*, pp. 1-7, Mar. 4-8, 2012.

[70] I. Trintis, S. Munk-Nielsen, and R. Teodorescu. Cascaded H-bridge with bidirectional boost converters for energy storage. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-9, Aug. 30- Sept. 1, 2011.

[71] N. Kawakami, S. Ota, H. Kon, S. Konno, H. Akagi, H. Kobayashi, and N. Okada. Development of a 500-kW Modular Multilevel Cascade Convertor for Battery Energy Storage Systems. *IEEE Transactions on Industry Applications*, PP(99):1–1, 2014.

[72] M. Schroeder, S. Henninger, J. Jaeger, A. Rasic, H. Rubenbauer, and H. Leu. Integration of batteries into a Modular Multilevel Converter. In *Proc. of the 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-12, Sept. 2-6, 2013.

[73] A. Hillers and J. Biela. Optimal design of the modular multilevel converter for an energy storage system based on split batteries. In *Proc. of the 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-11, Sept. 2-6, 2013.

[74] I. Trintis, S. Munk-Nielsen, and R. Teodorescu. A new modular multilevel converter with integrated energy storage. In *Proc. of the 37th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 1075-1080, Nov. 7-10, 2011.

[75] L. Baruschka and A. Mertens. Comparison of Cascaded H-Bridge and Modular Multilevel Converters for BESS application. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 909-916, Sept. 17-22, 2011.

[76] DOE Global Energy Storage Database. http://www.energystorageexchange.org/.

[77] S. Haghbin, S. Lundmark, M. Alaküla, , and O. Carlson. Grid-Connected Integrated Battery Chargers in Vehicle Applications: Review and New Solution. *IEEE Transactions on Industrial Electronics*, 60(2):pp. 459–473, Feb. 2013.

[78] J.-Y. Lee and H.-J. Chae. 6.6-kW Onboard Charger Design Using DCM PFC Converter With Harmonic Modulation Technique and Two-Stage DC/DC Converter. *IEEE Transactions on Industrial Electronics*, 61(3):1243–1252, March 2014.

[79] Z. Amjadi and S.S. Williamson. Power-Electronics-Based Solutions for Plug-in Hybrid Electric Vehicle Energy Storage and Management Systems. *IEEE Transactions on Industrial Electronics*, 57(2):608–616, Feb. 2010.

[80] M. Yilmaz and P.T. Krein. Battery Charger for Electric Vehicle Traction Battery Switch Station. *IEEE Transactions on Industrial Electronics*, 28(5):151–2169, May 2013.

[81] A. Kuperman, U. Levy, A. Zafransky, and A. Savernin. Battery Charger for Electric Vehicle Traction Battery Switch Station. *IEEE Transactions on Industrial Electronics*, 60(12):pp. 5391–5399, Dec. 2013.

[82] M. Takagi, Y. Iwafune, K. Yamaji, H. Yamamoto, K. Okano, R. Hiwatari, and T. Ikeya. Economic Value of PV Energy Storage Using Batteries of Battery-Switch Stations. *IEEE Transactions on Sustainable Energy*, 4(1):pp. 164–173, January 2013.

[83] Q. Dai, T. Cai, S. Duan, and F. Zhao. Stochastic Modeling and Forecasting of Load Demand for Electric Bus Battery-Swap Station. *IEEE Transactions on Power Delivery*, PP(99):1–1, 2014.

[84] B. Kang and G. Ceder. Battery materials for ultrafast charging and discharging. *Nature*, 458:190–193, 2009.

[85] H. Zhang, X. Yu, and P. V. Braun. Three-dimensional bicontinuous ultrafast-charge and -discharge bulk battery electrodes. *Nature Nanotechnology*, 6:277–281, 2011.

[86] S.-J. Huang, B.-G. Huang, and F.-S. Pai. Fast Charge Strategy Based on the Characterization and Evaluation of LiFePO$_4$ Batteries. *IEEE Transactions on Power Electronics*, 28(4):pp. 1555–1562, April 2013.

[87] D. Aggeler, F. Canales, H. Zelaya De La Parra, N. Butcher, and O. Apeldoorn. Ultra-fast DC-charge infrastructures for EV-mobility and future smart grids. In *Proc. of the Innovative Smart Grid Technologies Conference Europe (ISGT)*, pp. 1-8, Oct. 11-13, 2010.

[88] K. Yunus, H. Zelaya De La Parra, and M. Reza. Distribution grid impact of Plug-In Electric Vehicles charging at fast charging stations using stochastic charging model. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-11, Aug. 30-Sept. 1, 2011.

[89] S. Bai, D. Yu, and S. Lukic. Optimum design of an EV/PHEV charging station with DC bus and storage system. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.1178,1184, Sept. 12-16, 2010.

[90] G. Joos, M. De Freige, and M. Dubois. Design and simulation of a fast charging station for PHEV/EV batteries. In *Proc. of the IEEE Electric Power and Energy Conference (EPEC)*, pp.1-5, Aug. 25-27, 2010.

[91] H. Hõimoja, M. Vasiladiotis, S. Grioni, M. Capezzali, A. Rufer, and H.B. Püttgen. Towards Ultrafast Charging Solutions of Electric Vehicles. In *Cigré Session 44*, Aug. 26-31, 2012.

[92] S. Bai and S.M. Lukic. Unified Active Filter and Energy Storage System for an MW Electric Vehicle Charging Station. *IEEE Transactions on Power Electronics*, 28(12):5793–5803, Dec. 2013.

[93] H. Hõimoja, M. Vasiladiotis, and A. Rufer. Power Interfaces and Storage Selection for an Ultrafast EV Charging Station. In *Proc. of IET Power Electronics, Machines and Drives Conference*, March 27-29, 2012.

[94] G. Waltrich, J.L. Duarte, and M.A.M Hendrix. Multiport Converter for Fast Charging of Electrical Vehicle Battery. *IEEE Transactions on Industry Applications*, 48(6):pp. 2129–2139, November/December 2012.

[95] A. Maitra. Utility Direct Technology Boosts Efficiency Of Fast Charging For Electric Vehicles. *how2power today newsletters*, April 2012.

[96] S. Wang, R. Crosier, and Y. Chu. Investigating the power architectures and circuit topologies for megawatt superfast electric vehicle charging stations with enhanced grid support functionality. In *Proc. of the IEEE International Electric Vehicle Conference (IEVC)*, pp. 1-8, Mar. 4-8, 2012.

[97] C. Zhao, D. Dujic, A. Mester, J.K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti. Power Electronic Traction Transformer–Medium Voltage Prototype. *IEEE Transactions on Industrial Electronics*, 61(7):pp. 3257–3268, July 2014.

[98] D. Dujic, C. Zhao, A. Mester, J.K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti. Power Electronic Traction Transformer-Low Voltage Prototype. *IEEE Transactions on Power Electronics*, 28(12):pp. 5522–5534, Dec. 2013.

[99] F. Iov, F. Blaabjerg, J. Clare, P. Wheeler, A. Rufer, and A. Hyde. UNIFLEX-PM - A Key-Enabling Technology for Future European Electricity Networks. *European Power Electronics and Drives Association (EPE) Journal*, 19(4), Oct.-Dec. 2009.

[100] H. Akagi and R. Kitada. Control and Design of a Modular Multilevel Cascade BTB System Using Bidirectional Isolated DC/DC Converters. *IEEE Transactions on Power Electronics*, 26(9):2457–2464, Sept. 2011.

[101] T. Zhao, G. Wang, S. Bhattacharya, and A.Q. Huang. Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer. *IEEE Transactions on Power Electronics*, 28(4):pp. 1523–1532, April 2013.

[102] X. She, A.Q. Huang, and R. Burgos. Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems. *IEEE Trnsactions on Emerging and Selected Topics in Power Electronics*, 1(3):pp. 186–198, Sept. 2013.

[103] R. Teodorescu, M. Liserre, and P. Rodriguez. *Grid Converters for Photovoltaic and Wind Power Systems.* John Wiley & Sons, Ltd., 2011.

[104] S.P. Engel and R.W. De Doncker. Control of the Modular Multi-level Converter for minimized cell capacitance. In *Proc. of the 14th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Aug. 30 - Sept. 1, 2011.

[105] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Ängquist, and H.P. Nee. Capacitor Voltage Ripple Shaping in Modular Multilevel Converters Allowing for Operating Region Extension. In *Proc. of the 37th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 4403-4408, Nov. 7-10, 2011.

[106] H. Bühler. *Réglage de systèmes d'électronique de puissance - Volume 1: Théorie.* PPUR, Presses Polytechniques et Universitaires Romandes, 1997.

[107] R. Teodorescu, F. Blaabjerg, M. Liserre, and P.C. Loh. Proportional-resonant controllers and filters for grid-connected voltage-source converters. *Electric Power Applications, IEE Proceedings*, 5(5):750–762, September 2006.

[108] D.N. Zmood and D.G. Holmes. Stationary frame current regulation of PWM inverters with zero steady-state error. *IEEE Transactions on Power Electronics*, 18(3):814–822, May 2003.

[109] B. Bahrani, A. Rufer, S. Kenzelmann, and L.A.C. Lopes. Vector Control of Single-Phase Voltage-Source Converters Based on Fictive-Axis Emulation. *IEEE Transactions on Industry Applications*, 47(2):831–840, March-April 2011.

[110] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg. A New Single-Phase PLL Structure Based on Second Order Generalized Integrator. In *Proc. of the 37th IEEE Power Electronics Specialists Conference (PESC)*, pp. 1-6, June 18-22, 2006.

[111] P. Rioual, H. Pouliquen, and J.-P. Louis. Regulation of a PWM rectifier in the unbalanced network state using a generalized model. *IEEE Transactions on Power Electronics*, 11(3):495–502, May 1996.

[112] H.-.S. Song and K. Nam. Dual current control scheme for PWM converter under unbalanced input voltage conditions. *IEEE Transactions on Industrial Electronics*, 46(5):953–959, Oct. 1999.

[113] Yongsug Suh and T.A. Lipo. Control scheme in hybrid synchronous stationary frame for PWM AC/DC converter under generalized unbalanced operating conditions. *IEEE Transactions on Industry Applications*, 42(3):825–835, May/June 2006.

[114] D. Siemaszko and A.C. Rufer. Power compensation approach and double frame control for grid connected converters. In *Proc. of the 10th IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, pp. 1263-1268, 22-25 April, 2013.

[115] R.W. Erickson and D. Maksimović. *Fundamentals of Power Electronics*. Kluwer Academic Publishers, 2004.

[116] D. Barthélémy. Evaluation of power interfaces between Modular Multilevel Converter submodules and split battery energy storage systems (*in French*). Technical report, EPFL, Switzerland, 2013.

[117] S. Rivera, S. Kouro, B. Wu, J.I. Leon, J. Rodríguez, , and L.G. Franquelo. Cascaded H-Bridge multilevel converter multistring topology for large scale photovoltaic systems. In *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 1837-1844, June 27-30, 2011.

[118] M. Coppola, A. Del Pizzo, and D. Iannuzzi. A power traction converter based on Modular Multilevel Architecture integrated with energy storage devices. In *Proc. of the International Conference on Electrical Systems for Aircraft, Railway and Ship Propulsion (ESARS)*, pp. 1-7, Oct. 16-18, 2012.

[119] A.D. Aquila, M. Liserre, V.G. Monopoli, and P. Rotondo. An energy-based control for an n-H-bridges multilevel active rectifier. *IEEE Transactions on Industrial Electronics*, 52(3):670–678, June 2005.

[120] R.E. Betz and T.J. Summers. Using a cascaded H-bridge STATCOM for rebalancing unbalanced voltages. In *Proc. of the 7th International Conference on Power Electronics (ICPE)*, pp. 1219-1224, Oct. 22-26, 2007.

[121] C. Fahrni, A. Rufer, F. Bordry, and J.P. Burnet. A Novel 60 MW Pulsed Power System based on Capacitive Energy Storage for Particle Accelerators. *European Power Electronics and Drives Association (EPE) Journal*, 18(4):5–13, Dec. 2008.

[122] B. Bahrani, S. Kenzelmann, and A. Rufer. Multivariable-PI-Based dq Current Control of Voltage Source Converters With Superior Axis Decoupling Capability. *IEEE Transactions on Industrial Electronics*, 58(7):3016–3026, July 2011.

[123] P. Rodriguez, J. Pou, J. Bergas, J.I. Candela, R.P. Burgos, and D. Boroyevich. Decoupled Double Synchronous Reference Frame PLL for Power Converters Control. *IEEE Transactions on Power Electronics*, 22(2):584–592, March 2007.

[124] M. Vasiladiotis, N. Cherix, and A. Rufer. Accurate Capacitor Voltage Ripple Estimation and Current Control Considerations for Grid-Connected Modular Multilevel Converters. *IEEE Transactions on Power Electronics*, 29(9):pp. 4568–4579, September 2014.

[125] H. Li, F.Z. Peng, and J.S. Lawler. A Natural ZVS Medium-Power Bidirectional DC-DC Converter With Minimum Number of Devices. *IEEE Transactions on Industry Applications*, 39(2):525–535, Mar.-Apr. 2003.

[126] F.Z. Peng, H. Li, G.-J. Su, and J. S. Lawler. A New ZVS Bidirectional DC-DC Converter for Fuel Cell and Battery Application. *IEEE Transactions on Power Electronics*, 19(1):pp. 54–65, Jan. 2004.

[127] Z. Wang and H. Li. Optimized operating mode of current-fed dual half bridges dc-dc converters for energy storage applications. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 731-737, Sept. 20-24, 2009.

[128] H. Daneshpajooh, A. Bakhshai, and P. Jain. Optimizing dual half bridge converter for full range soft switching and high efficiency. In *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1296-1301, Sept. 17-22, 2011.

[129] X. Liu, H. Li, and Z. Wang. A Fuel Cell Power Conditioning System With Low-Frequency Ripple-Free Input Current Using a Control-Oriented Power Pulsation Decoupling Strategy. *IEEE Transactions on Power Electronics*, 29(1):159–169, Jan. 2014.

[130] A. Karimi and G. Galdos. Fixed-order H∞ controller design for nonparametric models by convex optimization. *Automatica*, 46(8):1388–1394, 2010.

[131] G. Galdos, A. Karimi, and R. Longchamp. H∞ controller design for spectral MIMO models by convex optimization. *Journal of Process Control*, 20(10):1175–1182, 2010.

[132] H. Li and F.Z. Peng. Modeling of a new ZVS Bi-directional DC-DC Converter. *IEEE Transactions on Aerospace and Electronic Systems*, 40(1):272–283, Jan. 2004.

[133] I.D. Landau, R. Lozano, M. M'Saad, and A. Karimi. *Adaptive Control: Algorithms, Analysis and Applications. Second Edition.* Springer, 2011.

[134] B. Bahrani, M. Saeedifard, A. Karimi, and A. Rufer. A Multivariable Design Methodology for Voltage Control of a Single-DG-Unit Microgrid. *IEEE Transactions on Industrial Informatics*, 9(2):589–599, May 2013.

[135] B. Bahrani, M. Vasiladiotis, and A. Rufer. High-Order Vector Control of Grid-Connected Voltage-Source Converters With LCL-Filters. *IEEE Transactions on Industrial Electronics*, 61(6):2767–2775, June 2014.

[136] N. Cherix. Conception et réalisations d'un convertisseur modulaire multiniveaux triphasé (MMC) (*in French*). Master's thesis, EPFL, Switzerland, 2010.

[137] Powerizer product catalog. Available online: http://www.batteryspace.com.

[138] N. Mohan, T. M. Undeland, and W. P. Robbins. *Power Electronics: Converters, Applications and Design.* John Wiley & Sons, Inc., 2003.

[139] N. Burger. Study and Implementation of an Isolated DC-DC Converter for a Power Electronic Transformer-based Ultra-Fast EV Charger. Technical report, EPFL, Switzerland, 2013.

[140] N. Cherix, S. Delalay, P. Barrade, and A. Rufer. Fail-safe modular control platform for power electronic applications in R&D environments. In *Proc. of the 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, Sept. 2-6, 2013.

[141] N. Cherix. *Functional Description and Control Design of Modular Multilevel Converters.* PhD thesis, EPFL, 2014.

[142] J.A. Sabaté, V. Vlatkovic, R.B. Ridley, F. Lee, and B.H. Cho. Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter. In *Proc. of the 5th Annual Applied Power Electronics Conference and Exposition (APEC)*, pp. 275-284, March 11-16, 1990.

[143] V. Vlatković, J.A. Sabaté, R.B. Ridley, F.C. Lee, and B.H. Cho. Small-Signal Analysis of the Phase-Shifted PWM Converter. *IEEE Transactions on Power Electronics*, 7(1):128–135, 1992.

[144] L. Zhu, X. Xu, and F. Flett. A 3 kW Isolated Bi-directional DC/DC Converter for Fuel Cell Electric Vehicle Application. In *Proc. of the 43th International Power Electronics Conference (PCIM 2001)*, June 19-21, 2001.

Michail Vasiladiotis
Curriculum Vitae

Born in Feb. 8, 1986
Nationality: Greek
✆ *+41 (76) 27 58 021*
✉ *michail.vasiladiotis@gmail.com*

━━━━━━ Education

09.2010-09.2014	**PhD, Energy**, *Swiss Federal Institute of Technology (EPFL)*, Lausanne, Switzerland. PhD thesis: Modular Multilevel Converters with integrated split battery energy storage. Advisor: Prof. A. Rufer
09.2003-09.2009	**Diploma, Electrical and Computer Engineering**, *National Technical University of Athens (NTUA)*, Greece. Diploma thesis: Analysis, implementation, and experimental evaluation of control systems for a Modular Multilevel Converter. Supervisors: Prof. H.-P. Nee and Prof. S. Manias

━━━━━━ Experience

08.2010-Present — **Doctoral and Teaching Assistant**, *Laboratory of Industrial Electronics (LEI)*, EPFL, Lausanne, Switzerland.

- Designed and validated innovative control methods for Modular Multilevel Converters (MMC) with integrated split battery energy storage systems (BESS).
- Devised and investigated a novel Modular Multiport Power Electronic Transformer (M2PET) for compact medium voltage ultra-fast electric vehicle (EV) charging stations.
- Worked as member of a team which developed a versatile multifunctional prototype of MMC- and PET-based topologies with integrated split BESS.
- Implemented software for projects dealing with the experimental verification of advanced control methods for power electronic systems.
- Gave several course lectures and supervised various student projects.

10.2009-06.2010 — **Research Assistant**, *Laboratory of Electrical Machines and Power Electronics*, NTUA, Athens, Greece.

Designed, implemented and experimentally validated Model Predictive Control (MPC) schemes with focus on: a) single- and three-phase active rectifiers, b) asymmetrical Cascaded H-Bridge (CHB) converters.

03.2009-09.2009 — **Diploma Thesis Preparation**, *Laboratory of Electrical Energy Conversion*, KTH, Stockholm, Sweden.

Worked as a member of a research group focusing on the design and implementation of control systems for one of the first down-scaled MMC prototype demonstrators worldwide.

━━━━━━ Technical skills

Programming	Matlab, C, LaTeX, basic VHDL skills
Design	Altium Designer, Eagle, Actel Libero
Simulation	Simulink, PLECS, Portunus, Typhoon HIL, PSCAD, EMTPWorks
Experimentation	Code Composer Studio, LabVIEW, Simulink Real-Time Workshop
Applications	Maple, Adobe Illustrator

Scientific Record

Publications Author/co-author of 8 journal articles and 14 conference papers, cited by 351, h-index 8 (Source: Google Scholar–October 2014)

Awards Best paper in the special session on Modular Multilevel Converters, IECON 2013, Vienna, Austria

Activities IEEE Power Electronics Society Member, Reviewer for IEEE transactions/conferences and IET journals

Languages

English	**C2, Fluent**	*CPE-University of Cambridge, written/spoken fluency*
French	**C1, Advanced**	*Working language for the last three years*
German	**A2, Elementary**	*ZMP-Göthe Institut in 2001, very limited use ever since*
Greek	**Fluent**	*Native speaker*

Extracurricular Activities/ Interests

○ Degree in classical guitar performance, Hellenic Ministry of Culture, Jan. 2009
○ Degree in classical harmony, Hellenic Ministry of Culture, June 2009

Publication List

Under Review

[R1] **M. Vasiladiotis**, N. Cherix, and A. Rufer, "Impact of Grid Asymmetries on the Operation and Design of Modular Multilevel Converters." submitted to IEEE Trans. Ind. Electron., 2014.

Journal Articles

[J1] **M. Vasiladiotis** and A. Rufer, "A Modular Multiport Power Electronic Transformer with Integrated Split Battery Energy Storage for Versatile Ultra-Fast EV Charging Stations," *accepted in IEEE Trans. Ind. Electron.*, 2015.

[J2] **M. Vasiladiotis** and A. Rufer, "Analysis and Control of Modular Multilevel Converters with Integrated Battery Energy Storage," *IEEE Trans. Power Electron.*, vol. 30, pp. 163–175, Jan. 2015.

[J3] **M. Vasiladiotis** and A. Rufer, "Dynamic Analysis and State Feedback Voltage Control of Single-Phase Active Rectifiers with DC-Link Resonant Filters," *IEEE Trans. Power Electron.*, vol. 29, pp. 5620–5633, Oct. 2014.

[J4] **M. Vasiladiotis**, N. Cherix, and A. Rufer, "Accurate Capacitor Voltage Ripple Estimation and Current Control Considerations for Grid-Connected Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 29, pp. 4568–4579, Sept. 2014.

[J5] B. Bahrani, **M. Vasiladiotis**, and A. Rufer, "High-Order Vector Control of Grid-Connected Voltage Source Converters with LCL-Filters," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 2767–2775, June 2014.

[J6] N. Cherix, **M. Vasiladiotis**, and A. Rufer, "Sizing of branch inductors parameters in modular multilevel converters: An analytical approach," *Eur. J. Elect. Eng.*, vol. 16, pp. 389–408, 2013.

[J7] K. Pavlou, **M. Vasiladiotis**, and S. Manias, "Constrained Model Predictive Control Strategy for Single-Phase Switch-Mode Rectifiers," *IET Power Electron.*, vol. 5, pp. 31–40, January 2012.

[J8] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, **M. Vasiladiotis**, and H.-P. Nee, "Open-loop Control of Modular Multilevel Converters using Estimation of Stored Energy," *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2516–2524, Nov.-Dec. 2011.

Conference Papers

[C1] **M. Vasiladiotis**, B. Bahrani, N. Burger, and A. Rufer, "Modular Converter Architecture for Medium Voltage Ultra Fast EV Charging Stations: Dual Half-Bridge-based Isolation Stage," in *Proc. Int. Power Electron. Conf. (IPEC)*, Hiroshima, Japan, May 18-21, 2014.

[C2] **M. Vasiladiotis**, N. Cherix, D. Siemaszko, and A. Rufer, "Operation of Modular Multilevel Converters Under Grid Asymmetries," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc. (IECON)*, Vienna, Austria, Nov. 10-13, 2013.

[C3] **M. Vasiladiotis** and A. Rufer, "Fictive Axis Emulator-based State Feedback Vector Current Control for Single-Phase Voltage Source Converters," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc. (IECON)*, Vienna, Austria, Nov. 10-13, 2013.

[C4] **M. Vasiladiotis** and A. Rufer, "Balancing Control Actions for Cascaded H-Bridge Converters with Integrated Battery Energy Storage," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Lille, France, Sep. 3-5, 2013.

[C5] **M. Vasiladiotis**, N. Cherix, and A. Rufer, "Accurate Voltage Ripple Estimation and Decoupled Current Control for Modular Multilevel Converters," in *Proc. 15th Int. Power Electron. Motion Control Conf. (EPE-PEMC)*, Novi Sad, Serbia, Sep. 4-6, 2012.

[C6] N. Cherix, **M. Vasiladiotis**, and A. Rufer, "Functional Modeling and Energetic Macroscopic Representation of Modular Multilevel Converters," in *Proc. 15th Int. Power Electron. Motion Control Conf. (EPE-PEMC)*, Novi Sad, Serbia, Sep. 4-6, 2012.

[C7] H. Hõimoja, **M. Vasiladiotis**, S. Grioni, M. Capezzali, A. Rufer, and H. Püttgen, "Toward Ultrafast Charging of Electric Vehicles," in *Proc. CIGRE Session*, Paris, France, Aug. 26-31, 2012.

[C8] H. Hõimoja, **M. Vasiladiotis**, and A. Rufer, "Power Interfaces and Storage Selection for an Ultrafast EV Charging Station," in *Proc. IET 6th Int. Conf. Power Electron., Mach. Drives (PEMD)*, Bristol, UK, March 27-29, 2012.

[C9] **M. Vasiladiotis**, A. Rufer, and A. Béguin, "Modular Converter Architecture for Medium Voltage Ultra Fast EV Charging Stations: Global System Considerations," in *Proc. 1st IEEE Int. Electric Vehicle Conf. (IEVC)*, Greenville, SC, USA, March 4-8, 2012.

[C10] **M. Vasiladiotis**, K. Pavlou, S. Manias, and A. Rufer, "Model Predictive-based Control Method for Cascaded H-Bridge Multilevel Active Rectifiers," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Phoenix, AZ, USA, Sep. 17-22, 2011.

[C11] **M. Vasiladiotis**, S. Kenzelmann, N. Cherix, and A. Rufer, "Power and DC Link Voltage Control Considerations for Indirect AC/AC Modular Multilevel Converters," in *Proc. 14th Eur. Conf. Power Electron. Appl. (EPE)*, Birmingham, UK, Aug. 30- Sep. 1, 2011.

[C12] S. Kenzelmann, A. Rufer, **M. Vasiladiotis**, D. Dujic, F. Canales, and Y. D. Novaes, "A Versatile DC-DC Converter for Energy Collection and Distribution using the Modular Multilevel Converter," in *Proc. 14th Eur. Conf. Power Electron. Appl. (EPE)*, Birmingham, UK, Aug. 30- Sep. 1, 2011.

[C13] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, **M. Vasiladiotis**, and H.-P. Nee, "Inner Control of Modular Multilevel Converters - An Approach using Open-loop Estimation of Stored Energy," in *Proc. IEEE Int. Power Electron. Conf. (IPEC)*, Sapporo, Japan, June 21-24, 2010.

[C14] D. Siemaszko, A. Antonopoulos, K. Ilves, **M. Vasiladiotis**, L. Ängquist, and H.-P. Nee, "Evaluation of Control and Modulation Methods for Modular Multilevel Converters," in *Proc. IEEE Int. Power Electron. Conf. (IPEC)*, Sapporo, Japan, June 21-24, 2010.