A 5.43-μW 0.8-V Subthreshold Current-Sensing $\Sigma\Delta$ Modulator for Low-Noise Sensor Interfaces

Nikola Katic, *Student Member, IEEE*, Ibrahim Kazi, *Student Member, IEEE*, Armin Tajalli, *Member, IEEE*
Alexandre Schmid, *Member, IEEE*, Yusuf Leblebici, *Fellow, IEEE*

***Abstract*—A micro-watt power subthreshold current modulator suitable for low-power and low-noise sensor interfaces is presented. The prototype design is based on Subthreshold Source Coupled Logic (STSCL) cells and implemented in a 0.18 μm standard CMOS technology. The modulator operates with the supply voltage of 0.8 V which is significantly lower than the nominal supply of the technology node (1.8 V). It consumes 5.43 μW of power at the maximum bandwidth of 20 kHz. The obtainable current-sensing resolution ranges from ENOB=7.1 bits at a 5 kHz bandwidth to ENOB=6.5 bits at a 20 kHz bandwidth. The obtained power-efficiency of 1.5 pJ per conversion outperforms any existing current-mode analog-to-digital converter (ADC) design and is comparable to conventional voltage-mode Continuous-Time (CT) $\Sigma\Delta$ modulators. The modulator generates very low levels of switching noise thanks to the continuous-time operation and subthreshold current-mode circuits that draw a constant subthreshold current from the voltage supply. The modulator is used as an interface for sensors with current-mode output in ultra low-power conditions and can also be used for power monitoring circuits.**

***Index Terms*—Sensor Interfaces, Current Sensing, Current-mode, Low-Power, Low-Voltage, Sigma-Delta Modulation**

I. Introduction

Many state-of-the-art IC sensors have current-mode or charge-packet-based outputs [1]–[6]. In these cases, a current-to-voltage conversion is necessary in order to utilize voltage-mode ADCs (except in [6] where a current-input ADC is used). Using integrated resistors for current-to-voltage conversion is generally avoided because on-chip high-value resistors are large, non-linear and introduce high thermal noise. Hence, conversion is preferably performed by integrating the current output on an on-chip (integrated) capacitor. However, current integration on a capacitor typically suffers from low bandwidth and/or high non-linearity which is inefficient in some applications. Another possible solution is the implementation of active integrated Trans-Impedance Amplifiers (TIAs) with high trans-impedance-gain (in Giga-Ω range). However, implementing a low-power low-voltage linear active high-gain TIA is a challenging task. At relatively high supply voltages, if fairly linear, even state-of-the-art integrated TIAs (see [7], [8]) consume relatively high amount of power. Thus, even extremely efficient voltage-mode low-power ADCs placed in the following stage can not compensate for the power inefficiency introduced by the active TIA.

For noise-sensitive front-end circuits, it is very important to minimize the voltage supply noise and substrate noise by minimizing the switching activity of the surrounding circuits. Continuous-time (CT) operation minimizes the spikes in the supply current (small dI/dt) and results in low-noise generation. This work focuses on the design of a CT subthreshold current-mode modulator.

Current-mode circuits suffer from the limited accuracy of the current transfer which limits their final performance. Consequently, a very few such designs and promising concepts have been proposed in literature. Current-mode pipeline ADCs were presented in [9] and [10]. Furthermore, a Successive-Approximation ADC with current-mode comparator was presented in [11]. Current-mode interpolation stage has also been used by folding and interpolating ADCs [12] [13].

The presented modulator is used as a readout interface for sensors at low-power and low-voltage conditions. Moreover, it can be used for power monitoring schemes such as [14], which would take benefit of sensing small (divided and copied) replicas of the supply currents in the digital domain at low power cost.

II. Subthreshold-Current-Sensing $\Sigma\Delta$ Modulator

The proposed current-sensing modulator implements a first-order $\Sigma\Delta$ architecture with a quantizer based on subthreshold STSCL cells forming a ring-oscillator. A top-level diagram of the modulator is shown in Figure 1. In order to simplify the testing procedure and allow better input control, the input current is generated on-chip by converting the input voltage. The input current is combined with the reference currents and the DAC output currents and delivered to the differential current-mode low-pass filter operating in subthreshold mode. The filter output provides the control current for the ring-oscillator replica-biasing (RB) circuit (Figure 2). The RB circuit generates the tail current for the differential STSCL inverters within the ring-oscillator. Ring-oscillator outputs are used as inputs to the phase-to-frequency converter which performs the first-order differentiation of the phase in the digital domain. The number of logical "ones" in the phase-to-frequency converter output, represents the number of inverters within the ring-oscillator that underwent an output transition during the sampling cycle. The sum of the phase-to-frequency converter outputs is therefore proportional to the ring-oscillator frequency and the input current, and represents the final modulator digital output. The phase-to-frequency converter outputs are delivered to the thermometer-coded differential current-mode DAC which generates the feedback currents. The first-order $\Sigma\Delta$ loop results in second-order noise-shaping of the modulator, due to additional (intrinsic) first-order noise shaping property of the ring-oscillator-based quantizer [15].

978-1-4799-5442-1/14/$31.00 ©2014 IEEE

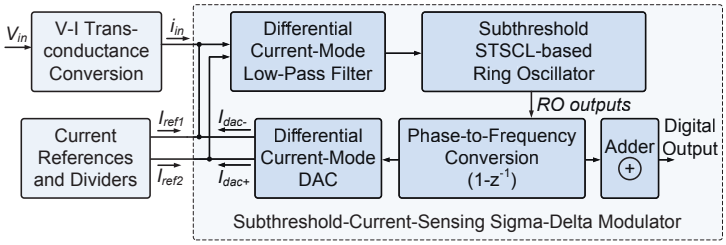

Figure 1: Top-level circuit-diagram of the current-sensing modulator

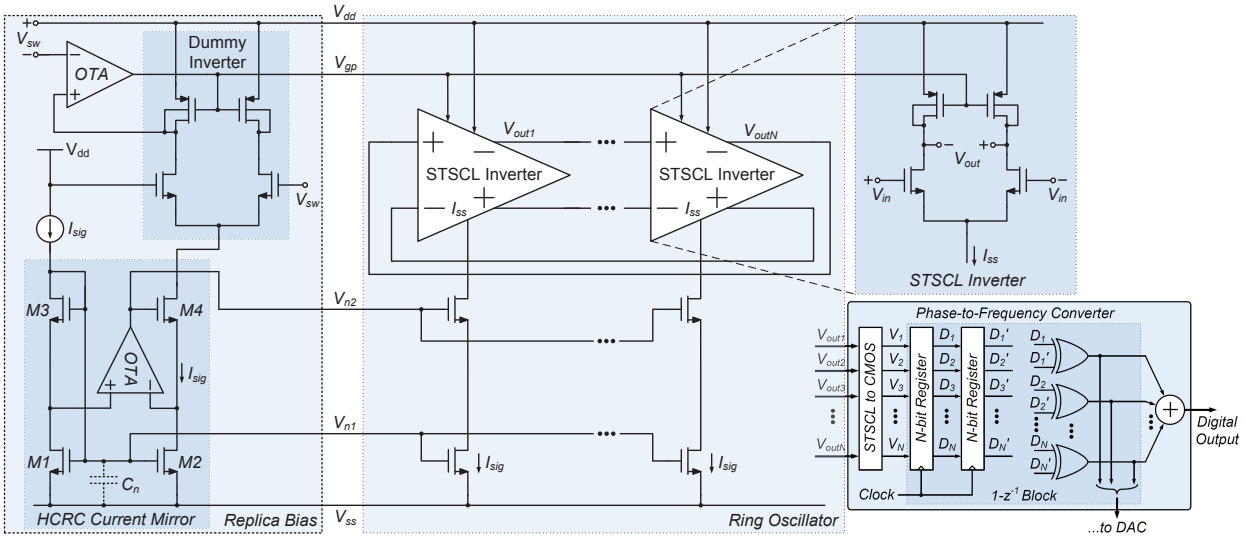

Figure 2: STSCL current-controlled ring oscillator and replica biasing circuit

III. Subthreshold Current Quantizer

The top-level schematic of the proposed current-quantizer is shown in Figure 2. Based on the current-signal input (I_{sig}), the RB circuit generates the controlling voltages for the cascoded current mirrors (V_{n1} and V_{n2}) and the gates of the BD-connected load devices V_{gp}. The current I_{sig} is copied by the High-Compliance-Regulated-Cascode (HCRC) current mirror [16] (modified for the subthreshold operation) to the corresponding STSCL inverter cells within the (current-controlled) ring oscillator. The low-swing STSCL voltage outputs of the Current-Controlled-Oscillator (CCO) are converted into full-swing CMOS outputs and delivered to the digital phase-to-frequency converter. The digital phase-to-frequency converter measures the frequency of the oscillator by performing a first-order differentiation ($1-z^{-1}$) in the digital domain (see [15]). The XOR outputs are directly connected to the thermometer-coded DAC in the feedback loop (see Figure 1).

The concept of Subthreshold Source-Coupled Logic for ultra-low power digital gates was introduced in [17]. The inverter cell is biased with the subthreshold current (I_{ss} - copy of I_{sig} in Figure 2) which is typically in the nA range, but can be set as low as 10 pA [17]. The replica-biasing circuit allows a dynamic control of the load bias by adjusting the gate voltage of the PMOS devices (V_{gp}). The RB feedback keeps the output voltage swing constant independently of the tail current I_{ss} and minimizes the effect of process variation. Having constant output swing is also important to guarantee the desired delay, noise margin and proper switching of the differential inverter. Random device mismatch remains as a dominant cause of load resistance variation. The load output node is connected to the bulk to modulate the depth of the depletion region underneath the gate, therefore modulating the drain current. This results in lower small-signal output impedance compared to bulk-source connection improving the stability of the feedback loop while maintaining enough load resistance for the desired output voltage swing. The power consumption is also reduced because the same stability (small-signal output impedance) would require significantly higher biasing current in the case of bulk-source connection.

Simulation results show that the Total-Harmonic-Distortion of less than -60 dB is achievable over 3 decades of the input current (from 100 pA to 100 nA) using appropriate device matching in the quantizer. The STSCL ring oscillator quantizer can therefore be used as a stand-alone subthreshold current-sensing modulator. A simplified version of the standalone quantizer is presented in [18], and the measurement results confirm the wide input current range. In [18], the measured distortion level is mainly limited by low output impedance of the current mirrors.

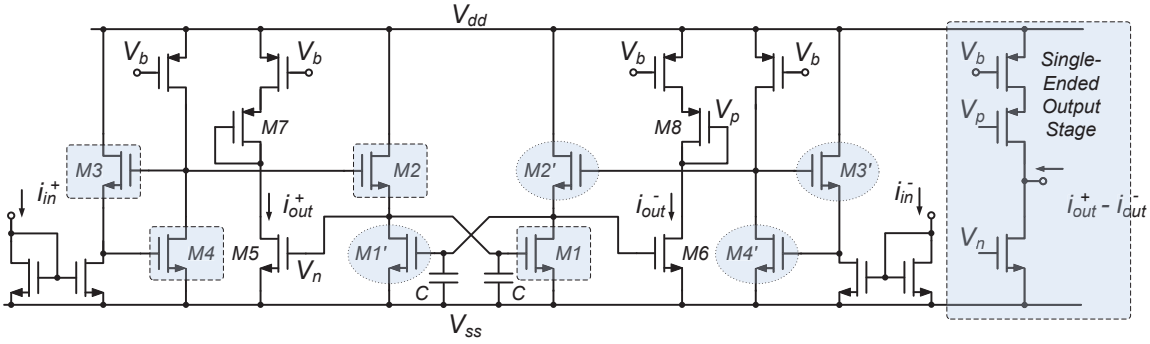

Figure 3: Companding current-mode low-pass filter with two translinear loops: M1-M2-M3-M4 and M1'-M2'-M3'-M4'

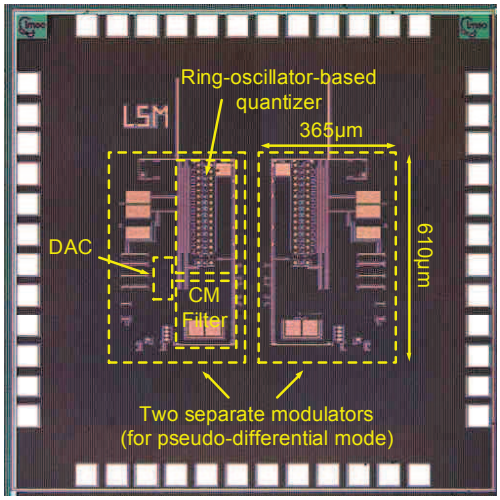

Figure 4: Die micrograph

IV. Current-Mode Low-Pass Filter

The translinear circuit technique is convenient for designing continuous-time analog processing circuits under low supply voltage conditions [19]. The low-pass filter implemented in this design is based on the translinear Companding Integrator (CI) originally designed in bipolar technology [20]. The class AB differential CI presented in [20] is implemented using subthreshold MOS devices and complemented with a single-ended output stage. The complete schematic of the filter is shown in Figure 3.

V. Measurement Results

A prototype of the current-sensing modulator (shown in Figure 1) is implemented in a standard 0.18 μm CMOS process. Two identical modulators are placed on the same die, and can be used in parallel operating in a pseudo-differential mode (Figure 4). A single modulator achieves 20 kHz of bandwidth while consuming 5.43 μW of power operating at a 0.8 V supply voltage. Most of the power is consumed by the quantizer (P_{ROQ} = 2.95 μW) and the DAC (P_{DAC} = 1.85 μW). The remaining power of 630 nW is consumed by the current-mode low-pass filter. The current references and the input transconductance stage are not considered as the part of the modulator core and their power consumption is not included in the measured 5.43 μW of total power. The peak measured SNDR is 44.5 dB at a 5 kHz bandwidth, and 40.89 dB at a 20 kHz bandwidth using a 1 kHz input signal and 1 MHz sampling rate (Figure 5). The maximum measured SNDR in differential mode is 43.6 dB (ENOB = 7) at a 20 kHz and 47.5 dB at 5 kHz bandwidth (ENOB=7.6). The summary of the modulator performance is presented in Table I. The efficiency (FoM) is defined as FoM = Power/(2·BW·2^{ENOB}).

Thanks to the current-mode operation and analog-to-digital conversion of the modulator, the presented design is compared to the best current-mode ADCs available in literature. The result of the comparison is given in (Table II) and expressed in terms of power efficiency.

VI. Conclusion

A micro-watt power subthreshold current-to-digital $\Sigma\Delta$ modulator is presented. The circuit is based on subthreshold-operation low-power low-voltage technique for continuous-time $\Sigma\Delta$ modulation. The presented prototype achieves current quantization of ENOB = 6.5 (ENOB = 6.8 in pseudo-differential mode) at a 20 kHz and ENOB = 7.1 (ENOB = 7.4 in pseudo-differential) at a 5 kHz bandwidth. The sampling rate of the converter is 1 MHz, the power consumption is 5.43 μW while operating at 0.8 V supply voltage. The power efficiency of the presented modulator outperforms all previously reported current-mode designs, and is comparable to many voltage-mode CT $\Sigma\Delta$ modulators.

The modulator is primarily intended for sensors with current-mode outputs at ultra low-power conditions where both passive and active current-to-voltage conversions are ineffective. Extremely low switching noise due to mainly static subthreshold current consumption makes it very attractive for low noise front-end circuits and interfaces. Due to micro-watt power operation the presented current-sensing modulator can also be used for on-chip current measurements in power management units.

The presented technique is scalable and would benefit from newer nanometer CMOS technology nodes. Increased matching would enable higher bandwidth or higher precision for the same size devices. Implementing a fully-differential topology would further improve the performance of the presented prototype. Future work will also include improving the current-

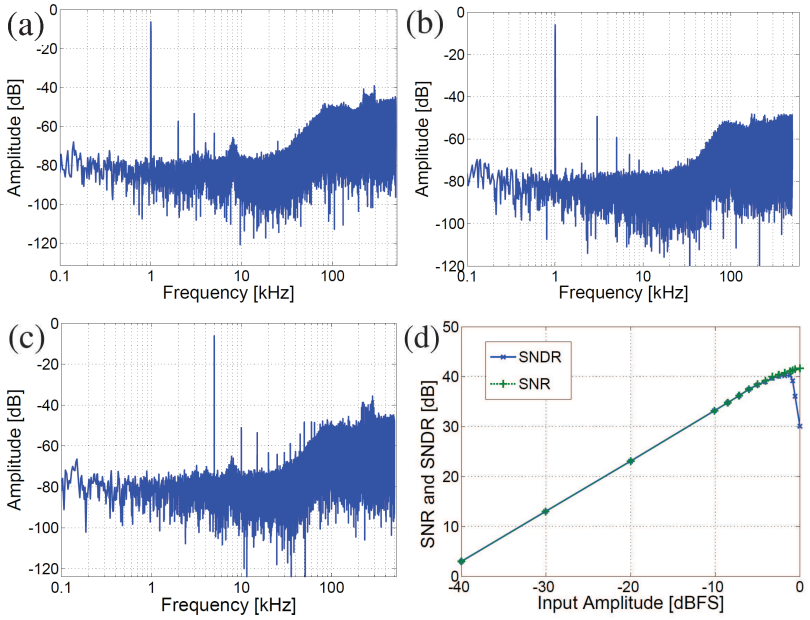

Table I: Performance Summary

Specification	Value
Input Range (Chip)	0-1.6V
Input Range (Mod.)	0-280nA
Sampling Frequency	1MHz
Input Bandwidth	5kHz/20kHz
Peak SNDR	44.5dB/40.5dB
Peak SNR	46dB/42dB
Power Consumption	5.43μW
Peak Efficiency (FOM)	1.5pJ/conv
Core Area	610μm $\times$ 210μm
Total Area	610μm $\times$ 365μm
Technology	0.18μm Std CMOS

Table II: Comparison with Current-Mode ADCs

	Power Efficiency [pJ/conv]
[9] ISSCC 2002	8.9
[10] CICC 2007	23
[11] JSSC 2000	26.5
[12] JSSC 2000	3.12
[13] JSSC 2003	13
This Work	1.5

Figure 5: Fast-Fourier-Transform (FFT) of the output signal for: (a) 1 kHz (1003.26 Hz) single-ended (b) 1kHz pseudo-differential (c) 5 kHz (4985.81 Hz) single-ended input signal at 1 MHz sampling rate and -6 dbFS. (d) SNR and SNDR versus input amplitude at 1kHz input frequency, 20kHz bandwidth and 1MHz sampling

mode DAC and using digitally-assisted and digitally-calibrated circuits to improve the resolution which is currently limited by the non-linearity. Therefore, digital calibration can additionally boost the performance of the presented subthreshold current-sensing technique.

REFERENCES

[1] R. Steadman, B. J. Hosticka et al., "A High Dynamic Range Current-Mode Amplifier for Computed Tomography," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 41, pp. 1615–1619, Jul. 2006.

[2] H.-S. Kim, G.-H. Cho et al., "An Asynchronous Sampling-Based 128x128 Direct Photon-Counting X-Ray Image Detector with Multi-Energy Discrimination and High Spatial Resolution," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 48, pp. 541–558, Feb. 2013.

[3] M. A. Szelezniak, A. Himmi et al., "Current Mode Monolithic Active Pixel Sensor With Correlated Double Sampling for Charged Particle Detection," *IEEE Sensors Journal*, vol. 7, pp. 137–150, Jan. 2007.

[4] P. M. Levine, K. L. Shepard et al., "Active CMOS Sensor Array for Electrochemical Biomolecular Detection," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 43, pp. 1859–1871, Aug. 2008.

[5] R. M. Philipp, R. Etienne-Cummings et al., "Linear Current-Mode Active Pixel Sensor," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 42, pp. 2482–2491, Nov. 2007.

[6] D. H. Woo, H. C. Lee et al., "Current Input Extended Counting ADC With Wide Dynamic Range for LWIR FPAs," *IEEE Sensors Journal*, vol. 9, pp. 441–448, 2009.

[7] G. Ferrari, M. Sampietro et al., "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 44, pp. 1609–1616, May 2009.

[8] A. Sharma, F. Ayazi et al., "A 104-dB Dynamic Range Transimpedance-Based CMOS ASIC for Tuning Fork Microgyroscopes," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 42, pp. 1790–1802, Aug. 2007.

[9] K. Poulton, M. Heshami et al., "A 4GSamples/s 8b ADC in 0.35μm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 2, pp. 126–434, 2002.

[10] N. Yoshii, Y. Sugimoto et al., "A Current-mode ADC with Current Exchanging and Averaging Capabilities by Switching the Currents and Calculating Data in the Digital Domain," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 209–212, 2007.

[11] S. Mortezapour, E. K. F. Lee, "A 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 35, pp. 642–646, Apr. 2000.

[12] B.-S. Song, S. F. Gillig et al., "A 1-V, 6-b 50-MSamples/s Current-Interpolating CMOS ADC," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 35, pp. 647–651, Apr. 2000.

[13] Y. Li, E. Sanchez-Sinencio, "A Wide Input Bandwidth 7-bit 300-MSample/s Folding and Current-Mode Interpolating ADC," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 38, pp. 1405–1410, Aug. 2003.

[14] M. Nomura, Y. Hagihara et al., "Delay and Power Monitoring Schemes for Minimizing Power Consumption by Means of Supply and Threshold Voltage Control in Active and Standby Modes," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 41, pp. 805–814, Apr. 2006.

[15] M. Z. Straayer, M. H. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 43, pp. 805–814, Apr. 2008.

[16] O. Charlon, W. Redman-White, "Ultra High-Compliance CMOS Current Mirrors for Low Voltage Charge Pumps and References," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 227–230, 2004.

[17] A. Tajalli, E. Vittoz et al., "Subthreshold Source-Coupled Logic Circuits for Ultra-Low-Power Applications," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 43, pp. 1699–1710, Jul. 2008.

[18] A. Tajalli, Y. Leblebici, "Subthreshold Current-Mode Oscillator-Based Quantizer with 3-Decade Scalable Sampling Rate and Pico-Ampere Range Resolution," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 174–177, 2010.

[19] E. Seevinck, E. Vittoz et al., "CMOS Translinear Circuits for Minimum Supply Voltage," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, pp. 1560–1564, Dec. 2000.

[20] E. Seevinck, "Companding Current-Mode Integrator: A New Circuit Principle for Continuous-Time Monolithic Filters," *IEEE Electronics Letters*, vol. 26, pp. 2046–2047, Nov. 1990.