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Ga-assisted growth of GaAs nanowires on silicon, comparison of surface SiOx of different nature

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ABSTRACT

Physical properties of surfaces are extremely important for initiation and nucleation of crystal growth, including nanowires. In recent years, fluctuations in surface characteristics have often been related to unreproducible growth of GaAs nanowires on Si by the Ga-assisted method. We report on a systematic study of the occurrence of GaAs nanowire growth on silicon by the Ga-assisted method for different kinds of silicon oxides: native, thermal and hydrogen silsesquioxane (HSQ). We find that success in achieving nanowires and the growth conditions such as gallium rate and substrate temperature depend mainly on the physical properties of the surface: oxide stoichiometry, oxide thickness and surface roughness. These results constitute a step further towards the integration of GaAs technology on the Si platform.

1. Introduction

Semiconducting nanowires provide a wide range of possibilities both in applied and fundamental science [1–3]. Within the range of possible applications III–V semiconductors are among the most promising materials. The small footprint of nanowires allows for virtually defect-free integration of mismatched materials, which would not be possible in the thin film form [4,5]. Moreover, III–V nanowires can be obtained on Si [6–11], providing a path for combining the III–V and Si platforms. As nanowires start growing generally in a single nucleation event followed by a layer-by-layer mode, III–V nanowires grown on silicon appear also free from anti-phase boundaries otherwise often found in thin film counterparts [12–14]. Still, the lack of polarity of the silicon substrate leads to non-perpendicular growth nanowires grown on Si(111) due to the existence of three-dimensional twinning under certain growth conditions [13,15].

One of the most successful ways of growing nanowires is the vapor–liquid–solid method (VLS) in which a liquid droplet (denominated as catalyst) is used for the gathering and preferential decomposition of growth precursors [16,17]. Upon supersaturation of the droplet, precipitation occurs at the interface with the substrate in the form of a nanowire. One of the most successful catalysts used for VLS is gold. However, when heating a Si substrate with gold on top, the gold droplets incorporate a significant amount of silicon by the formation of an eutectic alloy. The presence of Si in the Au interferes with the decomposition and precipitation of precursors. As a consequence, growth of III–V nanowires on Si using gold as a catalyst is quite more challenging than on III–Vs. Many groups working on the growth of III–V nanowires on silicon have looked for alternative methods, including the selective area epitaxy and Ga-assisted growth of GaAs nanowires [6–8,13,18–21]. In the latter, it was found that the presence of an oxide at the surface was necessary for the formation of the liquid droplet necessary for VLS.

The physical characteristics of the silicon oxide have always been an important parameter in Ga-assisted nanowire growth [9–11]. It was observed that the oxide thickness plays a role in achieving nanowires with an epitaxial relation to the substrate [22]. Interestingly, the critical thicknesses reported by the various groups are significantly different depending on the preparation method of the oxide: 5 nm for Hydrogen Silsesquioxane (HSQ), 0.9–2 nm for thermal oxide and 30 nm for sputtered oxide [22,23]. In these works, the existence of a critical oxide thickness on a GaAs substrate was discussed in terms of the opening of craters in the oxide, either by the reaction of Ga with the substoichiometric oxide and/or due to the desorption of As at GaAs surface temperatures above 500 °C. Few works report on successful growth without the presence of an oxide on the silicon surface [24,7,10]. One should note that in all of these cases, there was a non-negligible time lapse between substrate preparation and loading in the ultra-high-vacuum environment. It is well established that

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Si surfaces naturally undergo oxidation even at room temperature, simply by exposing them to air. The same oxidation process takes place also in the case of hydrogen passivated surfaces [25–27]. As a consequence, what was claimed as oxide-free surface had most probably oxidized to Si +1 (i.e. Si–O–Si) as shown from X-Ray photoelectron spectroscopy data of refs [10,28].

Most of the works discussing the role of the oxide in the growth of GaAs nanowires by the Ga-assisted method were performed on GaAs substrates [22,7,9–11]. To the best of our knowledge, there are no reports on the role of oxide in Ga-assisted growth of GaAs nanowires on silicon. Different groups have used different types of surface preparation, but no systematic comparison between different types of oxide has been realized. Additionally, it is generally accepted that growth conditions for obtaining GaAs nanowires can strongly depend on the wafer batches and providers used, despite identical nominal properties. There is a clear need for finding out the physical origin of this in order to deduce a reproducible preparation method of the silicon surface. In this work, we address the following unanswered questions on the Ga-assisted growth of GaAs nanowires on silicon: is the presence of an oxide needed? What is the ideal oxide stoichiometry for reproducible growth? What is the ideal critical oxide thickness? Is it possible to relate the physical characteristics of the surface with the ideal growth conditions? For this, we analyze the physical characteristics of different types of oxides and relate them to the optimized GaAs nanowires growth conditions. This work constitutes a step towards systematic use of silicon as a substrate for Ga-assisted growth of GaAs nanowires and could be potentially extended to other materials systems.

2. Experimental details

GaAs nanowires have been grown by Ga-assisted self-catalyzed method on Si(111) 2-inch wafers RCA treated (ended with an HF etch) from different providers (Virginia and Siltronix, p-doped Boron, 10–20 Ω cm) from now on named Batch A and B respectively. The growth was performed in a Molecular Beam Epitaxy machine (MBE) with solid state sources (DCA P600). Previous to growth and in order to ensure a clean surface, all substrates were annealed at 500 °C in a separate UHV chamber for 2 h; from now on we will refer to this process as degassing. The effect of this step on oxide chemistry, thickness and roughness is reported in the Supplementary Information. All the values of roughness, thickness and chemistry characterization reported in the manuscript have been performed after degassing, unless differently specified. After this step, the samples were moved to the growth chamber, always in UHV.

The silicon substrates were prepared with different types of oxides: thermal, native and Hydrogen Silsesquioxane (HSQ). Thermal oxide was produced by means of dry oxidation of the wafer of batch B in a Centrotherm furnace at 950 °C in a cleanroom environment. The native oxide was obtained by natural exposure of the Si wafers (of batch A and B) to air in cleanroom environment (21 ± 0.5 °C, humidity 44%). HSQ oxide was obtained by spinning a HSQ:MIBK solution (XR-1541-002, Dow Corning) on wafers of batch B at 6000 rpm with subsequent annealing for 5 min at 180 °C for removal of the solvent. Without diluting the solution, the oxide thickness achieved was of 28–30 nm. By diluting it (1:4–1:8), thinner oxides were obtained (8–4 nm). The films were transformed into silicon oxide by annealing them at 475 °C in N_2 atmosphere for 1 h. The solutions were spun right after exposing the Si wafers to an HF solution, in order to avoid the presence of the native oxide. The oxide thickness was controllably reduced by chemical etching with a NH_4F:HF (500:1) solution. The etching rate was calibrated independently for every type of oxide used. The oxide thickness was measured with spectroscopic ellipsometry (Sopra GES 5E) and confirmed by Atomic Force Microscopy (AFM) on etched steps. Each thickness value obtained by ellipsometry is the result of the average of five measurements in different points on the wafer. Attenuated total reflection (ATR) IR spectroscopy (Jasco FT/IR 6300 with Pike MIRacle holder with single reflection diamond crystal) was realized for the characterization of the oxide stoichiometry, by scanning in the 650–4000 cm^{-1} range with 100 accumulations. Although, since the intensity of the signal-to-noise ratio above 1500 cm^{-1} is extremely low, only the low range (650–1500 cm^{-1}) is considered and reported. Each ATR-FTIR measurement was repeated 3 times on each sample in different points. Finally, AFM (Bruker) was also used for the determination of the surface roughness: each surface roughness value is the result of the average of three measurements of 5×5 μm, 1×1 μm and 500×500 nm areas. It is important to remark that the reported values of roughness have been measured after the degassing. The roughness before degassing are reported in the Supplementary Information. In the case of completely etched oxides, the substrates were immersed in an isopropanol bath immediately after etching, and then dried under Nitrogen flow just before loading in the UHV environment. We used the following range of growth conditions:

- the substrate temperature between 580 °C and 660 °C, as measured by means of a calibrated pyrometer;
- Ga rates between 0.25 A/s and 1.25 A/s, as calibrated on planar growth on GaAs (111) by means of Reflection High Energy Electron Diffraction (RHEED);
- As_4 fluxes were from 2.5×10^{-6} torr to 4.9×10^{-6} torr; as calibrated by means of a beam flux monitor gauge.

Scanning Electron Microscopy (SEM) (Zeiss Merlin) was used for the morphological characterization of the samples.

3. Experimental results

3.1. Chemical composition of the oxides

We start by presenting the nature of the various oxides used in this work. Thermal oxide is a mostly stoichiometric oxide (SiO_2), which can be produced by oxidation of Silicon at 800–1200 °C under a controlled oxygen flux; it exhibits low as-grown roughness ($\sim > 0.6$ nm) [34].

Native oxide is a thin layer of oxide formed by the natural exposure of a Si wafer to air; it follows the surface roughness of the underlying silicon substrate and it grows monolayer by monolayer [25,35,27]. The chemical composition of native oxide depends on its thickness. For thicknesses of few monolayers, it mainly consists of Si–O–Si [36]. The oxygen content increases for larger thicknesses, though it remains sub-stoichiometric with respect to thermal oxide.

HSQ oxide is obtained by annealing a Hydrogen Silsesquioxane resin on a silicon wafer previously etched with HF. The thickness can be tuned by the dilution of the resin solution and the spinning rate [37,38]. Annealing the HSQ resin at 450 °C transforms the cage structure of HSQ monomer into a network, whose chemical composition is SiO_x with $1 < x < 2$, depending on the annealing temperature [37,38].

By investigating these three types of oxides, we can understand the influence of the stoichiometry in the nucleation and growth mechanism of GaAs nanowires. The stoichiometry of silicon oxide can be characterized with Fourier Transform Infrared Spectroscopy (FTIR). The main absorption bands characteristic of silicon oxide are the interstitial oxygen band (Si–O–Si), centered at 1107 cm^{-1},

[29,31,32] the transverse optical phonon (TO) of SiO_2 around 1075 cm^{-1} [33], as well as the longitudinal optical phonon (LO) around 1250 cm^{-1} [33], as reported in Table 1. Suboxides of the form SiO_x with $1 \le x < 2$ are characterized by an absorption band downshifted and broadened with respect to the TO SiO_2. The shift can be directly related to the stoichiometry [33]. Examples of ATR-FTIR spectra obtained from the different oxides are shown in Fig. 1.

In Fig. 1 the Si–O–Si absorption band is observed for all the oxides (thermal, native and HSQ), albeit with different intensities. The spectra at higher wavenumbers depend on the oxide type:

- Thermal oxide shows a clear LO–SiO_2 positioned at 1250 cm^{-1}, indicating it being stoichiometric oxide.
- HSQ oxide shows an absorption band (1226 cm^{-1}), indicating that it is substoichiometric oxide SiO_x with $(1 \le x < 2)$ [33].
- Native oxide does not show any additional absorption band than the already described Si-O-Si related, consistently with reported results on films of similar thickness [29].

Table 1
Characteristic phononic modes of silicon oxide.

Phononic mode	Position (cm^{-1})	Ref.
Si–O–Si	1107	[29–32]
TO SiO_2	1075	[33]
LO SiO_2	1250	[33]

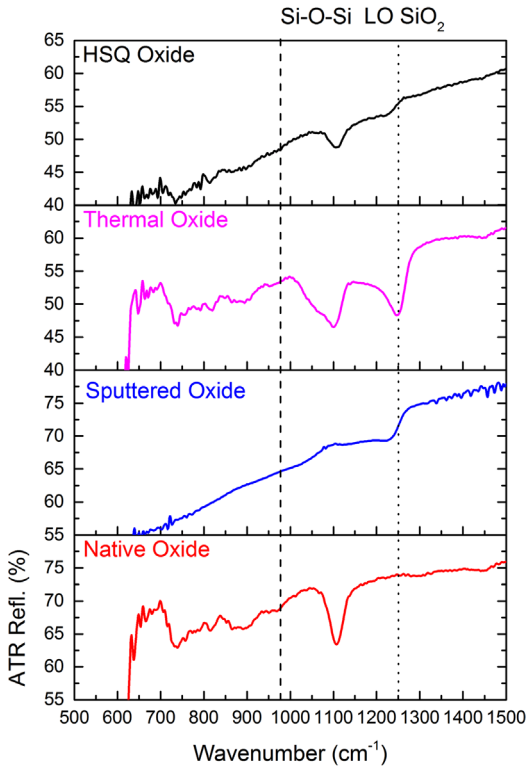

Fig. 1. ATR FTIR spectroscopy of different oxides. The peak at 1250 cm^{-1} corresponds to the LO mode of SiO_2, whereas the peak at 1107 cm^{-1} is related to the presence of interstitial oxide Si–O–Si. The TO mode of SiO_2 is located around 1075 cm^{-1}. Thermal oxide is the only oxide that shows TO and LO modes of SiO_2. HSQ presents a downshifted broad peak around 1225 cm^{-1} correspondent to non-stoichiometric oxide SiO_x with $x < 2$. All the oxides show the interstitial oxide peak (1107 cm^{-1}) but not the sputtered oxide on GaAs; this proves that Si–O–Si is peculiar of Si/SiO_2-interface. A similar result was obtained with HSQ oxide on GaAs substrate (see Supplementary Information).

In order to demonstrate that the interstitial oxide is characteristic only of the interface between the silicon and the silicon oxide, the spectra of sputtered oxide on GaAs is also shown (see Fig. 1); the same result has been achieved with HSQ on GaAs (see Supplementary Information). No absorption band is observed at 1107 cm^{-1}, showing that no interstitial oxide is present. On the other hand a broad absorption is observed around 1226 cm^{-1}, characteristic of sub-stoichiometric oxide. As a remark, interstitial oxide is present in every type of oxides on silicon since it represent the initial step of oxidation of every silicon surface, being followed by oxide of different composition, depending on the processing [27]. In the following, FTIR spectrum of Si substrate is used as a tool to investigate the physical properties that influence the early stages of growth of self-catalyzed GaAs nanowires.

3.2. Thermal oxide

We first present our results on thermally oxidized silicon substrates. As introduced earlier in this manuscript, three physical properties of the substrates will be considered: thickness, roughness and chemical composition. First we investigate substrates with four different thicknesses of the same oxide, by a combination of optical lithography and etching (see supplementary information). This allowed us to investigate simultaneously several oxide thicknesses under identical experimental conditions.

Fig. 2 shows SEM micrographs of oxidized substrates with varying oxide thicknesses after performing the same growth process. The growth conditions were substrate temperature $T = 600$ °C, Gallium rate Ga = 1.25 A/s and Arsenic beam flux pressure As = 2.5×10^{-6} torr. Under these conditions nanowire growth was observed only for an oxide thickness between 1 and 2 nm (Fig. 2(c)). Similar thickness selectivity results were obtained under other conditions ($T = 590$–630 °C, Gallium rate 0.5–1.25 A/s) leading to nanowire growth. In the case of thicker oxides, Ga droplets were always observed on the surface (see Fig. 2(a) and (b)). Oppositely, for oxide-free silicon surfaces, textured two-dimensional growth was found (see Fig. 2(d)). Such a change in growth mechanism could be related to the difference in surface energy of the SiO_2 compared to the bare Si and thereby influence the initial Ga droplet formation and pinning on the surface. The question here is what makes 1–2 nm thermal oxide so prone for Ga-assisted nanowire growth. In order to shed some light to this question, we show the ATR-FTIR spectra of the thermal oxide of different thickness (see Fig. 2 (e)), with comparable pre-degassing roughness (~ 0.3 nm). It is interesting to note that the intensity of the LO SiO_2 is proportional to the thickness, while the Si–O–Si mode exhibits the identical amplitude for all. This corroborates the interface nature of Si–O–Si. Moreover, when the oxide thickness is around 1–2 nm, roughness was comparable to thickness (see Table 2), and only the Si–O–Si band is observed. These results are in good agreement with the results obtained by Muller et al. [34]: stoichiometric silicon dioxide is formed only for thicknesses higher than 2 nm.

3.3. Native oxide

From our study on thermal oxide we understand that when roughness is comparable to thickness, nanowire growth can be achieved. In other words, this condition corresponds to the exposure of Si/SiO_2-interface (i.e. Si–O–Si) Based on the thermal oxide results, we also speculate that the substoichiometric composition of the oxide might help in the achievement of nanowire growth. As described in the first section, native oxide appears naturally upon exposing silicon wafers to air. This would supposedly make native oxide a reliable candidate. Still, one observes an extreme variation within batches and providers on the success in nanowire growth, which to date is not understood. In order to

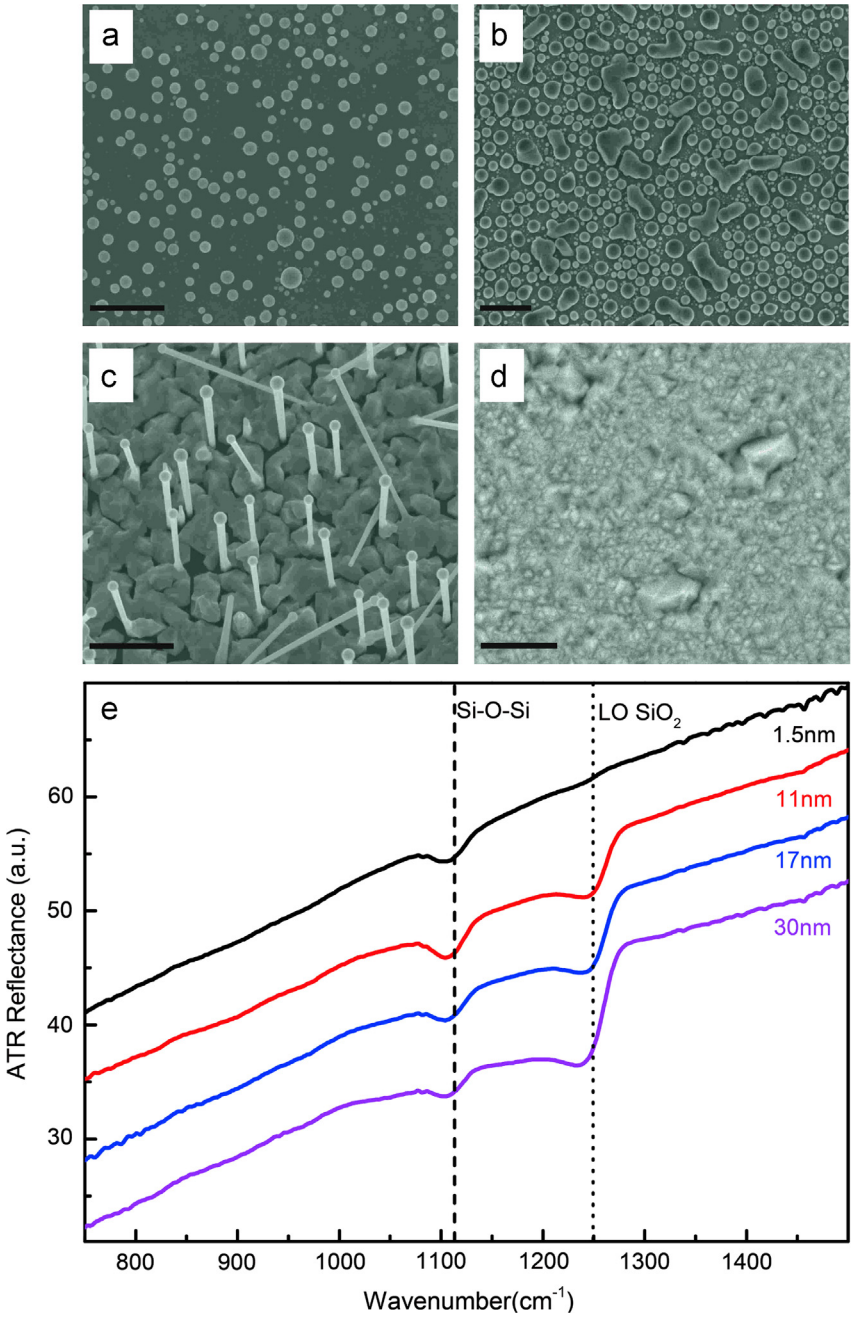

Fig. 2. Growth of GaAs nanowires on Si (111) substrates covered by thermal oxide. The same substrate has been etched with NH_4F:HF (500:1). SEM micrographs of GaAs nanowires growth attempt on (a) 24 nm, (b) 10 nm and (c) 1.5 nm thick thermal oxide. In (d) growth without oxide is reported. Growth has been performed simultaneously for all the different oxide thicknesses. In (e) ATR-FTIR spectra of thermal oxides with different thicknesses and comparable roughness pre-degassing ($\sim$0.3 nm) are reported. By decreasing the oxide thickness the LO–SiO_2 is decreasing in intensity, whereas the Si–O–Si remain unchanged. The scale-bar corresponds to 1 μm.

Table 2
Thickness and roughness of different types of oxides after degassing. The measurements have been performed by ellipsometry.

Oxide type	Annealing (°C)	Thickness (nm)	Roughness RMS (nm)
Native oxide (Batch A)	500	0.8 ± 0.6	0.5 ± 0.5
Native oxide (Batch B)	500	2.1 ± 0.6	5.3 ± 0.5
Thermal oxide	500	1.2 ± 0.6	1.3 ± 0.5
HSQ etched	300	8.8 ± 0.9	3.1 ± 0.5
HSQ as spun	300	8.1 ± 0.6	1.2 ± 0.5

demonstrate that this variability is not a provider issue, we take a closer look at the physical properties of the native oxide of substrates coming from different providers that, despite having identical specifications, gave rise to different growths. One should note that the characteristics may not be specific of a certain company and may vary from batch to batch. As a first observation we find that at comparable roughness pre-degassing (0.3–0.8 nm, see supplementary information) the oxide is slightly thicker in the case of batch B than batch A (see Table 2). Secondly, the ATR-FTIR spectra (Fig. 3 (a)) show that the intensity of the Si–O–Si peak is much higher for Batch B wafers, pointing out a rougher Si/SiO_2-interface. This is in accordance with the post degassing roughness measurements (see Table 2). Finally, we show the SEM micrographs of the growth performed on the two type of substrates (see Fig. 3 (b) and (c)). The two growths were performed under identical conditions (T=610 °C, Ga=0.27 A/s, As=2.5×10^{-6} torr). However, while a forest of nanowires is obtained on batch B wafers

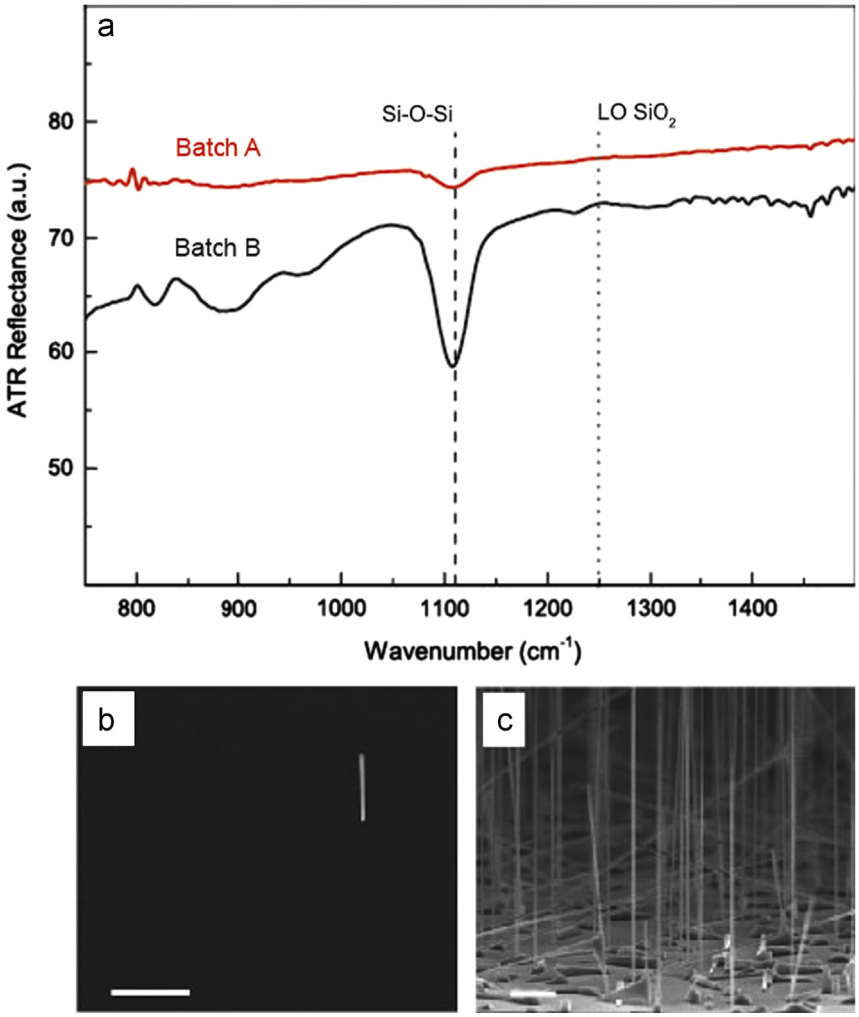

Fig. 3. Native oxide grown on wafers of different providers (batch A and B) with same doping concentration and same surface treatment (see Section 2). In (a) the ATR-FTIR spectra of batch A and B native oxides are shown. Batch B shows stronger absorption band of Si–O–Si compared to batch A, at higher thickness (see Table 2) and comparable roughness (0.3–0.8 nm, see Supplementary Information). Growth has been performed with same process parameters (T=610 °C, Ga=0.27 A/s, As=2.5×10^{-6} torr), and in the case of Batch A extremely low nanowire density ($<10^4$ cm^{-2}) was achieved (b), whereas in the case of batch B higher nanowire density ($\sim1.5\times10^7$ cm^{-2}) was achieved (c). The scale-bar corresponds to 2 μm.

(roughest surface), an extremely low density of nanowires is observed on the batch A (smoothest surface). The different nanowire density can be understood in terms of changes in surface diffusion: a lower roughness results in an augmented surface diffusion, that lead to a lower nanowire density [39]. Vice versa, a rougher substrate (i.e. batch B) leads to a higher nanowire density, as shown in Fig. 3 (c). In a nutshell, the Si/SiO_2-interface seems to be a key parameter in the GaAs nanowire growth on Si. Further studies should involve the intentional modification of this roughness for engineering the nanowire density in a reproducible manner.

3.4. HSQ oxide

So far we have evaluated the growth on SiO_2 and interstitial oxide (Si–O–Si) exposed to the surface. Now we want to evaluate the possibility of growth on an oxide with intermediate composition. For this purpose we used silicon substrates covered with silicon oxide from HSQ processing. Further information about the processing of HSQ can be found in the Supplementary Information. Analogously to the thermal oxide investigation, several growths were performed simultaneously on oxide thicknesses ranging from 2 nm up to 24 nm. Representative SEM images of samples grown under at a substrate temperature of 595 °C, Ga rate of 1.1 A/s and As flux of 2.5×10^{-6} torr are reported in Fig. 4. As the SEM micrographs show, growth of vertical nanowires was only achieved for thin oxide layers ($<5-6$ nm). This value is higher than in the case of thermal oxide, and comparable to what has been reported for HSQ on GaAs substrates [40]. Similar to what was observed for thermal oxide, the Si–O–Si band is the most dominant feature in the FTIR spectra of HSQ oxide of around the critical thickness and below. We note that the IR spectrum of 4 nm thick HSQ presents a non-negligible SiO_x-related absorption band.

For this reason we performed the following experiment; we prepared two substrates with the same HSQ oxide thickness, achieved by

- Spinning HSQ from a MIBK diluted solution (1:8) to form directly a film with a thickness of 4–5 nm. This type of sample will be called “as spun”.
- Spinning HSQ from non-diluted solution, and etched it down to a similar thickness. In the following, this type of sample will be called “etched”.

The IR spectra are virtually identical (see Fig. 5 (a)), indicating the same composition of Si–O–Si and SiO_x. Interestingly, successful

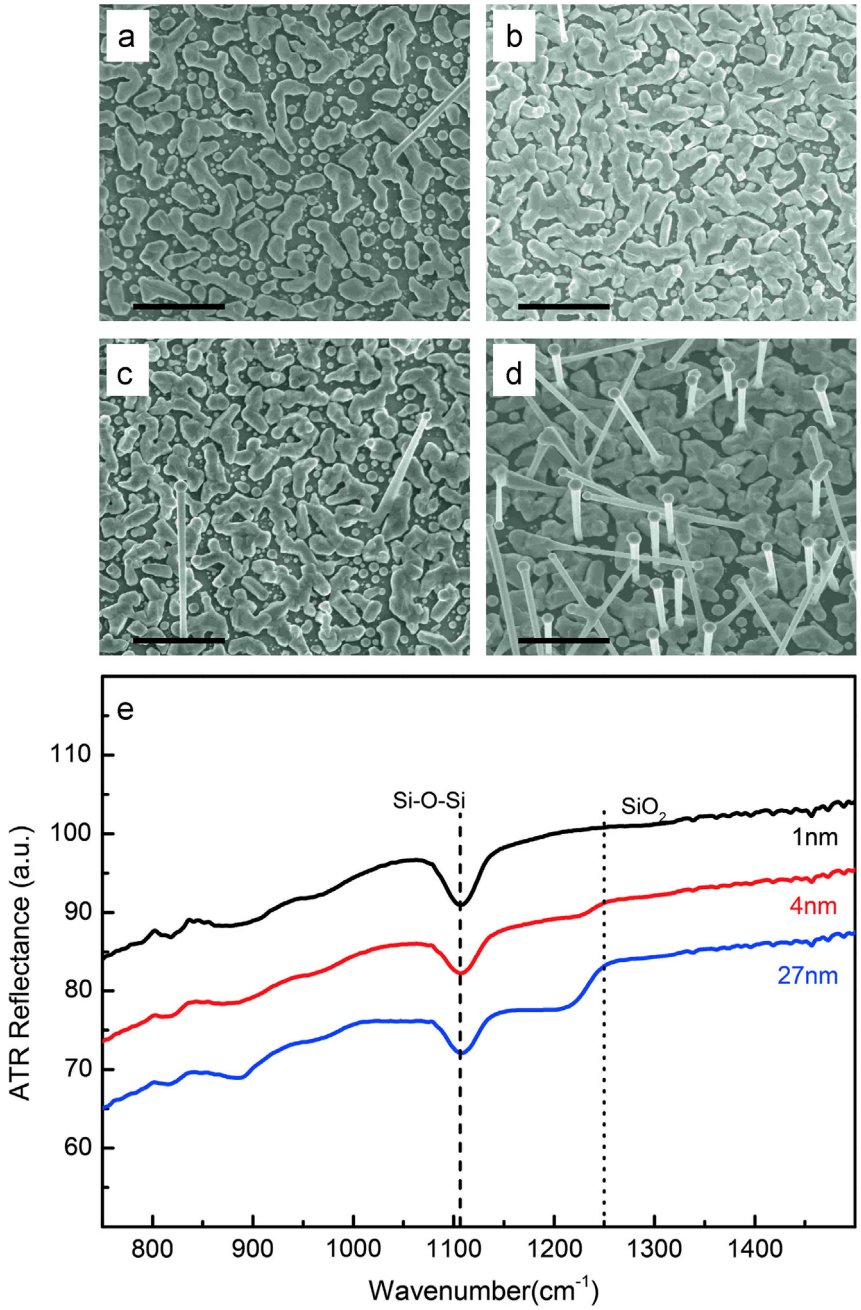

Fig. 4. Growth of GaAs nanowires on Si (111) substrates covered with HSQ oxide. Thickness was controlled by etching down the oxide with NH_4F:HF diluted 500:1. In (a)-(b)-(c) and (d) the SEM micrographs show the growth attempts on respectively 19-15-8 and 5 nm oxide thicknesses. Only in the latter case growth was performed successfully; the growth conditions were substrate temperature 595 °C, Ga rate of 1.1 A/s and As flux of 2.5×10^{-6} torr. (e) ATR-FTIR spectra of HSQ oxides with different thicknesses: the absorption band of SiO_x decreases in intensity by decreasing oxide thickness. On the other hand the absorption band of Si–O–Si does not decrease in intensity, showing that it is related to the Si/SiO_2-interface. The scale-bar corresponds to 2 μm.

growth had been achieved only in the case of etched HSQ (see Fig. 5). Even though the substrates seemed to be identical, the AFM analysis revealed a difference in surface roughness (see Table 2). In the case of low roughness (as spun) only Ga droplets were obtained, whereas for roughness of the order of the oxide thickness (etched), vertical nanowires were observed. We believe that, as schematically depicted in inset of Fig. 5, the Ga droplet cannot reach the Si/SiO_2-interface and no growth is observed in the case of a smooth and compact oxide layer. On the other hand, for large surface roughness (i.e. comparable to thickness), the Si/SiO_2-interface can be exposed to the precursors, allowing vertical nanowire growth.

4. Discussion

We discuss now the results in views of generalizing our findings for nanowire growth. We first review the impact of stoichiometry and roughness of the oxide on nanowire growth. We have varied the composition of the silicon oxide SiO_x with x ranging from 0 to 2. For simplicity's sake, we start considering growth on the two extreme cases: stoichiometric SiO_2 ($x=2$), namely thermal oxide thicker than 2 nm, and oxide-free silicon ($x=0$), see for example Fig. 2. In both cases it was not possible to obtain GaAs nanowire growth in any of the conditions used. Instead, we observe a droplet-like deposit on the SiO_2, while a

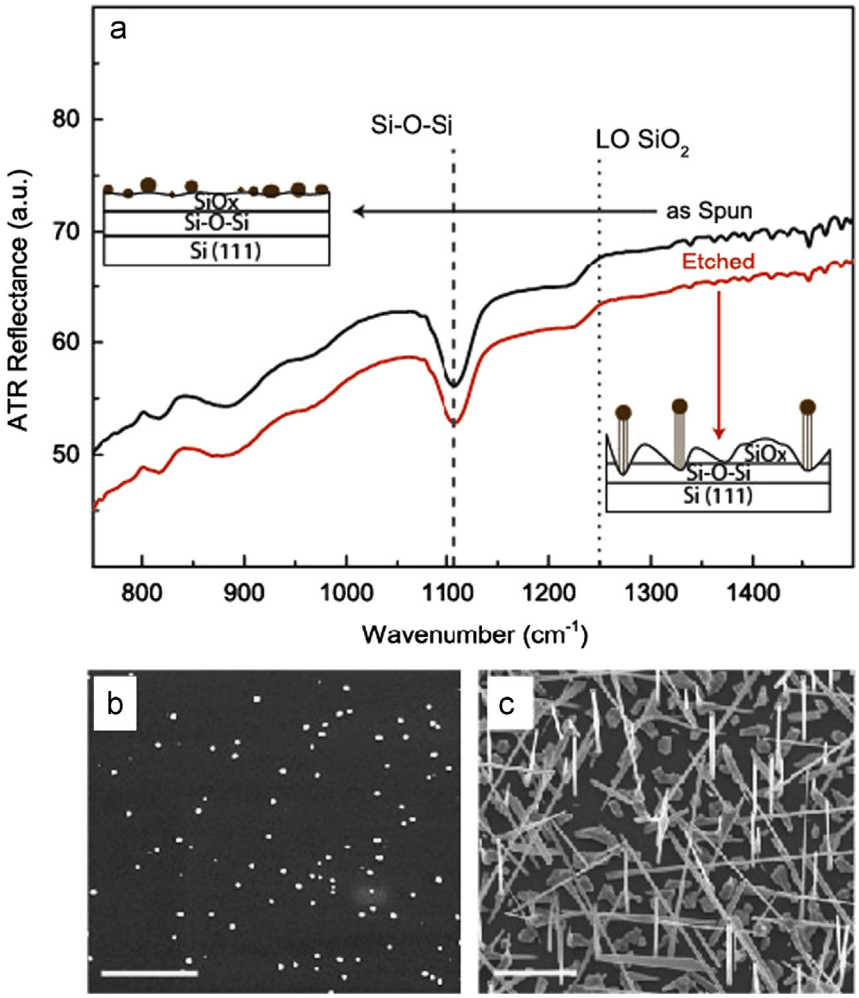

Fig. 5. (a) ATR-FTIR spectra of HSQ oxides with identical thickness but different preparation method: the as spun was prepared by direct dilution, whereas the etched was prepared by a more concentrated solution and then etched down. In (b) and (c) the SEM micrographs report the growth attempts on respectively the as spun and etched HSQ. Nanowires growth was successful only in the case of the etched HSQ. The insets in (a) show the proposed mechanisms for etched and as spun HSQ: the latter present a lower roughness compared to the etched HSQ (see Table 2), that did not allow Si/SiO_2-interface exposure to the surface, leading to no nanowire growth. Differently, successful growth was achieved for the etched HSQ since the roughness allowed Si/SiO_2-interface exposure to the surface (see Table 2). The scale-bar corresponds to 2 μm.

polycrystalline growth is observed in the oxide-free surface. The droplet-like deposit suggests that the diffusion coefficient of Ga-adatoms on the oxide is higher than on the silicon surface. It is interesting to note that in the case of growth on Si substrates covered with oxide thickness comparable to roughness, nanowires were always obtained. This condition suggests a nucleation model based on the formation of a pin-hole that provides the epitaxial relation with the substrate, coherently with what reported from other researchers [41,22]. The conditions of roughness comparable to thickness that allow the pin-hole formation, necessary to achieve nanowire growth can be obtained in various manners: thermal oxide thinner than 2 nm, HSQ etched thinner than 4–5 nm and native oxide. A clear proof of the importance of roughness vs thickness is shown in Fig. 5 (b) and (c), where two substrates were prepared with HSQ with identical thickness and composition, but different roughness. We have also seen that the roughness/thickness conditions that lead to successful growth seems to be correlated to Si/SiO_2-interface (i.e. Si–O–Si), as shown in Fig. 6. The recurrent observation of such an interface layer has been described in other works, where though successful growth of GaAs nanowires on patterned silicon dioxide is not related to the presence of interstitial oxide at the SiO_2 hole opening [42–44]. However the role of Si/SiO_2-interface in the growth mechanism is still not fully understood and requires further investigation.

In parallel, we explored growth on smooth surfaces (batch A substrates) to understand if nanowire density could be controlled by the "processing parameters", as Ga rate or substrate temperature. We varied both Ga rate and substrate temperature respectively from 0.3 A/s to 1.1 A/s, and from 600 °C to 660 °C, as shown in Fig. 6. At low Ga flux and substrate temperatures ((a) and (b)) extremely low density of vertical nanowires is observed, as already reported in Fig. 3. On the other hand the higher the Ga flux ((c)-(e)-(g)), the more material is deposited on the surface, resulting in an increased nanowire density and polycrystalline parasitic islands density. By increasing temperature, the polycrystalline parasitic layer decreases ((g)-(h)-(i)). Coherently with what mentioned before, the diffusion length of Ga atoms augment with increasing temperature, decreasing the polycrystalline islands density.

In order to generalize these results, we have correlated the surface characteristics with the conditions needed to achieve growth with comparable density number of vertical nanowires ($(1.5 \pm 0.5) \times 10^7$ cm^{-2}). Fig. 7 depicts the general conditions for obtaining comparable nanowire density as a function of surface roughness and Si–O–Si content. In general, a lower surface roughness requires higher substrate temperature and Ga rate to achieve

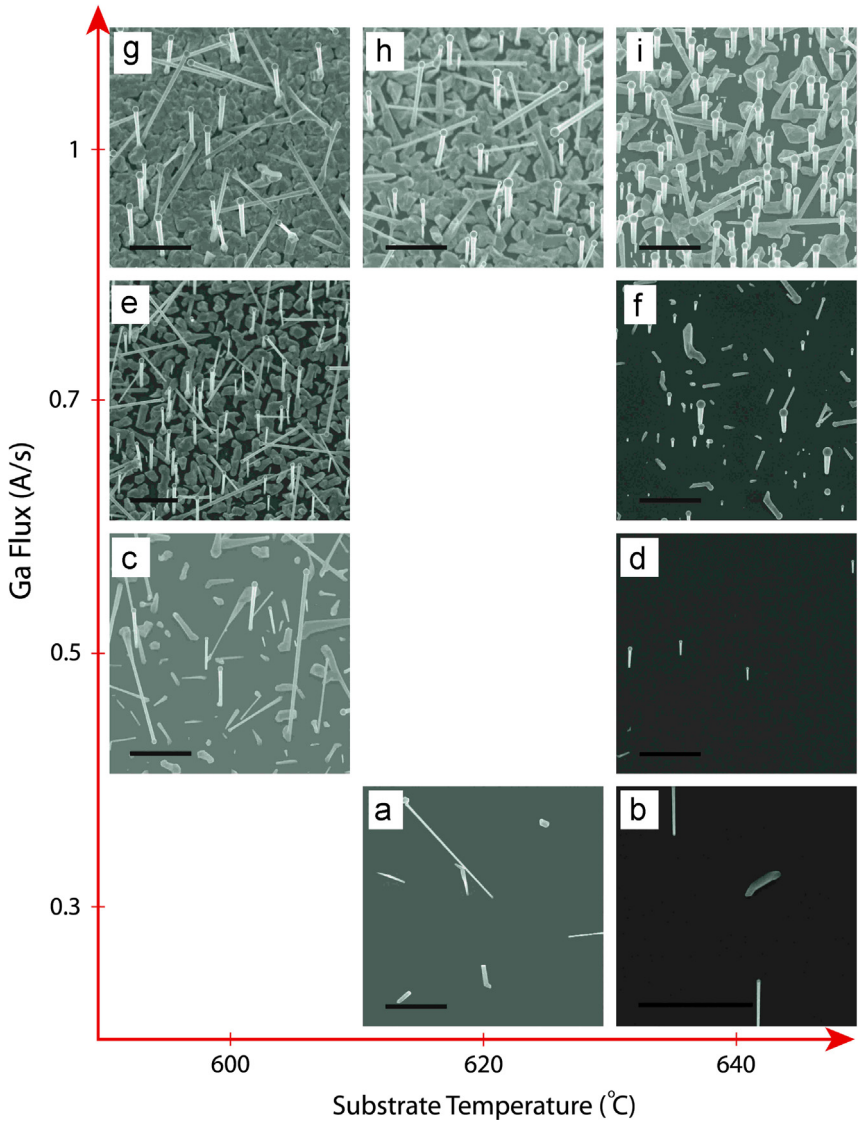

Fig. 6. SEM micrographs of GaAs nanowires grown on batch A wafers covered with native oxide. The as flux used in all the growths shown is constant at 2.5×10^{-6} torr. By moving from bottom to top Ga rate increases, whereas from left to right the substrate temperature increases. At low Ga rate and substrate temperatures (a) and (b) low material deposition is observed. On the other hand the higher the Ga rate (c)-(e)-(g), the more material is deposited on the surface, increasing at the same time nanowire density and polycrystalline island density. If also temperature is increased, the density of vertical nanowire strongly increases (g)-(h)-(i), decreasing polycrystalline island density. Growth at temperature above 640 °C was also attempted, but no growth was observed anymore. The scale-bar corresponds to 2 μm.

comparable nanowire density. As an example, in the case of batch A Si wafers (smoothest surface), the conditions to achieve the desired nanowire density were of Ga=0.75 A/s and T_{sub}=640 °C.

Thermal oxide presented the second lowest surface roughness: the desired nanowire density was achieved with Ga=0.75 A/s and T_{sub}=625 °C. The trend is followed by HSQ for which the conditions for the desired nanowire density were Ga=0.45 A/s and T_{sub}=610 °C. In the case of the highest surface roughness, a comparable nanowire density was achieved at Ga=0.27 A/s and T_{sub}=610,°C.

We explain the change in Ga rate conditions for creating comparable nanowire density with surface diffusion: a decrease in roughness produce an increase in surface diffusion, forming less nanowires [39]. Therefore, to increase nanowire density for lower roughness substrates (i.e. native oxide batch A) Ga rate and substrate temperature have to be increased compared to rougher substrate (i.e. native oxide batch B).

As shown in Fig. 7, roughness and interstitial oxide content are directly correlated, suggesting that the sharpness of the Si/SiO_2-interface affects the characteristic roughness for the bottom up oxides (i.e. thermal oxide and native oxide). Presently, how to achieve control over interstitial oxide formation remains still open and it needs further investigation.

5. Conclusions

In conclusion, we have shown that roughness is a key parameter for forming pinholes necessary for successful GaAs nanowire growth. This explains the different optimal oxide thicknesses to achieve growth reported in literature: the critical oxide thickness depends on the surface roughness as it is related to the thickness leaving Si/SiO_2-interface exposed to the surface. For example, we found a critical thickness of 1–2 nm for thermal and native oxide, 5–6 nm for oxide from HSQ. The lower the roughness, the higher the temperature and the Ga rate needed for achieving the comparable nanowire density, and vice versa. Additionally, we have also shown that the "provider dependence"

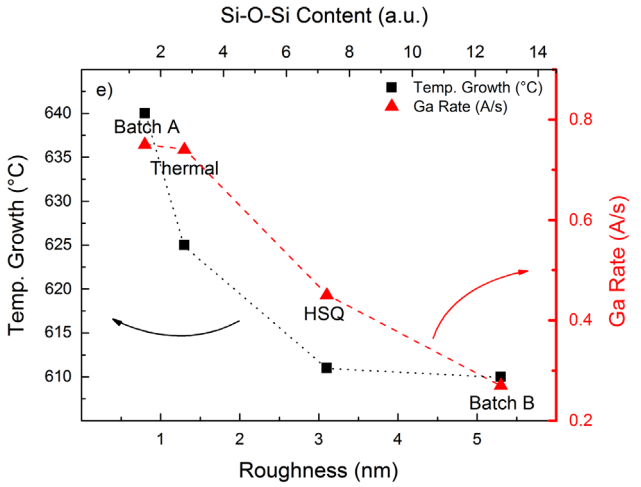

Fig. 7. The relation between optimal growth conditions (substrate temperature and Ga rate) at comparable density number of vertical nanowires ($(1.5 \pm 0.5) \times 10^5$ cm^{-2}) with surface roughness and interstitial oxide content is shown. The higher the Si–O–Si content, the rougher the Si/SiO_2-interface. To achieve comparable nanowire density lower roughness lead to higher substrate temperature and Ga rate, and vice versa.

on growth conditions has physical reason, and it is related to the interface roughness of the substrates, that seems to be correlated to Si/SiO_2-interface. Still, to clarify the latter point further investigation is needed. Systematic AFM and FTIR on the received substrates might help in determining the conditions to achieve the desired nanowire density. This work opens new perspectives for the reproducible integration of GaAs nanowires on silicon.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.jcrysgro.2014.07.034.

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