Novel Configurable Logic Block Architecture Exploiting Controllable-Polarity Transistors

Pierre-Emmanuel Gaillardon, Xifan Tang, Giovanni De Micheli
EPFL, Lausanne, Switzerland
pierre-emmanuel.gaillardon@epfl.ch

Abstract—**Controllable-polarity transistors exhibit a device-level configurability. Indeed, they can be dynamically configured between *n*-type and *p*-type. Such property can be exploited in *Field Programmable Gate Arrays* (FPGAs) to replace traditional *Look-Up Tables* (LUTs) by more powerful configurable units. We report here on a new FPGA logic block architecture, called *MCluster*, that takes a direct advantage of configurable transistors. The performance of the approach is evaluated and compared to its traditional *Complementary Metal-Oxide-Semiconductor* (CMOS) counterpart at 22-nm technology node. We note an average saving of 64% in area×delay×power product.**

Keywords—Controllable-polarity transistors; ultra-fine grain logic; Reconfigurable logic

I. Introduction

In modern semiconductor technologies, Schottky contacts are often used to reduce the access resistances at the source and drain interfaces of *Metal-Oxide-Semiconductor Field Effect Transistors* (MOSFETs). However, Schottky barriers can also lead to ambipolarity. The ambipolar phenomenon consists of observing both hole and electron conductions in the same devices and limits the performances of semiconductors. Nevertheless, it is possible to exploit this phenomenon in order to enrich the logic capabilities of the elementary transistors by creating double-independent-gate structures. More precisely, the additional gate electrode can be used to control the device polarity dynamically. While being recently demonstrated using *Silicon Nanowire FETs* (SiNWFETs) [1], such transistor property defines a new class of emerging devices that inherently implement a two-input comparator rather than a simple switch. Controllable-polarity devices can be realized in diverse technologies, such as silicon nanowires [1,2], carbon nanotubes [3], graphene [4] and nanorelays [5].

The intrinsic device configurability enables many innovations from a design perspective, ranging from arithmetic logic [6] down to compact reconfigurable logic [7]. Compact reconfigurable logic cells are appealing to re-think the standard reconfigurable architectures, such as the traditional *Field Programmable Gate Arrays* (FPGAs) architectural scheme.

In this paper, we present a novel logic block architecture that exploits the polarity control at the device level. The logic blocks use ultra-fine grain logic gates grouped in 2×2 matrices in order to realize more efficient combinational logic. The new logic blocks then replace the LUTs in the standard FPGA structure. System-level performance evaluations conclude that such an approach leads to an average saving of 64% in area×delay×power figure-of-merit as compared to its standard counterpart architecture at 22-nm node.

The remainder of the paper is organized as follows. In Section II, we devise on the opportunities brought by controllable-polarity devices to realize compact reconfigurable cells and novel FPGA structures. In Section III, we briefly report on the performances improvements given by the approach. In Section IV, we conclude the paper.

II. Leveraging Device Polarity Control in Reconfigurable Systems

In this section, we discuss the opportunities given by controllable-polarity devices to realize efficient reconfigurable logic blocks.

A. Ultra-Fine Grain Reconfigurable Logic

We first review the behavior of controllable-polarity transistors, then we report on their use in compact logic cell design.

1) Transistors with Controllable Polarity

Controllable-polarity transistors typically control the height of the Schottky barriers formed at the source and drain contacts. This control is enabled by double-independent-gate structures. In such devices, one gate electrode, called the *Control Gate* (CG), acts conventionally by turning *on* and *off* the device. The other electrode, called the *Polarity Gate* (PG), acts on the side regions of the device, in proximity of the *Source/Drain* (S/D) Schottky junctions, and switches the device polarity dynamically between *n*- and *p*-type, as illustrated in Fig. 1. The input and output voltage levels are compatible, resulting in directly-cascadable logic gates [1]. For a complete review on the design opportunities brought by these transistors, we refer the reader to [6].

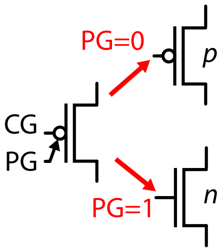
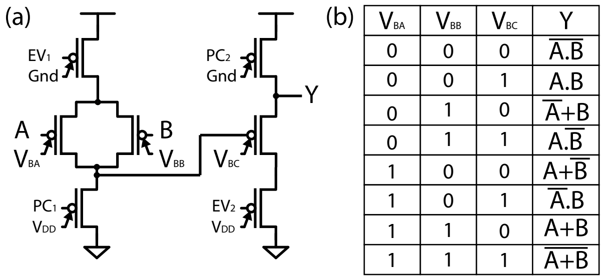


Fig. 1. Transistor with polarity control behavior operating principle.

2) Ultra-Fine Grain Reconfigurable Logic Gates

The property of in-field reconfigurability has been used in [7] to build a compact reconfigurable cell. The cell, reported in Fig. 2-a, can realize any of the 8 Boolean logic functions *Y* of the two inputs *A* and *B*, reported in Fig. 2-b.



V_{BA}	V_{BB}	V_{BC}	Y
0	0	0	$\overline{A.B}$
0	0	1	$A.B$
0	1	0	$\overline{A}+B$
0	1	1	$A.\overline{B}$
1	0	0	$A+\overline{B}$
1	0	1	$\overline{A}.B$
1	1	0	$A+B$
1	1	1	$\overline{A+B}$

Fig. 2. Ultra-Fine grain reconfigurable cell schematic [7] (a) and associated configurations (b).

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The cell is built with only 7 transistors arranged in two dynamic logic stages: logic function and follower/inverter. Signals PC_1, EV_1, PC_2 and EV_2 are respectively the global precharge and evaluation signals of the two stages. The reconfiguration of the cell depends on the signals applied to the polarity gates V_{BA}, V_{BB} and V_{BC}. Each of these signals is biased with either V_{DD} or Gnd. This results in configuring the related transistors to either *n*- or *p*-type, thereby customizing the gate internal circuit. For a detailed description of the circuit operation, we refer the reader to [7].

B. Matrix Cluster Logic Blocks

In this work, we replace the traditional LUTs by ultra-fine grain logic gates. However, a one-to-one replacement would result in a large overhead in terms of programmable connections and would worsen the already significant imbalance between routing and logic resources in FPGAs. Indeed, in conventional FPGA systems, less than 15% of the area is dedicated to the logic computation while the other resources are used for the structure reconfigurability [8]. Therefore, to increase the logic coverage of the structure, we group the logic gates in layered 2×2 matrices. This arrangement is called *Matrix Cluster* (MCluster). For the intra-matrix interconnect, we use a butterfly pattern between the two layers of logic cells. Mclusters perform combinational logic functions and place the original LUTs. Fig. 3 shows the organization of a logic block. Each *Basic Logic Elements* (BLEs) consists of a collection of *N* MCluster-based BLEs.

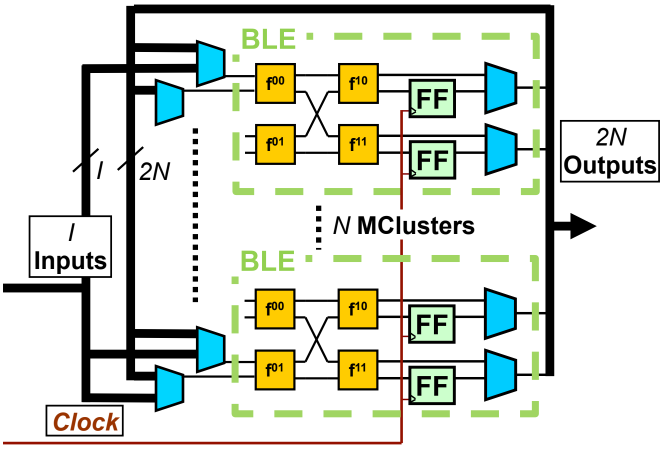

Fig. 3: MCluster-based logic block organization.

III. Experimental Results

The impact of replacing standard LUTs by MCluster-based structures is evaluated through system-level benchmarking of a set of logic circuits taken from MCNC and ISCAS'89. Our reference FPGA architecture corresponds to a fully homogeneous FPGA architecture. The CMOS reference architecture with 4-input non-fractionable LUTs arranged in logic blocks of *N*=10 BLEs and *I*=22 external inputs. This architecture is optimal for homogeneous FPGAs [10]. Our novel structure follows the organization depicted in Fig. 3 with *N*=10 BLEs of 2×2 MClusters. The evaluations are performed using the VTR benchmarking flow [9]. To handle MCluster-based architectures, we use a specific packer, called MPack [12]. The physical parameters of the different architectures are extracted for a 22-nm technological node, while the electrical performances, i.e. delay and power consumption numbers, of the elementary MCluster and LUT are electrically characterized using HSPICE.

The architectural evaluation considers, as metrics, the area, the critical path delay, the dynamic power consumption and the leakage power. These metrics are computed during the place and route iterations of the flow. The area corresponds to the sum of the logic area, i.e., the area of used CLBs, and the routing area, i.e., the area of the used routing resources. The critical path delay corresponds to the most constrained delay through the implemented structures. Finally, the power consumptions include both the contribution of logic blocks and the contribution of routing structures. All the metrics are normalized with respect to the most constrained CMOS design.

Fig. 4 depicts the area×delay×power estimation for MCluster-based FPGA and compares it to its CMOS counterpart. The benchmarks show an improvement of 64% on average. This can be accounted (i) to the performance of a logic-gate-based computation (as compared to the LUT approach) and (ii) to the low area impact of ultra-fine grain logic cells, compared to the rather larger area required by a CMOS LUT. At the same 22-nm technology node, a 2 by 2 cluster is 2× smaller than a 4-input LUT ($2.22\mu m^2$ *vs.* $5.45\ \mu m^2$ respectively) and is able to reach higher functionalities. A 4-input LUT computes a single output signal depending on 4 inputs. While MClusters can only realize a subset of the functions reachable by a LUT, they are capable to produce up to 2 outputs that are functions of the same 4 inputs. Thus, MClusters can potentially output 2× more results for roughly 2× less area. Correlated to the efficiency of the packing tool for matrix clustering, this demonstrates a clear advantage of our proposal as compared to the CMOS approach.

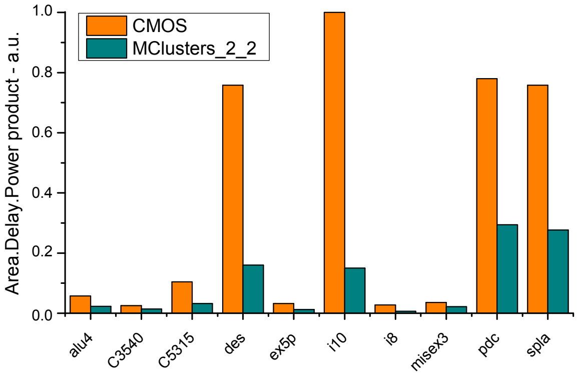

Fig. 4: Area×Delay×Power product comparisons between CMOS-based and MClusters-based FPGAs.

IV. Conclusion

In this paper, we report on a novel FPGA logic block architecture that leverages the additional degree of freedom given by controllable-polarity transistors. In particular, we use controllable-polarity transistors to create compact reconfigurable logic cells. These cells, once arranged in 2×2 clusters, replace the traditional LUTs to perform basic combinational operations. Thanks to the increased logic capabilities of these cells, it is possible to improve the performance of FPGA structures with on average a 64% reduction in area×delay×power product as compared to its standard counterpart at 22-nm technology node.

Acknowledgments

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[12] The *Matrix Packer* (MPack) tool available online at:
https://sites.google.com/site/pegaillardon/downloads