A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current

Jian Zhang, Michele De Marchi, Pierre-Emmanuel Gaillardon, Giovanni De Micheli

Integrated Systems Laboratory, EPFL, Lausanne, Switzerland
Tel: +41 21 6938164, E-mail: jian.zhang@epfl.ch

Abstract

In this paper, we demonstrate a steep *S*ubthreshold *S*lope (SS) silicon FinFET with Schottky-barrier source/drain. The device shows a minimal SS of 3.4 mV/dec and an average SS of 6.0 mV/dec over 5 decades of current swing. Ultra-low leakage floor of 0.06 pA/μm is also achieved with high I_{on}/I_{off} ratio of 10^7.

Introduction

In low-power applications, small operation voltages and leakage currents are considered as the main technology means to reduce power consumption. However, the fundamental limitation of SS in conventional MOSFETs (~60 mV/dec at room temperature) becomes the bottleneck for continuously lowering the operation voltages. To break this limit, different types of devices have been proposed based on various mechanisms. *T*unnel *FET*s (TFET) based on band-to-band tunneling demonstrate SS below 30 mV/dec [1]. Nevertheless, the sensitivity of SS to gate voltage leads to a worse average SS over the entire subthreshold region [1-3]. *I*mpact-ionization *MOS* (IMOS) achieves sub-5 mV/dec SS based on avalanche breakdown [4], though requiring high V_{DS} and suffering from reliability issues. Based on an asymmetric structure similar to TFET and IMOS, feedback FET realizes steep SS with large hysteresis due to the charge trapping [5]. Recently, positive feedback based on weak impact ionization was proposed to achieve super-steep SS on UTBOX FDSOI substrate [6]. However, the steep transition only appears for 2 decades of current and rapidly degrades to ~100 mV/dec.

In this paper, we experimentally demonstrate a silicon FinFET with silicided source/drain, exploiting biased *S*chottky *B*arriers (SB). By combining a positive feedback induced by weak impact ionization with a dynamic modulation of the Schottky barriers, the device achieves a minimal subthreshold slope of 3.4 mV/dec and an average subthreshold slope of 6.0 mV/dec over 5 decades of current at room temperature. Ultra-low leakage current of 0.06 pA/μm and high I_{on}/I_{off} ratio of 10^7 are also obtained by effectively modulating the Schottky barriers.

Device Structure and Fabrication

The fin-based device structure is shown in Fig. 1. The *S*chottky-*B*arrier *B*ias (SBB) electrostatically modulates the Schottky barriers at S/D, while the gate controls the potential barrier in the channel to turn the device *on* or *off*.

Fig. 2a shows the fabrication steps of the device. Starting from a lightly *p*-type doped SOI substrate with 340 nm silicon device layer and 2 μm BOX, the channel is patterned into an 800 nm long and 50-70 nm wide fin shape with e-beam lithography (Fig. 2b). A layer of SiO_2 (~15 nm) is formed and followed by a conformal polysilicon deposition. Then, the SBB region is patterned. After a second oxidation (~15 nm) and polysilicon deposition, the gate is self-aligned to the SBB. The achieved gate length is 200 nm. After the gate process, silicon nitride spacers are formed to isolate the structures. A 20-nm nickel layer is deposited by sputtering and a specific annealing process is performed to produce NiSi at the S/D and gate contacts [7]. The device (Fig. 2c) has a channel length of ~600 nm and the final width of the fin is designed to be either 40 nm, 50 nm, or 60 nm. Although currently limited by our academic cleanroom facilities, the device can be scaled down easily thanks to the dopant-free process.

Working Principle

The working principle is shown in Fig. 3. For *n*-type behavior, i.e., when $V_{SBB}>0$, electrons are selected to tunnel through the Schottky barrier into the channel. When V_G is at threshold voltage, a transition occurs in the device. Weak impact ionization generates electron/hole pairs (step 1). The generated electrons drift to the drain, and the holes accumulate in the potential well induced by the gate (step 2). This lowers the barrier, and provides more electrons for impact ionization. Then, more accumulated holes continue to lower the barrier and thus form a positive feedback [6]. In addition to the FinFET structure enhancing carrier multiplication [4], the second important contribution is from the dynamic modulation of the Schottky barrier. Parts of the generated holes are swept towards the source, increasing the hole density in SBB region (step 3). This helps to lower the energy band under SBB. Schottky barrier at source becomes thinner and more electrons tunnel through it. In the meantime, the potential well is kept until the final *on* state. This mechanism improves the I_{on}/I_{off} ratio, and is considered as a key to achieve steep transition for 5 decades of current. The operation of *p*-type is similar but with $V_{SBB}<0$.

Fig. 4 shows the TCAD simulation of the proposed device. Polarity of the device changes by adapting the polarity of V_{SBB}. Steep SS is obtained in both *n*-type and *p*-type (Fig.4a). A sudden change of the surface potential just before and after the *on* state is observed (Fig. 4b). The hole density in the device shows the accumulation of holes after the *on* state as predicted in the proposed mechanism (Fig. 4c).

Results and Discussions

All measurements are carried out at room temperature. Fig. 5 shows the characteristics of the steep SS FinFET. Minimum SS of 3.4 mV/dec is achieved. When decreasing V_{DS} (i.e., the lateral electric field), the impact ionization rate decreases, and the SS gradually degrades to 61 mV/dec at V_{DS}=1V. Compared to counterparts with significant hysteresis [5][8], double sweep confirms the negligible hysteresis in the characteristics of the proposed device. Fig. 5b illustrates the SS as a function of I_D. The average SS of 6.0 mV/dec is observed for 5 decades of current. V_{SBB} controls the tunneling of electrons from SB and thus modulates the SS and I_{on}/I_{off} ratio (Fig. 5c). *n*-type and *p*-type characteristics, obtained by changing the polarity of V_{SBB} in the same device, are demonstrated in Fig. 6. The SS of *p*-type is above 70 mV/dec, possibly due to a lower impact ionization rate of holes. Both *n*-/*p*-types show $>10^6/10^7$ I_{on}/I_{off} ratio. The steep SS in devices with different width of fin (W_{fin}) is shown in Fig. 7a. The SS is independent on W_{fin} within the range of 40-60 nm, while V_{th} increases in devices with a thinner fin. The statistics based on all the measured devices (~50) at lower voltages support this relation (Fig. 7b).

In order to show the effect of the SBB, we fabricated a FinFET with a single SBB region (Fig. 8). In this second device, the channel length and the impact ionization region are the same as in the proposed device. However, there is no potential well for accumulating holes under gate due to the absence of the SBB at source (Fig. 8b). As a result of the weak positive feedback, the SS is slightly below 60 mV/dec for less than 2 decades (Fig. 8d,e). This result verifies the importance of the potential well and the SBB at source. Fig. 9 shows statistical distribution of SS. At operation voltage of 5V, 63% of the measured devices demonstrate SS below 10 mV/dec. When reducing the operation voltage down to 4V, there are still 80% showing SS below 50 mV/dec. As observed in the output characteristics in Fig. 10, weak impact ionization occurs at low V_G and high V_{DS}. When increasing V_G, the lateral electric field decreases and impact ionization vanishes. Compared to IMOS, which is based on strong impact ionization and suffers from reliability problems, the weak impact ionization in the proposed device requires lower V_{DS} and only occurs during the transition. Thus, the device exhibits good reliability as shown in Fig. 11. In the test for hot carrier injection and bias temperature instability, no significant degradation is observed. Moreover, thanks to the FinFET structure, the device exhibits an excellent electrostatic control at low operation voltages (both V_{SBB} and V_{DS}) down to 0.5V (SS <70 mV/dec, and good control of DIBL effect) (Fig. 12). Table I compares the recently reported technologies with sub-60 mV/dec SS and the proposed device. Despite the thicker oxide and longer channel, the proposed device demonstrates ultra-low leakage current, high I_{on}/I_{off} ratio as well as good minimum and average SS at both high and low V_{DS}. Since the impact ionization rate strongly depends on the electric field, the performance at low V_{DS} can be further improved in scaled devices as suggested by the simulation shown in Fig. 4.

Conclusions

We experimentally demonstrated steep SS in a silicon FinFET, exploiting the electrostatic biasing of the S/D Schottky barriers. Minimal SS of 3.4 mV/dec and average SS of 6.0 mV/dec are achieved. Ultra-low leakage floor and high I_{on}/I_{off} ratio (0.06 pA/μm, 10^7 @V_{DS}=5V and ~3 fA/μm, 10^8 @V_{DS}=1V) are suitable for low-power applications.

Acknowledgement

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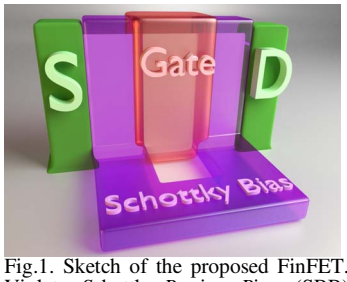

Fig.1. Sketch of the proposed FinFET. Violet: *S*chottky-*B*arrier *B*ias (SBB) region modulating the Schottky barriers. Red: Gate controlling the channel conduction.

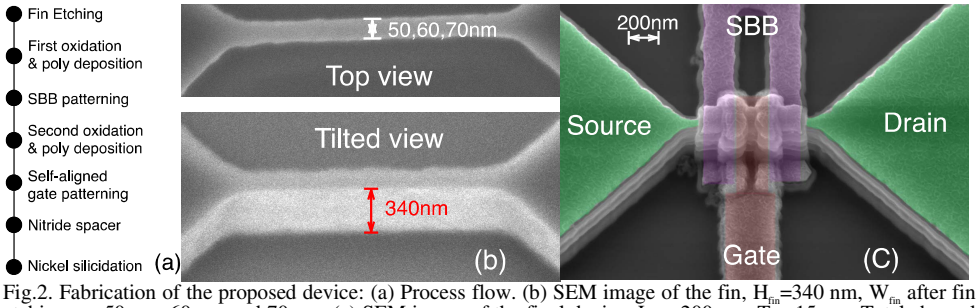

Fig.2. Fabrication of the proposed device: (a) Process flow. (b) SEM image of the fin, H_{fin}=340 nm, W_{fin} after fin etching are 50 nm, 60 nm and 70 nm. (c) SEM image of the final device, L_{gate}=200 nm, T_{ox} ~15 nm. Total channel length ~600 nm, the final W_{fin} are 40 nm, 50 nm and 60 nm considering the silicon consumed during oxidation.

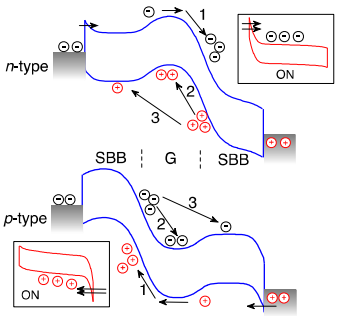

Fig.3. Band diagram of *n*-type (V_{SBB}>0) and *p*-type (V_{SBB}<0). Main switching mechanisms: 1: impact ionization, 2: generated carriers accumulating in the potential well under the gate, 3: carriers accumulating under the SBB region. When completely *on*, impact ionization and potential well vanish (inset diagrams).

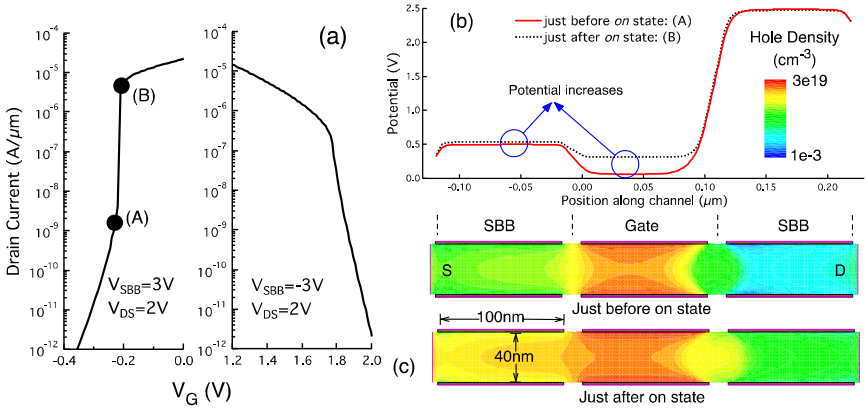

Fig.4. (a) TCAD-predicted device characteristics with L_{gate}=100 nm, T_{ox}=2 nm, W_{fin}=40 nm. Steep transition is observed in both *n*-type (~5 mV/dec) and *p*-type (~35 mV/dec). The device polarity changes by adapting the polarity of V_{SBB}. (b) Surface potential distribution just before and after *on* state (*n*-type). Potential increases under both Gate and SBB. (c) Hole density showing the accumulation of holes under Gate and SBB.

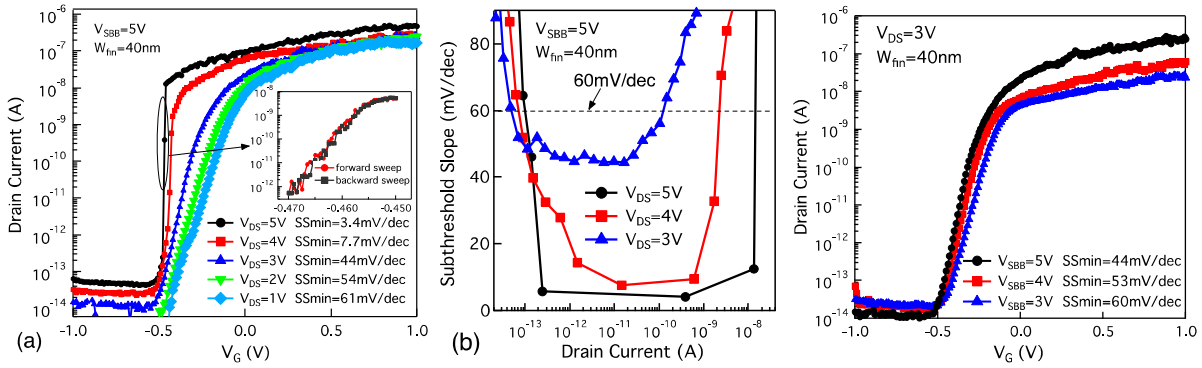

Fig.5. (a) Measured characteristics of the proposed device at different V_{DS} (room temperature). Inset: double sweep showing negligible hysteresis and minimal SS=3.4 mV/dec. GIDL is well suppressed. The applied V_{DS} are much smaller compared to IMOS [4]. (b) SS vs. I_D, showing average SS of 6.0 mV/dec for 5 decades of current. (c) I_D-V_G at different V_{SBB}. Higher V_{SBB} improves both SS and I_{on}/I_{off} ratio thanks to a better control of Schottky barriers.

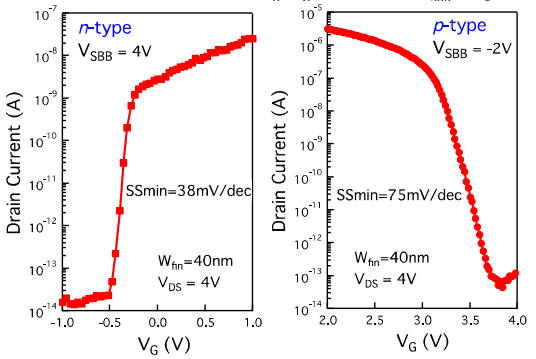

Fig.6. Measured *n*-type and *p*-type characteristics in the same device. The polarity of V_{SBB} determines the device polarity. *n*-type demonstrates 38 mV/dec SS, while the SS of *p*-type is above 70 mV/dec. Both show good I_{on}/I_{off} ratio and maintain good SS for over 5 decades of current.

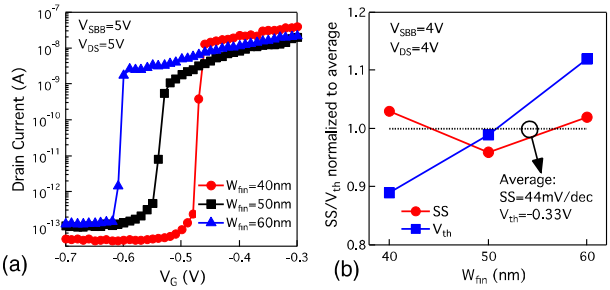

Fig.7. (a) Measured characteristics in devices with different W_{fin}. V_{SBB}=V_{DS}=5V. SS does not significantly depend on W_{fin}, while larger W_{fin} reduces the V_{th}. W_{fin}=40 nm shows better electrostatic control of the SB, thus enhancing I_{on}/I_{off}. (b) Statistics of SS and V_{th} based on all measured devices (~50) at lower voltage (V_{SBB}=V_{DS}=4V), confirming the dependence of V_{th} on W_{fin}. The values are normalized to the average value.

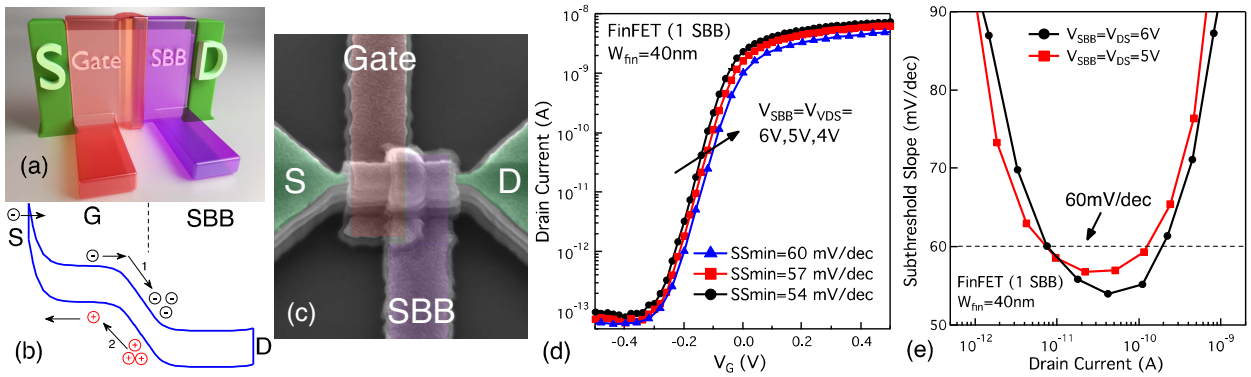

Fig.8. (a) Sketch of the FinFET with a single SBB region controlling the SB at drain to block holes tunneling. Gate controls the SB at source and electrons tunneling, thus turns the device *on* or *off*. (b) Band diagram shows no potential well in the channel, leading to a weak positive feedback. (c) SEM image. (d) Measured characteristics of the device. SSmin is slightly below the thermal limit. (e) SS vs. I_D. SS is below 60 mV/dec for less than 2 decades of current.

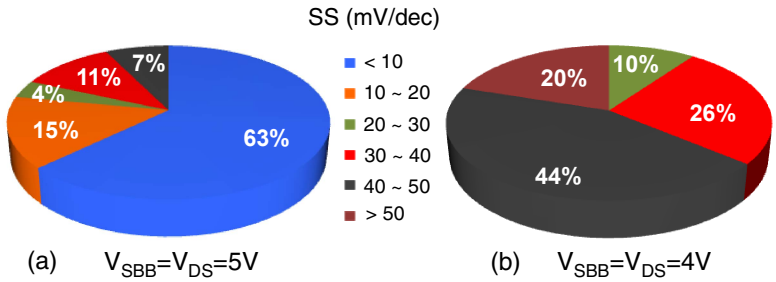

Fig.9. Statistical distribution of subthreshold slope of the proposed device illustrated in Fig. 1. (a) 63% of the measured devices are working with SS<10mV/dec at V_{SBB}=V_{DS}=5V. (b) 80% of the devices show SS below 50mV/dec at V_{SBB}=V_{DS}=4V.

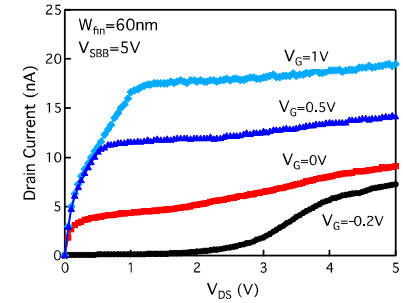

Fig.10. Output characteristics of the proposed device. Impact ionization occurs at low V_G and high V_{DS}, but vanishes when the device is completely *on* (high V_G).

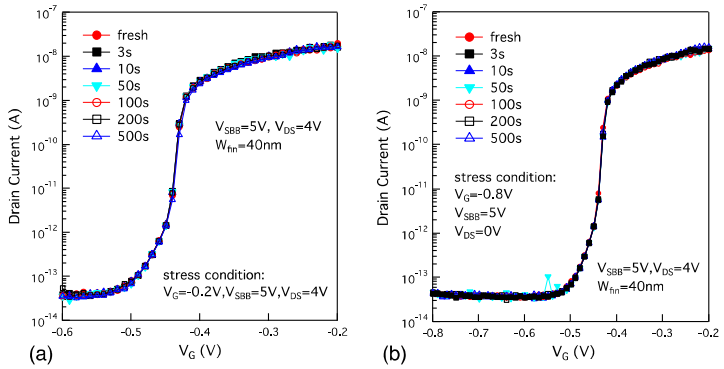

Fig.11. Reliability assessment during fast transition (SS<10 mV/dec): (a) hot carrier injection and (b) bias temperature instability with different stress period. No significant degradation is observed, proving the good reliability of the device.

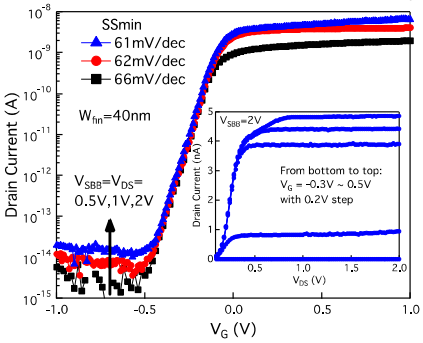

Fig.12. Characteristics under low operation voltages. Near-ideal SS and high I_{on}/I_{off} ratio show the excellent electrostatic control. Inset: Output characteristics show a good control of the DIBL effect.

Table I. Comparison between state-of-the-art technologies with sub-60 mV/dec SS

	[4] IEDM'07	[6] IEDM'10	[2] IEDM'12	[1] IEDM'13	This work	
Principle	Impact ionization	Positive feedback	Band-to-band tunneling	Band-to-band tunneling	Positive feedback + Schottky barrier modulation	
Technology	SiGe Nanowire	UTBOX FDSOI	Pocket + junction modulation in silicon TFET	InGaAs Nanowire/Si Heterojunction	Schottky-barrier silicon FinFET	
Symmetric	No	Yes	No	No	Yes	
EOT (nm)	3	2.5	5	1.91	15	
Channel length (nm)	90	55		150	600	
V_{DS} (V)	5.75	1.3	0.6	1	1	5
I_{on} (μA/μm)*	300	100	0.15	0.006	0.28	0.59
I_{off} (pA/μm)*	10000	1	0.42	0.06	0.003	0.06
I_{on}/I_{off}	10^4	10^8	10^5	10^5	10^8	10^7
SS min	<5	0.058	36	23	61	3.4
SS average (Decades of current)	<10 (4)	~70 (6)	81 (3)	~80 (4)	63 (6)	6.0 (5)

* In this work, the current is normalized to the effective width of the channel, i.e., W_{eff}=W_{fin}+2×H_{fin}.