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A subthreshold current-sensing ΣΔ modulator for low-voltage and low-power sensor interfaces

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SUMMARY

A continuous-time (CT) ΣΔ modulator for sensing and direct analog-to-digital conversion of nA-range (subthreshold) currents is presented in this work. The presented modulator uses a subthreshold technique based on subthreshold source-coupled logic cells to efficiently convert subthreshold current to digital code without performing current-to-voltage conversion. As a benefit of this technique, the current-sensing CT ΣΔ modulator operates at low voltage and consumes very low power, which makes it convenient for low-power and low-voltage current-mode sensor interfaces. The prototype design is implemented in a 0.18 μm standard complementary metal-oxide semiconductor technology. The modulator operates with a supply voltage of 0.8 V and consumes 5.43 μW of power at the maximum bandwidth of 20 kHz. The obtainable current-sensing resolution ranges from effective number of bits (ENOB) = 7.1 bits at a 5 kHz bandwidth to ENOB = 6.5 bits at a 20 kHz bandwidth (ENOB). The obtained power efficiency (peak FoM = 1.5 pJ/conv) outperforms existing current-mode analog-to-digital converter designs and is comparable with the voltage-mode CT ΣΔ modulators. The modulator generates very low levels of switching noise thanks to CT operation and subthreshold current-mode circuits that draw a constant subthreshold current from the voltage supply. The presented modulator is used as a readout interface for sensors with current-mode output in ultra low-power conditions and is also suitable to perform on-chip current measurements in power management circuits. Copyright © 2014 John Wiley & Sons, Ltd.

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KEY WORDS: sensor interfaces; current sensing; current mode; low-power; low voltage; sigma-delta modulation

1. INTRODUCTION

Many state-of-the-art IC sensors deliver current-mode or charge-packet-based outputs [1–6]. Hence, current-to-voltage conversion is necessary in order to utilize voltage-mode analog-to-digital converters (ADCs) (except in [6] where a current input ADC is used). Current-to-voltage conversion is usually performed by integrating the current output on an on-chip (integrated) capacitor, because on-chip high-value resistors are nonlinear, occupy large area, and introduce high thermal noise. However, property which is in common to many complementary metal-oxide semiconductor (CMOS) integrated sensors (such as sensors [1–6], all CMOS integrated photodiodes [7], and biosensors [8]), relates to the very small sensor's output current level (pA–nA range). Hence, even when integrated on a CMOS integrated capacitor (typically fF–pF range), the integration time can be significant and consequently limit the achievable bandwidth. In addition, integrated capacitors

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(such as MOS-capacitors or PN-junction parasitic capacitances) have variable capacitance values that depend on the capacitor voltage [9], causing nonlinearity of the response. In that case, a possible solution consists of implementing active integrated transimpedance amplifiers (TIAs) with high transimpedance-gain (in Giga-Ω range). Nevertheless, implementing a low-power low-voltage linear active high-gain TIAs is a challenging task. Even at high supply voltages, if fairly linear, state-of-the-art integrated TIAs (e.g., [10, 11]) consume a relatively high amount of power. Thus, even extremely efficient voltage-mode low-power ADCs [12, 13] in the following stage can not compensate for the power inefficiency introduced by the active TIA.

Sensing and direct analog-to-digital conversion of nA-range (subthreshold) currents provide an efficient solution for such sensor interfaces. This work proposes a modulator that can successfully fulfill these tasks while maintaining a few μW-range low-power operation. Moreover, minimizing the voltage supply noise and substrate noise by limiting the switching activity of the surrounding circuits is crucial to support noise-sensitive front-end circuits. Power-efficient discrete-time modulators [14] are typically based on switched-capacitor circuits and generate supply current spikes because of high switching activity. Continuous-time (CT) operation minimizes the spikes in supply current (small dI/dt) and results in low-noise generation. This work focuses on the design of a CT subthreshold current-mode modulator, designed to obtain low supply and substrate noise generation.

Current-mode circuits suffer from the limited accuracy of the current transfer, which limits their final performance. Consequently, very few designs that are comparable with this work have been proposed in literature. Current-mode pipeline ADCs were presented in [15] and [16]. Furthermore, a successive-approximation ADC with current-mode comparator was presented in [17]. Current mode has also been used by folding and interpolating ADCs in the current interpolation stage [18–20]. A CT ΣΔ modulator with current-mode feedback is presented in [21]. Current mode is also used to implement switched-current memory cells and differential current comparators in a low-power switched-current ΣΔ ADC [22]. Another integrated current-mode ΣΔ ADC for motor-drive applications is presented in [23]. In [24], a high-speed pipelined ADC is designed using current-mode sample-and-hold and pipeline stages.

The presented modulator is used as a readout interface for sensors at low-power and low-voltage conditions. Moreover, it can find an efficient usage in power monitoring schemes such as [25], which would take benefit of sensing small (divided and copied) replicas of the supply currents in the digital domain at low-power costs.

2. SUBTHRESHOLD CURRENT-SENSING ΣΔ MODULATOR

The proposed current-sensing modulator follows a first-order ΣΔ architecture with a quantizer based on subthreshold source-coupled logic (STSCL) cells forming a ring oscillator. A top-level diagram of the modulator is shown in Figure 1. In order to simplify the testing procedure and allow better input control, the input current is generated on-chip by converting the input voltage. The input current is combined with the reference currents and the analog-to-digital converter (DAC) output currents and delivered to the differential current-mode low-pass filter (Section 4) operating in subthreshold mode.

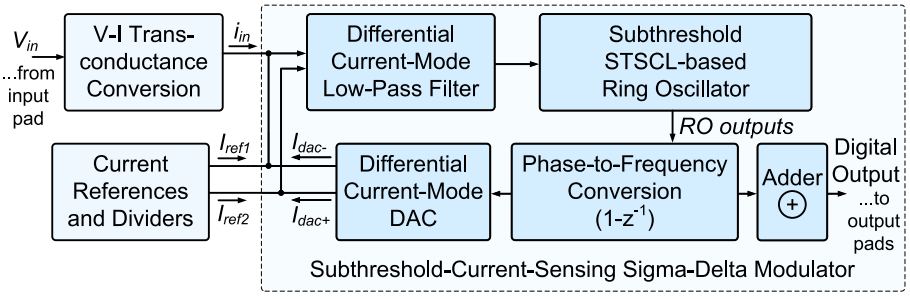

Figure 1. Top-level circuit diagram of the current sensing modulator.

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The filter output provides the control current for the ring-oscillator (RO) replica-biasing (RB) circuit. The RB circuit generates the tail current of the differential STSCL inverters within the RO (Section 3). The RO outputs are used as inputs to the phase-to-frequency converter, which performs a first-order differentiation of the phase in the digital domain ([26]). The phase-to-frequency converter outputs are passed to the thermometer-coded differential current-mode DAC, which generates the feedback currents. The first-order ΣΔ loop in Figure 1 results in second-order noise shaping of the modulator, because of additional (intrinsic) first-order noise shaping property of the ring-oscillator-based quantizer [26].

3. SUBTHRESHOLD CURRENT QUANTIZER

The quantizer is based on an STSCL RO followed by the digital phase-to-frequency converter. The top-level schematic of the proposed current quantizer is shown in Figure 2, and the detail schematic of the STSCL RO and the RB circuit is shown in Figure 3. The RB circuit generates the controlling voltages for the cascoded current mirrors V_{n1}(and V_{n2}) and the gates of the bulk-drain (BD)-connected load devices V_{gp} (Figures 2 and 3), based on the current-signal input (I_{sig}). The STSCL inverter output voltage swing (V_{sw}) is controlled by the RB feedback and fixed to approximately 300 mV by the reference voltage V_{ref} ($V_{sw} = V_{dd} - V_{ref}$; e.g., for a 0.8 V supply voltage, V_{ref} is set to 0.5 V). The RB circuit contains a complete dummy STSCL inverter for improved device matching. The current I_{sig} is copied by the High Compliance Regulated Cascode (HCRC) current mirror [27] to the corresponding STSCL inverter cells within the (current-controlled) ring oscillator. The low-swing STSCL voltage outputs of the current-controlled oscillator (CCO) are converted into full-swing CMOS outputs and delivered to the digital phase-to-frequency

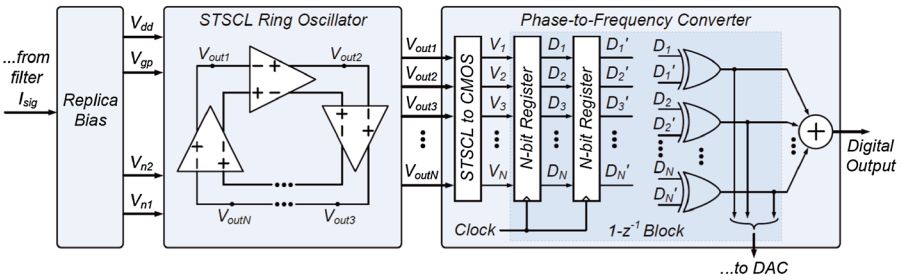

Figure 2. The subthreshold current quantizer based on subthreshold source-coupled logic (STSCL) current-controlled-oscillator and digital phase-to-frequency converter.

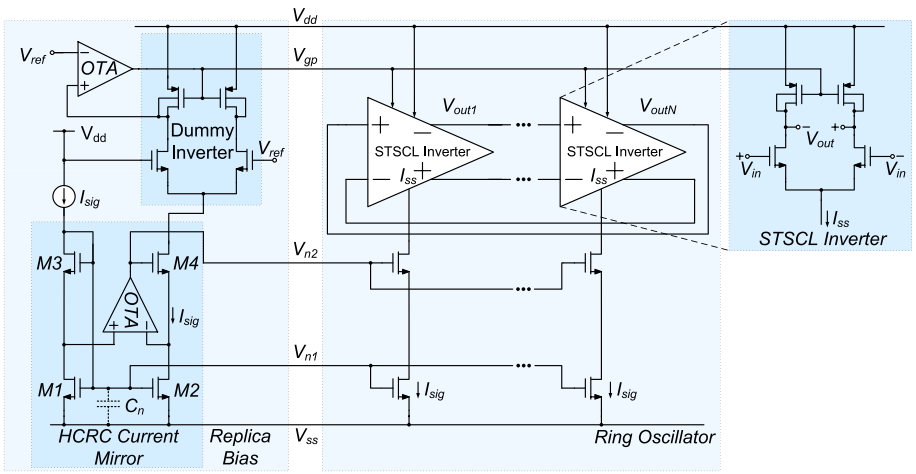

Figure 3. The subthreshold source-coupled logic current-controlled ring oscillator and replica-biasing circuit.

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converter (Figure 2). The digital phase-to-frequency converter measures the frequency of the oscillator by performing a first-order differentiation ($1 - z^{-1}$) in the digital domain ([26]). If a certain RO inverter undergoes a transition ($1 \rightarrow 0$ or $0 \rightarrow 1$) within one sampling cycle, the output of the corresponding XOR gate is equal to one. Hence, the summed output represents the total number of inverters within the ring that have flipped their output value during one sampling cycle. As a result, the final digital output in Figure 6 is directly proportional to the RO frequency [26]. The XOR outputs are directly fed to the thermometer-coded DAC in the feedback loop (Section 5).

3.1. Subthreshold source-coupled logic inverter cells

The concept of STSCL for ultra-low power digital gates was introduced in [28]. In this work, STSCL inverter cells are used to design a RO-based subthreshold current quantizer. Hence, a short review of STSCL is presented in this section, addressing the most important features in the context of ΣΔ modulator design.

The schematic of an STSCL cell with dynamically controlled biasing is presented in Figure 4. The inverter cell is biased with the subthreshold current I_{ss}, which is typically in the nA range, but can be set as low as 10 pA [28]. The RB circuit allows a dynamic control of the load bias by adjusting the gate voltage of the P-type metal-oxide semiconductor (PMOS) devices (V_{gp}). The RB feedback maintains the output voltage swing constant independently of the changes in the threshold voltage of the load transistors because of process and temperature variations. Moreover, it maintains the output voltage swing constant independently of the tail current I_{ss}. Within small design blocks, the transistor *MPB* (Figure 4) can be matched very well with the load devices of the logic gates. The effects of global process and temperature variations are therefore minimized, and only the random device mismatch remains a dominant cause of load resistance variation. Consequently, the delay of STSCL inverters only depends on the corresponding tail currents and capacitive load at the inverter output. Because the nominal values of tail currents are dictated by the current reference circuit, this allows robustness of the quantizer with respect to temperature and process variations.

The minimum required input voltage swing of a differential pair operated in subthreshold region is $V_{sw,min} = 4 \cdot n \cdot U_T$ [29], where n is the subthreshold slope factor and U_T is the thermal voltage ($U_T = kT/q \approx 26$ mV at room temperature). This results in $V_{sw,min} \approx 150$ mV for a standard bulk process at room temperature. Therefore, the load devices should produce very high resistance values in order to achieve the desired output voltage swing. Two types of PMOS-based active load devices can be used in the desired configuration from Figure 4 and achieve resistances in MΩ and GΩ ranges: BD connected PMOS and bulk-source (BS) connected PMOS (Figure 5).

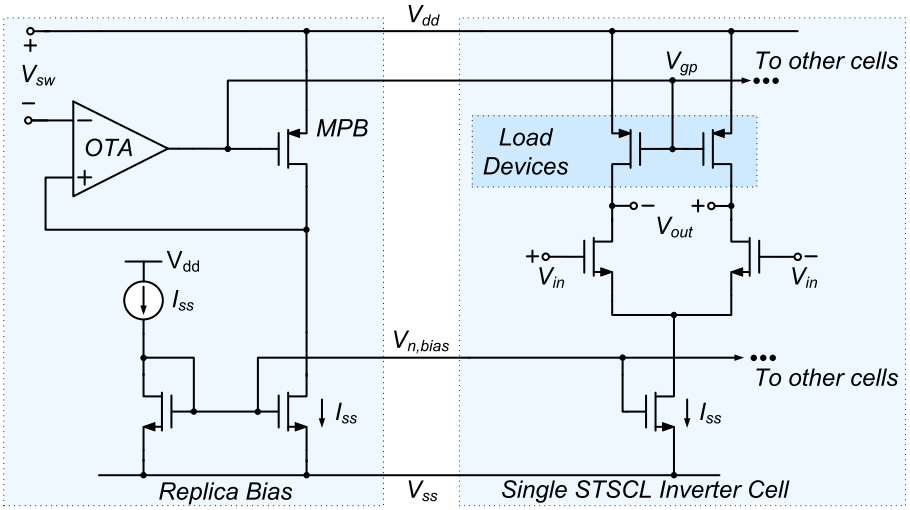

Figure 4. Subthreshold source-coupled logic (STSCL) inverter cell with dynamically controllable biasing.

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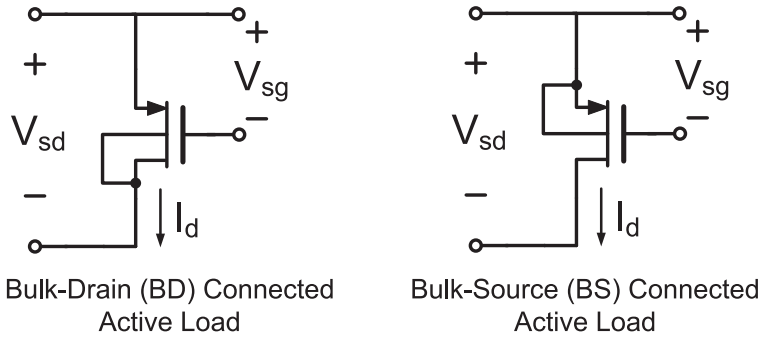

Figure 5. Two different active load configurations.

Considering a BS-connected PMOS device in weak inversion, the resulting output impedance is extremely high if $V_{sd} > 4 \cdot U_T$. However, when utilized in the desired configuration of Figure 4, the extremely high small-signal output impedance becomes a drawback rather than a benefit. High output impedance results in a very high two-stage gain, making it extremely hard to stabilize the RB feedback loop. The BD-connected device has considerably lower small-signal output impedance. Because the output node is connected to the bulk, the drain voltage can modulate the depth of the depletion region underneath the gate, therefore modulating the drain current. The difference between the BS and BD connected load for the minimum size devices is illustrated in Figure 6(a), considering the 0.18 µm standard CMOS process used in this work. The gates of both devices are biased such that they approximately provide 200 mV of source-drain voltage at 2 nA drain current. With the assumption that the output swing requires control within the 100–300 mV range, the BD-connected load provides a significantly wider controllable current range. A small-signal output impedance comparable with the BD-connected device can be achieved by the BS-connected device (Figure 6(b)) for the minimum size devices. The absolute current range within the same output voltage swing is similar, and therefore, the same controllability can be obtained in the feedback loop. However, the BS-connected device requires higher biasing current for the same output voltage swing, thereby directly increasing the power consumption.

The difference between the BD and BS connected load becomes more pronounced using high device lengths. Because of matching requirements, minimum-length devices can not be used if a precise inverter delay is needed. For higher length devices, the drain-induced barrier lowering effect is reduced; the drain voltage can not modulate the drain current, and the small-signal output impedance becomes very high. This is simulated and shown in Figure 6(c) considering identical BD and BS connected load device lengths of $L = 4$ µm. The gate biasing of both devices is identical as applied in Figure 6(a). While the BD-connected device presents an acceptable small-signal impedance and therefore enables controllable current range, the small-signal impedance of the BS-connected device is practically infinite. In conclusion, the BD-connected load device is best suitable to the STSCL configuration in Figure 4.

The source-drain current of the PMOS device in weak inversion is expressed by the Enz–Krummenacher–Vittoz model [29] as

$$I_{SD} = I_0 \cdot e^{\frac{V_{BG} - V_{T0}}{n_p U_T}} \left(e^{\frac{V_{SB}}{U_T}} - e^{\frac{V_{DB}}{U_T}} \right), \tag{1}$$

with $I_0 = 2 n_p \mu C_{ox} U_T^2 W / L_{eff}$, where n_p is the PMOS transistor subthreshold slope factor, μ is the charge-carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area, W is the physical PMOS gate width, L_{eff} is the effective gate length, and V_{T0} is the threshold voltage (nominal value at room temperature) of the transistor. By setting $V_{BD} = 0$, and differentiating with respect to V_{DS}, the small-signal resistance can be expressed as

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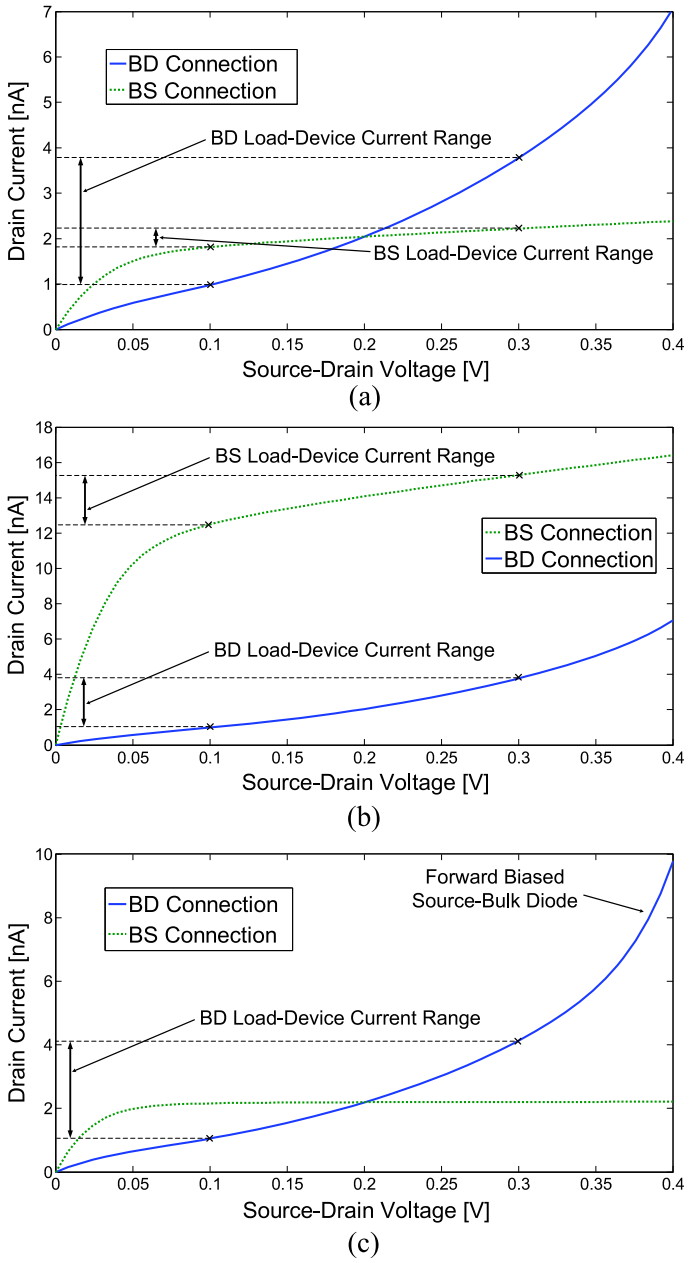

Figure 6. Comparison of bulk-drain (BD) versus bulk source (BS) connected load device characteristics: (a) minimum size devices, same biasing; (b) minimum size devices, same impedance; (c) long devices ($L = 4\,\mu m$), same biasing.

$$r_{DS} = \frac{n_p U_T}{I_0} A_{V_{SD}} e^{-\frac{V_{SG}-V_{T0}}{n_p U_T}}, \tag{2}$$

where for a specific source-drain voltage biasing (output swing), $A_{V_{SD}}$ is constant:

$$A_{V_{SD}} = \left[(n_p - 1) e^{\frac{(n_p-1)V_{SD}}{n_p U_T}} + e^{\frac{V_{DS}}{n_p U_T}} \right]^{-1}. \tag{3}$$

Thanks to the exponential dependence of r_{DS} on V_{SG}, the resistance can be controlled in a very wide range by dynamically adjusting the gate voltage V_{gp} (Figure 4). Nevertheless, this characteristic is

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balanced by a relatively poor matching of the resistances. Because r_{DS} also has an exponential dependence on the threshold voltage (V_{T0}, Eq. (2)), the variation of the threshold voltage significantly varies the r_{DS} value.

The small-signal resistance value is approximately proportional to the inverter delay and therefore defines the accuracy limit of the RO quantizer. The results of 1000 Monte-Carlo simulations of the PMOS devices used in this work ($W \times L = 4\ \mu m \times 4\ \mu m$) are shown in Figure 7. The simulations were performed for biasing currents $I_{ss} = 10\,nA$ (Figure 7(a)) and $I_{ss} = 1\,nA$ (Figure 7(b)) at $V_{SD} = 150\,mV$. The devices achieve a relative standard deviation of resistance of approximately 2% in both cases. Thanks to the intrinsic Data Weighted Averaging (DWA) of the RO-based quantizer (Section 3.4), this level of random mismatch enables up 8 bits of quantizer resolution.

Increasing the width of the load device for better resistance matching is limited by the forward-biased source-bulk diode of the BD-connected device. The effect of the source-bulk diode can be observed in Figure 6(c). With the increase of the load device width, the junction diode area increases and the overall resistance of the load decreases. Therefore, the source-bulk diode limits the width of the device for the specified desired output voltage swing. Increasing the length of the load device improves the matching while equally decreasing the power consumption and the bandwidth of the quantizer, therefore maintaining a constant power efficiency.

3.2. High compliance regulated cascode current mirror in subthreshold mode

A HCRC current mirror [27] operated in weak inversion is used to increase the output impedance and allow low-voltage and low-noise operation. When an HCRC operates in strong inversion as in [27], transistors *M1*, *M2*, *M3*, and *M4* (Figure 3) are sized with identical *W*/*L* ratios, which results in triode region operation of transistors *M1* and *M2*. In the general case (and in [27]), a high-gain operational amplifier can be used in the regulation loop (in place of the Operational Transconductance Amplifier (OTA) in Figure 3, which is used in this design), in order to compensate for the low output impedance of *M1* and *M2*. As a result, the output voltage can be extremely low ($V_{out,min} \approx 50$ mV), while the small-signal output resistance is boosted and given by

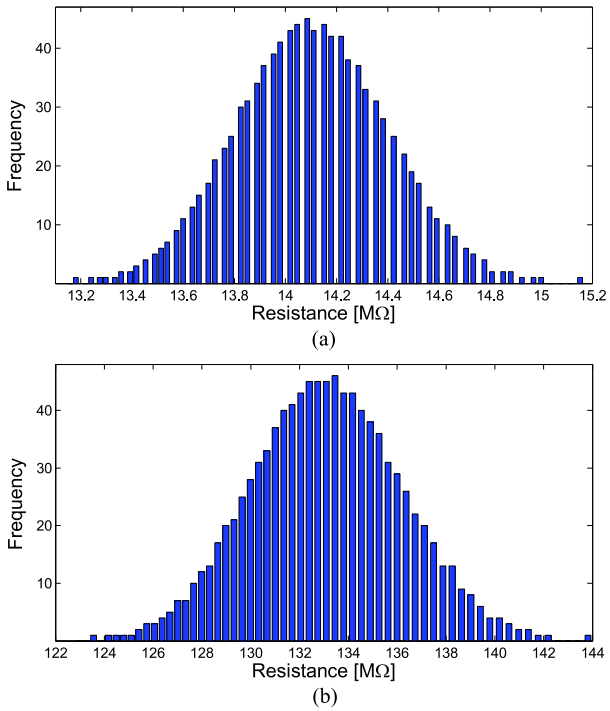

Figure 7. Bulk-drain (BD)-connected load resistance matching: (a) at $I_{ss} = 10\,nA$ and $V_{SD} = 150\,mV$; (b) at $I_{ss} = 1\,nA$ and $V_{SD} = 150\,mV$.

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$$r_{out} = \frac{A \cdot g_{m,M4}}{g_{ds,M4} \cdot g_{ds,M2}}, \tag{4}$$

where A is the amplifier gain, and $g_{m,Mj}$ and $g_{ds,Mj}$ are the transconductance and output conductance of transistor Mj, respectively ($j \in [2, 4]$).

Equation (4) still holds in weak inversion. However, because of low-power constraints, a high-gain operational amplifier in the regulation loop can not be implemented in this design. Instead, an operational low-gain and low-power transconductance amplifier operated in weak inversion is used (OTA in Figure 3). Moreover, because of a very low drain current, the transconductance of the device *M4* ($g_{m,M4}$) is significantly reduced compared with the observed transconductance when the device is operated in strong inversion with large drain current (as in [27]). Hence, the regulating loop does not have sufficient gain to effectively compensate the low output impedance of transistors *M1* and *M2* if the devices enter the linear region of weak inversion. Therefore, the drain voltages of the devices *M1* and *M2* can not be allowed to decrease below $4 \cdot U_T$, which would result in the linear region operation and low output impedance. Consequently, the devices *M1* through *M4* have to be sized such that $V_{gs,M1}$ and $V_{gs,M2}$ are at least $4U_T$ higher than $V_{gs,M3}$ and $V_{gs,M4}$, simultaneously considering that increasing the length of *M*1 and *M2* limits the bandwidth of the current mirror. As an example, the *W*/*L* of *M*1, *M*2 is set to 2 μm/5 μm while the *W*/*L* for *M*3, *M*4 is set to 5 μm/2 μm in order to satisfy the requirements in the final design. The sizes of the RO inverters' tail bias transistors are set accordingly.

3.3. Ring oscillator

The nominal delay of each individual STSCL inverter can be expressed as

$$t_d = \frac{V_{sw} C_L}{I_{sig}} \cdot \ln 2, \tag{5}$$

where V_{sw} is the output voltage swing controlled by the replica bias feedback (Figure 3), C_L is the output load capacitance, and I_{sig} is the signal current. The oscillation period is $T_{osc} = 2Nt_d$ resulting in a linear CCO with the current-to-frequency conversion curve defined by

$$f_{osc} = \frac{1}{2NV_{sw}C_L ln\, 2} I_{sig}. \tag{6}$$

As a result, the quantizer can achieve high linearity over a wide range of input currents. Simulation results show that the total harmonic distortion of less than −60 dB is achievable over three decades of the input current (from 100 pA to 100 nA). In [30], a simplified and lower frequency version of the standalone quantizer was tested confirming the wide input current range. The measured distortion level in [30] is mainly limited by low performance current mirrors.

3.4. Oscillator delay matching and data weighted averaging

Based on expression (5), the inverter delay mismatch depends on current-mirror matching (I_{sig}, Section 3.2), resistance matching (V_{sw}—Section 3.1), and capacitance matching (C_L). In addition to random capacitor mismatch, a significant systematic mismatch may appear in the load capacitance if the interconnections are not matched. For instance, if the output of the last inverter in an array (ring) is connected to the input of the first inverter, a long interconnection metal line with a significantly higher parasitic capacitance than the rest of the ring interconnections is required. To balance and match the parasitic capacitances of the inverter interconnections, the physical metal lines need to be exact replicas with respect to each other. Consequently, the RO inverters are connected as illustrated in Figure 8 to achieve high interconnection matching. Moreover, to further reduce the influence of parasitics and additionally linearize the

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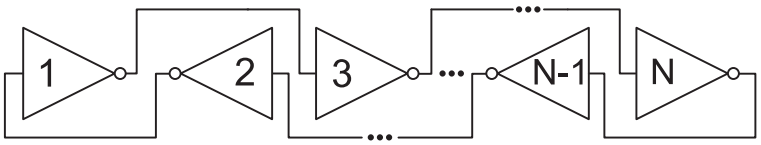

Figure 8. Inverter connections within the ring oscillator.

current-to-frequency response, 100fF metal insulator metal capacitors are used as a dominant inverter load. The capacitors are isolated from the dummy metal patterns by matched metal stripes to increase the control over the load capacitance value (Figure 9).

The implicit DWA reduces the effect of delay mismatch by barrel shifting the inverters undergoing an output transition in each sampling period. Averaging takes effect over a large number of samples and randomizes the error. After p samples, where $p = OSR$ (over-sampling ratio), the Nyquist equivalent relative error is

$$e_{avg} = \frac{1}{T_s \cdot OSR} \sum_{i=1}^{S} \Delta t_{d,i}, \tag{7}$$

where $\Delta t_{d,i}$ is the absolute delay error because of mismatch of the i-th inverter undergoing a transition, T_s is the sampling rate and S is the total number of transitions during $OSR \cdot T_s$. The number of transitions in each sampling cycle is equal to the digital output d_j. An average value of d_j after $OSR \cdot T_s$ can be considered as a Nyquist equivalent of the digital amplitude (as obtained after the decimation filter). Hence, the average number of transitions during each sampling cycle is

$$\overline{d} \approx \frac{1}{OSR} \sum_{j=1}^{OSR} d_j. \tag{8}$$

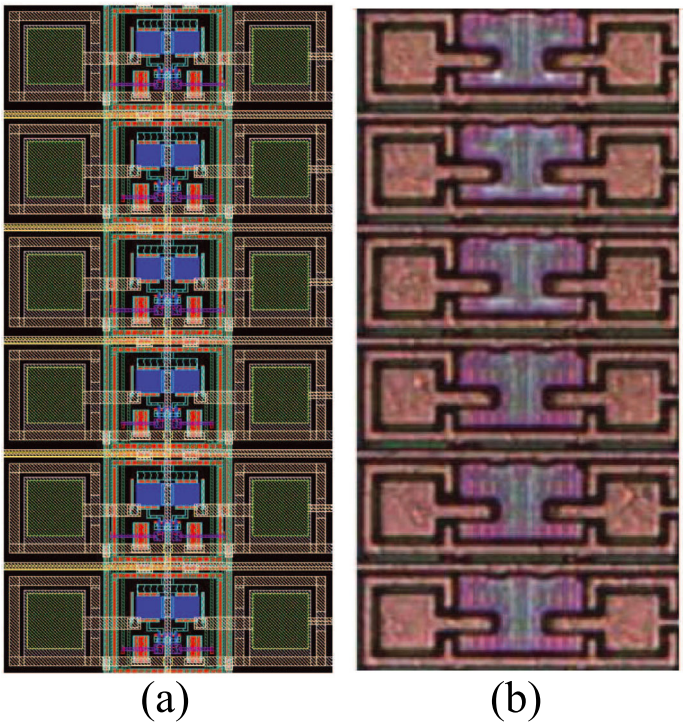

Figure 9. Six subthreshold source-coupled logic (STSCL) inverters in the ring oscillator: (a) mask layout; (b) die micrograph.

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Therefore, on average, the sampling period is expressed as $T_s = \overline{d} \cdot t_d$, while the total number of transitions is $S = \overline{d} \cdot OSR$. If the full ring undergoes k transitions during $OSR \cdot T_s$, then $OSR \cdot \overline{d} = k \cdot N + m$, where m is the residual number of transitions ($m < N$). When a transition has propagated across the full ring, the absolute mismatch error is constant and equal to the sum of absolute errors of all N inverters. Hence, the error becomes fully correlated, and the amplitude instead of the variance must be summed. The variance of the relative error due to delay mismatch (7) is then given as

$$Var(e_{avg}) = \frac{1}{\overline{d}^2 \cdot t_d^2 \cdot OSR^2} \left[k^2 Var\left(\sum_{i=1}^{N} \Delta t_{d,i} \right) + Var\left(\sum_{i=1}^{m} \Delta t_{d,i} \right) \right], \tag{9}$$

which after substituting $m = \alpha N (0 < \alpha < 1)$ becomes

$$Var(e_{avg}) = \frac{k^2 + \alpha}{(k + \alpha)^2} \cdot \frac{\sigma_{\Delta t_d}^2}{N}. \tag{10}$$

For a small number of inverters N, k becomes significantly larger than α, hence

$$\sigma_{e_{avg}} \approx \frac{\sigma_{\Delta t_d}}{\sqrt{N}}. \tag{11}$$

In the considered design, a large number of inverters is not possible because increasing N linearly increases the power consumption of the ring. The number of inverters in the ring is set to $N = 13$, which satisfies the power consumption limit and the target resolution. It should be noted that the error randomized by the DWA is further additionally filtered by noise shaping. Hence, the resulting standard deviation in the base band is actually lower than given by (11), but still proportional to $1/\sqrt{N}$.

3.5. Ring oscillator jitter

The RO jitter can become a significant source of quantizer noise at extremely low tail-current levels. The jitter standard deviation in the RO is shown to increase with the square root of the measurement time [31]:

$$\sigma_j = \kappa \sqrt{\Delta T}, \tag{12}$$

where κ is a proportionality constant, which depends on the circuit topology and parameters. For differential ROs, it was shown [32] that

$$\kappa \geq \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{ss}} \right)}, \tag{13}$$

where η is the ratio between the inverter rise/fall time and delay, N is the number of inverters, k is the Boltzmann constant, T is the junction temperature, P is the total power of the RO, and $V_{char} \approx V_{sw}/2$ for subthreshold operation. In case of the proposed RO, $R_L = V_{sw}/I_{ss}$, $V_{sw} \approx 12 \cdot U_T$, and $P \approx N \cdot V_{DD} \cdot I_{ss}$, which yields

$$\kappa \geq \sqrt{\frac{2q}{3\eta I_{ss}}}, \tag{14}$$

where q is the elementary charge. The RO jitter is subjected to the same noise transfer function as the quantization noise, because they are both generated by the quantizer. Therefore, RO jitter is first-order shaped by the quantizer [26]. Consequently, the worst-case jitter is $\sigma_j = \kappa \cdot \sqrt{T_s}$ during a single sampling period. Considering a tail current of approximately 100 nA and 1 MHz sampling rate, expression (12) yields $\sigma_j \approx 1.2$ ns. Because the nominal delay (quantization level) is higher than

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200–250 ns, and with the additional shaping generated by the ΣΔ loop, the quantizer provides satisfying results. In addition, flicker noise is not an important issue for the RO-based quantizer (and this design in general) despite the subthreshold operation. All the transistors in the signal path are relatively large because of the matching requirements imposed by the current-mode operation (typically several micrometer in both length and width). Because the metal-oxide-semiconductor field-effect transistor transistor flicker noise power is inversely proportional to transistor dimensions (proportional to $1/(W \cdot L)$), the effect of flicker noise is practically negligible.

4. CURRENT-MODE LOW-PASS FILTER

The translinear circuit technique is convenient for designing CT analog processing circuits under low supply voltage conditions [33]. The low-pass filter implemented in this design is based on the translinear companding integrator originally designed in bipolar technology [34]. The class AB differential companding integrator presented in [34] is implemented using subthreshold MOS devices and complemented with a single-ended output stage (Figure 10). The filter output node is directly connected to the input of the replica bias (replacing of I_{sig} in Figure 3).

The filter operates using two translinear loops in differential mode (loops: $M1$–$M2$–$M3$–$M4$ and $M1'$–$M2'$–$M3'$–$M4'$). Following the circuit analysis in [33] and [34], and using $I_0 = 2n_n\mu C_{ox}U_T^2 W/L$ yields

$$\frac{i_{M1}}{(W/L)_1}\cdot\frac{i_{M2}}{(W/L)_2} = \frac{i_{M3}}{(W/L)_3}\cdot\frac{i_{M4}}{(W/L)_4}. \tag{15}$$

Hence, considering the positive differential side (Figure 10) yields

$$\frac{i_{in}^{+}}{(W/L)_3}\cdot\frac{I_b}{(W/L)_4} = \frac{i_{out}^{-} + C\frac{dV}{dt}}{(W/L)_2}\cdot\frac{i_{out}^{+}}{(W/L)_1}, \tag{16}$$

where $I_b = i_{M4}$ is the biasing current from the PMOS current source. Equivalently, considering the negative side (loop: $M1$–$M2$–$M3$–$M4$) yields the following expression:

$$\frac{i_{in}^{-}}{(W/L)_{3'}}\cdot\frac{I_b}{(W/L)_{4'}} = \frac{i_{out}^{+} + C\frac{dV}{dt}}{(W/L)_{2'}}\cdot\frac{i_{out}^{-}}{(W/L)_{1'}}, \tag{17}$$

where $I_b = i_{M4'} = i_{M4}$. The transistors Mj and Mj' are matched for every $j \in \{1, 2, 3, 4\}$; hence, subtracting (17) from (16) and integrating yields

$$i_{out}^{+} - i_{out}^{-} = \frac{K \cdot I_b}{n_n \cdot U_T \cdot C}\int_{-\infty}^{t}\left(i_{in}^{+} - i_{in}^{-}\right)dt, \tag{18}$$

where $K = (W/L)_3 \cdot (W/L)_4/[(W/L)_1 \cdot (W/L)_2]$.

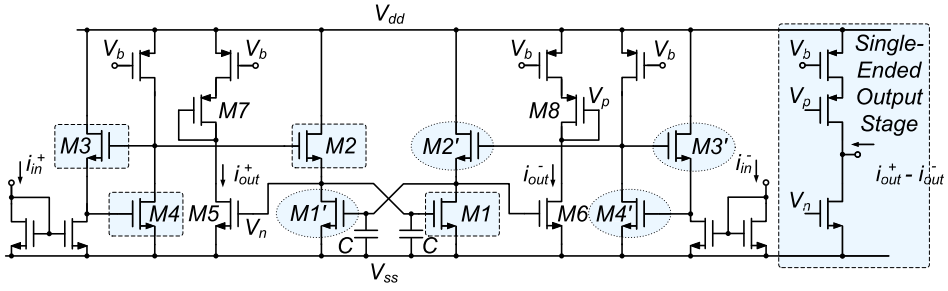

Figure 10. The companding current-mode low-pass filter.

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The circuit in Figure 10 acts as an ideal integrator only if MOS transistor output impedance is infinitely large and $g_{m,M1}$, $g_{m,M1'}$, $g_{m,M2}$, and $g_{m,M2'}$ are exactly equal. However, limited output impedance and other parasitic effects limit the achievable gain and the positioning of the dominant pole. The frequency response of the filter is shown in Figure 11. The translinear loop requires an exponential dependence between the drain current and gate-source voltage of the metal-oxide-semiconductor field-effect transistor devices. Therefore, for an optimal filter response, it is very important to keep the translinear loop transistors in weak inversion. Hence, the translinear loop transistors should be biased such that they are deeply in weak inversion to compensate for any possible threshold voltage decrease due to temperature or process variations. For the technology process used in this work, a reasonable margin that ensures proper operation of the filter at 125 °C in fast-N-type metal-oxide semiconductor (NMOS) (low threshold) process corner is obtained by a gate-source biasing of 150 mV below the threshold voltage.

5. CURRENT-MODE DIGITAL-TO-ANALOG CONVERTER

The outputs of the XOR gates within the phase-to-frequency converter (Figure 2) are provided to the thermometer-coded differential current-mode DAC. The input of the DAC is single-ended because the phase-to-frequency converter operates based on (single-ended) CMOS logic. A complete schematic of the DAC is shown in Figure 12 (the number of unit elements is $N = 13$). Each unit-element DAC consists of two cascoded PMOS devices in which the upper device has a higher threshold voltage. This results in higher drain-source voltage of the upper PMOS and hence better current matching between the unit elements. The single-ended DAC output current is converted to a differential signal using ordinary current mirrors (Figure 12). This conversion is necessary because the output of the DAC is used as the input of the low-pass filter, which

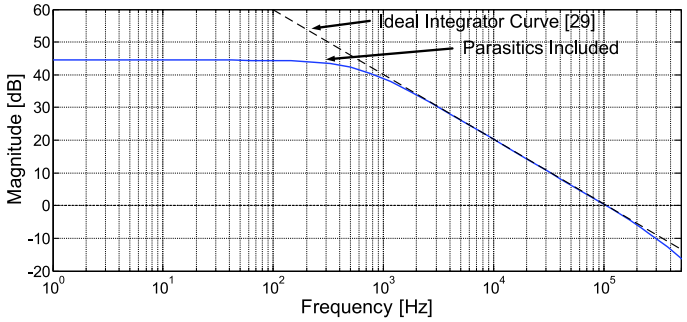

Figure 11. The low-pass filter frequency response.

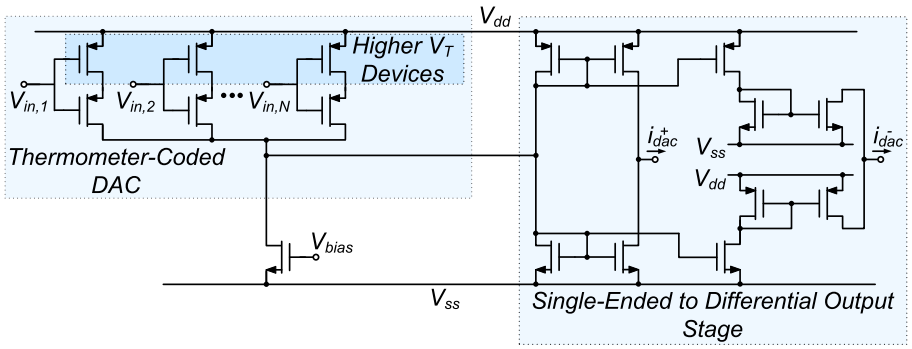

Figure 12. Thermometer-coded current-mode digital-to-analog converter (DAC).

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operates in differential mode. The subthreshold current-mode filter needs differential operation to overcome the limitation of the single-ended subthreshold current-mode filter, which would be extremely sensitive to process and temperature variations. Finally, the mismatch between i_{dac}^{+} and i_{dac}^{-} due to current copying in the output stage was shown to add an acceptable level of distortion for the target resolution.

6. MEASUREMENT RESULTS

A prototype of the current-sensing modulator (shown in Figure 1) is implemented in a conventional 0.18 µm CMOS process. A micrograph of the fabricated chip is shown in Figure 13. Two identical modulators are placed on the same die and can be used in parallel operating in a pseudo-differential mode. The active silicon area of a single modulator core is 610 µm × 210 µm. The complete modulator occupies an area of 610 µm × 365 µm including the current references and the input transconductance stage. The modulator achieves 20 kHz of bandwidth while consuming 5.43 µW of power operating at a 0.8 V supply voltage. Most of the power is consumed by the quantizer (P_{ROQ} = 2.95 uW) and the DAC (P_{DAC} = 1.85 µW). The remaining power of 630 nW is consumed by the current-mode low-pass filter. The current references and the input transconductance stage are connected to a separate power supply, and their power consumption is not included in the presented 5.43 µW of total power. The peak measured signal-to-noise and distortion ratio (SNDR) is equal to 44.5 dB at a 5 kHz bandwidth, and 40.89 dB at a 20 kHz bandwidth using a 1 kHz input signal and 1 MHz sampling rate.

The input transconductance stage consists of a 10 µS transconductance followed by a 1:140 current divider. The full-scale (FS) voltage input amplitude used is 800 mV, which translates into an approximate modulator input current amplitude of 57 nA. The current input range of the modulator is 0–280 nA, and the effective measured range is 130–250 nA. According to simulations, the maximum SNDR of the modulator is typically achieved at approximately −12 dBFS of the current FS amplitude (47 nA); hence, the transconductance stage was designed to target this amplitude range. In the following, we refer to FS as the input pad (voltage) FS.

A fast Fourier transform of the output signal is shown in Figure 14 for a 1 kHz (1003.26 Hz) input signal and 1 MHz sampling rate at −6 dBFS. The second-order noise shaping can be

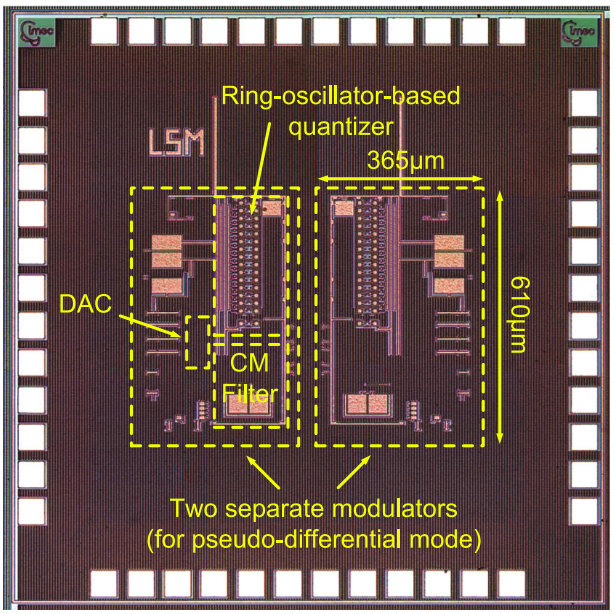

Figure 13. Die micrograph.

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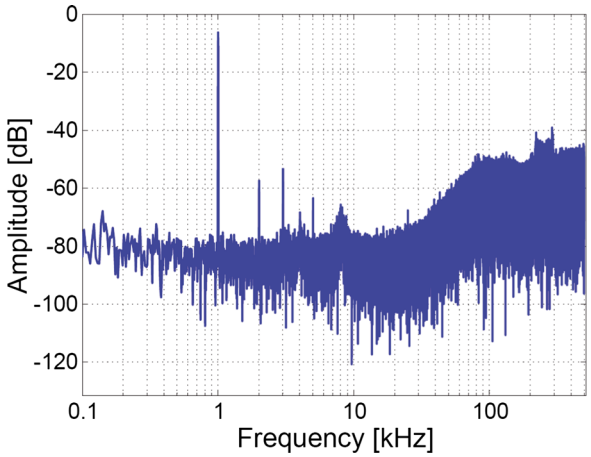

Figure 14. Output fast Fourier transform spectrum normalized to full scale with 1 kHz input signal and 1 MHz sampling rate.

observed within the 40–100 kHz range. The flat spectrum below 40 kHz is mainly a consequence of the lossy current-mode integrator (filter) in the ΣΔ loop. The high-frequency noise feature observed in the 200 kHz to 300 kHz range (around $F_s/4$) is common for voltage-controlled oscillator and CCO-based quantizers and is mainly caused by the mismatch between rising and falling edges of the quantizer [26]. A fixed-frequency noise skirt centered around 8 kHz originates from the measurement setup; however, the exact origin is not experimentally confirmed. An output signal spectrum is shown in Figure 15 for a 5 kHz (4985.81 Hz) input signal and 1 MHz sampling rate at −6 dBFS. The noise skirt remains centered at an approximate frequency of 8 kHz.

The measured signal-to-noise ratio and SNDR versus the voltage input signal amplitude for a single modulator (single-ended mode) is shown in Figure 16 for a 1 kHz input signal in the 20 kHz bandwidth. Because the FS current range is not measured, the steep decline in the measured SNDR is mainly caused by the input transconductance stage. The maximum measured SNDR is 40.5 dB, which translates into an ENOB of 6.5 at a 20 kHz bandwidth and 44.5 dB at a 5 kHz (ENOB = 7.1). The summary of the modulator performance is given in Table I. The converter efficiency (Figure of Merit) is defined as $\mathrm{FoM} = \mathrm{Power}/(2 \cdot \mathrm{BW} \cdot 2^{\mathrm{ENOB}})$.

Two separate on-chip modulators can operate in pseudo-differential mode. The even-order distortion and 8 kHz noise skirt cancel out, and typically, an SNDR improvement of 3 dB is

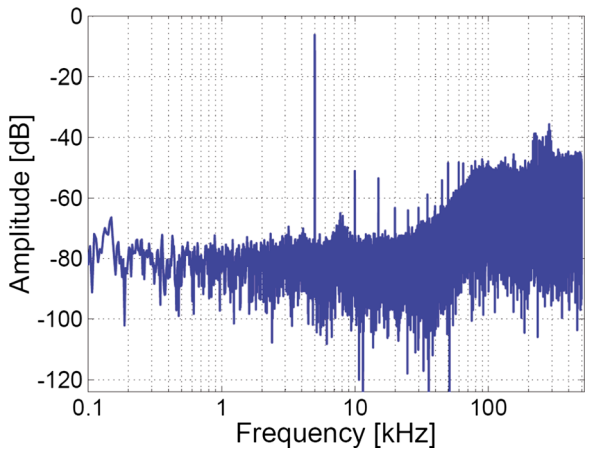

Figure 15. Output fast Fourier transform spectrum normalized to full scale with 5 kHz signal and 1 MHz sampling rate.

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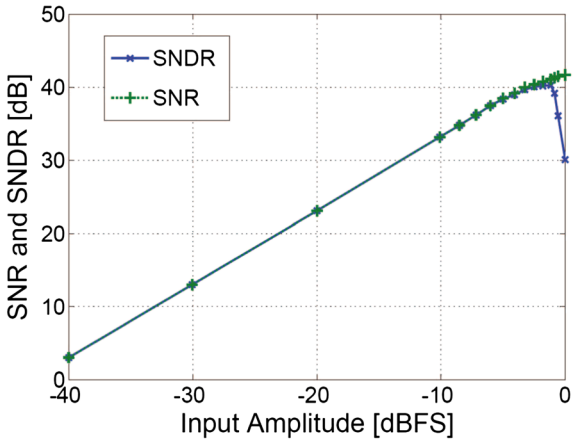

Figure 16. Signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) versus input amplitude (single-ended) at 1 kHz input frequency and 20 kHz bandwidth.

Table I. Performance summary.

Specification	Value
Input range (chip)	0–1.6 V
Input range (modulator)	0–280 nA
Sampling frequency	1 MHz
Input bandwidth	5 kHz/20 kHz
Peak SNDR	44.5 dB/40.5 dB
Peak SNR	46 dB/42 dB
Power consumption	5.43 µW
Peak efficiency (FoM)	1.5 pJ/conv
Core area	610 µm × 210 µm
Total area	610 µm × 365 µm
Technology	0.18 µm Standard CMOS

CMOS = complementary metal-oxide semiconductor; SNR = signal-to-noise ratio; SNDR, signal-to-noise and distortion ratio.

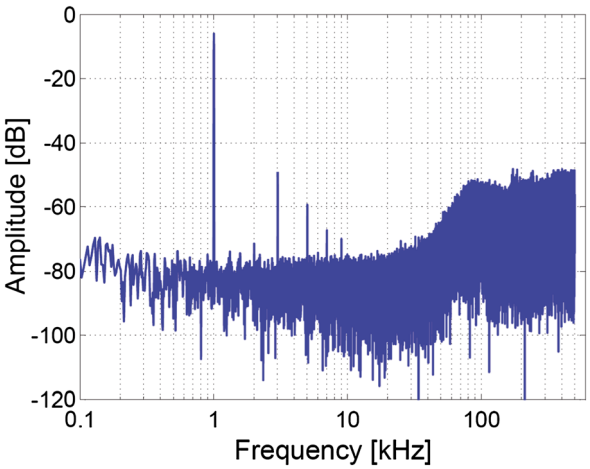

Figure 17. Pseudo-differential output fast Fourier transform spectrum normalized to FS with 1 kHz input signal.

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Table II. Comparison with current-mode analog-to-digital converters.

	Topology	Process (μm)	Supply (V)	ENOB	Bandwidth	Power	Efficiency [pJ/conv]
[15] ISSCC 2002	Pipeline	0.35	3.3	7	2 GHz	4.6 W	8.9
[16] CICC 2007	Pipeline	0.25	2	7	10 MHz	60 mW	23
[24] IMWS-IRFPT 2011	Pipeline	0.09	1.2	5	250 MHz	52.8 mW	3.2
[17] JSSC 2000	SAR	1.2	1	7.9	25 kHz	340 μW	26.5
[18] JSSC 2000	Folding	0.35	1	6	25 kHz	10 mW	3.12
[19] JSSC 2003	Folding	0.35	3.3	7	60 MHz	200 mW	13
[21] ESSCIRC 2003	ΣΔ	0.5	1.5	10	25 kHz	250 μW	4.9
[22] TCAS-I 2006	ΣΔ	0.18	0.8	7.5	5 kHz	180 μW	70
[23] TPE 2012	ΣΔ	0.35	3.3	11.7	10 kHz	12.1 mW	182
This work	ΣΔ	0.18	0.8	6.5–7.1	20 kHz	5.43 μW	1.5

ENOB = effective number of bits; SAR = Successive-Approximation Register.

Table III. Comparison with voltage-mode continuous-time ΣΔ analog-to-digital converters.

	Process (nm)	Supply (V)	ENOB	BW	Power	Efficiency [pJ/conv]
[26] JSSC 2008	130	1.2	11.7	10 MHz	40 mW	0.61
[35] JSSC 2011	65	1.2	10	20 MHz	10.5 mW	0.32
[36] JSSC 2010	110	1.1	10	10 MHz	5.32 mW	0.24
[37] JSSC 2009	90	1.2	10	1.92 MHz	5 mW	1.27
[38] JSSC 2005	130	1.5	11.7	2 MHz	3 mW	0.22
[39] JSSC 2003	180	1.8	10	2.5 MHz	2.2 mW	0.43
[40] ISSCC 2004	130	0.9	8.16	1.92 MHz	1.5 mW	1.36
[41] ISSCC 2004	180	1.8	9.6	1 MHz	1.15 mW	0.74
This Work	180	0.8	6.5–7.1	20 kHz	5.43 μW	1.5

observed. Figure 17 shows the output spectrum of the pseudo-differential mode for 1 kHz input signal. The maximum measured SNDR in the differential mode is 43.6 dB (ENOB = 7) at 20 kHz and 47.5 dB at 5 kHz bandwidth (ENOB = 7.6). Nevertheless, the power consumption is doubled in the pseudo-differential mode degrading the overall power efficiency (FoM = 2.12 pJ/conv).

The presented current-sensing modulator outperforms all existing ADCs implementing current-mode operation (Table II) in terms of power efficiency. Moreover, the power efficiency is comparable with the conventional voltage-mode CT ΣΔ modulators (Table III). For ultra low-power applications where current sensing is necessary, this modulator represents an optimal alternative to voltage input ADCs, because active current-to-voltage conversion would require significant power, substantially reducing the efficiency of the voltage converters.

7. CONCLUSION

A subthreshold current-to-digital CT ΣΔ modulator capable of sensing nA-range subthreshold currents is presented in this work. The micro-watt power conversion technique is based on STSCL cells and enables the modulator to perform direct current-to-digital conversion without using any current-to-voltage conversion stage. Based on this technique, the subthreshold current-sensing modulator prototype is designed and analyzed in detail. The measured prototype achieves a current quantization of ENOB = 6.5 (ENOB = 6.8 in pseudo-differential mode) at a 20 kHz and ENOB = 7.1 (ENOB = 7.4 in pseudo-differential) at 5 kHz bandwidth. The sampling rate of the converter is 1 MHz, and the power consumption is 5.43 μW while operating at 0.8 V supply voltage. The power efficiency of the presented modulator outperforms all previously reported current-mode designs and is comparable with many voltage-mode CT ΣΔ modulators.

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The modulator is primarily intended for sensors with current-mode outputs operating in ultra low-power conditions where both passive and active current-to-voltage conversions are ineffective. Extremely low switching noise mainly owing to static subthreshold current consumption makes it very attractive for low-noise front-end circuits and interfaces. Thanks to micro-watt power operation, the presented current-sensing modulator can also be used for on-chip current measurements in power management units.

The presented technique is scalable and would benefit from newer nanometer CMOS technology nodes. Increased matching would enable higher bandwidth or higher precision for the same size devices. The achievable bandwidth is mainly limited by the capacitive load of the STSCL inverters, which can be optimized and reduced. Moreover, the size of RO transistors may be optimized to increase bandwidth or decrease the power consumption. The resolution (SNDR) of this prototype is limited by nonlinearity, which originates from different sources including the low-pass filter, DAC, and on-chip transconductance stage (which is only implemented for measurement purposes). The nonlinearities introduced by each source combine, which eventually limits the overall SNDR. Additional optimizations of both the low-pass filter and DAC in order to linearize the response and limit the distortion of the signal are possible. Implementing a fully-differential topology would further improve the performance of the presented prototype. Future work will also include using digitally assisted and digitally calibrated circuits to limit the nonlinearity and improve the resolution. Therefore, digital calibration can additionally boost the performance of the presented subthreshold current-sensing technique.

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REFERENCES

1. Steadman R, Hosticka BJ, *et al.* A high dynamic range current-mode amplifier for computed tomography. *IEEE Journal of Solid-State Circuits (JSSC)* 2006; **41**:1615–1619.
2. Kim H-S, Cho G-H, *et al.* An asynchronous sampling-based 128×128 direct photon-counting x-ray image detector with multi-energy discrimination and high spatial resolution. *IEEE Journal of Solid-State Circuits (JSSC)* 2013; **48**:541–558.
3. Szelezniak MA, Himmi A, *et al.* Current mode monolithic active pixel sensor with correlated double sampling for charged particle detection. *IEEE Sensors Journal* 2007; **7**:137–150.
4. Levine PM, Shepard KL, *et al.* Active CMOS sensor array for electrochemical biomolecular detection. *IEEE Journal of Solid-State Circuits (JSSC)* 2008; **43**:1859–1871.
5. Philipp RM, Etienne-Cummings R, *et al.* Linear current-mode active pixel sensor. *IEEE Journal of Solid-State Circuits (JSSC)* 2007; **42**:2482–2491.
6. Woo DH, Lee HC, *et al.* Current input extended counting ADC with wide dynamic range for LWIR FPAs. *IEEE Sensors Journal* 2009; **9**:441–448.
7. Murari K, Etienne-Cummings R, *et al.* Which photodiode to use: a comparison of CMOS-compatible structures. *IEEE Sensors Journal* 2009; **9**:752–760.
8. Guan JG, Zhang QJ, *et al.* Impedimetric biosensors. *Elsevier Journal of Bioscience and Bioengineering* 2004; **97**:219–226.
9. Pierret RF. Semiconductor Device Fundamentals. Addison-Wesley Reading: MA, 1996.
10. Ferrari G, Sampietro M, *et al.* Transimpedance amplifier for high sensitivity current measurements on nanodevices. *IEEE Journal of Solid-State Circuits (JSSC)* 2009; **44**:1609–1616.
11. Sharma A, Ayazi F, *et al.* A 104-dB dynamic range transimpedance-based CMOS ASIC for tuning fork microgyroscopes. *IEEE Journal of Solid-State Circuits (JSSC)* 2007; **42**:1790–1802.
12. Porrazzo S, Cantatore E, *et al.* A design methodology for power-efficient reconfigurable SC $\Delta\Sigma$ modulators. *Wiley International Journal of Circuit Theory and Applications* 2014. DOI: 10.1002/cta.1992
13. Zarifi MH, Judy JW, *et al.* A low-power small-area 10-bit analog-to-digital converter for neural recording applications. *Wiley International Journal of Circuit Theory and Applications* 2011; **39**:385–395.
14. Sohrabi Z, Yavari M. A 13-bit 10 MHz bandwidth MASH 32 $\Delta\Sigma$ modulator in 90 nm CMOS. *Wiley International Journal of Circuit Theory and Applications* 2013; **41**:1136–1153.
15. Poulton K, Heshami M, *et al.* A 4G samples/s 8b ADC in 0.35 μm CMOS. *IEEE International Solid-State Circuits Conference (ISSCC)* 2002; **2**:126–434.
16. Yoshii N, Sugimoto Y, *et al.* A current-mode ADC with current exchanging and averaging capabilities by switching the currents and calculating data in the digital domain. *IEEE Custom Integrated Circuits Conference (CICC)* 2007:209–212.
17. Mortezapour S, Lee EKF. A 1-V, 8-bit successive approximation ADC in standard CMOS process. *IEEE Journal of Solid-State Circuits (JSSC)* 2000; **35**:642–646.

18. Song B-S, Gillig SF, *et al.* A 1-V, 6-b 50-Msamples/s current-interpolating CMOS ADC. *IEEE Journal of Solid-State Circuits (JSSC)* 2000; **35**:647–651.
19. Li Y, Sanchez-Sinencio E. A wide input bandwidth 7-bit 300-MSample/s folding and current-mode interpolating ADC. *IEEE Journal of Solid-State Circuits (JSSC)* 2003; **38**:1405–1410.
20. Zhang C, Shao Z. Analysis and simulation of distributed T/H with averaging technique in folding and interpolating A/D converters. *Wiley International Journal of Circuit Theory and Applications* 2010; **38**:901–933.
21. Ortmanns M, Manoli Y, *et al.* A continuous-time sigma-delta modulator with switched capacitor controlled current mode feedback. *IEEE European Solid-State Circuits Conference (ESSCIRC)* 2003:249–252.
22. Lee S-Y, Cheng C-J. A low-voltage and low-power adaptive switched-current sigma-delta ADC for bio-acquisition microsystems. *IEEE Transactions on Circuits and Systems-I: Regular Papers* 2006; **53**:2628–2636.
23. Sung G-M, Hsieh H-Y, *et al.* Mixed-mode chip implementation of digital space SVPWM with simplified-CPU and 12-bit 2.56 Ms/s switched-current delta-sigma ADC in motor drive. *IEEE Transactions on Power Electronics* 2012; **27**:916–930.
24. Tanifuji S, Tsubouchi K, *et al*. High sampling rate 1 GS/s current mode pipeline ADC in 90 nm Si-CMOS process. *2011 IEEE MTT-S International Microwave Workshop Series on Intelligent Radio for Future Personal Terminals (IMWS-IRFPT)*, August 2011; pages 1–4.
25. Nomura M, Hagihara Y, *et al.* Delay and power monitoring schemes for minimizing power consumption by means of supply and threshold voltage control in active and standby modes. *IEEE Journal of Solid-State Circuits (JSSC)* 2006; **41**:805–814.
26. Straayer MZ, Perrott MH. A 12-bit, 10-MHz bandwidth, continuous-time ΣΔ ADC with a 5-bit, 950-MS/s VCO-based quantizer. *IEEE Journal of Solid-State Circuits (JSSC)* 2008; **43**:805–814.
27. Charlon O, Redman-White W. Ultra high-compliance CMOS current mirrors for low voltage charge pumps and references. *IEEE European Solid-State Circuits Conference (ESSCIRC)* 2004:227–230.
28. Tajalli A, Vittoz E, *et al.* Subthreshold source-coupled logic circuits for ultra-low-power applications. *IEEE Journal of Solid-State Circuits (JSSC)* 2008; **43**:1699–1710.
29. Enz C, Vittoz E. Charge-based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design. Wiley: New York, 2006.
30. Tajalli A, Leblebici Y. Subthreshold current-mode oscillator-based quantizer with 3-decade scalable sampling rate and pico-ampere range resolution. *IEEE European Solid-State Circuits Conference (ESSCIRC)* 2010:174–177.
31. McNeill J. Jitter in ring oscillators. *IEEE Journal of Solid-State Circuits (JSSC)* 1997; **32**:870–879.
32. Hajimiri A, Lee TH, *et al.* Jitter and phase noise in ring oscillators. *IEEE Journal of Solid-State Circuits (JSSC)* 1999; **34**:790–804.
33. Seevinck E, Vittoz E, *et al.* CMOS translinear circuits for minimum supply voltage. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 2000; **47**:1560–1564.
34. Seevinck E. Companding current-mode integrator: a new circuit principle for continuous-time monolithic filters. *IEEE Electronics Letters* 1990; **26**:2046–2047.
35. Dhanasekaran V, Pankratz EJ, *et al.* A continuous time multi-bit ΔΣ ADC using time domain quantizer and feedback element. *IEEE Journal of Solid-State Circuits (JSSC)* 2011; **46**:639–650.
36. Matsukawa K, Matsuzawa A, *et al.* A fifth-order continuous-time delta-sigma modulator with single-opamp resonator. *IEEE Journal of Solid-State Circuits (JSSC)* 2010; **45**:697–706.
37. Anderson M, Sundstrom L. Design and measurement of a CT ΔΣ ADC with switched-capacitor switched-resistor feedback. *IEEE Journal of Solid-State Circuits (JSSC)* 2009; **44**:473–483.
38. Dorrer L, Hartig T, *et al.* A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13 µm CMOS. *IEEE Journal of Solid-State Circuits (JSSC)* 2005; **40**:2416–2427.
39. Kappes MS. A 2.2-mW CMOS bandpass continuous-time multibit Δ–Σ ADC with 68 dB of dynamic range and 1-MHz bandwidth for wireless applications. *IEEE Journal of Solid-State Circuits (JSSC)* 2003; **38**:1098–1104.
40. Ueno T, Itakura T, *et al.* A 0.9 V 1.5 mW continuous-time ΔΣ modulator for WCDMA. *IEEE International Solid-State Circuits Conference (ISSCC)* 2004:78–514.
41. Philips K, Torralba A, *et al.* A 2 mW 89 dB DR continuous-time ΣΔ ADC with increased immunity to wide-band interferers. *IEEE International Solid-State Circuits Conference (ISSCC)* 2004:86–515.

DOI: 10.1002/cta