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A Versatile 1.4-mW 6-bits CMOS ADC for Pulse-Based UWB Communication Systems

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Abstract: An Analog to Digital Converter (ADC) using the low duty-cycle nature of pulse-based Ultra Wide-Band (UWB) communications to reduce its power consumption is proposed. Implemented in CMOS 180 nm technology, it can capture a 5 ns window at 4 GS/seach 100 ns, which corresponds to the acquisition of one UWB pulse at the pulse repetition rate of 10 mega pulses per second (Mpps). By using time-interleaved Redundant Signed Digit (RSD) ADCs, the complete ADC occupies only 0.15 mm^2 and consumes only 1.4 mW from a 1.8 V power supply. The ADC can be operated in two modes using the same core circuits (operational transconductance amplifier, comparators, etc.). The first mode is the standard RSD doubling mode, while the second mode allows improving the signal-to-noise ratio by adding coherently the transmitted pulses of one symbol. For example, for audio applications, a 300 kbps data rate and processing gain up to 15 dB can be achieved at a clock frequency of 10 MHz.

Key words: Analog-to-Digital conversion (ADC), redundant signed digit (RSD), impulse radio (IR), ultra wide band (UWB), CMOS.

1. Introduction

There has been recently a lot of interest for low-cost, low-power solutions short range wireless communications for applications such as body area networks or binaural hearing aids [1-3]. The ADC presented in this paper is designed for the system architecture published in [4], which allows reducing the receiver's complexity and power consumption with regard to a direct-conversion receiver. This system architecture is based on the transmission of Ultra Wide-Band (UWB) pulses and has been conceived to operate in three scenarios presented in Table 1. The corresponding specifications of the ADC have been derived as 4-6-bit resolution with input bandwidth of 1 GHz and sampling frequency of 2-4 GS/s. Due to the large bandwidth of the UWB signals, the ADC is one of the receiver's most critical circuit, and the subject of this paper.

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2. ADC Architecture

Time-Interleaved (TI) cyclic ADCs are ideally suited for high-speed, medium resolution applications which have low-power constraints [5]. Also, cyclic ADCs occupy a minimal area by reusing the same circuits for each conversion cycle. Moreover, the Redundant Signed Digit (RSD) architecture allows relaxing the comparators' accuracy, which in turn reduces the ADC's power consumption significantly. Based on these facts, and considering the specific UWB applications considered in this paper, a TI-RSD architecture has been chosen for the ADC.

The proposed ADC is shown in Fig. 1 and is composed of 20 TI ADC cells. Each cell consists of a RSD ADC [6] and few logics. In this implementation, the ADCs are operated at the master clock's (MCLK) frequency and the interleaving time between the ADC cells is set by a voltage controlled delay line (VCDL).

Table 1 Three communication scenarios considered and their respective requirements.

Parameter	Unit	Scenario		
		1	2	3
Number of simultaneous users		10	1	10
Data rate	kbps	300	50-300	1-50
Distance	m	10	1	< 1
Power consumption	mW	10	1-2	1

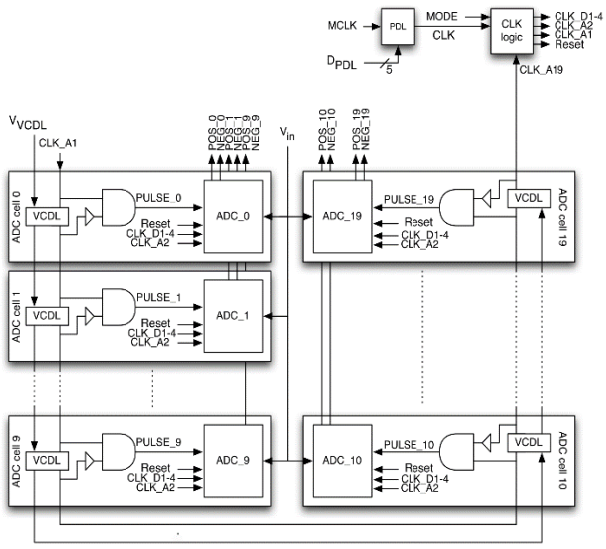

Fig. 1 Top level view of the ADC architecture.

The VCDL is composed of four cascaded inverters which are controlled by a control voltage to generate the desired delay. The nominal delay of the VCDL is 250 ps, allowing capturing a 5 ns window at 4 GS/s, as illustrated in Fig. 2.

A synchronization process is required for the ADC to find the position of the first pulse. During synchronization, a Programmable Delay Line (PDL) is used to delay the acquisition window by 2.5 ns increments until a pulse is found (Fig. 2 (a)-(d)). When the considered transmitter and receiver are synchronized, some of the 20 ADC cells may be turned off, depending on the duration of the considered pulse as well as the sampling rate (or time delay generated by VCDL), in order to further reduce the receiver's power consumption.

3. ADC Cell Architecture and Operation Modes

The RSD ADC architecture implemented in this work is represented in Fig. 3. It is based on the algorithm proposed in [7] and is composed of two track-and-hold stages (T/H_1 : M1-M3, C1 and T/H_2 : M4-M7, C2), one integrator (Operational Transconductance Amplifier (OTA), C3, M8), two clocked comparators and few logics. The offset logic adds, depending on POS/NEG value, a voltage offset equal to -FSR/2, 0 or FSR/2 to the signal, where FSR is the ADC's Full Scale Range voltage.

The ADC can be operated in two modes, a doubler mode and an adder mode. The doubler mode is the standard mode of operation of RSD ADCs in which the signal is sampled once and to reach n-bit of resolution, $n-1$ cycle of operations are needed. The adder mode is taking advantage of the pulse repetitions (within one symbol) available in low data-rate pulse-based UWB

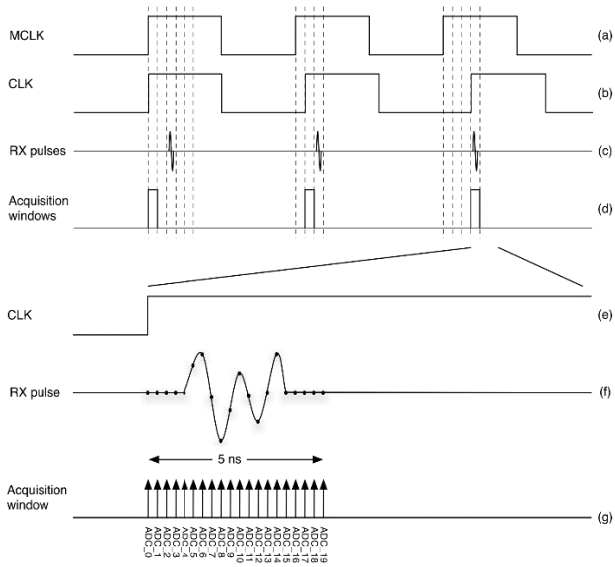

Fig. 2 (a)-(d) synchronization procedure, (e)-(g) zoom on an acquisition window.

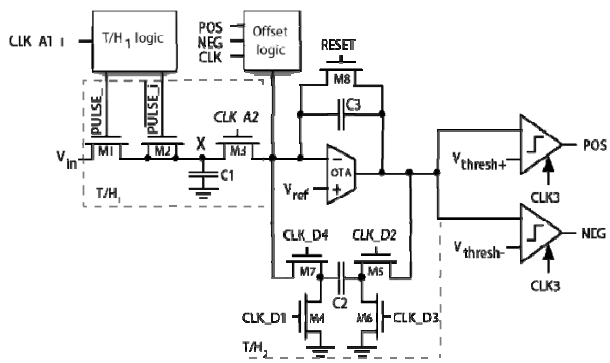

Fig. 3 Simplified schematic of the proposed RSD ADC.

communication systems [8-9] , in which, a single bit of information can be transmitted using multiple pulses.

3.1 Doubler Mode of Operation

In doubler mode, the ADC operates as a standard RSD ADC. During the initial 250 ps of the first half clock cycle, the signal is sampled by T/H_1 and the value of the integrator is reset. During the second half of the first clock cycle, the charge on C1 is transferred on C3. The resulting voltage is then compared with two threshold voltages, $V_{thresh+}$ and $V_{thresh-}$. During the following clock cycles, T/H_1 is inactive. Instead, T/H_2 is used to replicate the voltage at the output of the OTA to its input. Also, depending on the result of the comparison, a voltage offset of -FSR/2, 0 or +FSR/2 is added at the input of the integrator. In this mode of the ADC, $n-1$ cycles are required to provide a resolution of n bits. Therefore T/H_1 stays inactive for $n-1$ clock cycles. However the error sampled during the first half clock cycle is doubled at each clock cycle.

3.2 Adder Mode of Operation

In the adder mode, the signal is sampled by T/H_1 during the initial 250 ps of each clock cycle. Then the charge on C1 is transferred on C3 during the second half of each clock cycle. The replication module is inactive in this mode. Therefore, in order to achieve a resolution of n bits, 2^{n-1} instead of $n-1$ clock cycles are required. Hence the same symbol should be transmitted 2^{n-1} times and captured 2^{n-1} times by T/H_1. As a consequence, the maximum achievable data rate is reduced by 2^{n-1}. However, this mode also allows achieving a processing gain equal to $10\log(2^{n-1})$, which is of great help due to the limited transmitted power and the important Path Loss (PL) encountered by the UWB pulses when they propagate from a distant transmitter to the receiver. For example, for a carrier frequency of 5.5 GHz, 0 dBi antennas and a communication distance of 10 m, the PL can be computed using Friis transmission equation as:

$$PL(d) = 10\log_{10}\left(G_{tx}G_{rx}\left(\frac{\lambda}{4\pi d}\right)^2\right) = 67.3\,dB, \quad (1)$$

Where G_{tx} is the transmitter's antenna gain, G_{rx} is the receiver's antenna gain, λ is the signal's wavelength and d is the distance between the transmitter and the receiver. Considering a bandwidth of B_s = 1 GHz for the UWB signal, the maximum transmitted power S_{tx} according to regulations is

$$\begin{aligned} S_{tx} &= -41.3dBm/MHz + 10\log_{10}\left(B_s/1MHz\right) \\ &= -11.3\,dBm, \end{aligned} \quad (2)$$

resulting in a received signal power of:

$$S_{rx} = S_{tx} - PL(10) = -78.6\,dBm \quad (3)$$

At the receiver's antenna, the noise power is:

$$\begin{aligned} N_{ant} &= kTB + 10\log_{10}(B_s) = \\ &-174dBm/Hz + 10\log_{10}(1\text{GHz}) = -84\,\text{dBm}. \end{aligned} \quad (4)$$

Considering a receiver's noise figure (NF) of 6 dB, the receiver's noise power is -78 dBm leading to a Signal-to-Noise Ratio (SNR) of -0.6 dB whereas 7 dB is typically recommended to achieve a 0.1% Bit Error Rate (BER) for the modulation considered in [8].

Clearly, the adder and doubler modes can also be combined to achieve a desired processing gain in a minimum number of clock cycles. One of the strength of this implementation is that it uses the same circuits (OTA, comparators, etc.) for the two modes. The different combinations to achieve a 6-bit resolution as well as the associated processing gain and maximum achievable data rates for a 10 MHz master clock frequency are reported in Table 2Table 2. We can see that for the previous example, configuring the ADC for 8 cycles in adder mode followed by 2 cycles in doubler mode would be sufficient to achieve a larger than 7 dB SNR. The following subsection provides a closer look at the circuits of the ADC cell.

3.3 ADC Cell's Building Blocks

Most of the logic is used to generate non-overlapping control signals for the different switches in the RSD ADC (Fig. 3). Apart from the control signals of the input transistors of T/H_1 (M1, M2), all the control signals of the 20 ADC cells

Table 2 Possible configurations and their respective processing gain and maximum data rate (for a 10 MHz clock frequency).

Config.	Number of cycles					
	Res. bits	Adder mode	Doubler mode	Total	Processing Gain dB	Max. data Rate kpbs
32/0	6	32	0	32	15	312
16/1	6	16	1	17	12	588
8/2	6	8	2	10	9	10000
4/3	6	4	3	7	6	1428
2/4	6	2	4	6	3	1666

aresynchronous. M1's control signal could simply be, for the ith ADC cell, a replica of the master clock delayed by $i \cdot 250$ ps. Instead, It has been preferred to use a 250 ps pulse so that:

(a) The circuit preceding the ADC sees a constant capacitive load equal to C1.

(b) The T/H_1 stage of one ADC cell is not loaded by the T/H_1 stage of the other 19 ADC cells.

(c) The pulses are generated in the ADC cells, as shown in Fig. 1, which allows propagating a 10 MHz clock instead of a 250 ps pulse.

(d) For a given sampling frequency, i.e., for a given pulse spacing, the pulse duration is automatically set to the right value, and vice-versa.

The most challenging specification to achieve for the input track-and-hold (T/H_1) is to charge or discharge the sampling capacitor of T/H_1 by up to the FSR in less than 250 ps. In addition, the ADC's input bandwidth should be larger than 1 GHz. Note that T/H_2 type has a superior performance as compared to T/H_1 type regarding parasitic mitigations due to the symmetry of its circuit; however, it was not possible to implement T/H_1 as T/H_2. This is because T/H_2 samples and changes the polarity of the signal while T/H_1 is required to perform the fast sampling.

Another important design issue is related to the sampling capacitor C1. From a bandwidth, area and FSR point of view, the sampling capacitor's value should be minimized, while from a thermal noise and layout matching point of view, it should be maximized. Considering a tradeoff between these two requirements, we have then determined that, with a small sampling capacitor of 103 fF, a 250 mV_{pp} FSR at 1 GHz bandwidth could be achieved. Note also that the thermal noise contribution from the 103 fF sampling capacitor, kT/C = 200 μV, is negligible considering that one LSB is 3.9 mV (for a 6 bits resolution and 250 mV_{pp} FSR). Due to the ADC's moderate resolution and high-speed, we have decided to embed the sampling capacitors within each ADC cell rather than to use a capacitor array.

The integrator is based on a two-stage symmetrical OTA and has been designed to minimize its power consumption while having sufficient gain to achieve the desired ADC resolution and sufficient phase margin to guarantee stability. The comparators are based on the StrongArm Latch [10] which uses positive feedback rather than cascaded amplifiers and consumes no static power. The comparator is followed by an output latch which conserves the output state until the next clock's falling edge.

4. Experimental Results

The prototype ADC has been fabricated in 180 nm CMOS technology along with a LNA, mixer and VCO as a full UWB receiver chip. The die photography of the UWB receiver is shown in Fig. 4. The ADC cells are arranged in two rows separated from the analog signals and surrounded by the digital ones. For testing, the die has been wire bonded on a test PCB for measurements. The peak Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are 0.15 LSB and -1.0 LSB, respectively. Since the ADC is operating during 5 ns windows, computing the Fast Fourier Transform (FFT) of the signal measured at the ADC's output is not directly possible. Instead, its Signal-to-Noise

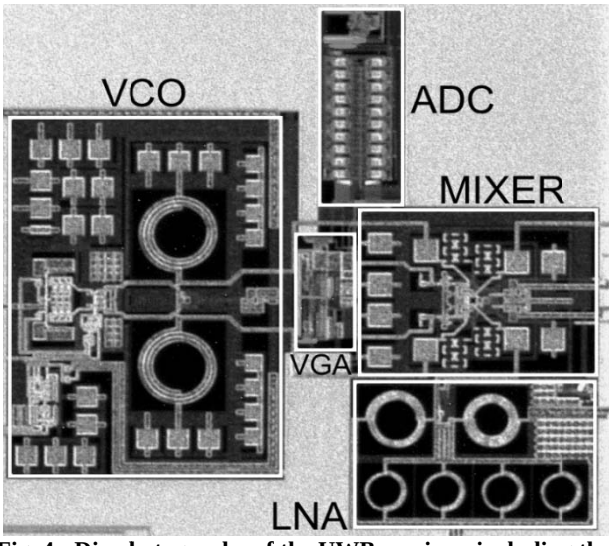

Fig. 4 Die photography of the UWB receiver, including the LNA, mixer, VCO and ADC.

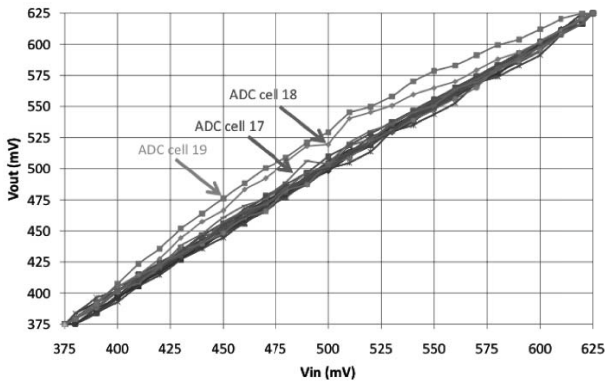

Fig. 5 Measurement of the static performance of the 20 time-interleaved RSD ADCs.

and Distortion Ratio (SNDR) has been evaluated from its INL and DNL to be 36 dB, leading to an Effective Number of Bits (ENOB) of 5.7-bit.

The measured input bandwidth is 900 MHz, which is slightly below the 1 GHz desired bandwidth. This difference is attributed to the impedance of the switches used to route the ADC's input to an external connector for testing, as well as to the parasitics of the bondwires. The outputs of the 20 ADC cells measured for an input signal consisting of a DC voltage source swept over the ADC's FSR, are reported in Fig. 5. The offset and gain error of each ADC has been corrected in the digital domain. As we can see, the performances of the last three ADC cells (in particular ADC cells 18-19) are degraded with regard to the other cells. This can be due to the fact that CLK_A1 skew accumulates and increases by passing through the VCDL of each ADC cell and since this clock is used to generate the sampling clock of 250 ps, its skew can directly affect the performance of each ADC cell, especially the last ones (ADC cell 18-19). Furthermore, CLK_A1 after passing through the ADC cell 19 is fed back into the logic to generate the reset signal, which loads ADC cell 19 and causes an extra skew on its 250 ps pulse.

The measured peak power consumption P_c of the complete ADC operating in the 32/0 configuration is 1.4 mW which corresponds to a data rate of 300 kbps. For the lower data rates in the other scenarios, the ADC would be turned off during longer period of times, resulting in a reduction of the averaged power consumption. The resulting averaged power consumptions, in the different configurations and for different data rates, are reported in Table 3. The performances of the ADC when operated in burst mode are summarized in Table 4. Since the ADC is designed to operate in burstmode, it is not possible to compare the numbers in Tables 3-4 directly to prior art. Indeed, we should consider the number of additional ADC cells required to sample continuously at 4 GS/s and adjust the power consumption accordingly. The ADC samples for 5 ns and the clock period is 100 ns so 19 more ADCs are required to make continuous sampling

Table 3 Power consumption in the different configurations for data rates of 1, 50 and 300 kpbs.

Configuration adder/doubler	Power consumption [μW]			
	@300 kbps	@50 kbps	@1 kbps	Processing Gain [dB]
32/0	1400	233	4.7	15
16/1	714	119	2.4	12
8/2	420	70	1.4	9
4/3	294	49	1.0	6
2/4	252	42	0.8	3

Table 4 Performances of the ADC in burst mode.

Parameter	Unit	Value
Resolution	bits	6
Technology	nm	180
FSR	mV_{pp}	250
Sampling Frequency	GS/s	4
Input bandwidth	GHz	0.9
DBL	LSBs	0.15
INL	LSBs	-1.0
ENOB	Bits	5.7
Active area	mm^2	0.15

Table 5 Performances of the ADC in continuous mode and comparison with state of the arts.

Parameter	Unit	This work	[11]	[12]	[13]	[14]
Type		RSD	SAR	Flash	Flash	Flash
Technology	nm	180	130	65	32-SOI	40
Resolution	bits	6	6	4	6	7
Conversion rate	GS/s	4	1.25	7.5	5	2.2
Supply voltage	V	1.8	1.2	1.1	0.85	1.1
Power	mW	28	32	52	8.5	27.4
INL	LSBs	0.15	NA	0.38	0.37	1
DNL	LSBs	-1.0	NA	0.35	0.52	0.6
FOM	pJ/conv.	0.14	0.4	0.50	0.059	0.2
Active area	mm^2	3.0	0.09	0.01	0.02	0.052

at 4 GS/s. Therefore:

$$FOM = \frac{P_c}{2^{ENOB} f_s} = \frac{2 \times 1.4mW}{2^{5.7} \times 4GHz} = 0.135 pJ / conv. \quad (5)$$

The performances of the ADC are adjusted, to allow fair comparison with prior art ADCs operating in continuous mode, and reported in Table 5. As we can see, despite using an older technology, the achieved FOM is smaller than the best FOM reported in Table 5 except [13] which uses 32 nm CMOS SOI technology. Currently, the area is larger than [11-14], due to the fact that we have considered that 20 times the active area reported in Table 4 Table 4would be required to sample continuously at 4 GS/s. In reality, if continuous sampling was the aim, an analysis would be performed to find the optimal balance between the master clock's frequency and the number of ADC cells required. Also, the use of a newer technology as well as smaller sampling capacitors may help to reduce the area by a great extent.

5. Conclusions

An ADC based on TI-RSD ADC cells has been proposed for pulsed-based UWB communications. The cyclic nature of the RSD ADC allows reducing the size of each ADC cell, while the RSD algorithm allows relaxing the comparators accuracy, which in turn allows reducing the power consumption. Interleaving 20 RSD ADC cells by 250 ps allows achieving sampling rates up to 4 GS/s during 5 ns, while only consuming a peak power of 1.4 mW and occupying an area of 0.15 mm^2.

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