Organic thin-film transistors: from technologies to circuits

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[2] Network of Excellence, 2010-2013, grant agreement n°247745, http://www.noe-flexnet.eu

[3] Performance of Organic Materials tor Mobile Electronics, 2010-2012, project n°10788, http://www.aramis.admin.ch/Default.aspx?page=Texte&ProjectID=27488

[4] SWiss Precision Electronic GRAvure PrintEr, 2012-2013, project n°13596, http://www.aramis.admin.ch/Default.aspx?page=Texte&ProjectID=30832

Abstract

Organic molecules (i.e. carbon-based) have opened a new and rapidly-growing industrial field in the optoelectronic market bringing to this field a new dimension of thinness and flexibility. In this context, this thesis has focused on one particular building block of the vast and emerging field of organic electronics: the organic thin-film transistor (OTFT) which uses organic compounds as semiconductor.

Whereas the OTFT-based circuits are not meant to compete with the silicon-based high-end industry (micro-processors...), their performance have already reached levels enabling their use in potential applications such as displays (e-paper, LCD, OLED) or radiofrequency identification (RFID) tags. The continuously growing number of available organic molecules exhibiting conductive, semi-conductive or insulating properties combined with the number of available deposition/patterning methods (e.g. gravure printing) gives more flexibility to the technology. These additional degrees of freedom raise two main questions: How to identify the most suitable OTFT platform for a given application and how to estimate its potential, as for instance in, of digital circuits? This thesis targets to answer to those questions.

For this purpose, several OTFT platforms have been screened and their performance have been discussed and compared through standard figures of merit. The self-aligned nano-imprinted technology has demonstrated state-of-the-art sub-micrometer OTFTs on 4-inch flexible substrates. This made this platform the most suitable candidate for developing the potential evaluation framework. For that purpose, a static model suitable for the sub-micrometer OTFTs has been developed which embeds almost all known electrical aspects of OTFTs. Then the device-to-device discrepancy often observed in OTFTs has been studied and statistical modeling methods introduced. This allowed the simulation of sub-micrometer inverters performed with commercially available tools. Next, a statistical method has been developed to evaluate the potential of the sub-micrometer OTFTs for digital applications. Whereas the method concludes that these sub-micrometer OTFTs are not mature enough to make complex digital circuits, this methodology is technology-independent and may thus serve as a basis to characterize unipolar-logic printed electronics and be further extended to complementary-logic circuits.

Last but not least, an automation effort has been undergone all along this thesis in order to increase the throughput for such demanding data analysis. The main outcome of this task is a

user-friendly multi-analysis and parameter extraction platform.

Keywords: Self-aligned, Nano-imprint, Sub-micrometer, Organic, OFET, OTFT, Inverter, Ring-oscillator, Design, Characterization, Rise-time, Lifetime, Modeling, g_m/I, Statistical modeling, Corner models, Noise margin, Yield, Technology assessment.

Résumé

Les molécules organiques (à base de carbone) ont ouvert un nouveau domaine industriel en rapide expansion qui procure au marché de l'optoélectronique une nouvelle dimension en termes de finesse et de flexibilité. Dans ce contexte, cette thèse s'est penchée sur un élément clé de ce vaste et émergent domaine qu'est l'électronique organique : le transistor en couches minces organiques (en anglais *Organic Thin-Film Transistor* ou OTFT) qui utilise des molécules organiques pour semiconducteur.

Bien que les circuits à bases d'OTFTs ne soient pas destinés à concurrencer l'industrie du semiconducteur à base silicium (micro-processeurs), leurs performances ont déjà atteint des niveaux permettant leur utilisation dans de potentielles applications telles les écrans (papier électronique, LCD, OLED) ou les puces radiofréquences d'identification (RFID). La croissance continue du nombre de molécules organiques disponibles démontrant des propriétés conductrices, semi-conductrices ou isolantes combinée au nombre de procédés de déposition/structuration disponibles (e.g. l'impression par gravure) donne plus de flexibilité à la technologie. Ces degrés de liberté additionnels conduisent à deux questions : Comment identifier la meilleure platforme d'OTFT pour une application donnée et comment estimer son potentiel, par exemple, au sein de circuits numériques ? Cette thèse a pour objectif de répondre à ces questions.

Pour cela, plusieurs platformes d'OTFTs ont été testées et leurs performances ont été discutées et comparées à partir de facteurs de mérite standards. La technologie par nano-impression auto-alignée a permis de faire la démontration d'OTFTs sub-micrométriques sur substrats flexibles de 4 pouces. Ceci a fait de cette platforme la plus appropriée pour développer le cadre d'évaluation de potentiel. Dans ce but, un modèle statique convenant aux OTFTs sub-micrométriques et incorporant la plupart des aspects connus des OTFTs a été développé. Dans un second temps, la disparité de composant à composant souvent observée chez les OTFTs a été étudiée et des méthodes de modélisation statistiques ont été introduites. Ceci a permis de simuler des inverseurs sub-micrométriques sur des logiciels commerciaux. Puis, une méthode statistique a été développée afin d'évaluer le potentiel des OTFTs sub-micrométriques pour des applications numériques. Bien que la méthode conclue que ces OTFTs sub-micrométriques ne soient pas encore assez matures pour réaliser des circuits numériques complexes, cette méthodologie est indépendante de la technologie et pourra ainsi servir de base pour caractériser l'électronique imprimée à logique unipolaire et être étendue aux circuits à logique

complémentaire.

Enfin un effort d'automatisation a été poursuivi tout au long de cette thèse dans le but d'augmenter la productivité du traitement de données. Le principal aboutissement de cette tâche se présente sous la forme d'une plateforme conviviale d'analyses multiples et d'extraction de paramètres.

Mots-clés : Auto-aligné, Nano-imprimé, Sub-micromètre, Organique, OFET, OTFT, Inverseur, Oscillateur en anneau, Design, Caractérisation, Temps de montée, Durée de vie, Modélisation, g_m/I, Modélisation statistique, Modèles de gabarit, Marge de bruit, Rendement, Validation de technologie.

Contents

Introduction

Organic electronics, market, roadmap

Organic i.e. carbon-based molecules have opened a new and rapidly-growing industrial field in the optoelectronic market bringing to this field a new dimension of thinness and flexibility. Nowadays the most mature active component is the organic light-emitting diode (OLED). OLEDs have been massively released in portable displays such as smartphones (Google Nexus One and Samsung Galaxy S I in 2010) and more recently in 55”-large curved televisions (LG 55EA980V in 2013). Knowing that only five years beforehand the first OLED TV released (Sony XEL-1 in 2008, in Japan only) was 11”-large and had four times less pixels illustrates the rapid progress rate of this field.

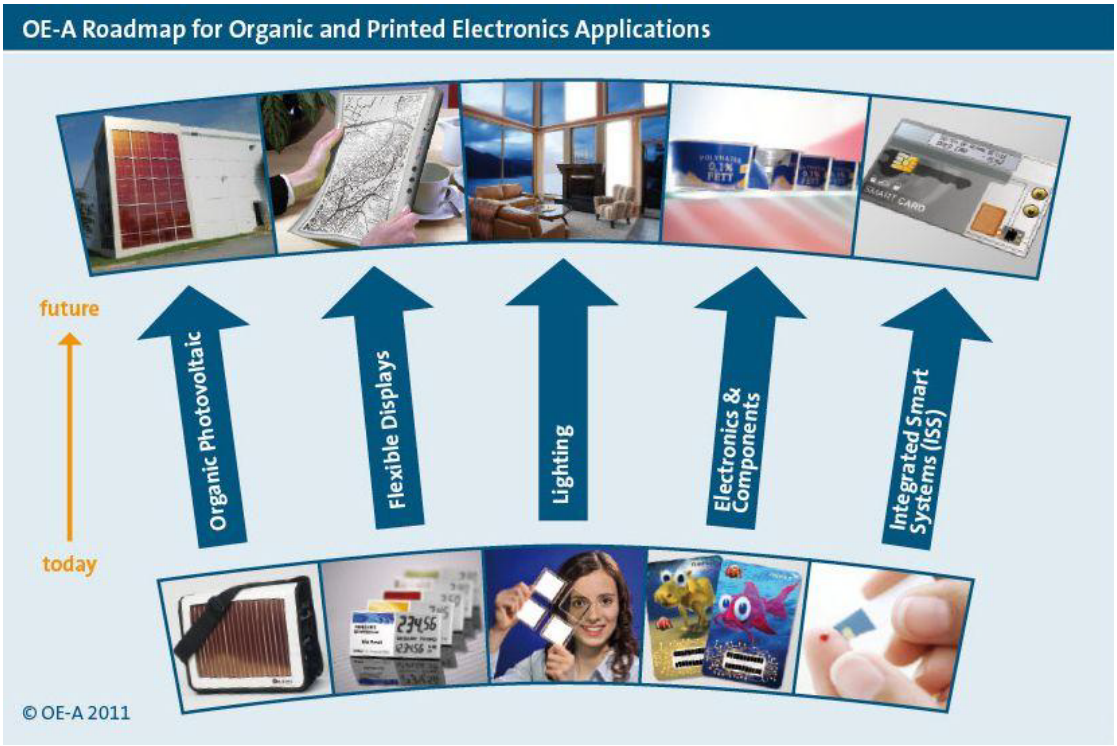


Figure 1: OE-A roadmap 2011 for organic and printed electronics. Forecast from existing devices towards future applications for the five main clusters. Adopted from [1].

In 2011 five main clusters of organic electronics applications were identified by the *Organic and Printed Electronics Association* (OE-A[5]). These clusters are: organic photovoltaic, flexible displays, lighting, electronics & components and integrated smart systems. Their current status and vision are shown in Figure 1 while their corresponding roadmaps are illustrated in Figure 2. The OE-A represents the entire value chain of this emerging industry from universities, institutes, companies to major shareholders, and can thus be seen as the organic/printed equivalent of the *International Technology Roadmap for Semiconductors* (ITRS).

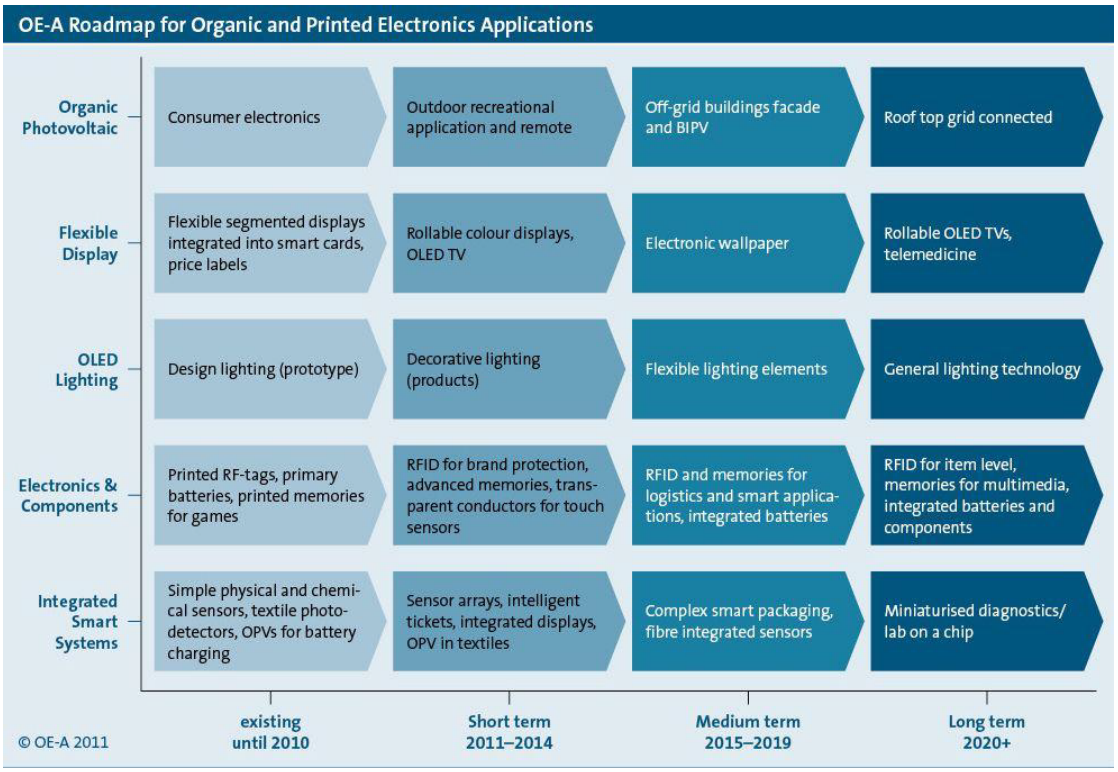


Figure 2: OE-A roadmap 2011 for organic and printed electronics, with forecast for the market entry in large volumes (general availability) for the different applications. Adopted from [1].

In parallel, IDTechEx [2] expects that the total market for printed, flexible and organic electronics will grow from $16.04 billion in 2013 to $76.79 billion in 2023, as depicted in Figure 3.

Three clusters among the five identified by the OE-A, namely Flexible Displays, Electronic & Components and Integrated Smart Systems, can embed transistors i.e. the basic electronic building block. Thus this thesis will focus on organic field-effect transistors (OFET), also known as organic thin-film transistors (OTFT), which use organic compounds instead of silicon as semiconductor.

Ever since the first OTFT were reported, the interest in this field has steadily risen. Indeed

[5] http://www.oe-a.org

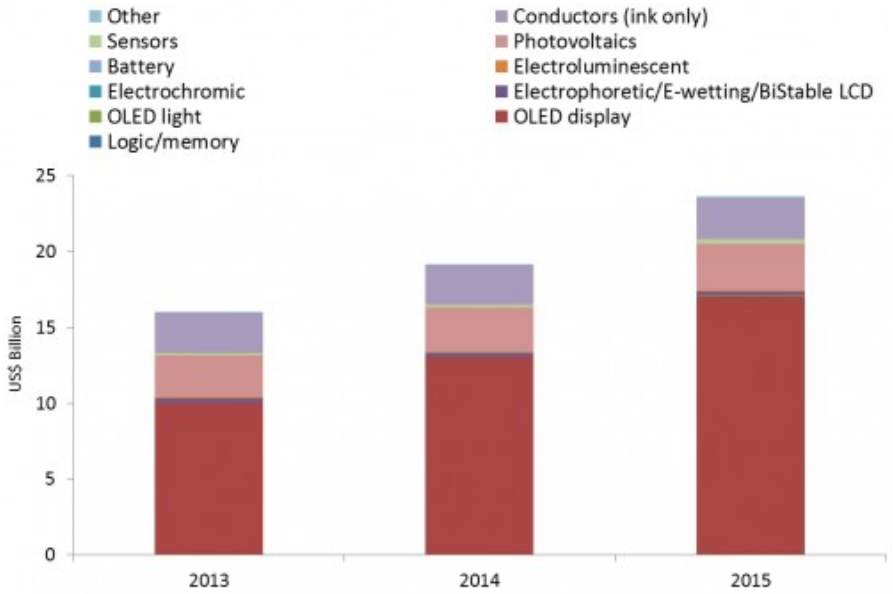


Figure 3: Market forecast by component type in US$ billions. Adopted from [2].

organic semiconductors allow producing low-cost and flexible circuits through the combination of low temperature processing – thus compatible with flexible substrates such as plastic foils or paper including bank notes [3] – and high-throughput fabrication techniques such as roll-to-roll. Among the applications embedding OTFTs reported so far, the three clusters mentioned before can be detailed as follows: active matrix as backplane in flexible (electrophoretic [4] or OLED [5]) displays, see Figure 4, or imagers [6], disposable flexible radio-frequency identification (RFID) tags [7] and analog/digital [8], digital/analog converters [9] or other analog building blocks [10] opening the way to front-end signal processing in smart disposable sensors e.g. for medical diagnostics.

More details about organic electronics in general and its applications can be found in these books [11, 12, 13, 14].

Figure 4: Rollable OLED display driven by OTFT by Sony.

Organic semiconductors and transistors

As for organic conductors, an organic semiconductor (OSC) is a molecular solid built from conjugated molecules. These molecules show an alternation of single and double bonds between carbon atoms. They originate from the sp_2 hybridization of molecular orbitals, depicted in Figure 5. The sp_2 hybridization forms a σ bond accounting for the molecule stability, and a p_z orbital normal to the σ bond. The overlap of p_z orbitals of two nearby molecules provides a π bond whose electrons are able to move under external electric fields giving rise to induced dipoles [15]. This mechanism allows the conjugated molecules to arrange themselves as a molecular solid. The interaction between the organic molecules is of Van der Waals nature, in other words, there exists no tight link as for the covalently bond silicon.

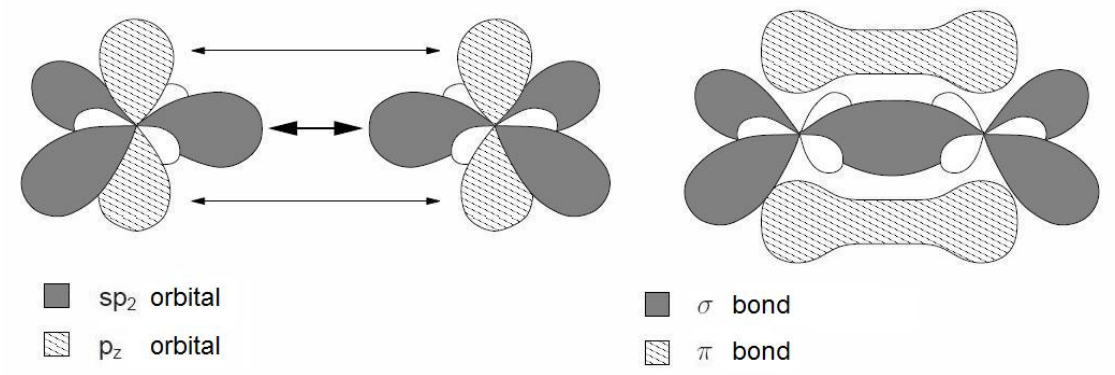


Figure 5: sp_2 hybridization. Adopted from [16].

The electronic structure for hole and electron is referred to as the Highest Occupied Molecular Orbital (HOMO) and the Lowest Unoccupied Molecular Orbital (LUMO) which can be understood as the valence band and the conduction band on the molecular level, respectively [17]. These two bands are separated by an energy gap, see Figure 6.

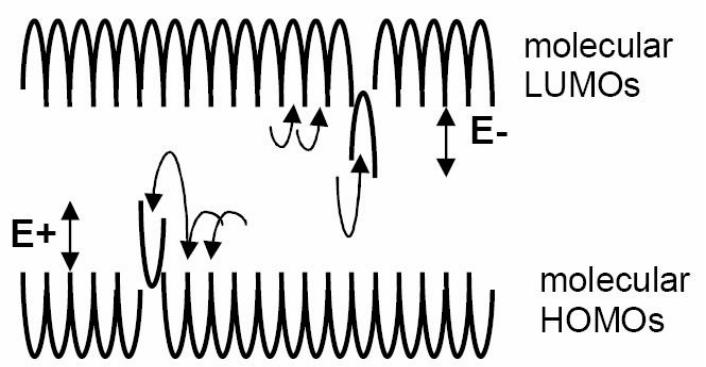


Figure 6: Molecular electronic trap states depicted as quantum-wells; hopping from molecule to molecule; trapping molecule inside the apparent gap, with trap depths E+ for holes and E- for electrons. Adopted from [18].

This band-like approach of the density of states (DOS) and thus its related charge transport model only stands for highly ordered crystalline microstructures e.g. rubrene [19]. Indeed the DOS and the charge transport mechanisms differ a lot depending on the organic semiconductor itself and the interface between the gate dielectric and the semiconductor [20, 21]. Multiple trap and release (MTR) [22], mobility-edge (ME) [23] and variable-range hopping (VRH) [24] are some dedicated and well-accepted charge transport models. Their corresponding mobility models were compared and a link between MTR and VRH was highlighted by Milani et al. [25].

An interesting feature of this class of materials, with respect to highly crystalline semiconductors e.g. silicon, is the temperature-dependency of the charge carrier mobility which depends on the degree of order of the semiconductor. This dependency can be generally seen as twofold:

- Particularly, in model OSCs (single crystal e.g. of rubrene [19]), the charge carrier mobility decreases with increasing temperature. The charge carrier is delocalized over several molecular units, therefore the band-like model describes the transport well [26].
- More generally, in amorphous OSCs, the mean free path of the charge carriers is of the order of an intermolecular distance or less. Therefore, the carrier is localized and hops from one site to the next. The hopping of the carrier depicted in Figure 6 is phonon assisted *i.e.* the transport process is thermally activated thus the charge carrier mobility increases with increasing temperature [17]. This is the main reason why the charge carrier mobility in organic semiconductors is three to five orders of magnitude lower than in crystalline semiconductors.

Another feature of these materials is trapping of the charge carriers which, for simplicity, can be treated as equivalents to electrons and holes: OSCs as the active layer in OFETs exhibit usually p-type conduction. Stable n-type conduction in OFETs is more difficult to obtain [27] but since 2009 n-type semiconductors with sufficiently high performances have been released such as PDI8-CN2 (Polyera's ActivInk™N1200 [28]) and P(NDI2OD-T2) (Polyera's ActivInk™N2200 [29]). This opens the way for the realization of performant organic complementary circuits [10]. Beside p-type and n-type organic semiconductors, an alternative is to use ambipolar materials: they can conduct both type of carriers and, beside ambipolar OTFTs exhibit higher OFF current, air-stable circuits have been demonstrated [30]. This interesting feature has already led to the realization of a promising optoelectronic device: the light emitting transistor (LEFET), reviewed in [31].

Two main organic semiconductors families exist: small molecules and polymers.

Small molecules, such as pentacene, exhibit charge carrier mobilities up to 5.5 cm^2/Vs (for pentacene [32]) and are generally deposited through evaporation. Indeed only few of them are soluble and thus can be solution-processed. State-of-the-art circuits and related models use small molecules and most of the time this is pentacene. Published circuits are rather p-type

only than CMOS because of the lack of performant n-type small molecules. Among the most used evaporated n-type OSCs, one can quote F_{16}CuPc [33] and fullerenes such as C_{60} [34]. The evaporation conditions, such as the evaporation rate, affect the semiconductor morphology and more especially the nano-crystal size which affects the charge transport. Weis et al. [35] demonstrated that smaller grains and thus more grain boundaries increase the presence of traps and decrease the effective mobility.

Polymers, such as poly(3-hexylthiophene) (P3HT), offer in theory an infinite number of possibilities for p-type and n-type semiconductors. They can be solution-processed e.g. inkjet printed [36]. The charge carrier mobilities are generally lower than for small-molecules but they are catching up since their properties are chemically tunable: up to 0.1 cm^2/Vs for P3HT [37] and up to 1 cm^2/Vs for pBTTT[6] [38].

Additionally precursors, such as TIPS-pentacene, can be solution processed [39] and then converted by annealing (around 200°C) to small molecule, here pentacene. Precursors thus combine easy processing of polymers and performances of small molecules. This positive combination can also be obtained with polymer-small molecule blends such as diF-TESADT:PTAA[7] achieving charge carrier mobilities over 2 cm^2/Vs [40].

OFET – MOSFET comparison: state of the art

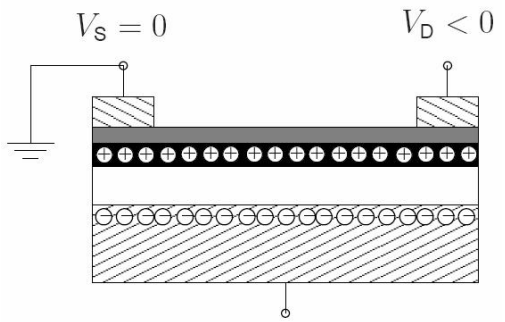
As mentioned before, the main advantage of organic semiconductors against their inorganic counterparts is their low processing temperature required which is typically below 200°C. In comparison the processing temperature of amorphous hydrogenated silicon (a-Si:H) is above 250°C [41].

Performance-wise, OFETs, and more specially polymer-based TFTs, exhibit field-effect mobility (mobility extracted from a transistor) at least three orders of magnitude below the one of inorganic crystalline silicon-based MOSFETs. Nevertheless, today they still compete and even surpass the mobility reported in amorphous hydrogenated silicon (a-Si:H) TFTs [42].

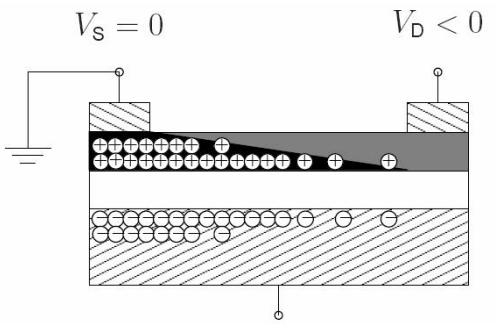
In addition to the molecular order (packing), the field-effect mobility in OTFTs depends on the magnitude of the transversal electrical field [43] (electric field normal to the channel) and eventually on the longitudinal field as well through space-charge limited current and Poole-Frenkel mechanisms [44].

Compared to a MOSFET, an OFET operates in accumulation only. The working principle of an OFET is depicted in Figure 7 and compared to a MOSFET for both linear and saturation regimes. The field-effect mobility is mostly not constant and strongly depends on the gate voltage [45, 43]. Conversely off-currents in OFET are mainly due to bulk current and gate leakage current [46]. The contact resistance is also an inherent limitation to OFETs performances due

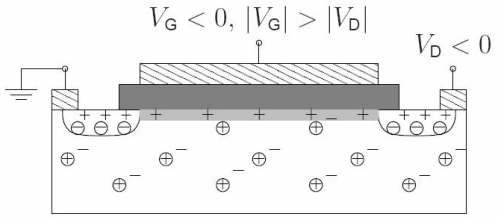
[6] Poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene)
[7] 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene:poly(triarylamine)



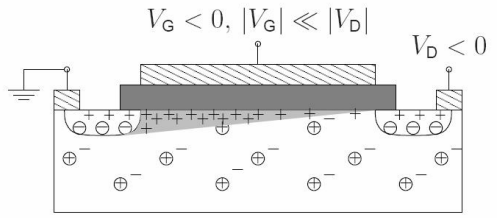
(a) OFET in the linear regime: $V_G < 0$ V, $|V_G| > |V_D|$.



(b) OFET in the linear regime: $V_G < 0$ V, $|V_G| \ll |V_D|$.



(c) MOSFET in the linear regime.

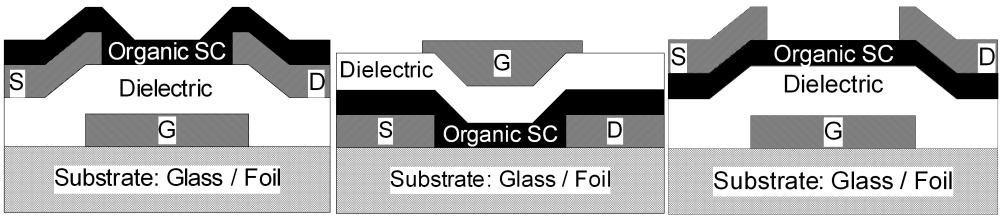


(d) MOSFET in the saturation regime.

Figure 7: OFET (bottom-gate top-contact architecture) and MOSFET working modes. Both devices are in the common source configuration: $V_G = V_{GS}$ and $V_D = V_{DS}$. Adopted from [16].

to the energy mismatch between the organic semiconductor HOMO and the work function of the contact. For instance the P3HT-Au Schottky barrier is about 0.3 eV for the best case [47]. A summary of the main differences between OFETs and MOSFETs is given in Table 1.

Three main architectures can be used for OTFTs as depicted in Figure 8. These can actually be seen as two topologies: coplanar and staggered.



(a) BG-BG. (b) TG-BC. (c) BG-TC.

Figure 8: Main OTFT architectures. From left to right: Bottom-Gate Bottom-Contacts, Top-Gate Bottom-Contacts and Bottom-Gate Top-Contacts.

Coplanar stands for a charge carrier injection from the edges of the source/drain contacts, coplanar to the channel. The so-called bottom-gate bottom-contact (BG-BC) architecture corresponds to this category. The edge injection leads to larger contact resistance because of a smaller injection area. However this architecture has a major advantage: the critical organic

Table 1: OFET – MOSFET comparison

Aspect	MOSFET	OFET
Channel	Inversion	Accumulation
Mobility law	$f(T, V_{\text{channel}})$	$f(T, V_{\text{channel}})$
Bulk contact (B)	Present	N/A
OFF current	Good	Bad
Contact limited	No	Yes
Reproducibility	Excellent	Poor
Hysteresis	None	Possible
Doping	Required	Possible
Printable	Possible	Yes
Flexible	Possible	Yes
Cost	Low/transistor	Low/area

semiconductor layer is deposited as last and is not exposed to chemicals e.g. solvents/developers/acids during the patterning steps (e.g. photolithography) of the underneath layers. This is why the industry, such as Sony [48], adopts this architecture. However an encapsulation is often required to protect the semiconductor from oxygen/moisture.

On the other hand, there are two OTFT architectures which correspond to the staggered category. Here the carrier injection takes place on a larger area but the carriers must now cross the semiconductor layer in order to reach the channel. Thus the related contact resistance can be modeled with the current-crowding concept [49]. The so-called top-gate bottom-contacts architecture (TG-BC) looks more like a traditional MOSFET. Here the semiconductor deposition is the second process step meaning that it has to withstand subsequent steps as well. Note that layers deposited afterward also act as passivation barriers which protect the organic semiconductor. This is currently the most mature architecture for end-user applications. One can quote PolyIC (RFID tags [50]) and PlasticLogic (e-reader [51]).

The second staggered architecture is the so-called bottom-gate top-contacts (BG-TC) which is used in inorganic TFTs (a-Si/H). Here the semiconductor is deposited prior to the last layer, i.e. the S/D contacts, but then their patterning should be withstood. Currently the contacts are deposited through a shadow mask or stencil lithography [52]. Polymer Vision uses this architecture as well as BG-BC [53].

More recently, Polymer Vision has developed a BG-BC enhanced with an additional top-gate known as the back-gate steering technology [54]. This last double gate architecture, where the extra back-gate controls the OTFT threshold voltage, allowed the realization of the most complex organic circuit reported so far: an 8-bit organic microprocessor on plastic foil embedding 3381 OTFTs [55]. This breakthrough demonstrated that organic electronics can provide low-cost computing power to smart objects.

It is however clear that organic electronics is not meant to compete with monocrystalline

silicon on the high-end electronic market such as processors. There are other interesting and emerging technologies competing with organic electronics such as low-temperature polysilicon, nanocrystalline silicon and various metal oxide semiconductors, each with their pros and cons reviewed in [56]. For instance, metal oxide semiconductors have generally higher mobilities than OSCs – from 0.5 [57] to 31 cm^2/Vs [58] for ZnO and 21 cm^2/Vs for IGZO [59] – and transparent flexible IGZO TFTs have been demonstrated [60] but oxide semiconductors are mostly n-type (p-doping has just emerged thus limiting complementary logic) and, compared to organic semiconductors, they suffer from persistent photocurrents [56].

More details about OTFTs and the physics of organic semiconductors can be found in these books [61, 62, 63] and journal reviews [42, 64, 65, 66, 67, 68, 69, 70].

Objectives of this thesis

The main objective of this thesis is to complete the value chain depicted in Figure 9 in order to identify or give the methods to identify pros and cons of several technologies for organic circuits and quantify its potential upon the targeted application (e.g. digital circuits).

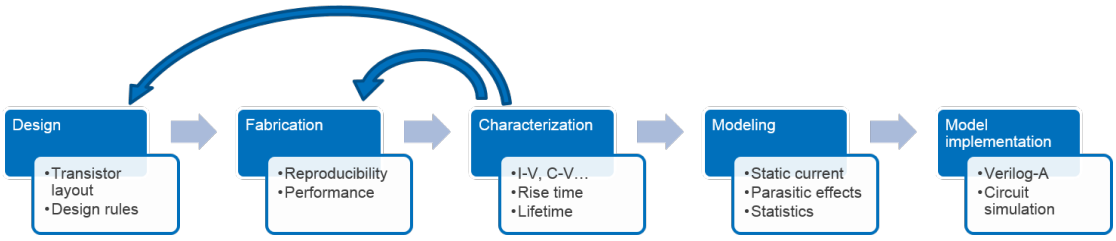


Figure 9: Value chain to be completed

In the first chapter, 10 different organic technologies will be introduced. The related standard static performances will be compared and discussed to identify potential candidates for circuit applications. The two latest OTFT technological platforms reported in this thesis are the self-aligned nano-imprinted sub-micrometer OTFTs from the European Community's Seventh Framework Programme (EU FP7) project POLARIC[8] – experimental data available for CSEM's use in October 2012 – and the gravure-printed OTFTs from the Swiss Commission for Technology and Innovation (CTI) project SWIPEGRAPE[9] – samples fabricated at CSEM in August 2013.

In the second chapter, the different electrical characterization methods which have been used and/or developed to study these technologies will be described. Additional measurements ($C-V$, rise-time, lifetime) will bring new inputs to identify potential technology candidates for circuit applications.

[8] Printable, Organic and Large-Area Realisation of Integrated Circuits, 2010-2014, grant agreement n°247978, http://www.vtt.fi/sites/polaric

[9] SWiss Precision Electronic GRAvure PrintEr, 2012-2013, project n°13596, http://www.aramis.admin.ch/Default.aspx?page=Texte&ProjectID=30832

In the third chapter, more insight will be given to the transistor behavior through modeling different figures of merit such as the OFF current, contact resistances and of course the drain current. A static model combining existing models will be proposed for a broad range of devices including the sub-micrometer OTFTs.

In the fourth chapter, statistical methods will be introduced in order to deal with the large data spread observed in different OTFT technologies. These will include analysis of the g_m/I characteristics, statistical parameter extraction and corner modeling. The latter one will be successfully applied to the self-aligned nano-imprinted sub-micrometer OTFTs.

In the fifth chapter, the current model will be implemented in a commercially available EDA software to simulate inverters and inverter pairs. From these simulations, two approaches – an adaptation of an existing method and the derivation of a new method – will aim to estimate the yield of a given technology in terms of digital circuits. For this purpose, the self-aligned nano-imprinted sub-micrometer OTFTs have been used as a case study.

1 Technologies and designs used for this thesis

1.1 Introduction

In this chapter, the different organic technologies and OTFT test structure designs used for this thesis will be introduced.

They were gathered by application (from material screening to circuits) as well as substrate size and chronology. Indeed the continuous improvement of this fast evolving field was also visible in CSEM's lab all along my Ph.D. contract from 2010 to the end of 2013: in such time frame I started working with 20 mm silicon substrates and ended up with 4 in. plastic foils.

The term "technology" refers in this thesis to a set comprising a given material stack and processing methods i.e. an OTFT platform.

My direct contribution to the different OTFT platforms introduced in this chapter was either the design of the test structures (Sections 1.2.2, 1.4.2, 1.4.3 and 1.4.4), or the sample fabrication (Sections 1.2.1, 1.3.1 and 1.4.1) or both (Sections 1.3.2 and 1.3.3).

Note: The layouts of the test structures for which I did not contribute to are gathered in Appendix A.1.

Next the figures of merit (FoM) used in this thesis to evaluate OTFTs and circuits will be introduced.

1.1.1 OTFT figures of merit

The performances of the OTFTs introduced in this chapter are evaluated using the recommendations from IEEE 1620-2004 [71]. IEEE-1620-2004 is a standard released in 2004 defining ways to extract the figures of merit of OTFTs. Those include the threshold voltage ,V_T, the charge carrier mobility, μ, the ON/OFF ratio ($I_{ON}/I_{OFF} = |I_D(V_{GS,max}, V_{DS,max})|/\min|I_D(V_{DS,max})|$) and

the subthreshold swing[1] ($S = \max|(\partial \log_{10}|I_D(V_{DS,max})|/\partial V_{GS})^{-1}|$).

Mobility and threshold voltage considerations

Depending on the law linking the mobility with the channel potential, μ and V_T can be extracted in the linear or in the saturation regime using Equations 1.1 and 1.2 [71], respectively.

$$\mu_{lin} = \frac{L}{WC_i V_{DS,lin}} \frac{\partial I_D}{\partial V_{GS}} \tag{1.1}$$

In particular, concerning silicon MOSFET, it can be shown that a fairly good relationship is given by:

$$\mu_{sat} = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \tag{1.2}$$

Then the $I_D(V_{GS}, V_{DS,lin})$ versus V_{GS} curve can be fitted to a line whose slope, once injected in Equation 1.1 as $\partial I_D/\partial V_{GS}$, and y-intercept give μ_{lin} and $V_{T,lin}$. This is depicted in Figure 1.1a.

Similarly, assuming the same field-mobility dependence as for silicon MOSFET (which is questionable as seen later), the $\sqrt{I_D(V_{GS}, V_{DS,sat})}$ versus V_{GS} curve can be fitted to a line whose slope, once injected in Equation 1.2 as $\partial \sqrt{I_D}/\partial V_{GS}$, and y-intercept give μ_{sat} and $V_{T,sat}$. This is depicted in Figure 1.1b.

The gate-voltage dependent linear and saturation mobilities shown in this chapter are also extracted according to IEEE 1620-2004: see Equations 1.1 and 1.3, respectively. The g_m extraction method of Equation 1.3 can also linearly fitted to get a constant value.

$$\mu_{gm,sat} = \frac{L}{WC_i(V_{GS} - V_{T,sat})} g_{m,sat}, \text{ with: } g_{m,sat} = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS,sat}} \tag{1.3}$$

Some definitions are however weak to some issues encountered with OTFTs. For example, a too high gate leakage will interfere with the drain current in the linear regime and disturb the linear fit to extract the linear mobility, μ_{lin}. Dominant contact resistances will also disturb the extraction of the linear mobility [43]. Similarly the gate-voltage dependency of the mobility in OTFTs can strongly affect the extraction of the saturation mobility, μ_{sat}. Whereas the fitting range recommended by the IEEE standard is 25%–75%, increasing the fitting range to 50%–100% to focus on the highest part of the curve can sometimes help and it also increases the obtained value for μ_{sat}. I illustrate all these effects on the extraction of [μ_{lin}; $V_{T,lin}$] and [μ_{sat}; $V_{T,sat}$] in Figures 1.1a and 1.1b, respectively.

[1] Also noted *SS* in some chapters.

Other extraction methods exist, reviewed in [72], such as:

- The apparent mobility:

$$\mu_{\text{app}} = \frac{L}{WC_i}\frac{\partial g_{\text{D,lin}}}{\partial V_{\text{GS}}}, \text{ with: } g_{\text{D,lin}} = \left.\frac{\partial I_{\text{D}}}{\partial V_{\text{DS}}}\right|_{V_{\text{DS,lin}}} \tag{1.4}$$

  Then the $g_{\text{D,lin}}$ versus V_{GS} curve can be fitted to a line whose slope and y-intercept give μ_{app} and $V_{\text{T,app}}$. This is depicted in Figure 1.1c. This method was further extended in [43].

- In case of a power law dependence of the mobility with the channel potential, another method known as the H method has been proposed by [73]. In the linear regime one gets:

$$H_{I_{\text{D,lin}}} = \frac{\int_{V_{\text{FB}}}^{V_{\text{GS}}} I_{\text{D,lin}}(v_{\text{GS}})\, dv_{\text{GS}}}{I_{\text{D,lin}}(V_{\text{GS}})} = \frac{V_{\text{GS}} - V_{\text{FB}}}{\gamma + 2} \tag{1.5}$$

  Then the $H_{I_{\text{D,lin}}}$ versus V_{GS} curve can be fitted to a line whose slope and y-intercept give γ and V_{FB} (also noted $V_{\text{T,H,lin}}$). This is depicted in Figure 1.1e. Next $I_{\text{D,lin}}^{\frac{1}{\gamma+1}}$ can be linearly fitted versus V_{GS} giving X = slope and finally $\mu_{\text{H,lin}}(V_{\text{GS}}) = \frac{L}{WC_i}\frac{X}{V_{\text{D,lin}}}(V_{\text{GS}} - V_{\text{FB}})^{\gamma}$ (more details in [73]). A constant value, $\mu_{\text{H,lin}}$, can be obtained with $V_{\text{GS}} = V_{\text{GS,max}}$.

- The H method applied in the saturation regime (details in Section 3.4):

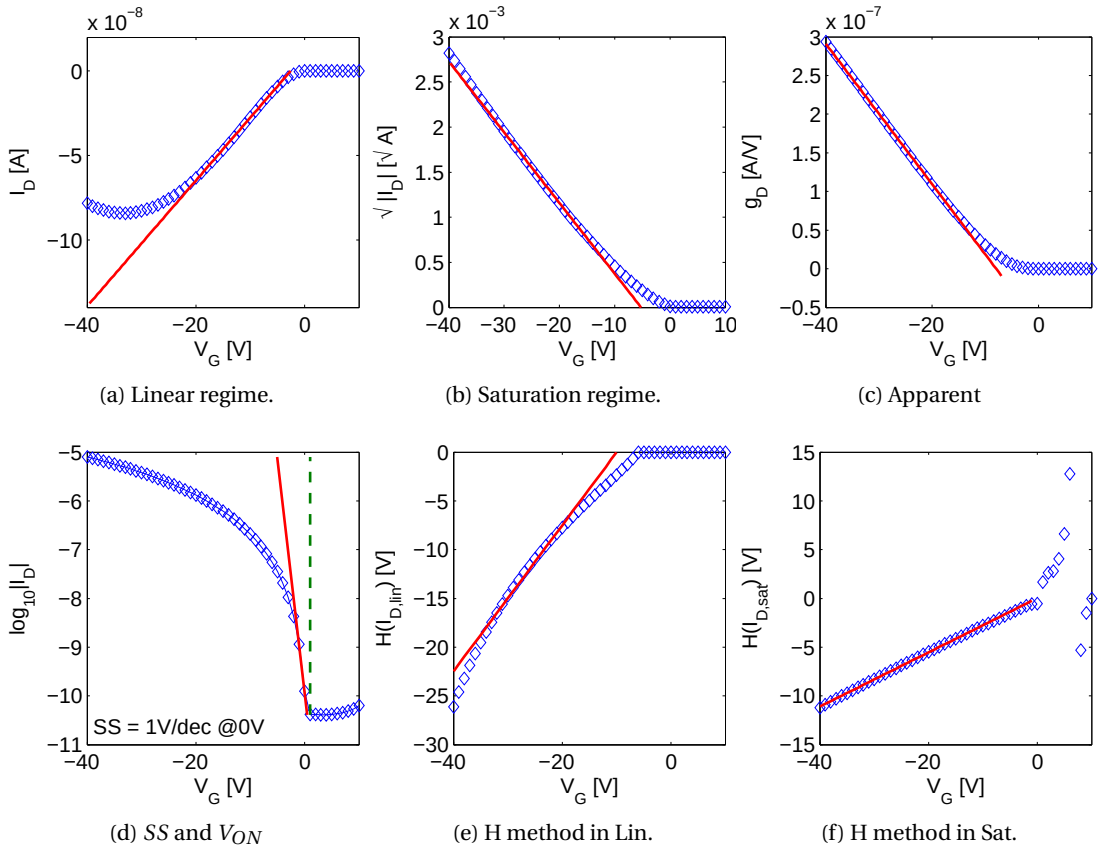
$$H_{I_{\text{D,sat}}} = \frac{\int_{V_{\text{FB}}}^{V_{\text{GS}}} I_{\text{D,sat}}(v_{\text{GS}})\, dv_{\text{GS}}}{I_{\text{D,sat}}(V_{\text{GS}})} = \frac{V_{\text{GS}} - V_{\text{FB}}}{\gamma + 3} \tag{1.6}$$

  γ and V_{FB} (also noted $V_{\text{T,H,sat}}$) are obtained in the same way, depicted in Figure 1.1f. The method to get a constant mobility value μ_0 (also noted $\mu_{\text{H,sat}}$) is detailed in Section 3.4.

Table 1.1: Mobility and threshold voltage obtained from Figure 1.1. Fitting range: 25%–75%

Method	[10^{-3}cm^2/Vs]	[V]
Linear	$\mu_{\text{lin}} = 3.72$	$V_{\text{T,lin}} = -2.58$
Saturation	$\mu_{\text{sat}} = 12.3$	$V_{\text{T,sat}} = -5.22$
Apparent	$\mu_{\text{app}} = 9.09$	$V_{\text{T,app}} = -6.95$
H, lin.	$\mu_{\text{H,lin}} = 3.36$	$V_{\text{T,H,lin}} = -9.97$
H, sat.	$\mu_{\text{H,sat}} = 1.44$	$V_{\text{T,H,sat}} = -0.08$
Other	$\mu_{\text{gm,sat}} = 14.5$	$V_{\text{ON}} = 1.00$

In addition to the several definitions of the threshold voltage given above, a practical one is the turn-on voltage (noted V_{ON} in this thesis) which is defined as the voltage at which the drain current exits the OFF mode and enters the subthreshold regime [74]. It can be extracted by using the maximum value of the second derivative of the drain current in logarithmic scale – as



(a) Linear regime. (b) Saturation regime. (c) Apparent

(d) SS and V_{ON} (e) H method in Lin. (f) H method in Sat.

Figure 1.1: Linear fit results for the different definitions of the mobility and the threshold voltage as well as the subthreshold swing and the turn-on voltage for a TG1 OTFT with W/L = 1 mm/10 μm.

done in Figure 1.1d, this method fails in presence of a noisy signal – or by using a subthreshold regime model, see Section 3.4.3.

For an ideal transistor, all the extraction methods for the mobility and threshold voltage should give the same value but, as shown in Table 1.1, they can vary a lot on a leaky/contact limited OTFT. On the transistor used in Figure 1.1, the obtained value for the mobility varies from 1.44×10^{-3} to 14.5×10^{-3} cm^2/Vs whereas for the threshold voltage the value varies from -9.97 V to 0.30 V (even 1 V if considering V_{ON}.

OTFT figures of merit and methods used in this chapter

In this chapter, the following standard ([71]) OTFT figures of merit are used for benchmarking purpose: the field-effect mobility in saturation (μ_{sat}, with 50%–100% fitting range), the threshold voltage ($V_{\mathrm{T,sat}}$), the ON/OFF ratio and the subthreshold swing (extraction example shown in Figure 1.1d). The normalized ON current: $\|I_{\mathrm{ON}}\| = \frac{L}{WC_i}|I_{\mathrm{ON}}|$ (in A/(F.cm^2)) and the

ON gate/drain current ratio: $I_G(V_{GS,max}, V_{DS,max})/I_{ON}$ are added to assess the current scaling and the impact of the gate leakage, respectively.

In order to compare them, almost all transistors shown in this chapter were measured in the same conditions (see Section 2.2.1) and with the same voltage ranges gathered in Table 1.2. The exception is for those of Section 1.4.3. Any variation on the voltage range used is detailed in the corresponding section.

Table 1.2: Voltage range used in this chapter for the OTFT characterization. Forward and reverse sweeps.

	Gate voltage	Drain voltage
Transfer	$10V > V_{GS} > -30V$, with $V_{step} = -1V$	$-1V > V_{DS} > -30V$, with $V_{step} = -14.5V$
Output	$0V > V_{GS} > -30V$, with $V_{step} = -10V$	$0V > V_{DS} > -30V$, with $V_{step} = -1V$

In order to assess the dynamic performance of OTFTs, the transit frequency, f_T, and the rise-time, t_{rise}, can be used. A rise-time measurement setup was developed and is described in the next chapter but its use was only possible for one technology among the 10 introduced in this chapter – results available in Section 2.5. Therefore t_{rise} is not used in this chapter. Similarly a transit-frequency measurement setup was developed but, at this day, it has not been validated yet. Therefore experimental values of f_T are not available. However an estimation can be obtained using the following expression valid in the saturation regime [75]:

$$f_T = \frac{g_m}{2\pi C_G} \tag{1.7}$$

This is performed at the end of this chapter, in Section 1.5, for comparison purposes.

1.1.2 Inverter figures of merit

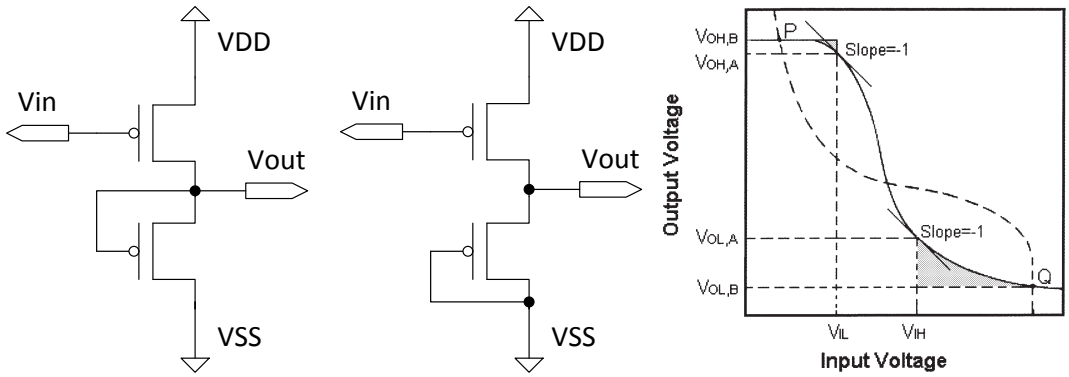
In this thesis, only unipolar logic (p-type) is investigated. The two used inverter topologies are depicted in Figure 1.2. Note: the performance of the so-called zero-V_{GS} topology depends on the current of the load transistor at V_{GS} = 0 V therefore this topology is not suitable to normally-OFF OTFTs.

Concerning the inverters, the main figures of merit are the trip-point voltage, the gain and the noise margins [76, 77].

The trip-point voltage, V_{trip}, is the point at which $V_{IN} = V_{OUT}$ i.e the switching point. Ideally $V_{trip} = V_{DD}/2$, where V_{DD} is the power supply.

The gain is defined as $\max\left|\frac{dV_{OUT}}{dV_{IN}}\right|$. The higher the sharper is the logical ($0 \leftrightarrow 1$) transition and thus the better is the inverter.

The noise margins are the limit voltage at which the input (0 or 1) starts to be wrongly under-



(a) Zero-V_{GS} topology. (b) Diode-connected topology. (c)

Figure 1.2: (a)–(b) Schematics of p-logic inverters. (c) Unity gain noise margin. $V_{SS} < V_{DD} \Leftrightarrow 0 < 1$ logic states.

stood which generates a wrong output. The noise margin for the low input is $NM_L = V_{IL} - V_{OL}$ and for the high input is $NM_H = V_{OH} - V_{IH}$. Different definitions exist for V_{IL}, V_{OL}, V_{OH} and V_{IH} which are reviewed in [76, 77] and two were selected: the unity gain approach and the maximum equal criteria approach (MEC). However only the MEC noise margin will be used in the next chapters.

In the unity gain approach, the two unity gain points (slope of the transfer curve equal to -1) have the following coordinates: (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}), see Figure 1.2c. On the other hand, the MEC noise margin was extracted with the algorithm from [78], see Figure 1.12 for illustration.

1.1.3 Ring-oscillator figures of merit

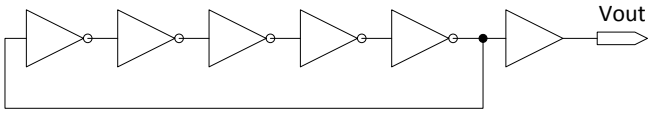


Figure 1.3: Schematic of a 5-stage ring-oscillator.

For oscillators, the oscillation frequency and amplitude are the principal characteristics. However these parameters vary with respect to V_{DD} thus the supply voltage has to be mentioned. Concerning ring-oscillators, the frequency, f, depends in addition on the number of inverter stages, N, thus the stage delay, τ, is an important dynamic figure-of-merit. τ is obtained from f through: $\tau = 1/(2Nf)$.

The buffer output stage of the 5-stage ring-oscillator depicted in Figure 1.3 is either an extra inverter stage (cf. Section 1.4.3) or an external buffer amplifier (cf. Section 1.3.1 with details on the buffer in Section 2.2.1).

Now that the set of figures of merit is defined for the basic building block, the technology screening can start.

1.2 Screening platforms using silicon substrates

In this section, the two first platforms described to make OTFTs are so-called screening platforms because they allow testing different semiconductors. Both use standard silicon wafers with source and drain contacts patterned by photolithography. The back-side of the wafer forms the gate contact which is common to all transistors. Pre-transistors are thus available with well controlled processes in a bottom-gate bottom-contact (BG-BC) architecture. Only one layer is missing to complete the transistor stack: the semiconductor. Thus with these pre-patterned substrates, different semiconductor deposition processes can be compared with each other through the transistor performance parameters. In the example of a spin-coated semiconductor, the spinning conditions (speed, acceleration and duration), the solution parameters (solvent, concentration...), the annealing conditions as well as the effect of dielectric/contact treatments can be screened in order to optimize the device performances.

Such screening can also be done automatically at CSEM thanks to a specific robotized system suitable for OLED, OPV and OTFT [79]. However process optimization was not the target of this thesis.

1.2.1 P3HT-based OTFTs on 20 mm silicon substrate

Process

Highly phosphorus doped silicon wafers (450 μm, 4.5 Ω.cm) with thermally grown silicon dioxide (SiO_2) are used as both substrate and gate dielectric. The thickness of the SiO_2 is 100 nm and its insulator capacitance is C_i = 32.6 nF/cm^2 – details about the capacitance measurement in Section 2.4. The Ti/Au (5 nm/60 nm) source and drain contacts are patterned by photolithography. The back side of the wafer is covered with 1 μm of aluminum to form the common gate contact. This results in a 20 mm large standard test substrate which is actually bought from a silicon fab.

The layout shown in Figure A.1 comprises 16 interdigitated transistors with channel lengths comprised between 4 and 30 μm. Transistors are available in two channel orientations in order to identify any anisotropic conduction behavior caused during the growth of the semiconductor.

After a full cleaning step – sonication in acetone, air plasma, ultra-pure water and isopropanol (IPA) – of the delivered test substrate, a self-assembled monolayer (SAM) is used to passivate the oxide surface: octadecyltrichlorosilane (OTS) deposited by dip-coating. On top of this stack, the organic semiconductor to be deposited is regioregular poly(3-hexylthiophene) (P3HT), chosen for its well-known p-type properties [37]. P3HT has been supplied by Merck®

(Lisicon™ SP001, 10 mg/mL in anhydrous chloroform) and is spin-coated 180 s at 1000 rpm in inert (N_2) atmosphere without further thermal annealing. The simplified process flow is depicted in Figure 1.4.

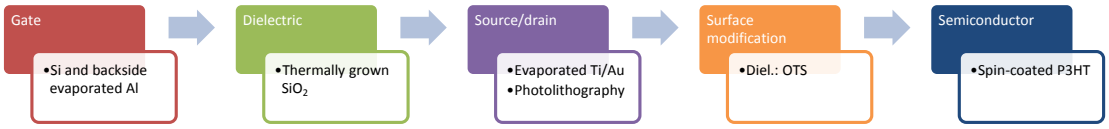


Figure 1.4: Simplified process flow for BG1.

In case of P3HT based OFET, OTS is reported to enhance mobility [80]. OTS molecules undergo a covalent bond via hydroxyl groups at the SiO_2 surface. Its methyl tail makes the modified surface hydrophobic compared to the untreated silica surface. The fatty C-8 chain will impede the charge transfer from the semiconductor to hydroxyl groups at the SiO_2 surface [81, 82]. Depending on the protocol used for the substrate cleaning and surface passivation with OTS, transistors can be obtained with either high mobility and non-uniform P3HT film (sometimes no film at all) or transistors with low mobility and good film uniformity. This is partially due to the fact that OTS can create more than monolayers depending on the process conditions. Since the roughness and the thickness of the dielectric are going to be changed, the field-effect performance will be affected. Umeda *et al.* [83] also reported poor reproducibility with an OTS-treated SiO_2 surface.

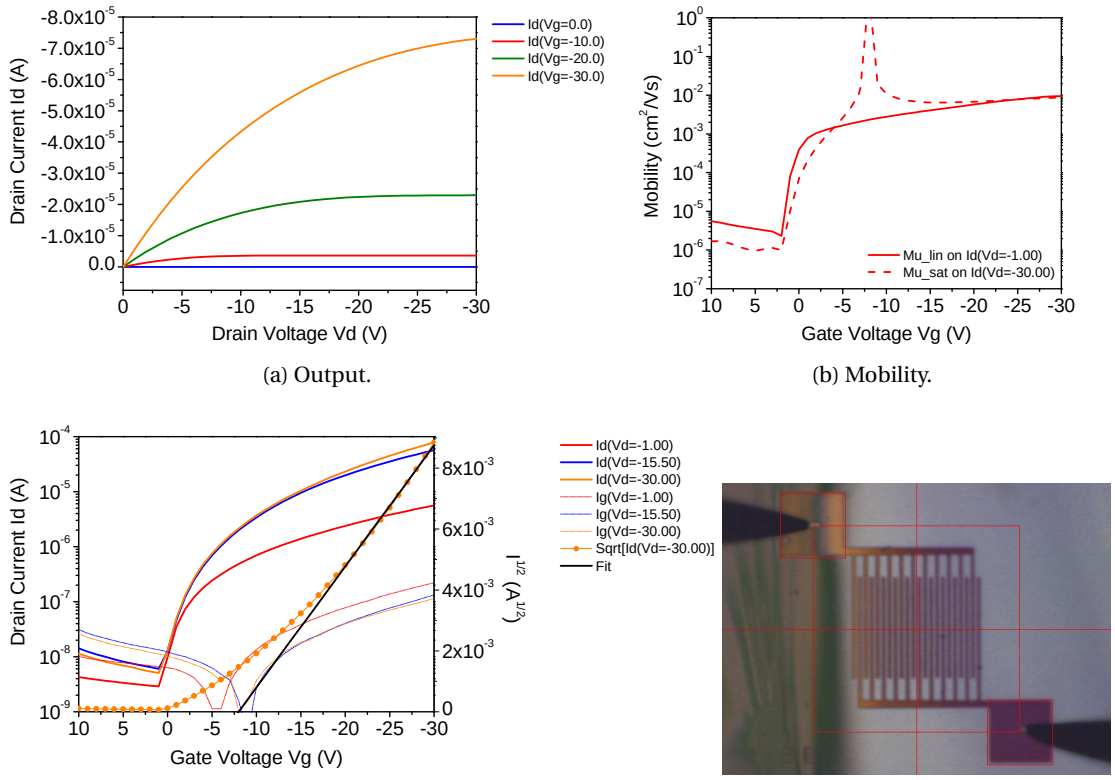
Electrical characteristics

Typical output and transfer characteristics[2] are given in Figures 1.5a and 1.5c, respectively, whereas the gate-voltage dependent mobility extracted in both linear and saturation regimes and a top-view of the characterized OTFT are given in Figures 1.5b and 1.5d, respectively.

The drain current exhibits a linear behavior at low V_{DS} as well as a proper saturation. The OFF current is dominated by the gate leakage. The mobility is strongly gate-voltage dependent: μ_{lin} increases and the linear fit to get μ_{sat} is not accurate. This inaccurate fit gives a too low value for $V_{T,sat}$ which is responsible for the peak observed in the curve of $\mu_{sat}(V_G)$. V_{ON} is around 1 V and can be seen in both the transfer curve and $\mu_{lin}(V_G)$ (when the curves start rising). The device picture reveals than the P3HT layer is inhomogeneous which could come from inhomogeneity of the OTS layer and related processing issues discussed above.

The performances of this technology, referred as **BG1** in the rest of the manuscript, are further discussed at the end of this chapter, in Section 1.5. The experimental data of the corresponding OTFTs are mainly used for this thesis in Section 4.2. Note: the key points of the ten technologies studied in this chapter are gathered in Section 1.5 Table 1.5.

[2] In this particular case, only the forward sweep was measured.



(a) Output.

(b) Mobility.

(c) Transfer.

(d) Micrograph.

Figure 1.5: BG1: Typical characteristics, $W/L = 10$ mm/8 μm, $C_i = 32.6$ nF/cm^2. FoM: $\mu_{\text{sat}} = 7.707 \times 10^{-3}$ cm^2/Vs, $V_{\text{T,sat}} = -8.003$ V, On/Off= 1.546×10^4, $S = 2.0$ V/dec, $I_{\text{G}}/I_{\text{D}}|_{V_{\text{G,max}}} = 1.462 \times 10^{-3}$ and $||I_{\text{ON}}|| = 1.904$ A/Fcm^2.

1.2.2 PTAA-based OTFTs on 2-inch silicon substrate

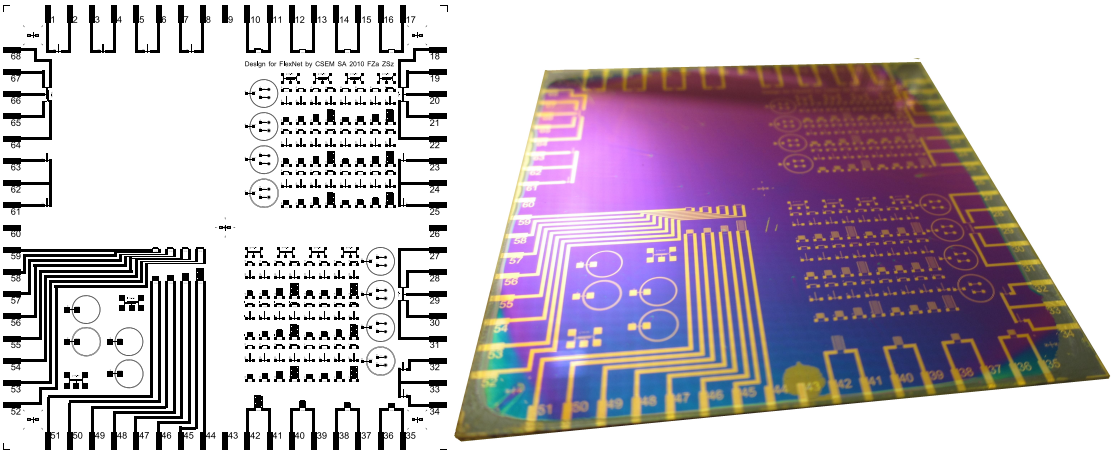
The technology described in this section was developed in the framework of the EU FP7 FLEXNET[3] project and the reported transistors were available in January 2011.

Process

Highly phosphorus doped silicon wafers with thermally grown silicon dioxide (200 nm SiO_2, $C_i = 15$ nF/cm^2) are used as both substrate and gate dielectric. The TiW/Au (5 nm/30 nm) source and drain contacts are patterned by photolithography. The back side of the wafer forms the common gate contact. This results in a 2 in. large standard test substrate.

The layout shown in Figure 1.6a comprises many OTFTs with channel lengths comprised between 5 and 50 μm and various channel widths. **I have actually designed** this chip layout for the Round-Robin Test 1 (RRT-1) following the partners recommendations.

[3] Network of Excellence, 2010-2013, grant agreement n°247745, http://www.noe-flexnet.eu



(a) Chip layout. (b) Finalized BG2 sample.

Figure 1.6: 2-inch silicon screening platform.

After a full cleaning step (sonication in acetone, air plasma, ultra-pure water and IPA) a self-assembled monolayer is used to passivate the oxide surface: hexamethyldisilazane (HMDS) [82] deposited by vapor deposition.

On top of this stack, the organic semiconductor to be deposited is polytriarylamine (PTAA), chosen for its well-known p-type properties [84] and reproducibility (amorphous). PTAA exhibits a lower mobility compared to P3HT, however it is supposed to be more air-stable [85] (more details in Section 2.6.2). PTAA has been supplied by Merck® (Lisicon™ SP006, 7 mg/mL in toluene). PTAA was spin-coated 20 s at 1000 rpm and annealed 2 min at 100°C. The simplified process flow is depicted in Figure 1.7.

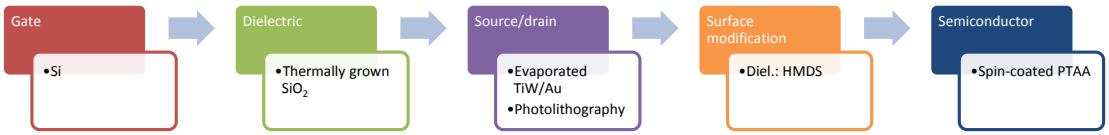
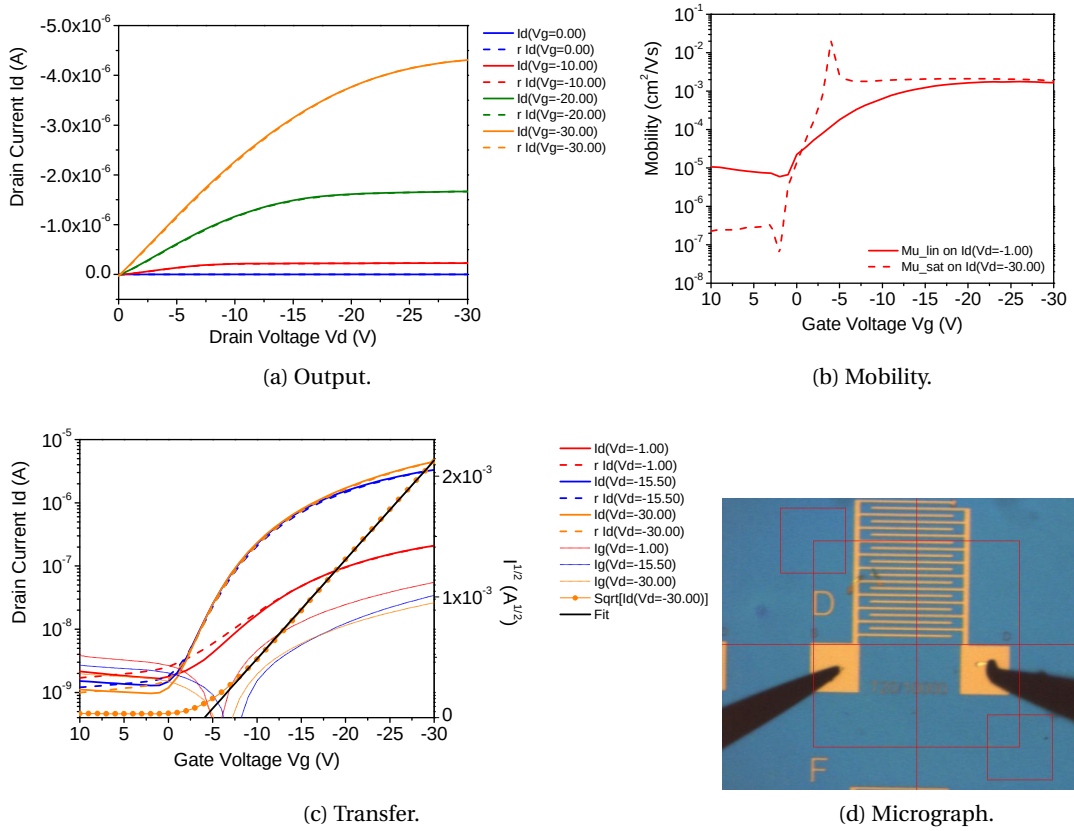


Figure 1.7: Simplified process flow for BG2.

Electrical characteristics

A fabricated sample is visible in Figure 1.6b whereas typical output and transfer characteristics are given in Figure 1.8.

Here also the drain current exhibits a linear behavior at low V_{DS} as well as a proper saturation. Similarly the OFF current is dominated by the gate leakage. No hysteresis is visible in the output characteristics as well as in the transfer characteristics, except in the subthreshold regime at low V_{DS}. The mobility is much less gate-voltage dependent. Indeed on one hand, the linear fit to get μ_{sat} is accurate and the $\mu_{sat}(V_G)$ curve is almost constant above $V_{T,sat}$. On



(a) Output.

(b) Mobility.

(c) Transfer.

(d) Micrograph.

Figure 1.8: BG2: Typical characteristics, $W/L = 10\,\text{mm}/20\,\mu\text{m}$, $C_i = 15.0\,\text{nF/cm}^2$. FoM: $\mu_{\text{sat}} = 2.05\times10^{-3}\,\text{cm}^2/\text{Vs}$, $V_{\text{T,sat}} = -4.07\,\text{V}$, On/Off$= 4.64\times10^3$, $S = 3.3\,\text{V/dec}$, $I_G/I_D|_{V_{G,\max}} = 5.84\times10^{-3}$ and $||I_{ON}|| = 0.683\,\text{A/Fcm}^2$.

the other hand, μ_{lin} slowly increases versus V_G before saturating. This inaccurate fit gives a too low value for $V_{\text{T,sat}}$ which is responsible for the peak observed in the curve of $\mu_{\text{sat}}(V_G)$. V_{ON} is around 0 V which is ideal. The device picture reveals than the PTAA layer is really homogeneous.

The performances of this technology, referred as **BG2** in the rest of the manuscript, are further discussed in Section 1.5. The experimental data of the corresponding OTFTs are mainly used for this thesis in Section 4.2.

Technology issues

Whereas the two platforms described in this section are meant for material screening, they are limited in several ways by their common gate electrode. First since the gate of individual transistors cannot be addressed independently, circuits cannot be realized. Secondly every structure on the source/drain layer forms a parasitic plate-to-plate capacitor with the gate. Thus for a transistor, the input/output (I/O) pads, the access interconnects and the

source/drain contacts themselves dominate the transistor channel capacitance which prevents the study of the dynamic properties.

In the next sections the gate electrode is patterned which solves the first issue and strongly reduces the second one (depending on the designed contact overlap).

1.3 1-inch glass/ITO platform

In this section, 1 in. glass substrates are used instead of silicon wafers which make them cheaper, less brittle and transparent (in the visible light). Glass substrates coated with a 100 nm layer of a solid solution of indium(III) oxide and tin(IV) oxide (ITO) were ordered from GEOMATEC's. Since ITO is a transparent conductor whose work function permits to inject holes, it is often used in OLEDs serving as anode. After a cleaning step of the delivered substrates, the ITO layer is then patterned by photolithography and wet etching to form the bottom gate electrode.

A commercially available polymer dielectric poly(4-vinyl phenol) (PVP, Aldrich® 436224) is then dissolved with the cross-linking agent poly(melamine-co-formaldehyde) methylated (PMCF) in propylene glycol monomethyl ether acetate (MPA), deposited by spin-coating and thermally cross-linked – more details in [86]. The obtained cross-linked PVP:PMCF dielectric is referred as "X-PVP". Gold is thermally evaporated and patterned with photolithography and wet etching (KI/I_2) to form the source and drain contacts. Finally the semiconductor is spin-coated to complete the BG-BC architecture depicted in Figure 1.9.

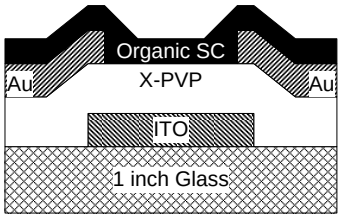


Figure 1.9: BG-BC stack common to the technologies of Section 1.3 (BG3, BG4 & BG5).

In the next sub-sections, different semiconductors (sub-section titles), dielectric thicknesses and surface treatments are used as well as different transistor layouts.

1.3.1 P3HT-based OTFTs and circuits

Process

The semiconductor is P3HT (same as in Section 1.2.1, spin-coated 120 s at 3000 rpm), the X-PVP dielectric is 200 nm thick (C_i = 13 nF/cm^2) and the layout of the used test structures is shown in Figure A.2. In addition the ITO layer is 75 nm thick in this section. The simplified process flow is depicted in Figure 1.10.

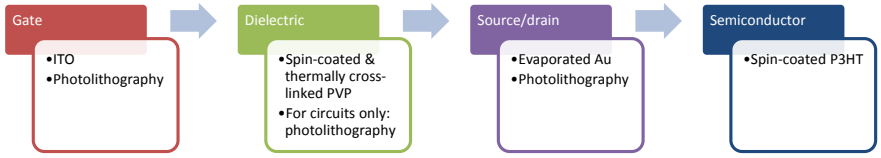
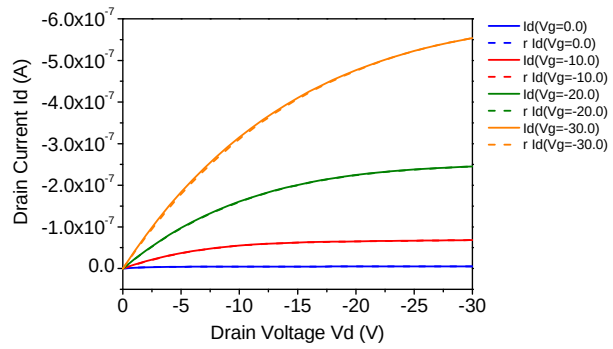


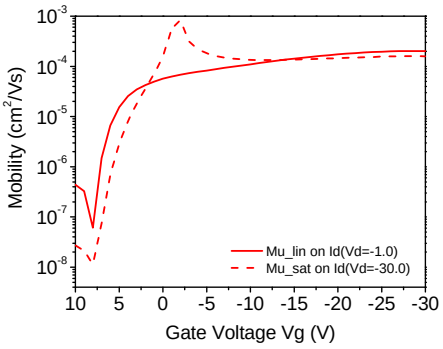
Figure 1.10: Simplified process flow for BG3.

Electrical characteristics

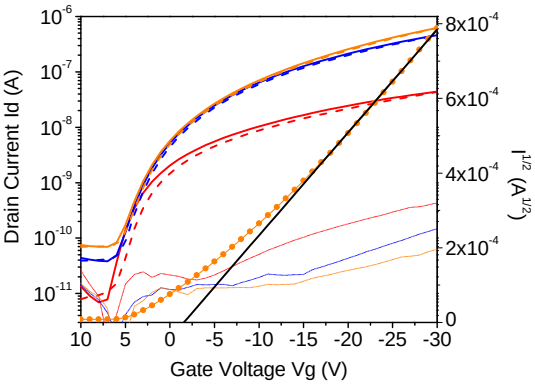
Typical output and transfer characteristics are given in Figure 1.11.



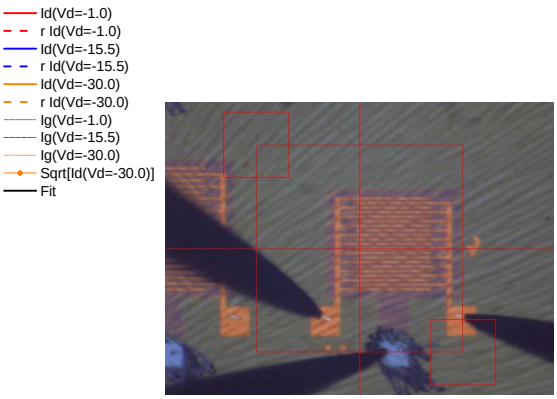
(a) Output.



(b) Mobility.



(c) Transfer.



(d) Micrograph.

Figure 1.11: BG3: Typical characteristics, $W/L = 10\,\text{mm}/10\,\mu\text{m}$, $C_i = 13.0\,\text{nF/cm}^2$. FoM: $\mu_{\text{sat}} = 1.52\times10^{-4}\,\text{cm}^2/\text{Vs}$, $V_{\text{T,sat}} = -1.55\,\text{V}$, On/Off$= 8.94\times10^3$, $S = 2.5\,\text{V/dec}$, $I_G/I_D|_{V_{G,\max}} = 1.00\times10^{-4}$ and $||I_{ON}|| = 4.79\times10^{-2}\,\text{A/Fcm}^2$.

Here also the drain current exhibits a linear behavior at low V_{DS} as well as a proper saturation. No hysteresis is visible in the output characteristics as well as in the transfer characteristics, except in the subthreshold regime at low V_{DS}. The OFF current is this time larger than the gate leakage (bulk conduction). The gate-voltage dependency of the mobility is the same as for BG1 (also P3HT): large. V_{ON} is around 7 V which is bad compared to BG1: such device is

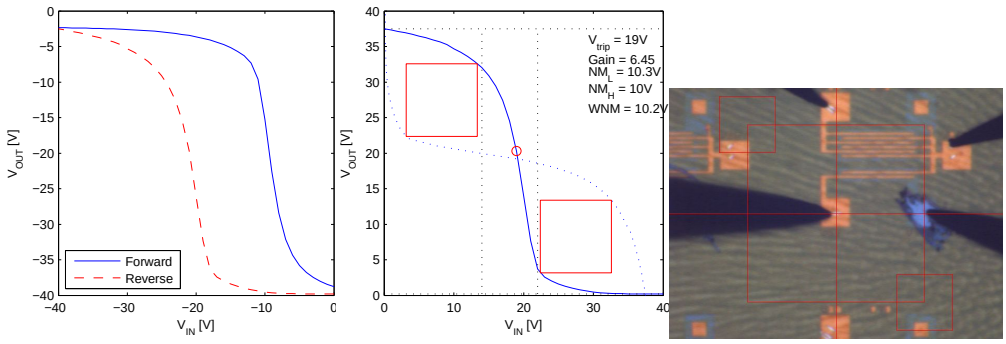
always ON. The device picture reveals than the P3HT layer is inhomogeneous. Indeed the film exhibits structures following a central symmetry attributed to the spin-coating process. However correlations with the device performances are not obvious which could mean that the first P3HT layers, where the charge transport occurs, are homogeneous and thus that only the top layers are impacted by these structures.

The performances of this technology, referred as **BG3** in the rest of the manuscript, are further discussed in Section 1.5. The experimental data of the corresponding OTFTs are mainly used for this thesis in Section 4.2.

Circuits

Another chip layout was used which comprises inverters and 5-stage ring-oscillators (R-O) only. The X-PVP layer was patterned with photolithography and oxygen plasma to define vias and working inverters and 5-stage ring-oscillators (R-O) were obtained. Since the chip layout does not embed any transistor, the impact of the via drilling process on the OTFT performance could not be characterized and thus was neglected.

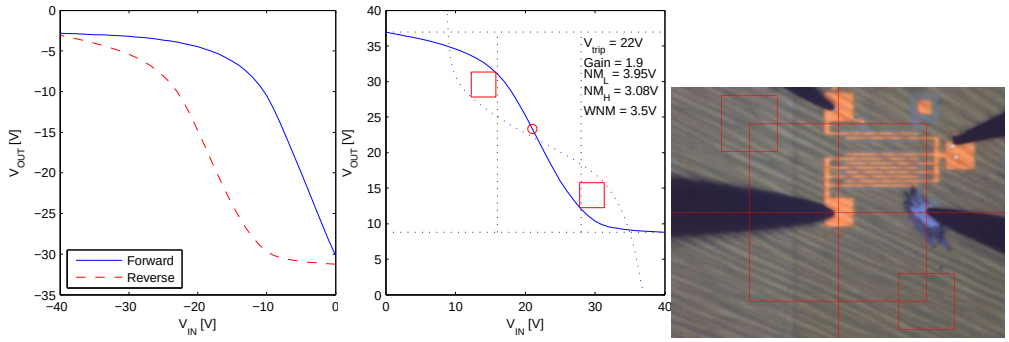
The raw measurements of a zero-V_{GS} inverter and of a diode-connected inverter are shown in Figures 1.12a and 1.13a, respectively. The corresponding post-processed characteristics showing the low level, the high level and the noise margins calculated using the unity gain method (NM_L and NM_H) and the maximum equal criteria (MEC, WNM) are visible in Figures 1.12b and 1.13b, respectively.



(a) (b) (c)

Figure 1.12: Typical characteristics of a zero-V_{GS} inverter from BG3. (a) raw measurement, (b) post-processed data and (c) micrograph. $V_{DD} = 40$ V, $L = 10$ μm and $W_{load}/W_{driver} = 5$.

In both cases, the inverter pictures exhibit the same film inhomogeneity as for the transistor depicted in Figure 1.11d. Also in both cases, a large hysteresis between the forward and the reverse sweep is observed making the curves looking like a memory cell. The origin of this behavior is not clear but my hypothesis is that during the forward sweep the inverter was first polarized and traps filled which can be seen as an initialization step, whereas on the reverse sweep the actual device is measured. Thus whenever this phenomenon occurs, the reverse



(a) (b) (c)

Figure 1.13: Typical characteristics of a diode-connected inverter from BG3. (a) raw measurement, (b) post-processed data and (c) micrograph. $V_{\mathrm{DD}} = 40$ V, $L = 10$ μm and $W_{load}/W_{driver} = 1/7$.

sweep is selected to extract the inverter performance parameters. The zero-V_{GS} inverter performs better than the diode-connected inverter: higher gain and larger noise margins, 6.45 and 10.2 V, respectively, at $V_{\mathrm{DD}} = 40$ V. This is because of the topology [87].

A zero-V_{GS} 5-stage ring-oscillator operated at $V_{\mathrm{DD}} = 50$ V is shown in Figure 1.14. The measured oscillation frequency and amplitude are 2.5 Hz and 15 V, respectively. This frequency, especially at such supply voltage, is far from the state of the art.

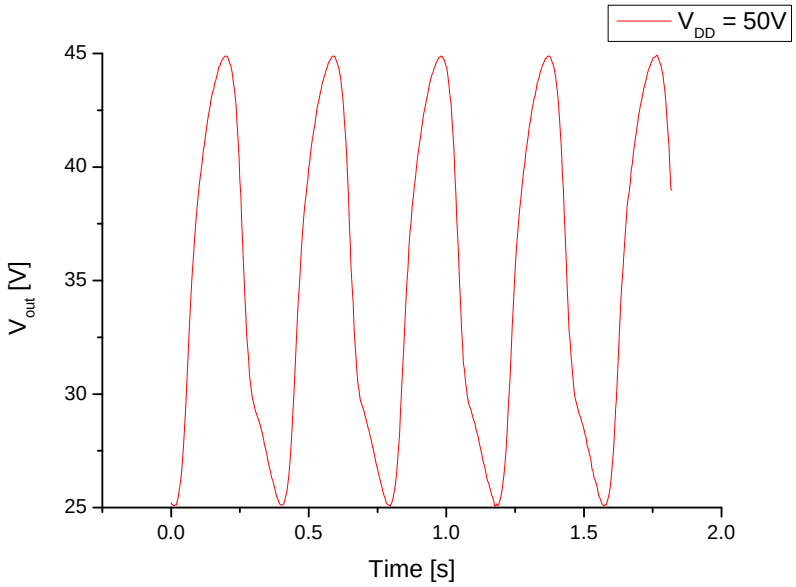


Figure 1.14: BG3 zero-V_{GS} 5-stage ring-oscillator with $L = 10$ μm.

1.3.2 PTAA-based OTFTs and circuits

Optimized X-PVP capacitance

In this section, the X-PVP dielectric was successfully thinned down to 120-130 nm thanks to an optimization of the solution and spin-coating parameters – 1500 rpm/5/50s, MPA solvent while still cross-linked at 200°C. In a first set of samples designated by **BG4**, the dielectric was not further patterned whereas for **BG5**, an additional photolithography step was performed to drill vias by oxygen plasma.

Figure 1.15 gives two information: firstly, the optimized X-PVP film is 130 nm thick and secondly, the via profile is clean (for BG5).

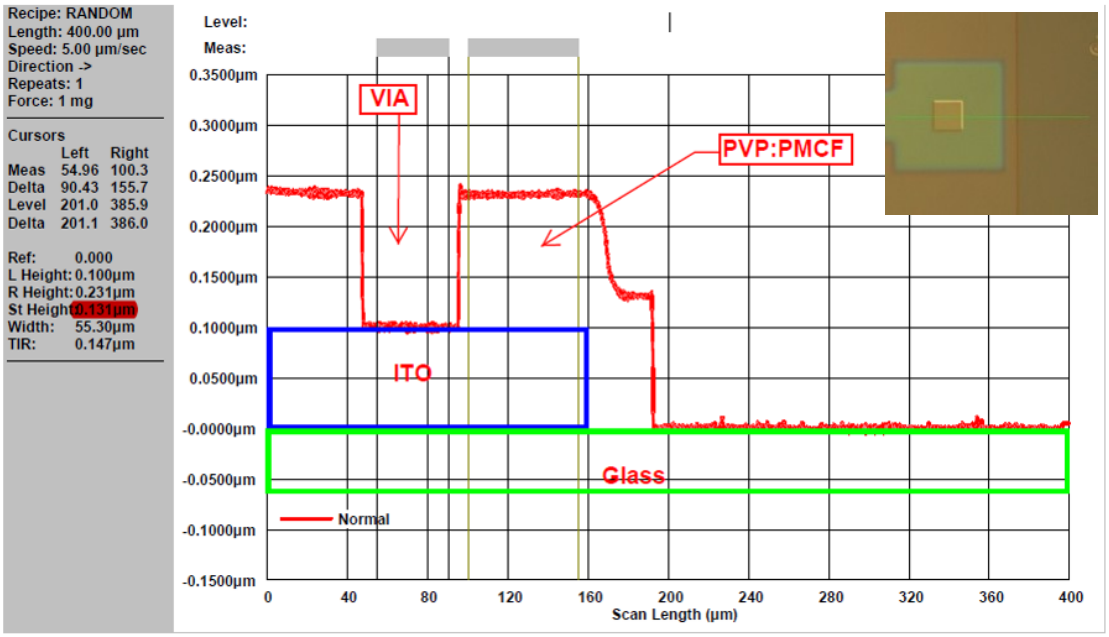
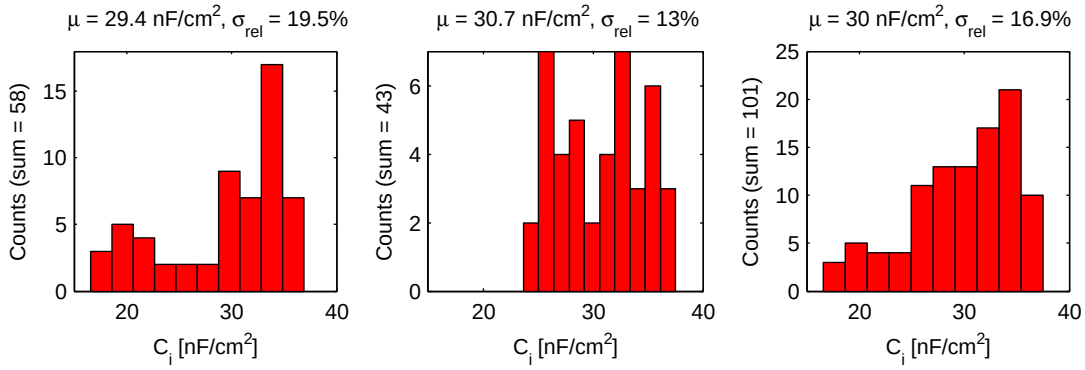


Figure 1.15: Profile of an I/O pad with drilled via (Tencor Profilometer). The measured X-PVP thickness is highlighted in red in the left panel. Inset: optical micrograph (top-view) showing the cross-section area.

I fabricated 5 samples with (BG5) and 5 samples without (BG4) via in order to evaluate the reproducibility of the capacitance. The device-to-device discrepancy is generally below 10% for each sample which validates the reproducibility at the sample scale. At the technology scale, the averaged capacitance measured on 58 capacitors of BG4 is 29 nF/cm^2 with a relative standard deviation of 20% whereas for BG5 (43 capacitors) the values are 31 nF/cm^2 and 13%, respectively. Thus the additional process step drilling the vias does not seem to affect the dielectric – at least in terms of capacitance. Combining BG4 and BG5 data gives finally C_i = 30 nF/cm^2 and $\sigma_{C_i,\text{relative}}$ = 17%. This is shown in Figure 1.16. Such deviation seems too high to validate the reproducibility at the technology scale but it is actually pretty good for such thin polymer dielectric.

Further details and tests of the dielectric layer are available in Appendix A.1.



(a) BG4. (b) BG5. (c) BG4 & BG5.

Figure 1.16: BG4 & BG5: dielectric capacitance.

Transistor layouts and design rule tests

In this section, the different transistor layouts used for BG4, BG5 but also BG3 are introduced. They are shown in Figure 1.17 and the chip layouts corresponding to the so-called T1, T3 and IC2 layouts are depicted in Figures A.2, 1.18a and 1.18b, respectively. Then some tests are introduced to evaluate the design rules used in the IC2 chip.

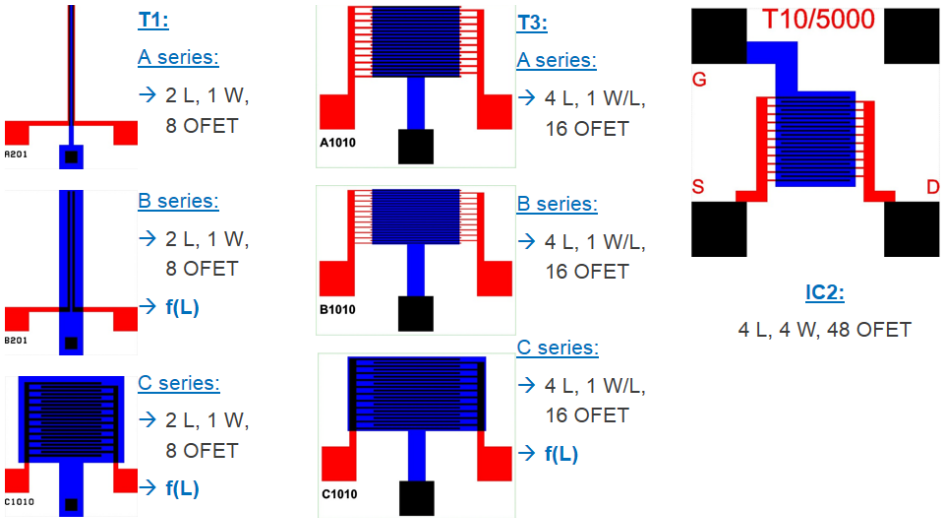
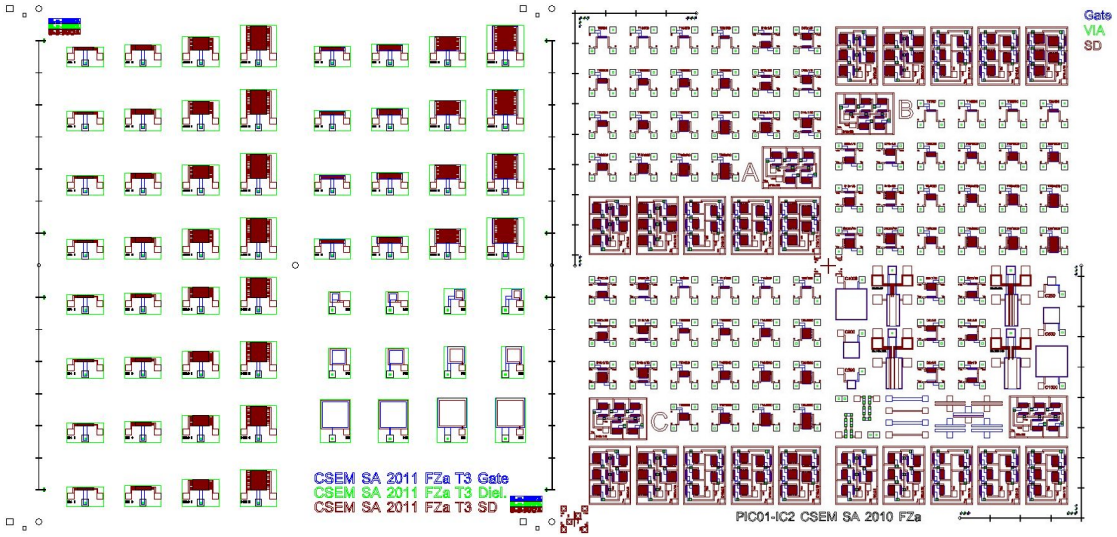


Figure 1.17: Various transistor layouts with finger or interdigitated topology as well as different gate overlaps and finger widths. Gate: blue. Source/drain: red. $f(L)$ points out that the overlap (source-drain/gate) area depends on L.

Two transistor layouts are available with the finger topology: the T1_A and T1_B. The latter one has a large gate electrode island independent from the channel length on which the source and drain contacts lie. On the other hand, for T1_A, the width of the gate electrode is tighter



(a) T3. (b) IC2.

Figure 1.18: Two 1-inch test structures layouts.

and equal to the channel length plus an alignment margin.

The interdigitated topology allows large channel width by putting in parallel multiple source-drain fingers. The T1_C and T3_C layouts are almost the same: the gate gets simply tighter to the source-drain contacts for T3_C. The IC2 layout brings the gate electrode withing the interdigitated area to only surround the channel. This is an improvement in terms of parasitic gate overlap but it is technologically more complex than the two previous layouts. Indeed depending on the thickness of the different layers (the gate metal, the dielectric and the source-drain metal), the gate electrode island may become a step which can break the electrical contact of the source-drain metal fingers. In the T3_A and T3_B layouts, the inner channel width is not anymore defined by the source-drain fingers but by the gate electrode width. This concept reduces further the parasitic overlap capacitance and the layout gets closer to the one of a silicon MOSFET. The finger width of the T3_B layout is reduced to 5 μm (10 μm for T3_A) to further lower the parasitic overlap capacitance.

In every case, 110 nm of gold was thermally evaporated and patterned through photolithography and wet etching to define the source/drain electrodes.

In the IC2 test structure layout I designed, I have placed some structures to test the chosen design rules. For a given interconnect layer, structures, namely resistors and planar capacitors, following the chosen design rules (line width and spacing) are available to measure respectively the sheet resistance and the parasitic capacitance between two neighbor interconnects. Chains of 10 vias allowing the measurement of the via resistance are part of these design rules test structures. The three main design rules test structures are depicted in Figure 1.19. Geometric details and raw measurement results are available for all these structures in Table 1.3.

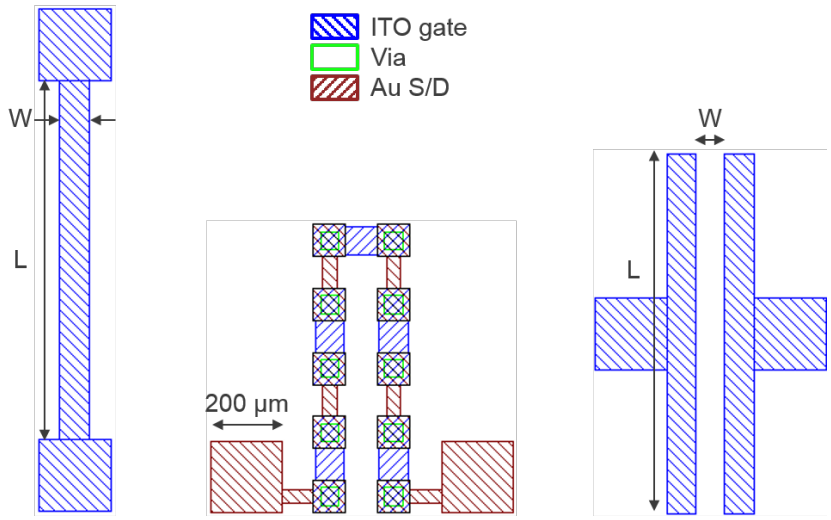


Figure 1.19: Test structures present on the IC2 layout to characterize the design rules. From left to right: resistor, via chain and planar capacitor.

Table 1.3: Parameters and measurements of the design rules test structures from Figure 1.19. Resistances were measured with a multimeter after removing the cable and contact resistances (short-circuit calibration). Capacitances were measured at 100 kHz with 1 V p-p after open-circuit and short-circuit calibration.

Layer(s)	L mm	W [μm]	R [Ω]	C [fF]
ITO	1	80	300	-
Au	1	40	7	-
ITO/ITO	1	80	-	38
ITO/Au	1	20	-	55
Au/Au	1	40	-	40

From the raw resistance measurement gathered in Table 1.3, the sheet resistance and resistivity of the ITO layer (gate and first level of interconnects) follow: $R_{S,ITO} = 24\ \Omega/\square$ and, since $t_{ITO} = 100$ nm, $\rho_{ITO} = 2.4\ \mu\Omega.m$. Similarly for the gold layer (source/drain and second level of interconnects): $R_{S,Au} = 0.28\ \Omega/\square$ and, since $t_{Au} = 110$ nm, $\rho_{Au} = 31\ n\Omega.m$ which is close to the theoretical value of 24.4 $n\Omega.m$ (at 293K). This allows estimating the resistance of the multiple access lines in the via chain structure around 140 Ω which, once subtracted from the total resistance of this structure (3.43 kΩ), gives the resistance of a single via around 330 Ω.

Table 1.3 also gives the parasitic capacitance between two neighbor interconnects. For instance, two parallel lines of the source/drain layer (made of gold) separated by a 40 μm gap (chosen design rule) have a 40 fF/mm parasitic capacitance.

All these parameters (sheet resistances, R_{via}, parasitic capacitances) are useful inputs together with the design rules for the technology file used by EDA tools such as Cadence Virtuoso.

They allow the extraction of the parasitic circuit resistors and capacitors (RCX step) for more realistic circuit simulations.

Results: BG4 and BG5

In this section, the OTFT stack is completed and the results of the corresponding transistors are given. The related experimental data is mainly used for this thesis in Section 2.6.

On top of the 110-nm thick gold source/drain layer, PTAA was deposited as for BG2: spin-coated 20 s at 1000 rpm and annealed 2 min at 100°C for both BG4 and BG5. In both cases, the best static performances are obtained with the T3_C transistor layout. The T3_A and T3_B OTFT layouts give indeed a much larger OFF current while having similar ON current than T3_C. The reason for the increased OFF current is the following: for T3_A and T3_B the source/drain fingers extend outside of the gate electrode, as visible in Figure 1.17, which, combined to the unpatterned semiconductor, forms a resistor which length is equal to the channel length and which width is equal to the finger extension. On the other hand, in T3_C (and all other interdigitated layouts in Figure 1.17) the gate electrode extends outside the channel area and deplete the semiconductor when polarized in the OFF regime which thus lowers the OFF current. For this reason, the OTFT data related to the T3_A and T3_B layouts are neither reported in this section nor in the technology summary in Section 1.5. The simplified process flow is depicted in Figure 1.20.

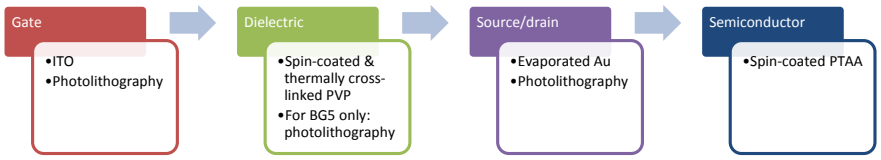
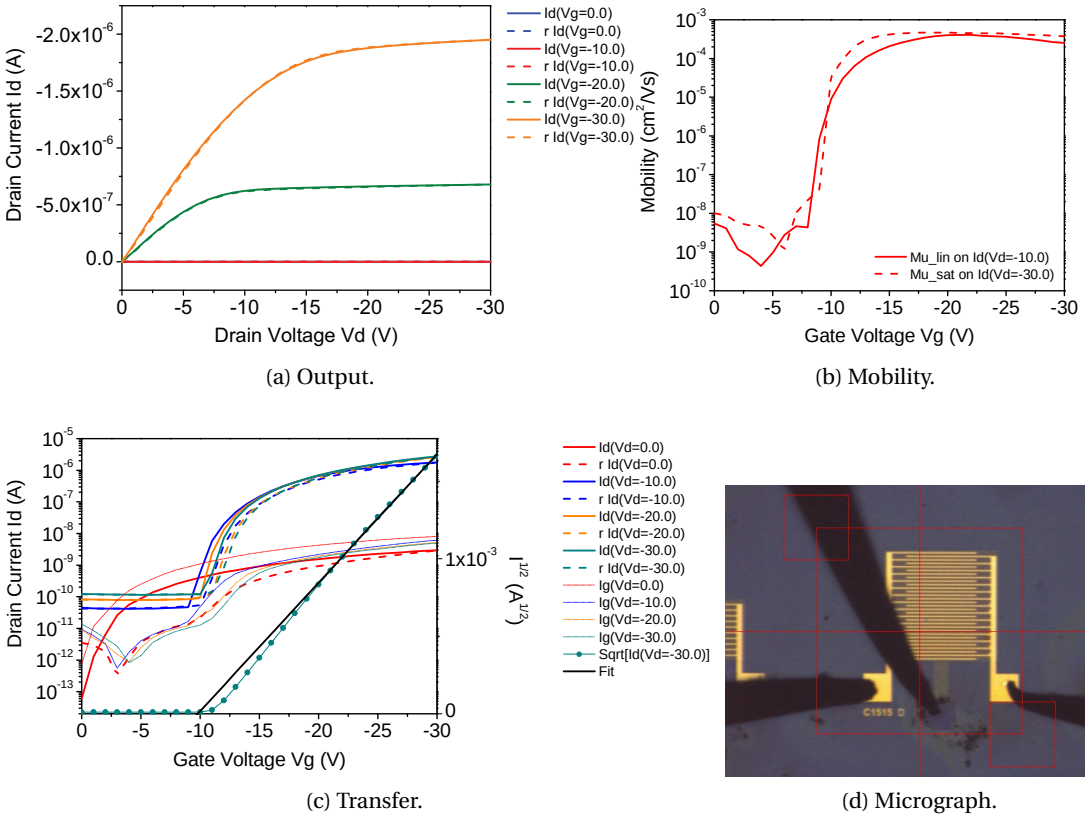


Figure 1.20: Simplified process flow for BG4 and BG5.

For both BG4 and BG5, the drain current exhibits a linear behavior at low V_{DS} as well as a proper saturation, as visible in Figures 1.21 and 1.22, respectively[4]. The OFF current is larger than the gate leakage (bulk conduction). An hysteresis is observed in the transfer characteristics for every V_{DS} even if none is visible in the output characteristics. The mobility is one order of magnitude lower than BG2 and the threshold voltage decreases from -4 V (for BG2) to -10 V for BG4 and down to -13 V for BG5, giving always-OFF OTFTs. Except for the subthreshold swing which gets improved for BG4 and BG5, BG2 performs better than BG4 and BG5. The remaining comments made for BG2 are valid for BG4 and BG5.

Concerning the BG5 technology, every OTFT performance parameter gets actually worse with respect to BG4. This is an evidence of damages caused by the via drilling process. The last step of this process i.e. the photoresist stripping is the main suspect. Indeed stripping the polymer

[4]Voltage range. Transfer: $0V > V_G > -30V$, with $V_{G,step} = -1V$ and $0V > V_D > -30V$, with $V_{D,step} = -10V$. Output: $0V > V_D > -30V$, with $V_{D,step} = -1V$ and $0V > V_G > -30V$, with $V_{G,step} = -10V$



(a) Output.

(b) Mobility.

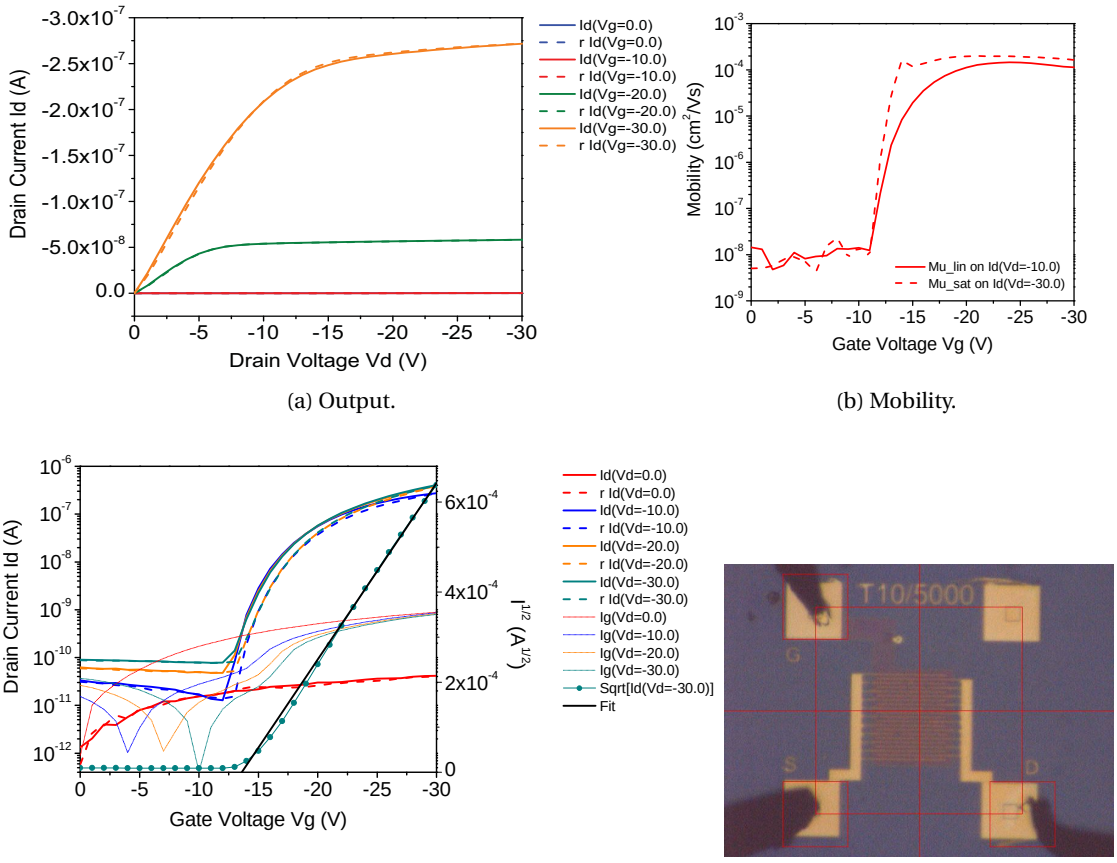
(c) Transfer.

(d) Micrograph.

Figure 1.21: BG4: Typical characteristics, $W/L = 15$ mm/15 μm, $C_i = 32.0$ nF/cm^2, T3_C OTFT layout. FoM: $\mu_{\text{sat}} = 4.29 \times 10^{-4}$ cm^2/Vs, $V_{\text{T,sat}} = -9.80$ V, On/Off= 2.38×10^4, $S = 1.1$ V/dec, $I_G/I_D|_{V_{G,\max}} = 1.81 \times 10^{-3}$ and $||I_{ON}|| = 8.62 \times 10^{-2}$ A/Fcm^2.

photoresist (Shipley 1805-G2) on top of the polymer dielectric (X-PVP) is not straightforward. The classical approach with acetone and IPA often leads to an incomplete stripping which is hard to correct even with N-methyl-2-pyrrolidinone (NMP, Shipley Microposit Remover 1165). Since a decrease of the threshold voltage is observed ($|V_T|$ increases), this process step adds dipoles at the dielectric surface which could be linked to the fact that NMP has a larger dipole moment and dielectric constant than acetone and IPA[5]. An experience to confirm this hypothesis (but not performed) would be to take two samples with ITO/X-PVP, rinse them with NMP, place one sample in vacuum for NMP degazing and one in ambient condition. After OTFT completion, the sample kept in vacuum should exhibit a threshold voltage like BG4's instead of varying like the sample kept in air i.e. like BG5's. On the other hand photoresist residuals can explain the global loss of performance as an additional dielectric layer decreasing C_i and whose non-uniformity leads to a non-optimal formation of the semiconductor film. Thus the stripping process was optimized by directly using NMP combined with sonication. This led

[5]Dipole moment: NMP = 4.09 D (at 30°C), acetone = 2.69 D (at 20°C)) & IPA = 1.66 D (at 30°C), http://macro.lsu.edu/howto/solvents/DipoleMoment.htm. Dielectric constant: NMP = 32.2, acetone = 20.7 & IPA = 19.92 (all at 25°C), http://macro.lsu.edu/howto/solvents/DielectricConstant.htm.



(a) Output.

(b) Mobility.

(c) Transfer.

(d) Micrograph.

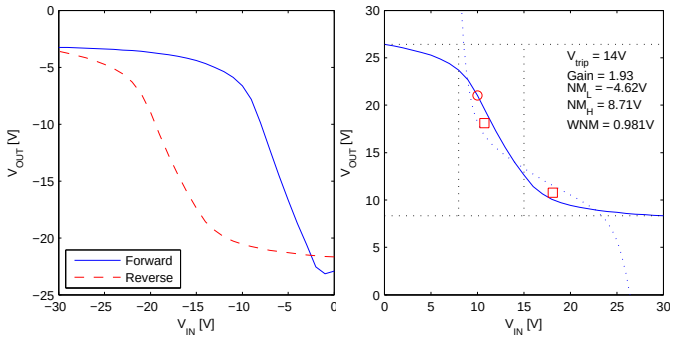
Figure 1.22: BG5: Typical characteristics. $W/L = 5$ mm/10 μm, $C_i = 32.9$ nF/cm^2, IC2 OTFT layout. FoM: $\mu_{\text{sat}} = 1.87 \times 10^{-4}$ cm^2/Vs, $V_{\text{T,sat}} = -13.6$ V, On/Off= 5.24×10^3, $S = 1.7$ V/dec, $I_{\text{G}}/I_{\text{D}}|_{V_{\text{G,max}}} = 1.98 \times 10^{-3}$ and $||I_{\text{ON}}|| = 2.47 \times 10^{-2}$ A/Fcm^2.

to samples qualified – through differential interference contrast (DIC) optical inspection – as residual-free. However most of the BG5 samples have undergone this optimized process and still the performances and the threshold voltage are lower than BG4 OTFTs.

Circuits (BG5)

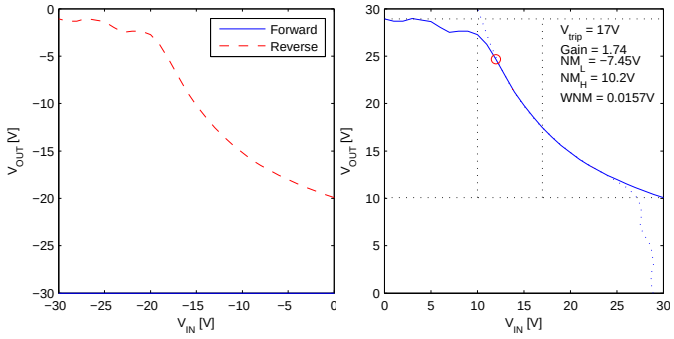
In terms of circuits, inverters of poor quality but still working were obtained, as visible in Figures 1.23 and 1.24. The low performances of the BG5 OTFTs discussed above can explain these results.

In order to increase the threshold voltage (closer to 0 V), reduce the hysteresis and electrical instability – more details in Section 2.6.1– different approaches were tested. The first one consists in applying a surface treatment to the dielectric with HMDS or poly(alpha-methylstyrene) (PαMS) [39]. In both cases, no change was observed.



(a) (b)

Figure 1.23: Typical characteristics of a diode-connected inverter from BG5. (a) raw measurement and (b) post-processed data. $V_{\mathrm{DD}} = 30$ V, $L = 10$ μm and $W_{load}/W_{driver} = 1/6$.



(a) (b)

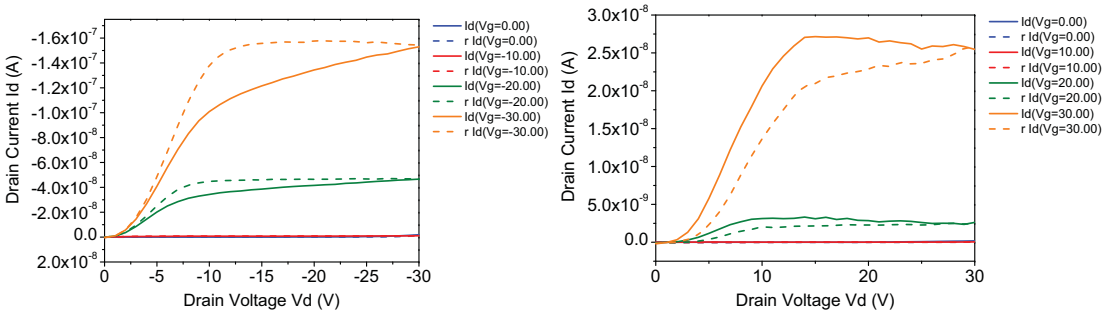
Figure 1.24: Typical characteristics of a zero-VGS inverter from BG5. (a) raw measurement and (b) post-processed data. $V_{\mathrm{DD}} = 30$ V, $L = 10$ μm and $W_{load}/W_{driver} = 8$.

A new hypothesis raised to explain this behavior: the polymers which were used to prepare the dielectric solution (PVP and PMCF) aged. A new dielectric solution was thus prepared with freshly bought polymers to check this point but again no change was observed. In a last attempt to validate this high-capacitance ITO/X-PVP stack, other commercially available semiconductors are tested in the next sub-section.

1.3.3 OTFTs made with other semiconductors

The same ITO/X-PVP stack has also been used to test two state-of-the-art commercially available semiconductors: p-type 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) from Sigma Aldrich (716006) and n-type [P(NDI2OD-T2)] from Polyera (ActivInk™ N2200). The deposition followed the recommendations given by the respective suppliers and, for TIPS-pentacene, inputs from [39]. Typical output characteristics of OTFTs made with TIPS-pentacene and N2200 deposited on bare X-PVP are shown in Figure 1.25. The obtained OTFTs

are of very poor quality and actually worse in every aspect than those with PTAA from BG4 and BG5.



(a) TIPS-pentacene, T1-C OTFT layout.

(b) N2200, T3-C OTFT layout.

Figure 1.25: Typical output characteristics of OTFTs with W/L = 10 mm/10 μm, C_i = 32.9 nF/cm^2 and state-of-the-art commercially available semiconductors.

In a last attempt new samples were treated prior the semiconductor deposition. One batch was treated with HMDS and another batch with PαMS as in [39]. In both cases, no improvement was observed.

This confirms once more that having the best semiconductor is not the only factor to get the best OTFT. The key point is to have the optimal dielectric/semiconductor interface [20, 21]. No further optimization was performed with these two semiconductors because the goal was not to develop dedicated processes. The thesis objectives defined the go/no-go conditions which the tests introduced in this section failed.

1.4 ITO-free platforms

ITO has many advantages such as transparency and conductivity however the main drawback is the shortage of the Indium mines which are in addition almost all located in China. Thus from both geological and geopolitical point of view there is a strong interest in finding substitutes.

The technologies described in this section are not claiming to fulfill all constraints – especially the optical ones – to replace ITO however they are ITO-free. Whereas the previously introduced technologies were all using the BG-BC architecture, 3 out of the 4 described next use the TG-BC architecture.

1.4.1 P3HT-based OTFTs on 1-inch glass substrate

Process

First Ti/Au (5 nm/50 nm) bottom source and drain contacts are evaporated onto the 1-inch glass substrate and patterned by photolithography. Then P3HT (same as for BG1) is spin-coated 120 s at 1500 rpm. Next two dielectrics were tested.

In the first case referred as **TG1**, diluted Cytop® CTL 809A was spin-coated 180 s at 1000 rpm to get a thickness of 300 nm. In the second case referred as **TG2**, Merck® Lisicon™ D139-FC43-045 (D139) was spin-coated 300 s at 1500 rpm to get a thickness of 300 nm. The measured dielectric capacitances are 7 nF/cm^2 and 6 nF/cm^2, respectively. Finally 70 nm of aluminum is evaporated through a shadow mask to define the gate electrode. The simplified process flow is depicted in Figure 1.26.

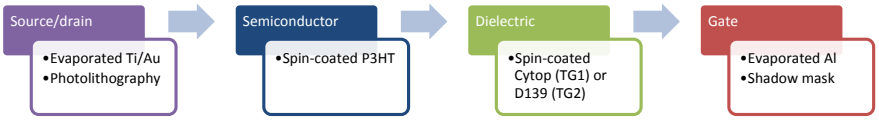
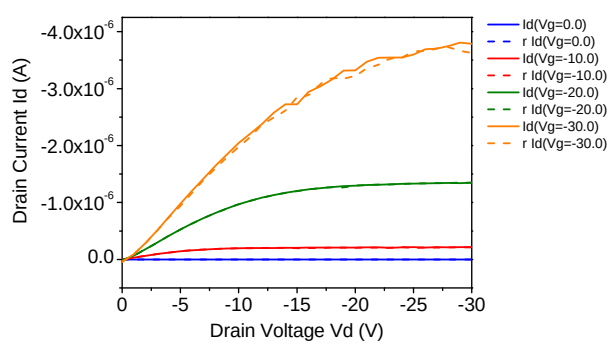


Figure 1.26: Simplified process flow for TG1 and TG2.

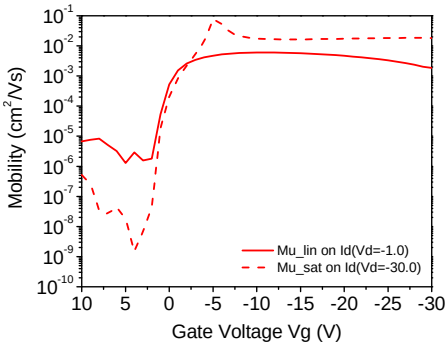
Electrical characteristics

The TG1 and TG2 OTFTs shown in Figures 1.27 and 1.28 share several characteristics:

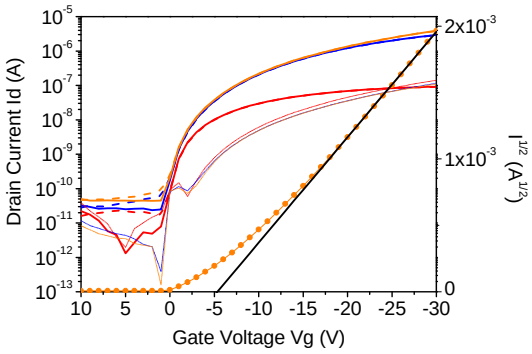
- A slight non-ohmic behavior is observed at low V_{DS}, cf. Figures 1.27a and 1.28a, respectively. It does not necessarily come from an injection issue into the semiconductor but rather by the dominance of the gate leakage in this V_{DS}-range. This is confirmed by the sign of the drain current which changes.
- The linear mobility extracted at $V_{\mathrm{DS}} = -1$ V is disturbed by the dominance of the gate leakage which slows down the increase of $I_{\mathrm{D,lin}}$. This translates by a decrease of μ_{lin} as $|V_G|$ increases. This is visible in Figure 1.27b and even more in Figure 1.28b where $I_{\mathrm{D,lin}}$ even starts to decrease causing the sign transition spike of μ_{lin} observed around -22 V.
- The linear fit performed to extract μ_{sat} and $V_{\mathrm{T,sat}}$ is inaccurate and disturbed by the gate-voltage dependency of the mobility. Still the extracted $V_{\mathrm{T,sat}}$ is almost the same.
- The P3HT spin-coating pattern discussed for BG3 is also visible, cf. Figures 1.27d and 1.28d, respectively.
- On the positive side, there is no visible hysteresis, V_{ON} is around 1 V, the OFF current is low and not dominated by the gate leakage (bulk conduction). More details about the device performance of both technologies are given in Section 1.5.



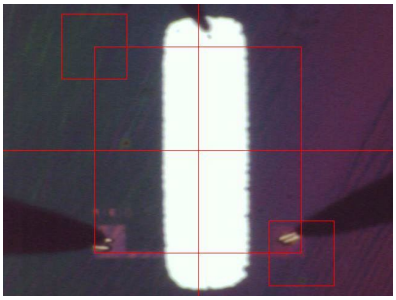
(a) Output.



(b) Mobility.



(c) Transfer.



(d) Micrograph.

Figure 1.27: TG1: Typical characteristics, $W/L = 1$ mm/10 μm, $C_i = 7$ nF/cm^2. FoM: $\mu_{\text{sat}} = 1.80 \times 10^{-2}$ cm^2/Vs, $V_{\text{T,sat}} = -5.34$ V, On/Off$= 8.71 \times 10^4$, $S = 1.3$ V/dec, $I_{\text{G}}/I_{\text{D}}|_{V_{\text{G,max}}} = 2.85 \times 10^{-2}$ and $||I_{\text{ON}}|| = 5.51$ A/Fcm^2.

These OTFTs exhibit nice characteristics and at the same time suffer from the side effects of organic technologies (gate leakage, gate-voltage dependency of the mobility...). That is why the OTFT from TG1 was actually selected to compare the extraction methods for the mobility and threshold voltage in the introduction of the chapter (Section 1.1.1).

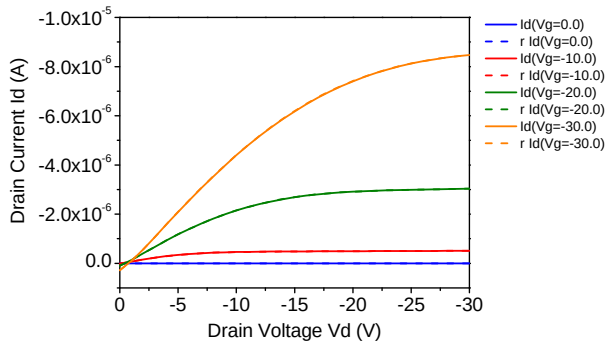
1.4.2 Photo-patterned OTFTs on 4-inch flexible substrate

The technology described in this section was developed in the framework of the CTI POMME[6] project and the reported transistors were available in March 2012.

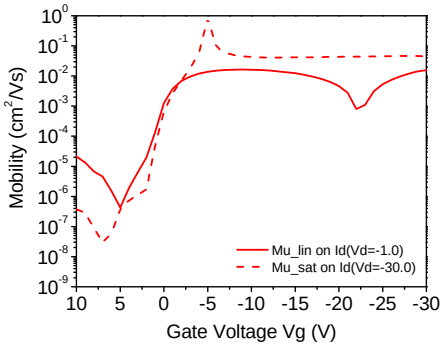
Process

After a cleaning step (IPA) of the 4-inch plastic substrate (PET), 60 nm of silver is thermally evaporated. This layer of silver is then patterned with photolithography and wet etching

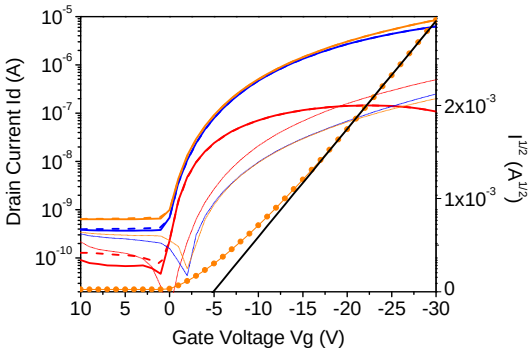
[6] Performance of Organic Materials tor Mobile Electronics, 2010-2012, project n°10788, http://www.aramis.admin.ch/Default.aspx?page=Texte&ProjectID=27488



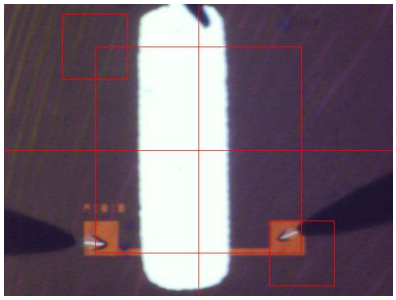
(a) Output.



(b) Mobility.



(c) Transfer.



(d) Micrograph.

Figure 1.28: TG2: Typical characteristics, $W/L = 1$ mm/10 μm, $C_i = 6$ nF/cm^2. FoM: $\mu_{sat} = 4.47\times10^{-2}$ cm^2/Vs, $V_{T,sat} = -4.91$ V, On/Off= 1.34×10^4, $S = 1.8$ V/dec, $I_G/I_D|_{V_{G,max}} = 2.35\times10^{-2}$ and $||I_{ON}|| = 14.2$ A/Fcm^2.

(HNO_3) to define the bottom source/drain contacts. A polymer semiconductor and a polymer dielectric both property of BASF are successively spin-coated and annealed at 90°C. The respective thicknesses are 50 nm and 500 nm whereas the dielectric capacitance is 4.5 nF/cm^2. Finally 100 nm of gold is thermally evaporated through a shadow mask to define the top gate electrode. The simplified process flow is depicted in Figure 1.29.

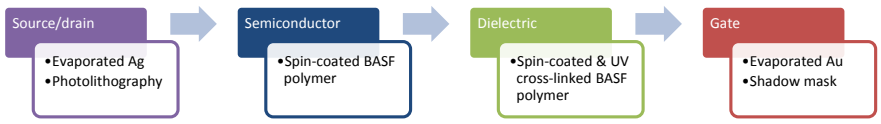
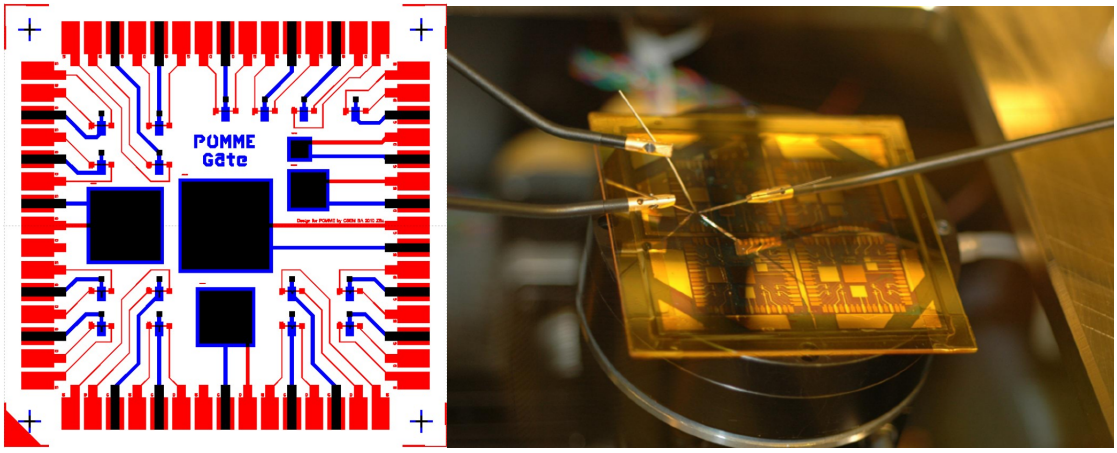


Figure 1.29: Simplified process flow for TG3.

The layout shown in Figure 1.30a comprises 16 OTFTs with channel lengths comprised between 2 and 20 μm and various channel widths.

Electrical characteristics

A fabricated sample is visible in Figure 1.30b whereas typical output and transfer characteristics are given in Figure 1.31.



(a) (b)

Figure 1.30: TG3: (a) 1-inch cell layout and (b) finalized sample with a 2 × 2 array of 1-inch cells which is taped on a glass carrier during the $I-V$ characterization on CSEM's TP-10.

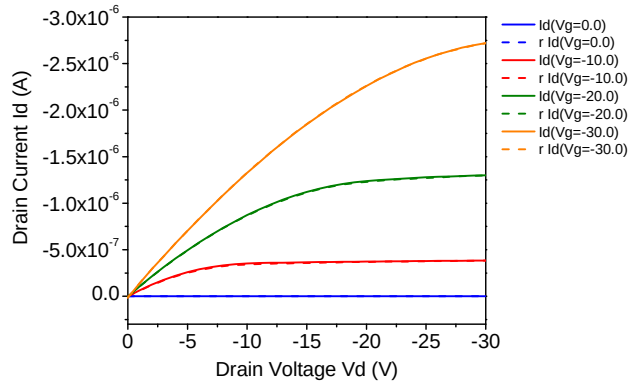
The drain current exhibits a linear behavior at low V_{DS} as well as a proper saturation. The OFF current dominates once more the gate leakage which is a sign of bulk conduction (the semiconductor is not patterned). No hysteresis is visible in the output characteristics as well as in the transfer characteristics, except slightly in the subthreshold regime. The subthreshold regime seems moreover dependent on the drain voltage. This is visible in both the transfer and mobility curves (V_G shift). A closer look shows that this observation is only valid for the forward sweep and thus should be ignored. On one hand, the linear fit to get μ_{sat} is accurate and the $\mu_{sat}(V_G)$ curve is almost constant above $V_{T,sat}$. The obtained value for $\mu_{sat} = 0.11$ cm^2/Vs is really good for a polymer semiconductor. On the other hand, μ_{lin} slowly decreases versus V_G which this time is more related to the contact resistances than the gate leakage. V_{ON} is around 0 V which is ideal. The device picture shows than the different layers are really homogeneous.

The performances of this technology, referred as **TG3** in the rest of the manuscript, are further discussed in Section 1.5. The experimental data of the corresponding OTFTs are mainly used for this thesis in Chapters 2 and 3.

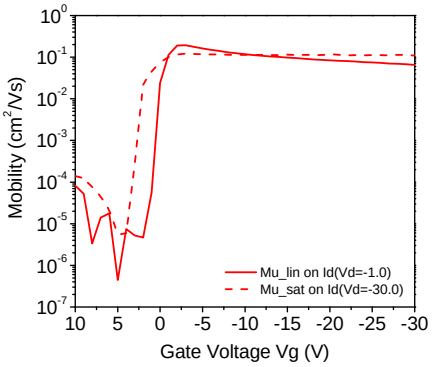
1.4.3 Nano-imprinted and self-aligned OTFTs on 4-inch flexible substrate

The technology described in this section was developed in the framework of the EU FP7 POLARIC[7] project and the reported transistors were available in October 2012. The content of

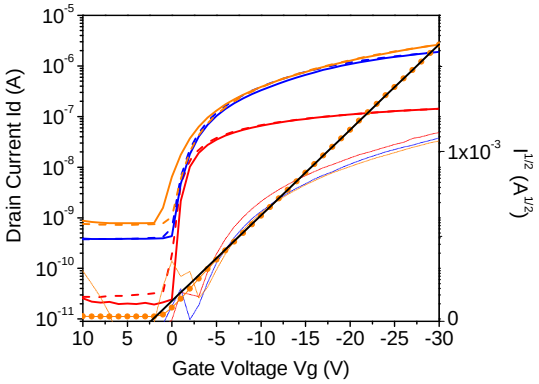
[7] Printable, Organic and Large-Area Realisation of Integrated Circuits, 2010-2014, grant agreement n°247978, http://www.vtt.fi/sites/polaric



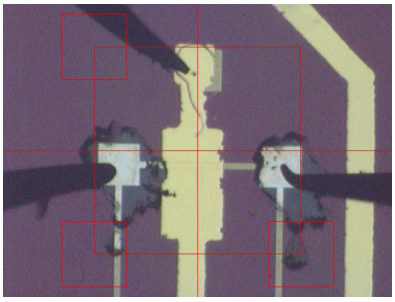
(a) Output.



(b) Mobility.



(c) Transfer.



(d) Micrograph.

Figure 1.31: TG3: Typical characteristics, $W/L = 200\ \mu$m$/20\ \mu$m, $C_i = 4.5$ nF/cm^2. FoM: $\mu_{\text{sat}} = 0.113$ cm^2/Vs, $V_{\text{T,sat}} = 2.39$ V, On/Off$= 3.41 \times 10^3$, $S = 1.9$ V/dec, $I_{\text{G}}/I_{\text{D}}|_{V_{\text{G,max}}} = 1.24 \times 10^{-2}$ and $||I_{\text{ON}}|| = 59.0$ A/Fcm^2.

this section was published in [88].

Process

As gate electrode, aluminum is thermally evaporated onto a 4-inch plastic foil. A sacrificial layer and a UV-NIL resist are applied by spin coating. A 4-inch nickel shim is used as a template for intermediate polymer stamp, which in turn is used for the UV-NIL step to define the gate structure. After etch of the imprinted residual layer and of the aluminum, the double resist layer is stripped in a solvent.

The dielectric is formed applying proprietary BASF material by spin-coating and subsequent UV-curing in ambient atmosphere. The dielectric is structured by photolithography with transfer of the structure through O_2 dry-etching. The devices have a nominal dielectric thickness of 200 nm and an averaged dielectric capacitance $C_i = 17$ nF/cm^2. Source-drain

(S/D) metal contact is structured with self-aligned photolithography. More details about the device fabrication will be published elsewhere [89].

Prior pentacene evaporation by organic molecular beam deposition (without further patterning, $t_{\text{pentacene}} = 30$ nm), surface modification of the gold source-drains contact was performed by means of a heptadecafluoro-1-decanethiol (HDFT) based self-assembled monolayer, while surface modification of the dielectric was realized by a 10 nm poly(alpha-methylstyrene) (PαMS) layer [90] (neglected in C_i). The simplified process flow is depicted in Figure 1.32.

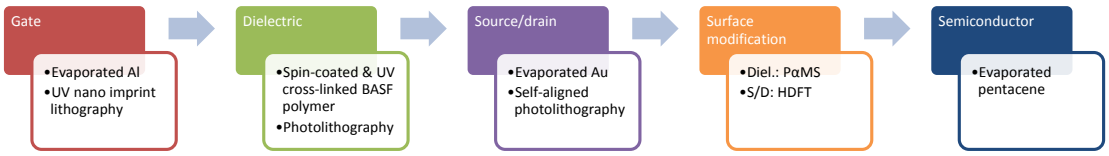
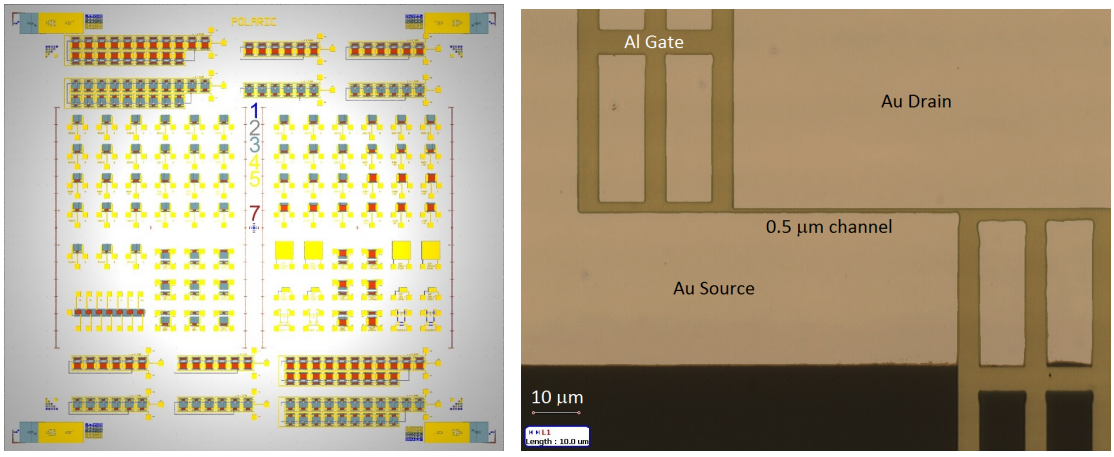


Figure 1.32: Simplified process flow for BG6.

A 2×2 array test layout compatible with this specific fabrication method was designed for modeling purpose. Each 28×25 mm^2 quadrant depicted in Figure 1.33a comprises OTFTs – including sub-micrometer ones as shown in Figure 1.33b – inverters, capacitors (Self-Aligned-NIL compliant design), ring-oscillators and other test structures.



(a) Quadrant layout.

(b) $W/L = 25\ \mu$m$/0.5\ \mu$m.

Figure 1.33: BG6: Test structures quadrant 28 × 25 mm^2 and micrograph showing the channel of a submicron OTFT.

Dummy structures were added uniformly in the design on the NIL area in order to prevent undesired resist displacement resulting in ghost features and ease the lift-off process.

Electrical characteristics

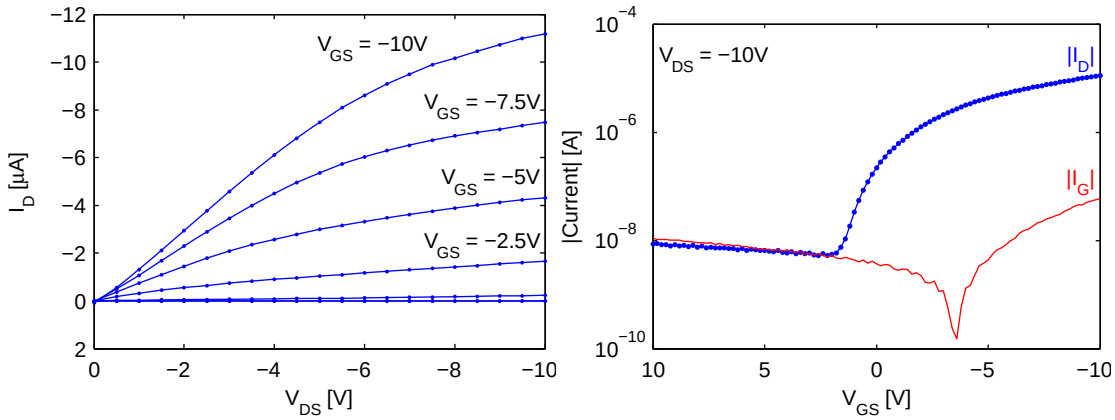
Transistors exhibited typical p-type enhanced mode behaviour when negatively biased, with field-effect mobility, extracted in the saturation regime (μ_{sat}), in the order of 10^{-1} cm^2/Vs.

Table 1.4: Voltage range used to characterize BG6 OTFTs. Forward and reverse sweeps.

	Gate voltage	Drain voltage
Transfer	$10V > V_G > -10V$, with $V_{step} = -0.2V$	$V_D = -10V$
Output	$5V > V_G > -10V$, with $V_{step} = -2.5V$	$0V > V_D > -10V$, with $V_{step} = -0.5V$

Whereas such values are common for large channel lengths (eg. 10 μm and beyond) they are exceptional for channel lengths in the (sub) micrometer range, indicating good charge injection from S/D contacts into the semiconductor [91].

We report average values and standard deviations such as $\overline{\mu_{\text{sat}}} = 0.5$ cm^2/Vs with $\sigma_{relative} = 55\%$ and $\overline{V_{\text{T,sat}}} = 0.6$ V with $\sigma = 1.0$ V.



(a) Output.

(b) Transfer.

Figure 1.34: BG6: Typical characteristics, $W/L = 25$ μm/0.5 μm, $C_i = 17.0$ nF/cm^2. FoM: $\mu_{\text{sat}} = 0.224$ cm^2/Vs, $V_{\text{T,sat}} = 1.66$ V, On/Off= 1.30×10^3, $S = 0.79$ V/dec, $I_G/I_D|_{V_{G,max}} = 5.31\times10^{-3}$ and $||I_{ON}|| = 13.1$ A/Fcm^2.

The performances of this state-of-the-art technology, referred as **BG6** in the rest of the manuscript, are further discussed in Section 1.5. The experimental data of the corresponding OTFTs are the most used for this thesis: especially in Chapters 3, 4 and 5.

Circuits

In terms of circuits, working 5-stage R-Os were obtained. The fastest one, shown in Figure 1.35, oscillates at 12.5 V with an amplitude of 4 V and a frequency of 23.3 kHz which corresponds to a stage delay of 4.29 μs. More details are given in Section 1.5 as well.

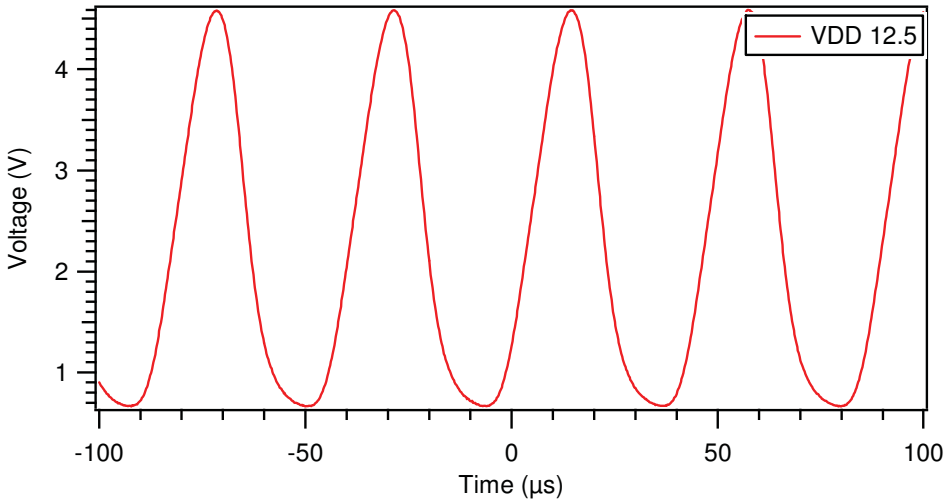


Figure 1.35: BG6 zero-V_{GS} 5-stage ring-oscillator with $L = 5$ μm.

1.4.4 Gravure-printed OTFTs on 4-inch flexible substrate

The technology described in this section was developed in the framework of the CTI SWIPE-GRAPE[8] project and the reported transistors were available in August 2013.

In this technology the materials selected for the semiconductor, the dielectric and the contact modification are all commercially available and are part of the Merck Lisicon product line.

Process

After a cleaning step (acetone and IPA) of the plastic substrate (Melinex ST506), 60 nm of gold is thermally evaporated. A photoresist (S1828) is printed on top using the Labratester-II gravure printer. The printed layer follows the pattern of the gravure cylinder which in this case is the layout of the source/drain layer. Then the photoresist is soft baked at 100°C; the gold layer is patterned by wet etching and finally the photoresist is removed. Thus this process step can be seen as a gravure lithography since a photoresist is used as an etch-mask whereas its pattern was defined by gravure instead of selective UV cross-linking.

The bottom source/drain contacts are then treated with M001 deposited by drop casting which is annealed at 90°C. Next the semiconductor (SP-300) is gravure printed (≈ 100 nm) and annealed at 100°C. Thus among all the studied technologies, this one is the only one featuring a patterned semiconductor layer. Next the dielectric (D320) is gravure printed (1.2 μm) and annealed at 100°C.

Finally 60 nm of gold is thermally evaporated through a shadow mask to pattern the top gate electrode. The gate deposition and patterning was also tested using gravure printing

[8] SWiss Precision Electronic GRAvure PrintEr, 2012-2013, project n°13596, http://www.aramis.admin.ch/Default.aspx?page=Texte&ProjectID=30832

however this led to OTFTs with large gate leakage meaning that the last printed layer dissolved the dielectric layer (non-orthogonal solvents). Thus it is just a matter of finding the proper material combination before getting a fully gravure-printed OTFTs. The simplified process flow is depicted in Figure 1.36.

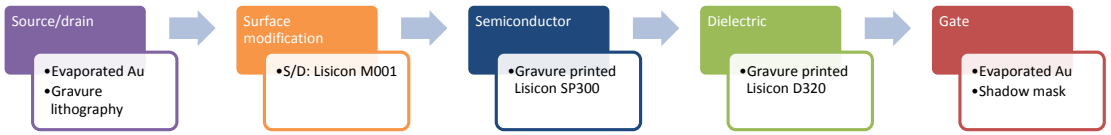
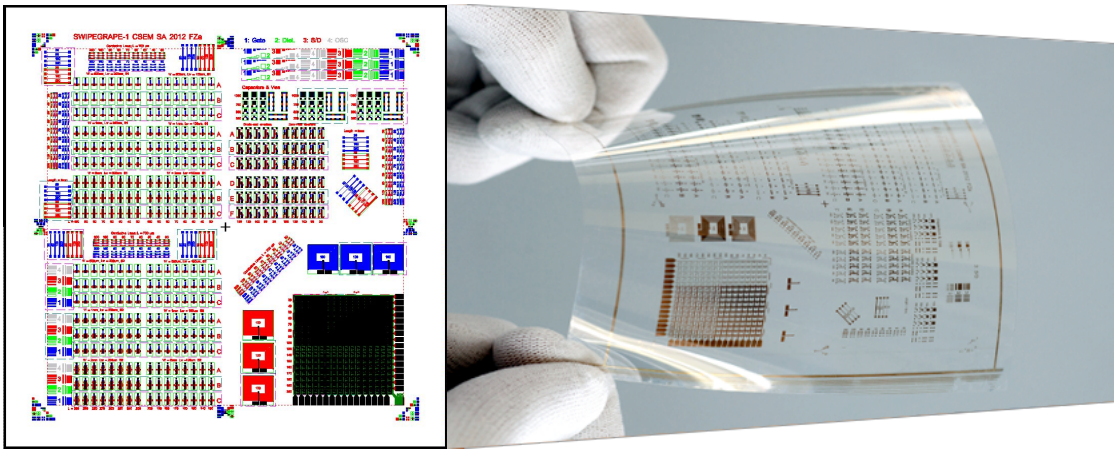


Figure 1.36: Simplified process flow for TG4.

The layout of the 4-inch test structure as well as a gravure-printed sample are depicted in Figure 1.37.



(a) Chip layout.

(b) 4-inch sample done at CSEM.

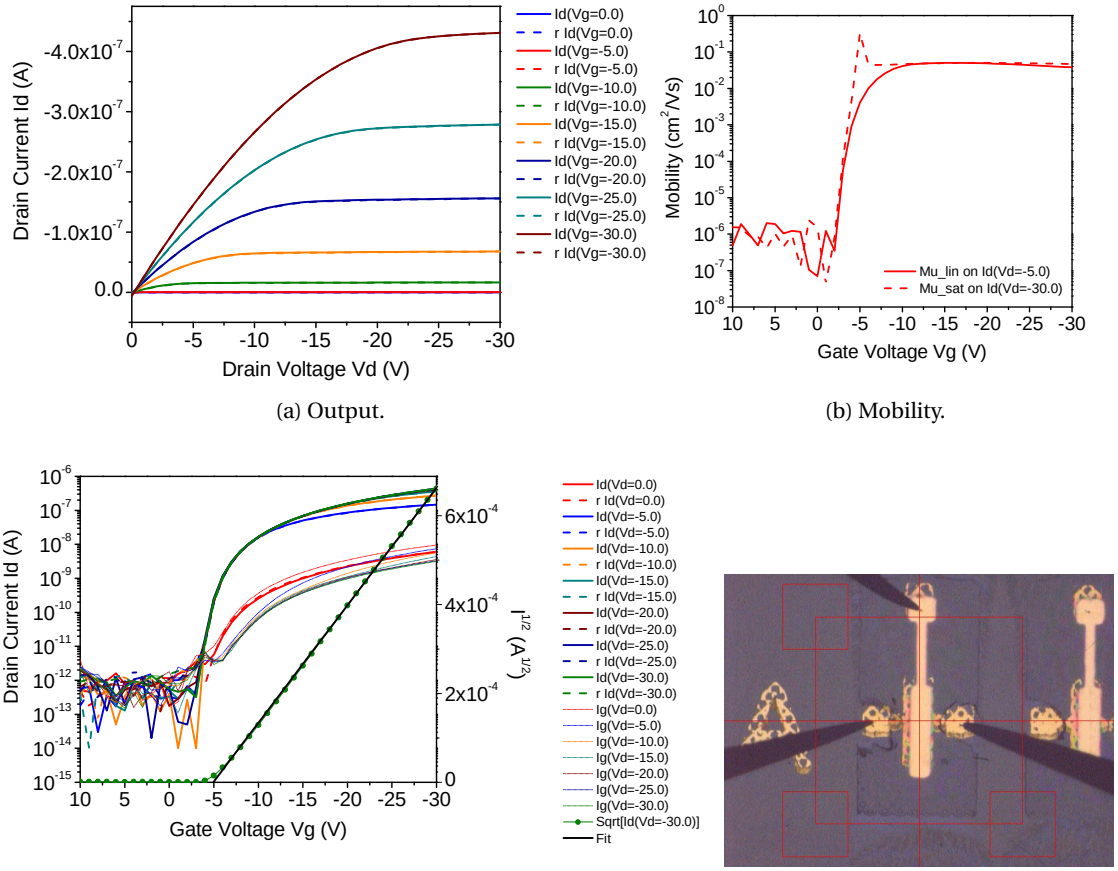
Figure 1.37: TG4

Electrical characteristics

Typical characteristics[9] are given in Figure 1.38.

The obtained OTFTs present almost ideal behavior: the OFF current reaches the noise level of the measurement setup (1 pA), no hysteresis at all, V_{ON} around 0 V. However the structures on the source-drain layer were enlarged due to the spread of the printed photoresist. This last effect actually reduces the channel length and increases the channel width by 70 μm: for the transistor visible in Figure 1.38, its design channel length is 130 μm but the measured one is around 60 μm. Still this channel length is much longer than the other technologies.

[9]Voltage range. Transfer: $10V > V_G > -30V$, with $V_{G,step} = -1V$ and $0V > V_D > -30V$, with $V_{D,step} = -5V$. Output: $0V > V_D > -30V$, with $V_{D,step} = -1V$ and $0V > V_G > -30V$, with $V_{G,step} = -5V$



(a) Output.

(b) Mobility.

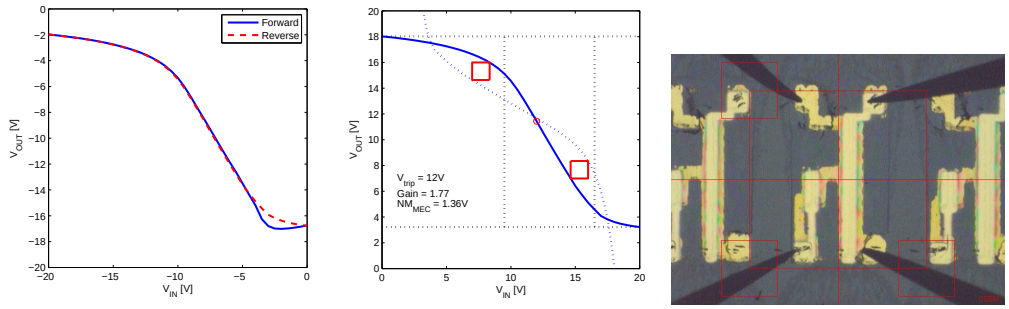
(c) Transfer.

(d) Micrograph.

Figure 1.38: TG4: Typical characteristics, $W/L = 1.07$ mm/60 μm, $C_i = 1.6$ nF/cm^2. FoM: $\mu_{\text{sat}} = 4.91 \times 10^{-2}$ cm^2/Vs, $V_{\text{T,sat}} = -4.94$ V, On/Off= 1.37×10^6, $S = 0.7$ V/dec, $I_G/I_D|_{V_{G,\max}} = 7.22 \times 10^{-3}$ and $||I_{ON}|| = 15.3$ A/Fcm^2.

Circuits

In terms of circuits, working inverters were obtained, see Figure 1.39. Their performance are discussed in Section 1.5.



(a) (b) (c)

Figure 1.39: Typical characteristics of a diode-connected inverter from TG4. (a) raw measurement, (b) post-processed data. V_{DD} = 20 V, L = 100/30 μm (nominal, with ink spread) and W_{load}/W_{driver} = 4 and (c) micrograph.

1.5 Global analysis and assessment of these OTFT platforms

A summary in terms of main processing method, transistor architecture and layer stack is available in Table 1.5 for the 10 technologies screened in this chapter. This table shows the transition from 20 mm silicon substrates to 4 in. plastic foils which took place during this thesis.

1.5.1 Static performances

Transistors

In terms of transistor performance, these 10 technologies are compared in Figure 1.40. This figure shows both the increase of performance and/or reproducibility which illustrates the rapid evolution of this field observed in the organic electronics community. Note that in order to compare the parameter spread, the number of OTFTs involved has to be in the same range.

Figure 1.40 shows that BG1 performs better than BG2, especially in terms of mobility, subthreshold swing and normalized ON current. This can come from the higher ordering of the semiconductive layer – packing of the regioregular P3HT – which eases the charge transport compared to the amorphous film of PTAA. It can also come from a better passivation with OTS of the silicon oxide surface – reducing the trapping process – compared to HMDS. On the other hand BG2 is slightly more reproducible than BG1 which is directly linked to the same reasons which decrease the device performance: the amorphous aspect of PTAA together with the known difficulties to deposit an homogeneous layer of OTS. Reproducibility is more

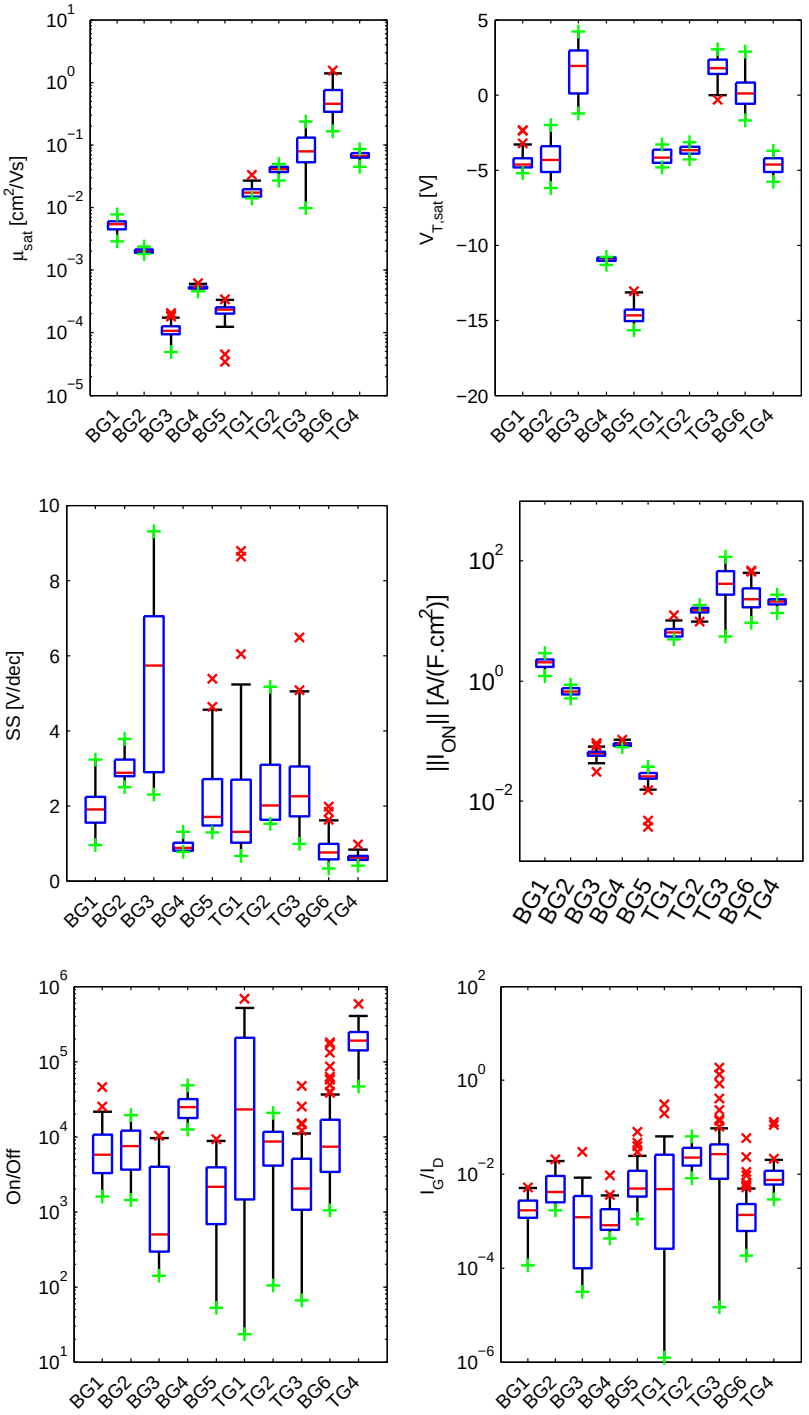


Figure 1.40: Comparison of the used technologies through standard performance parameters. Number of OTFTs per technology: 15 for BG1, 16 for BG2, 22 for BG3, 9 for BG4, 20 for BG5, 14 for TG1, 11 for TG2, 43 for TG3, 103 for BG6 and 21 for TG4. Total: 274 OTFTs.

Table 1.5: Technology summary. The substrate size is expressed in inch. “Topo.”, “SAM” and “OSD” refer to the device topology, surface treatments with self-assembled monolayer and organic semiconductor, respectively. “C” and “P” indicate whether the layer is common to all devices or patterned. “D” and “SD” indicate which layer was treated: the dielectric or the source/drain contacts, respectively. Confidential BASF materials are simply referred as “Polymer”.

ID	Process	Substrate	Size	Topo.	Gate	Dielectric	SAM	OSC
BG1	Photo.	Silicon	0.8	BG-BC	C, Si	C, SiO_2	D	C, P3HT
BG2	Photo.	Silicon	2	BG-BC	C, Si	C, SiO_2	D	C, PTAA
BG3	Photo.	Glass	1	BG-BC	P, ITO	C/P, X-PVP	-	C, P3HT
BG4	Photo.	Glass	1	BG-BC	P, ITO	C, X-PVP	-/D	C, PTAA
BG5	Photo.	Glass	1	BG-BC	P, ITO	P, X-PVP	-/D	C, PTAA
TG1	Photo.	Glass	1	TG-BC	P, Al	C, Cytop	-	C, P3HT
TG2	Photo.	Glass	1	TG-BC	P, Al	C, D139	-	C, P3HT
TG3	Photo.	Foil	4	TG-BC	P, Au	C, Polymer	-	C, Polymer
BG6	SA-NIL	Foil	4	BG-BC	P, Al	P, Polymer	D&SD	C, Pentacene
TG4	Gravure	Foil	4	TG-BC	P, Au	P, D320	SD	P, SP300

relevant than absolute performance, not only for industrial applications but also to define characterization standards through round-robin tests (one goal of the FLEXNET project).

In terms of performances, the PTAA-based technologies can be ordered as follows: BG2 > BG4 > BG5. This shows that the path from a Si/SiO_2 screening platform to circuits on glass with the exact same semiconductor is not straightforward. The HMDS-treated SiO_2 surface was not successfully reproduced with treated (HMDS or PαMS) or not X-PVP to reproduce BG2's performance. Even in BG2's case, the mobility around 2×10^{-3} cm^2/Vs is nowadays totally outdated.

The P3HT-based technologies (BG1, BG3, TG1 and TG2) perform better but the two top-gate architectures (TG1 and TG2) outrival the bottom gate ones in almost every aspect. Secondly TG2 performs better than TG1 both in terms of absolute values e.g. higher mobility around 5×10^{-2} cm^2/Vs (nowadays outdated but enough for some applications) and reproducibility: the data spread of TG2 is more contained than TG1's. This can be explained by the fact that the dielectric used for TG2 comes from the same supplier as the semiconductor and is moreover optimized for this particular semiconductor.

TG3 performs better than TG2 with a mobility around 0.1 cm^2/Vs. The data spread look similar but only 11 OTFTs are represented for TG2 versus 43 for TG3 which is again in favor of TG3. Two weak points of TG3 are the gate leakage (absolute values and spread) and the ON/OFF ratio. In addition no circuit was fabricated with this technology.

BG6 gathers the superlatives: highest mobility (above 1 cm^2/Vs) and normalized ON current, largest range of accounted channel lengths (L_{max}/L_{min} = 20) and OTFTs (103), smallest

channel length (L_{min} = 0.5 μm), lowest subthreshold swing (below 0.5 V/dec) while having a good ON/OFF ratio and reasonable gate leakage. It comes also with the most complicated process flow involving several European partners in order to be fulfilled. In addition, a 23 kHz 5-stage ring-oscillator was obtained. Unfortunately for this thesis, the samples were not available for me to perform the characterization techniques introduced in the next chapter.

The last studied technology, TG4, targets high throughput fabrication (low-cost) while having good performances. The lowest OFF current was obtained thanks to the patterned semiconductor layer. This boosts the ON/OFF ratio and put TG4 just behind TG2 but in a reproducible way. Compared to other technologies with similar number of accounted OTFTs, TG4 is the most reproducible. In addition, circuits were obtained. The only drawback for this thesis is its late availability (August 2013) which prevented deeper analysis e.g. dynamic.

Circuits

Only four out of ten technologies studied in this chapter allow the realization of circuits since they allow interconnections between transistors through the combination of a patterned gate layer and a patterned dielectric (via) layer, namely: BG3, BG5, BG6 and TG4. About circuit performances, the best inverters from BG3, BG5 and TG4 are compared in Figure 1.41 whereas the best 5-stage ring-oscillators from BG3 and BG6 are compared in Figure 1.42. Although BG3's inverters perform better than TG4's, a supply voltage of 40 V is required to get those performance whereas TG4's inverters are still operational at 10 V which is more suitable for practical/portable applications. Note: the used zero-V_{GS} inverter of TG4 is commented in Appendix, Figure A.8.

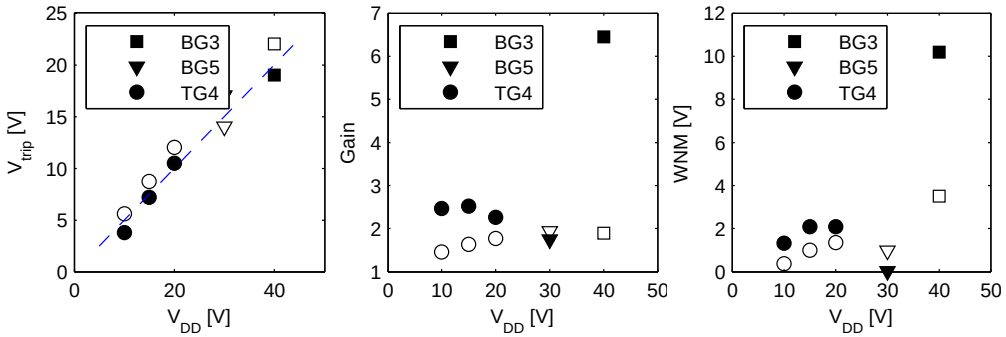


Figure 1.41: Comparison of three used technologies through standard performance parameters of inverters. Filled symbols: zero-V_{GS} topology. Open symbols: diode-connected topology.

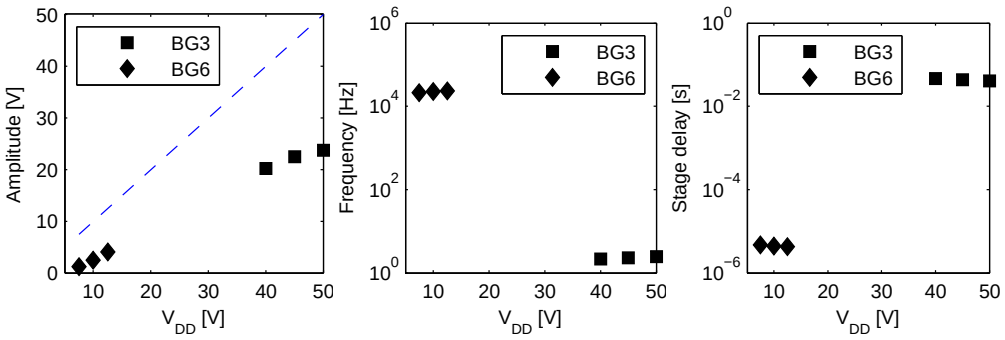


Figure 1.42: Comparison of two used technologies through standard performance parameters of 5-stage ring-oscillators (zero-V_{GS} topology).

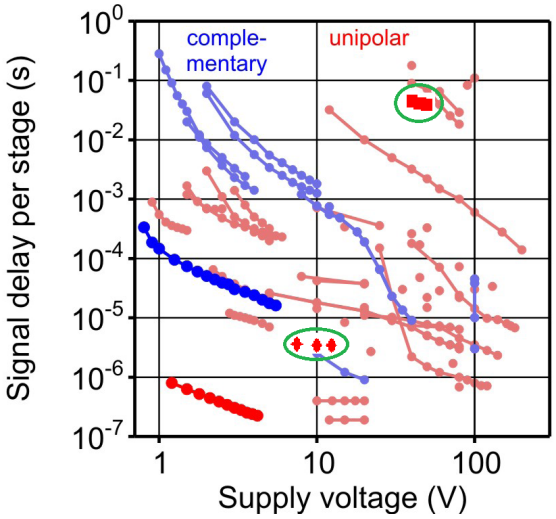


Figure 1.43: Literature summary on the signal delay per stage of organic complementary (light blue) and unipolar (light red) ring oscillators measured in air. Dark blue and red circles: Ante's results [92]. In addition, the results of BG3 and BG6 are also shown with red squares and diamonds, respectively. Adapted from [92].

1.5.2 Dynamic performances

Stage delay of ring-oscillators

Figure 1.42 gives a first experimental comparison of the dynamic performances. However only two out of four technologies are represented in this figure. Indeed ring-oscillators have first to be present in the chip layout, which is not the case for TG4, and working devices are required, which is not the case for BG5. Another aspect is that the extraction of the stage delay gets more precise when the number of inverter stages increases (averaging and better square signal) but the yield decreases at the same time i.e the probability to get a longer ring-oscillator working decreases. In addition, the inverter stage delay is not the same as the intrinsic delay of a single OTFT. All this shows the limits of this method.

The stage delay of BG3 and BG6 are further compared to the state of the art in Figure 1.43 which is originally a graph from Klauk [70] which was adapted in 2011 by Ante [92]. BG6 is in a good position considering the fact that the dielectric and the substrate are a spin-coated polymer and a 4-inch plastic foil whereas Ante's results use AlO_x combined to a SAM (phosphonic acid), and glass wafers, respectively.

Estimated transit frequency

The transit frequency, f_T, can be a better figure of merit but, as explained in the introduction of this chapter, no experimental data is available for any of the studied technology. In the following, an estimation of f_T will be calculated using the MOSFET approach in the saturation regime [75]:

$$f_T = \frac{g_m}{2\pi C_G} \text{ with: } g_m = \frac{W}{L} C_i \mu (V_{GS} - V_T) \text{ and: } C_G = C_i \left(A_{ov} + \frac{2}{3} WL \right) \tag{1.8}$$

$$\text{Thus: } f_T = \frac{W}{2\pi L} \frac{\mu (V_{GS} - V_T)}{A_{ov} + \frac{2}{3} WL} \tag{1.9}$$

A_{ov} designates the overlap area between source/drain and gate electrodes. The value of A_{ov} is given in Appendix A.1 for each technology and transistor layout.

μ_{sat} and $V_{T,sat}$ were used as μ and V_T, respectively, and the estimated f_T is plotted versus the channel length for several technologies in Figure 1.44. BG1 and BG2 are not represented because of their common gate architecture (screening platforms) whereas TG4 is isolated because of the much longer channel lengths.

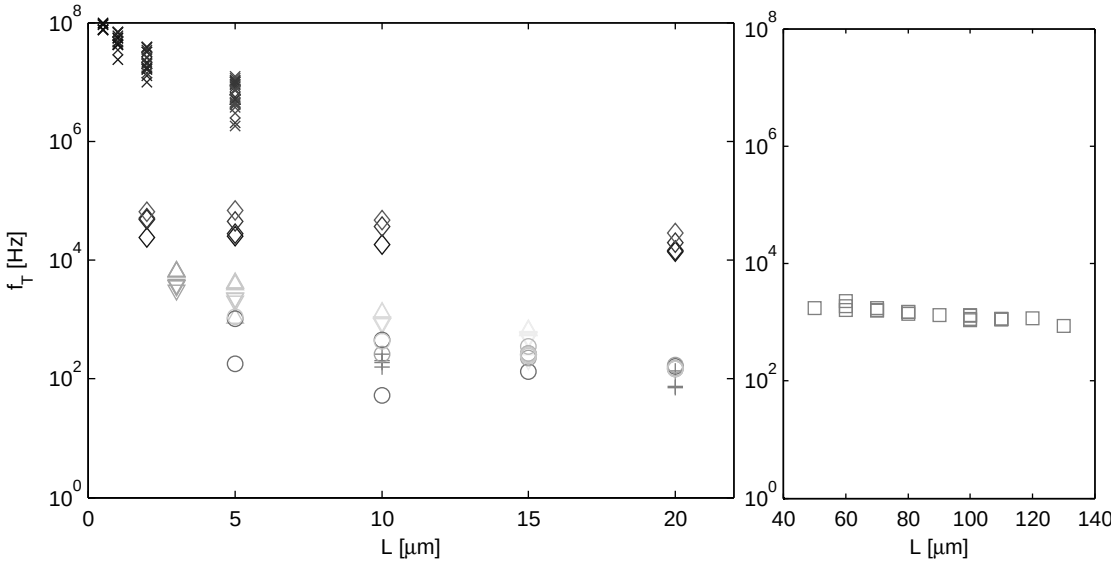


Figure 1.44: Estimation of the transit frequency plotted versus the channel length for different technologies and transistor layouts: BG3 (T1_A, +), BG4 (T3_A, ▽ and T3_B, △), BG5 (IC2 ◯), TG3 (◇), BG6 (×) and TG4 (□, right figure). The darker a marker is, the smaller the channel width is.

1.6 Summary

From these analysis and in my opinion, three technologies exhibit potential at this stage: TG3, BG6 and TG4. They all demonstrate on 4-inch plastic substrates OTFTs as well as circuits (except TG3) which are both well performing and reproducible.

Among these three technological OTFT platforms, TG3 was chronologically speaking the first available. This enabled deeper OTFT characterizations which are reported in the next chapter. However TG3's main drawback is that an additional process step will be required in order to make this technology suitable for circuits (via drilling).

The last studied technology, TG4, has the process flow exhibiting the highest throughput of this chapter. Whereas the static performances of TG4's OTFTs are comprised between those of TG3 and BG6 the dynamic performances are expected to be much lower than those of BG6's submicrometer OTFTs – see Figure 1.44 – because of channel lengths and source/drain-gate overlaps both two orders of magnitude larger.

BG6 is the most performing technological platform introduced in this chapter. Its state-of-the-art performances combined to the available dataset of OTFTs (> 100) make it the right candidate for single device and statistical modeling, respectively performed in Chapters 3 and 4, in order to better evaluate its circuit potential as done in Chapter 5. Nonetheless BG6's main weak point is its process flow which is complex and distributed between several partners.

2 Electrical Characterization

2.1 Introduction

Transistor-wise, the 10 technologies studied in the previous chapter were analyzed and compared using performance parameters extracted from their $I-V$ curves. In this chapter, the $I-V$ characterization platforms and other electrical characterization methods which were used or developed for this thesis will be introduced. These additional tests will bring new inputs to identify potential technology candidates for circuit applications.

Nonetheless those characterization methods were not systematically performed on every technology introduced in the previous chapter. Indeed the different technologies were not available at the same time but generally one after the other. On the other hand these characterization setups were independently developed and also in a serial way.

Table 2.1: Summary of the electrical characterization performed per technology. The platform used to get the $I-V$ curves is refered as "TP" (TP-10), "EP" (EP6) or "Ex" (external). About the stability and shelf columns, the checked technologies are discussed in this thesis but other ones were tested.

ID	$I-V$	Circuits	vs T°C	$C-V$	t_{rise}	Stability	Shelf	Stress
BG1	TP	-	-	-	-	-	-	-
BG2	TP	-	-	-	-	-	-	-
BG3	TP	✓	-	-	-	✓	-	-
BG4	TP/EP	-	-	✓	-	✓	-	-
BG5	TP/EP	✓	-	-	-	✓	-	-
TG1	TP	-	-	-	-	-	-	-
TG2	TP	-	-	-	-	-	-	-
TG3	TP/EP/Ex	-	✓	✓	✓	✓	✓	-
BG6	Ex	✓	-	-	-	✓	-	-
TG4	TP	✓	-	-	-	✓	✓	✓

First the $I-V$ and circuit characterization platforms are described in Section 2.2. The ad-

ditional electrical characterization methods introduced in this chapter are: temperature-dependent $I-V$ measurement (Section 2.3), capacitance-voltage ($C-V$, Section 2.4) measurement, rise-time (t_{rise}, Section 2.5) measurement, stability (mainly hysteresis and air-stability in Sections 2.6.1 and 2.6.2, respectively) as well as shelf (Section 2.6.3) and stress (Section 2.6.4) lifetimes. This is summarized in Table 2.1.

I have either directly contributed to the development of some of these characterization setups – software/hardware parts, including the related post-processing tools – or operated them. The details are given in the following sections.

2.2 Current-Voltage (I-V) characterization tools

Almost all $I-V$ curves present in the previous chapter were measured at CSEM by the TP-10 platform described below.

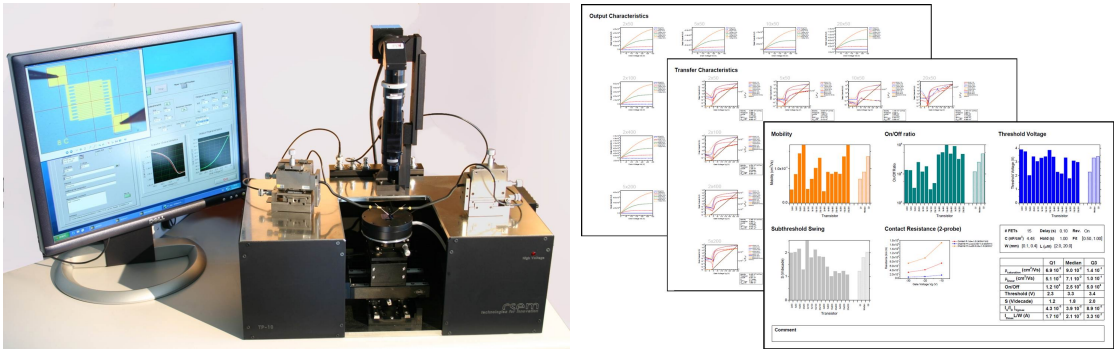
The only exception is the BG6 technology (Section 1.4.3) whose samples were finalized at imec (semiconductor deposition) and thus were characterized at imec. Additionally the temperature-dependent $I-V$ characteristics were measured at EPFL – more details in Section 2.3. In both cases, the characterization equipment used was an Agilent 4156C parameter analyser connected to the probe station through triax cables.

2.2.1 Features of CSEM's TP-10 platform

CSEM's main platform for $I-V$ characterization is the so-called Transistor Prober 10 (TP-10). TP-10 is a CSEM-made system comprising:

- a compact custom-made automated probe station – shown in Fig. 2.1a – placed in a controlled atmosphere (MBRAUN® glovebox filled with nitrogen, with oxygen and moisture level below 3 ppm and temperature at 303 ± 2K) and which is isolated from ambient light during the measurement,
- an Agilent® 4155C parameter analyzer connected through coaxial cables,
- a computer program developed with LabVIEW™ 8.5 (also visible in Fig. 2.1a) which controls the probe station, the measurement itself and takes micrographs of the measured devices (visible in the previous chapter) and
- a computer program (automatically called at the end of the measurement) which post-processes the raw data to generate PDF reports with the transfer, output and mobility curves as well as the statistics of the extracted standard IEEE-1420 performance parameters (threshold voltage, On/Off ratio...). The software also extracts the 2-probe contact resistance by the transmission line method (see Section 3.3.1). A preview of such generated report is given in 2.1b. **I was directly involved** in the development (upgrade)

of this post-processing software called *OFET Suite* using OriginPro® 8.5.1G. More details in Figure A.9. In addition, the transistor performance parameters can be automatically loaded into an Excel® database e.g. for tracking the best devices among all filed ones.



(a) Automated probe station.

(b) Generated PDF report.

Figure 2.1: Overview of the Transistor Prober 10 (TP-10) platform.

The current noise measured on TP-10 with a medium integration time (20 ms) is 1 pA. A long integration time (200 ms) reduces further the noise level but the measurement is slower and the longer bias time can affect the performance of the OTFT (continuous bias-stress [93]). Thus the minimum OTFT OFF current that TP-10 can measure in its standard configuration is 1 pA. In addition, the measurement time is below 5 min/OTFT with the "standard" voltage settings used in the previous chapter (see Table 1.2). Such high characterization throughput is rare in Europe as demonstrated within the FLEXNET[1] project: 11 European partners measured 30% of the nearly 4600 OTFTs produced whereas CSEM alone could measure the remaining 70%.

Not only the TP-10 platform can automatically measure the $I-V$ curves of OTFTs but it can also automatically measure the transfer curves of inverters. The inverters reported in the previous chapter were characterized in this way. The inverter performance parameters described in the previous chapter (gain, noise margins...) are then extracted by a MATLAB® routine **I wrote**.

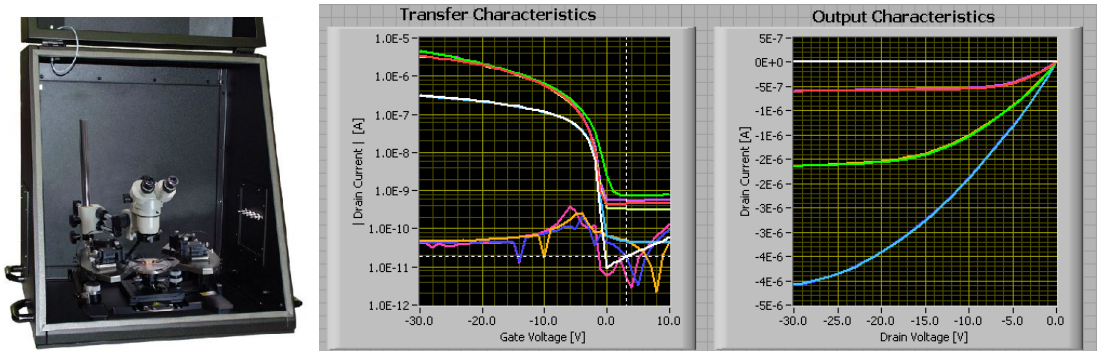
The TP-10 platform can also be used as a simple probe station connecting a sample to other measurement equipments operated either manually (e.g. for oscillators) or by controlling software developed for single devices e.g. $C-V$ (see Section 2.4), rise-time (see Section 2.5)...

To measure the BG3 oscillator reported in Section 1.3.1, a voltage-follower, embedding a Texas Instruments® OPA445 powered by an Agilent® 33250A, is mounted on the probe to act as an impedance buffer between the device and the Tektronix® TDS 3034 oscilloscope. V_{DD} and V_{SS} are supplied by a Keithley® 2400.

[1] Network of Excellence, 2010-2013, grant agreement n°247745, http://www.noe-flexnet.eu

A modular approach was developed in 2013 during a summer internship **I supervised** which can fully automatize these single-device measurement software/setups.

2.2.2 Features of the CascadeMicrotech EP6 platform



(a) Manual probe station.

(b) Raw data of OTFTs measured in air (TG3).

Figure 2.2: Overview of the Electrical Prober 6 (EP-6) platform.

CSEM has another $I-V$ characterization platform which was bought off-the-shelf. It comprises an EP6 manual probe station from CascadeMicrotech placed into a light-tight and electrically-shielded box (ShieldEnclosure SE750/EMC) which isolates the setup from electromagnetic interferences as shown in Figure 2.2a. The EP6 platform is in ambient atmosphere which allows characterization in air to assess the air-stability of organic transistors (see Section 2.6.2) but also to make quick tests on devices (e.g. capacitors, resistors...) by skipping the sample transfer to the glovebox. For $I-V$ characterization, EP6 is connected to an Agilent 4145B parameter analyzer through triax cables. I have slightly adapted the software operating the 4145B (preview in Figure 2.2b) for this purpose.

The Agilent 4155C of TP-10 can also be connected to EP-6 for low-noise $I-V$ measurement in air. The current noise measured with a medium integration time (20 ms) is 1 pA with the 4145B and 500 fA with the 4155C.

2.3 Temperature-dependent measurement

Temperature-dependent current-voltage measurement is a fundamental characterization method for charge transport study and modeling. Such measurements were performed at EPFL with a Süss MicroTec PMC-150 (in vacuum) and with the following procedure.

First the chamber is cooled from room temperature down to 200K using liquid nitrogen. After a stabilization time of 30 min, the first transfer characteristics is measured with the voltage settings gathered in Table 2.2. Then the temperature is increased by 20K and after a stabilization time of 15 min, the next characteristics is measured. The measurement loop

continues up to 300K.

Table 2.2: Voltage settings used for the temperature-dependent measurement. Forward sweep only.

	Start	Stop	Step
Gate voltage	2 V	-8 V	-0.1 V
Drain voltage	-0.1 V	-8.1 V	-1 V

Only one sample, TG3, and more particularly one single OTFT could be measured. The related raw measurements are visible in Figure 2.3 and are used in this thesis in the next Chapter.

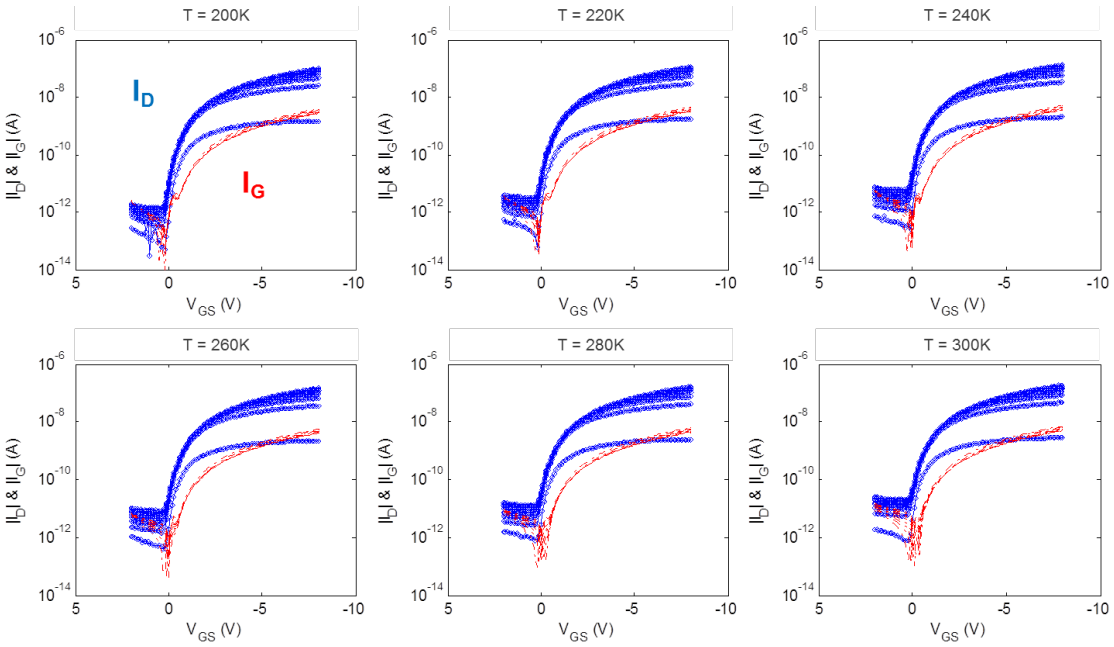


Figure 2.3: Raw temperature-dependent measurement of a TG3 transistor with W/L = 400 μm/20 μm, C_i = 4.48 nF/cm^2. I_D (blue) and I_G (red).

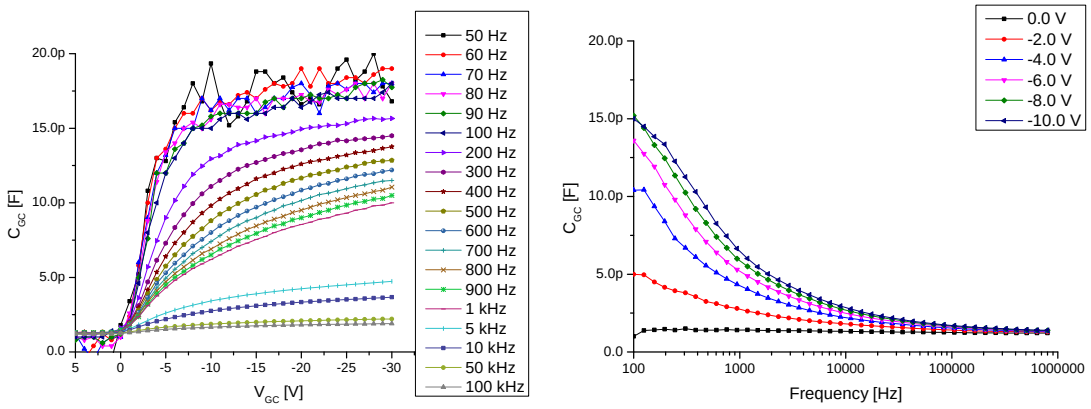
An additional step was added at 220K (and remaining upper temperatures) to the measurement loop described above. After the acquisition of the $I-V$ curves, the chamber light shutter is removed and the light of the microscope is set to its maximum intensity (value?). Then the transfer curves are measured again. This allows studying the impact of the photocurrent versus temperature as done in the next Chapter (Section 3.2).

2.4 Capacitance-Voltage (C-V) characteristics

In Chapter 1, the capacitance of the dielectrics were measured on capacitors with a low-frequency LCR meter (HP 4192A) using a sine signal of amplitude 1 V and frequency 1 kHz.

To perform $C-V$ measurement of transistors, the source and drain contacts are shorted

(V_{DS} = 0 V) and an additional bias, V_{GC}, is applied between the gate and the contacts and swept. Five capacitance values are measured per voltage step and averaged in order to reduce the noise level. $C-V$ and $C-f$ curves of a TG3 OTFT are available in Figure 2.4.



(a) C-V curves.

(b) C-f curves.

Figure 2.4: Raw capacitance versus voltage or frequency of a TG3 OTFT with W/L = 100 μm/20 μm.

The capacitance increases and saturates as the gate voltage decreases (p-type OTFT), indicating the formation of an accumulation channel. However the capacitance decreases when the frequency of the applied signal increases showing that the accumulation channel cannot follow the AC signal anymore. This might be attributed to non-quasi-static effects in the channel, the low mobility of the organic semiconductor and/or the interfacial states.

The measured capacitance has two main contributions: from the channel, C_{ch}, and from the overlap capacitance, C_{ov}, between the gate and the source/drain electrodes, which can be directly read on the $C-V$ curve in the OFF regime of the transistor where there is no channel. $C_{ov}(V_{GS} = 5V) \approx 1.2$ pF gives $C_i = C_{ov}/A_{ov} = 4.7$ nF/cm^2 which is close to the value measured on larger capacitors: 4.5 nF/cm^2. The area A_{ov} of a TG3 transistor layout is given in Appendix whereas the channel area is WL (finger topology). In addition $C_{ov} \approx C_{GC}(V_{GS} = 0V)$ is independent from the frequency as shown in Figure 2.4b which confirms that C_{ov} is not related to the channel.

2.4.1 Split C-V

In this section, the $C-V$ and $I-V$ characteristics are combined to extract the effective mobility, μ_{eff}, through the split $C-V$ technique [94]. The approach which follows was already reported for top-contact pentacene OTFTs by Ryu *et al.* [95] using quasi-static $C-V$ (QSCV).

First the induced channel sheet charge carrier density Q_i is extracted from the $C-V$ data.

$Q_i(V_{GC})$ is calculated as:

$$Q_i(V_{GC}) = \int_{+\infty}^{V_{GC}} \frac{C_{ch}}{A_{ch}} dV \approx \int_{5\,V}^{V_{GC}} \frac{C_{GC} - C_{ov}}{WL} dV \tag{2.1}$$

This is performed in Figure 2.5a. Then the drift mobility is calculated as:

$$\mu(V_{GS}) = \frac{L}{W} \frac{I_D(V_{GS}, V_{DS,lin})}{Q_i(V_{GS}) V_{DS,lin}} \tag{2.2}$$

Note: the largest channel length available on the TG3 sample (20 μm) was used to minimize effects of the contact resistance. This hypothesis is validated in Section 3.3.1.

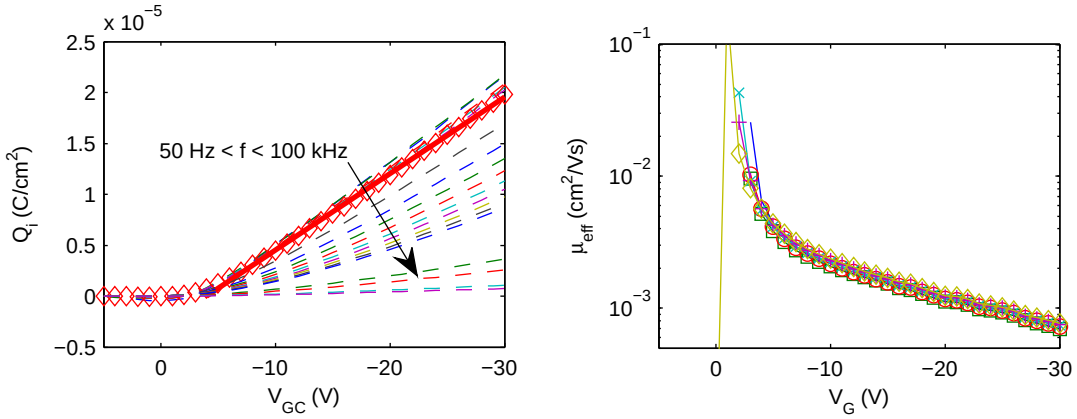


Figure 2.5: Induced charge density (a) and extracted mobility (b) versus gate voltage. Same transistor and frequencies as in Figure 2.4a. In (a), red markers: data at $f = 100$ Hz, red line: linear fit. In (b), $f = 50$ (–), 60 (□), 70 (∘), 80 (×), 90 (+) and 100 Hz (◊).

In Figure 2.5a, the 100 Hz frequency is selected because its $C-V$ curve is less noisy than for the lower frequencies while still being located on the quasi-static plateau visible in Figure 2.4a. The linear fit of $Q-V$ gives $Q_i = C_G(V_G - V_T)$ with $C_G = 752$ nF/cm^2 and $V_T = -4$ V. The strong accumulation charge approximation gives $Q_i \approx C_i(V_G - V_T)$ but here there is a mismatch between C_G and C_i: $C_G = 167C_i$. There is also a mismatch on V_T when compared to $V_{T,lin} = 0.44$ V – chosen since the extraction occurs in the linear regime.

A possible explanation is that trapped charges which do not contribute to the channel current are modulated and thus detected by the $C-V$ measurement. This was also reported by Ryu *et al.* [95] as: $Q_i = Q_{free} + Q_{trapped}$. In addition, since the semiconductor is not patterned and overlapped by the gate over an area larger than the channel itself, parasitic channels can increase the effective channel area. Note that the effective area required to validate the strong accumulation charge approximation is: $A_{eff} = 743 \times 450$ μm^2. This could be correlated to the main area of the gate electrode above the channel which is 800×450 μm^2. However

this is not straightforward to demonstrate since gate interconnects further extend this area. More experimental data would be required with different gate electrode areas and additional comparison with OTFTs with patterned semiconductor.

The maximum value obtained at f = 100 Hz for the mobility is 0.183 cm^2/Vs, see Figure 2.5b, whereas μ_{lin} = 0.226 cm^2/Vs and max($\mu_{\text{lin}}(V_G)$) = 0.299 cm^2/Vs. Additionally μ_{eff} drops down to 7.65×10^{-4} cm^2/Vs whereas $\mu_{lin} = 4.28\times10^{-2}$ cm^2/Vs, both at -30 V. The fact that $\mu_{eff} < \mu_{lin}$ can come from Q_{trapped}, which will overestimate the mobile charges and underestimate the mobility as confirmed in [95], and/or contact resistance effects [96].

Thus this method and obtained results are not further used for this thesis.

2.5 Rise-time measurement

In this section, the setup measuring the response of OTFT to an Heaviside step function is described. This is done by applying long-enough voltage pulses to the gate while measuring the rise-time (t_{rise}) of the drain current between its 10%-90% values. This gives the switching speed of the transistor and thus a figure-of-merit for the dynamic performance.

An autonomous setup was built including the hardware and the controlling software. This task was the main objective of a Bachelor Thesis [97] I supervised. The second objective of this Bachelor Thesis was to build an automated transit frequency (f_T) measurement setup as described in [98]. This latter task was fulfilled but not tested and thus will not be further discussed in this thesis.

The rise-time measurement setup includes a pulse generator (Agilent 33250A), an impedance matching resistor to actually get the desired pulse shape onto the gate, a resistor (R) to convert the current to a voltage (amplified by R) and a buffer amplifier (PCB-mounted with BNC connectors) to match the impedance with the output unit: an oscilloscope (Tektronix TDS3430). The equivalent circuit of the whole system including the capacitance of the cables is shown in Figure 2.6.

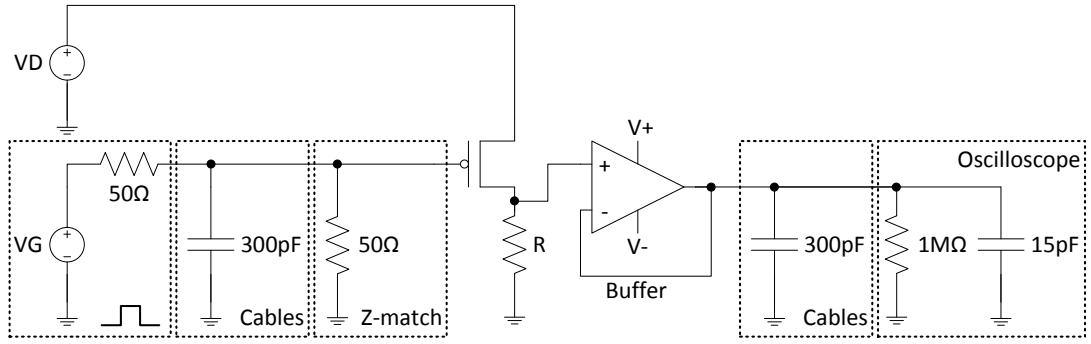


Figure 2.6: Equivalent circuit of the rise-time measurement setup (for a p-type OTFT, VD and VG are negative). Adapted from [97].

The developed system allows both direct and pseudo-differential measurement. In the latter case, a first measurement is performed at $V_{DS} = 0$ V. Then the actual measurement (at the user-defined value of V_{DS}) is performed [99]. Finally they are subtracted to get the signal used to extract t_{rise}: $Signal(V_{DS}) - Signal(V_{DS} = 0V)$. This is useful for noisy or spiky signals. This feature was not required for the measurements reported in this section.

A cut-off frequency can be associated from the measured rise-time. This can be done by using as model a single stage low-pass RC network and its time constant $\tau = RC = 1/(2\pi f_H)$. Through the step response of such network the link to the rise-time (10%-90%) can be obtained: $t_{\text{rise}} = \tau \ln 9$ (demonstration in Appendix, Section A.2). Therefore:

$$f_H = \frac{\ln 9}{2\pi t_{\text{rise}}} \tag{2.3}$$

All these steps are performed automatically with a user-friendly interface visible in Figure 2.7. This figure also shows the results for a TG3 OTFT with $W/L = 100\ \mu$m$/2\ \mu$m. The complete set of measured rise-time are studied in the next chapter in Section 3.6.

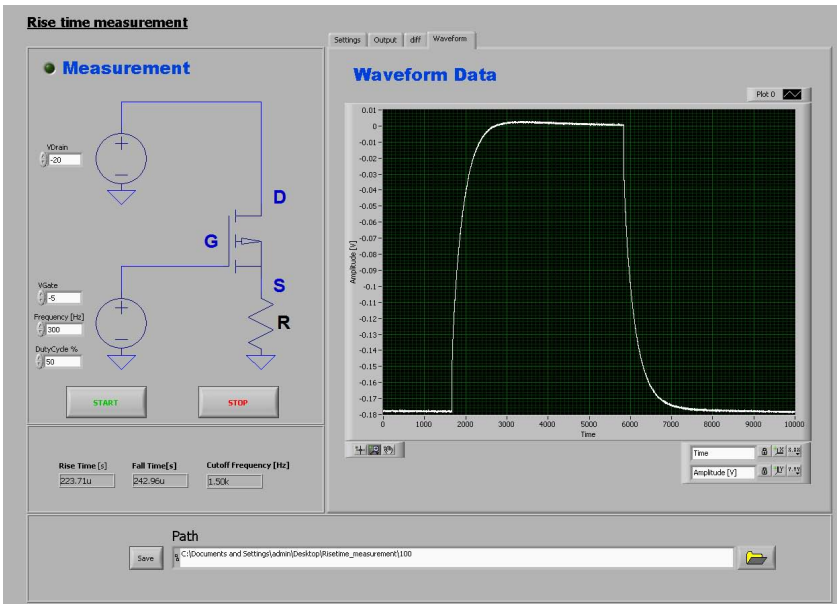


Figure 2.7: User interface and raw rise-time measurement of a TG3 OTFT: at $V_{GS} = -5$ V and $V_{DS} = -20$ V, $t_{\text{rise}} \approx 224\ \mu$s and $f_H \approx 1.56$ kHz. Adopted from [97].

Last but not least, this setup can also measure the rise-time of inverters by simply removing the resistor R.

2.6 Stability and lifetime

2.6.1 Early electrical stability

In this section, two methods are introduced which assess, what I refer, as "the early electrical stability". The first method is an analysis of the current variations between the forward and the reverse sweep of the transfer characteristics (hysteresis with potential V_T shift). In the second one, the current variations between the transfer and output characteristics are analyzed. A quantification of these variations is proposed in the next sub-sections using the relative error (RE) to be then able to automatize the detection of such variations.

Hysteresis

Using the following notation $I_{\mathrm{D,TR}} = I_{\mathrm{D}}$(Transfer characteristics, reverse sweep) and $I_{\mathrm{D,TF}} = I_{\mathrm{D}}$(Transfer characteristics, forward sweep) gives the following formula for the hysteresis:

$$RE_{\text{hysteresis}} = \left| \frac{I_{D,TR} - I_{D,TF}}{I_{D,TF}} \right| \tag{2.4}$$

This is performed for every available (V_{GS}, V_{DS}) data point and then the average gives the final result, as shown below:

$$\overline{RE_{\text{hysteresis}}} = \frac{1}{n(V_{GS})\, n(V_{DS})} \sum_{i=1}^{n(V_{GS})} \sum_{j=1}^{n(V_{DS})} \left| \frac{I_{D,TR}\left(V_{GS,i}, V_{DS,j}\right) - I_{D,TF}\left(V_{GS,i}, V_{DS,j}\right)}{I_{D,TF}\left(V_{GS,i}, V_{DS,j}\right)} \right| \tag{2.5}$$

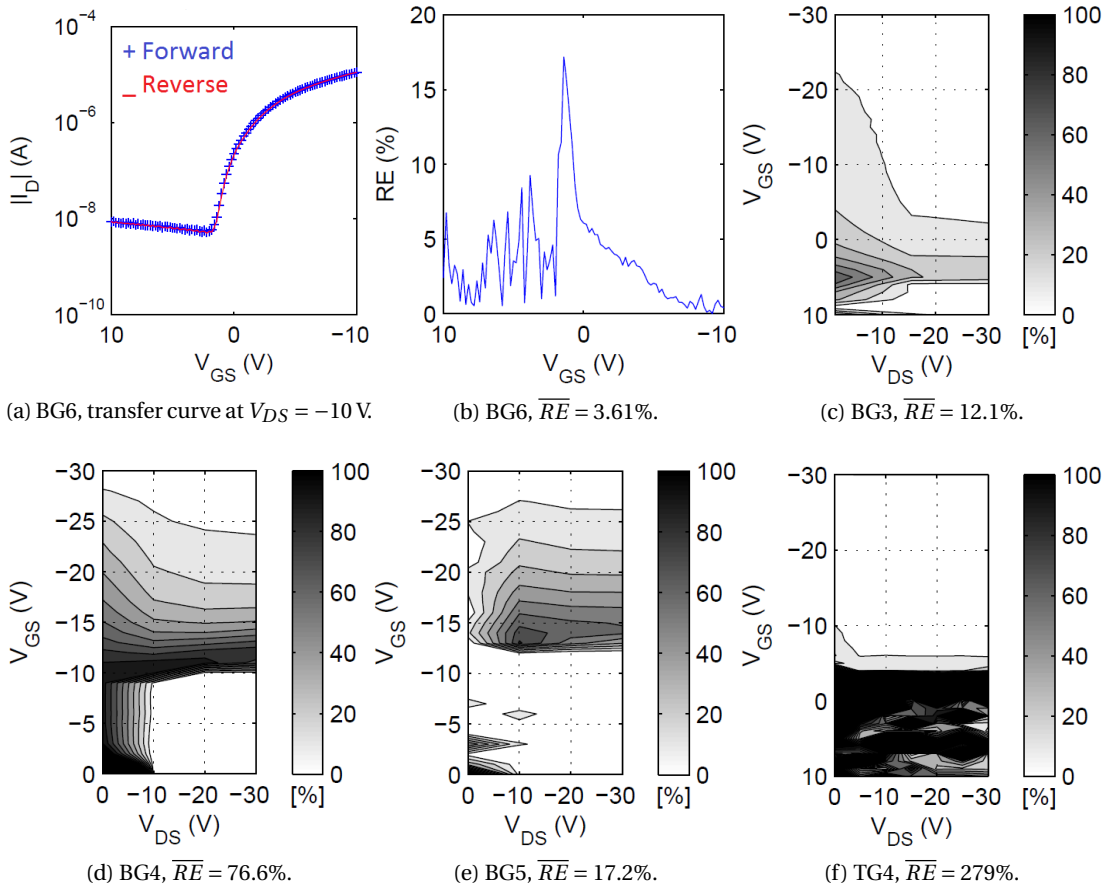
This process is illustrated on a hysteresis-free submicron OTFT of the technology BG6 in Figures 2.8a and 2.8b which gives an average relative error of 3.6% and a maximal relative error of 17%. For the other technologies represented in Figure 2.8, the V_{DS}-dimension is added resulting in a relative error map.

In the previous chapter the hysteresis was analyzed for the different technologies in a qualitative way. It turned out that the BG4 and BG5 technologies exhibit a large hysteresis. This is confirmed by this quantitative analysis. Indeed they exhibit the largest mismatch when compared to BG6 and BG3, as visible in Figure 2.8. However two issues rise:

1. The difference between the obtained values of $\overline{RE_{\text{hysteresis}}}$ for BG5 and BG3 is only of 5.1% which makes the definition of a hysteresis-detection threshold not so robust.

2. the overview given by these relative error maps shows another limit of confidence of $\overline{RE_{\text{hysteresis}}}$: indeed for TG4, there is no hysteresis at all (see Section 1.4.4) but, because of the noisy OFF current, the obtained value of $\overline{RE_{\text{hysteresis}}}$ is higher than BG4's and BG5's.

The second issue can be solved by starting the calculation above the turn-on voltage of the



(a) BG6, transfer curve at $V_{DS} = -10$ V. (b) BG6, $\overline{RE} = 3.61\%$. (c) BG3, $\overline{RE} = 12.1\%$.

(d) BG4, $\overline{RE} = 76.6\%$. (e) BG5, $\overline{RE} = 17.2\%$. (f) TG4, $\overline{RE} = 279\%$.

Figure 2.8: Forward and reverse sweep mismatch (hysteresis) of the transfer characteristics. $\overline{RE_{\text{hysteresis}}}$ is here noted $\overline{RE}$. Each gray level in the relative error maps depicts a 10% step. The selected OTFTs are the same as in Chapter 1.

transistor to remove the OFF regime: the obtained value of $\overline{RE_{\text{hysteresis}}}$ for TG4 decreased from 279% to 3.87%, see Table 2.3, and TG4 this time well-recognized as hysteresis-free.

The first issue comes from the relative error calculation. Indeed a reference has to be chosen to make the error "relative". In Equation 2.4, $I_{D,TF}$ was chosen as reference for the only reason that the forward sweep is measured first. But with this definition, the relative error will quickly saturate to 100% when $I_{D,TR} \ll I_{D,TF}$. This actually occurs in the sub-threshold regime where the hysteresis was the most observed in the previous chapter. In the particular case of BG4 and BG5, this issue can be solved by using $I_{D,TR}$ as reference.

With $I_{D,TR}$ as reference and without the OFF regime, the difference between a hysteresis/-free (BG5/BG3) OTFT increases from 5% to 33%, see Table 2.3.

In order to prevent the dominance of one sweep or the other and thus to increase the robust-

Table 2.3: Hysteresis quantification methods. Mean relative error ($\overline{RE}$) with $I_{D,TF}$ or $I_{D,TR}$ as reference and with or without ("ON") the OFF regime.

	$\overline{RE}\|I_{D,TF}$	$\overline{RE}\|I_{D,TF}$, ON	$\overline{RE}\|I_{D,TR}$, ON	$\overline{RE_{\text{hysteresis, 2}}}$, ON	$\|\Delta V_T\|$
BG6	3.61%	3.48%	3.76%	3.61%	0.10 V
BG3	12.1%	11.7%	16.2%	13.3%	0.20 V
BG4	76.6%	30.5%	124%	43.0%	1.05 V
BG5	17.2%	23.8%	49.4%	30.7%	1.03 V
TG4	279%	3.87%	6.07%	5.07%	0.09 V

ness of the method, the average signal can be used as follows:

$$\overline{RE_{\text{hysteresis, 2}}} = 2\left|\frac{I_{D,TR} - I_{D,TF}}{I_{D,TR} + I_{D,TF}}\right| \tag{2.6}$$

This makes the difference between a hysteresis/-free (BG5/BG3) OTFT slightly decreases to 17%, see Table 2.3.

Finally, to further increase the robustness of the method, the value of the relative error can be compared with the absolute V_T-shift, $|\Delta V_T|$. by defining thresholds for both $\overline{RE_{\text{hysteresis, 2}}}$ and $|\Delta V_T|$. In terms of $|\Delta V_T|$ the difference between a hysteresis/-free (BG5/BG3) OTFT is of 0.83 V.

Transfer-Output mismatch

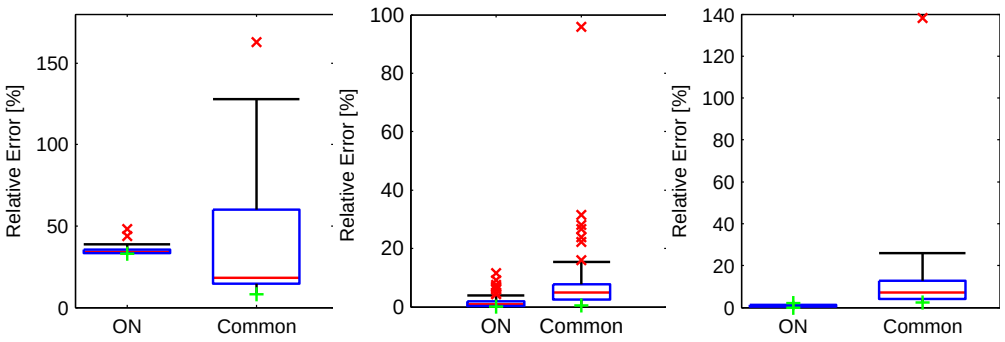
The current variations between the transfer and output characteristics are analyzed in the very same way except that common (V_{GS}, V_{DS}) points have to be first identified between the two characteristics.

A starting-point indicator is the mismatch of the ON current, $I_{\text{ON}} = I_{\text{D}}\left(V_{\text{GS,max}}, V_{\text{DS,max}}\right)$, which is calculated as in Equation 2.4 by replacing $I_{\text{D,TR}}$ and $I_{\text{D,TF}}$ by $I_{\text{ON,OF}}$ and $I_{\text{ON,TF}}$, respectively ("OF" meaning Output characteristics, Forward sweep).

The ON current variations as well as the transfer and output characteristics mismatch are shown in Figure 2.9 for an unstable technology (e.g BG5) and two stable ones (e.g. BG6 and TG3). The difference between un-/stable technologies is clearly shown.

2.6.2 Air stability

Two technologies were tested in air (with EP6 cf. Section 2.2.2): BG4 and TG3. The technologies based on P3HT were not because of the known photo-oxidation of P3HT [100]. The air stability has to be checked for application purposes: if successful, the need of a complex encapsulation system decreases. In my case, I had to assess the air stability in order to identify a candidate technology which could withstand the unavoidable air exposure during the sample transfer



(a) BG5, 16 common points. (b) BG6, 4 common points. (c) TG3, 121 common points.

Figure 2.9: Transfer and output characteristics mismatch: ON current only and other common points.

from the sample carrier to the cryostat for temperature-dependent measurement at EPFL. In other words, to be able to run those measurements the sample had to be air-stable.

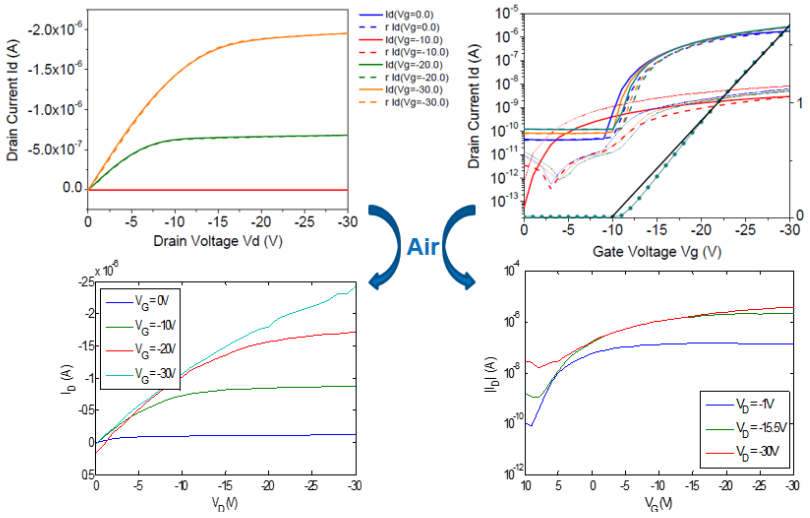


Figure 2.10: BG4 OTFT measured in N_2 and in air.

As visible in Figure 2.10, the semiconductor and/or dielectric of the BG4 OTFT got doped [101]: the threshold voltage shifted from -9.8 V to 7.6 V *i.e.* ΔV_T = 17.4 V, while the OFF current increased making the On/Off ratio decreased from $2.4E4$ to $1.4E2$. The other performance parameters (mobility, gate leakage ratio, normalized ON current) remained more or less stable (slight increase of the ON current because of doping). However this shows that BG4 (and thus BG5) are not air-stable.

On the other hand, the performance parameters of the TG3 OTFT are stable and even slightly improve as depicted in Figure 2.11. The threshold voltage only shifts of ΔV_T = 0.31 V, the ON current increases of 8%, the ON/OFF ratio increases by 54% because the OFF current also slightly improves, the mobility increases of less than 2% and the subthreshold swing

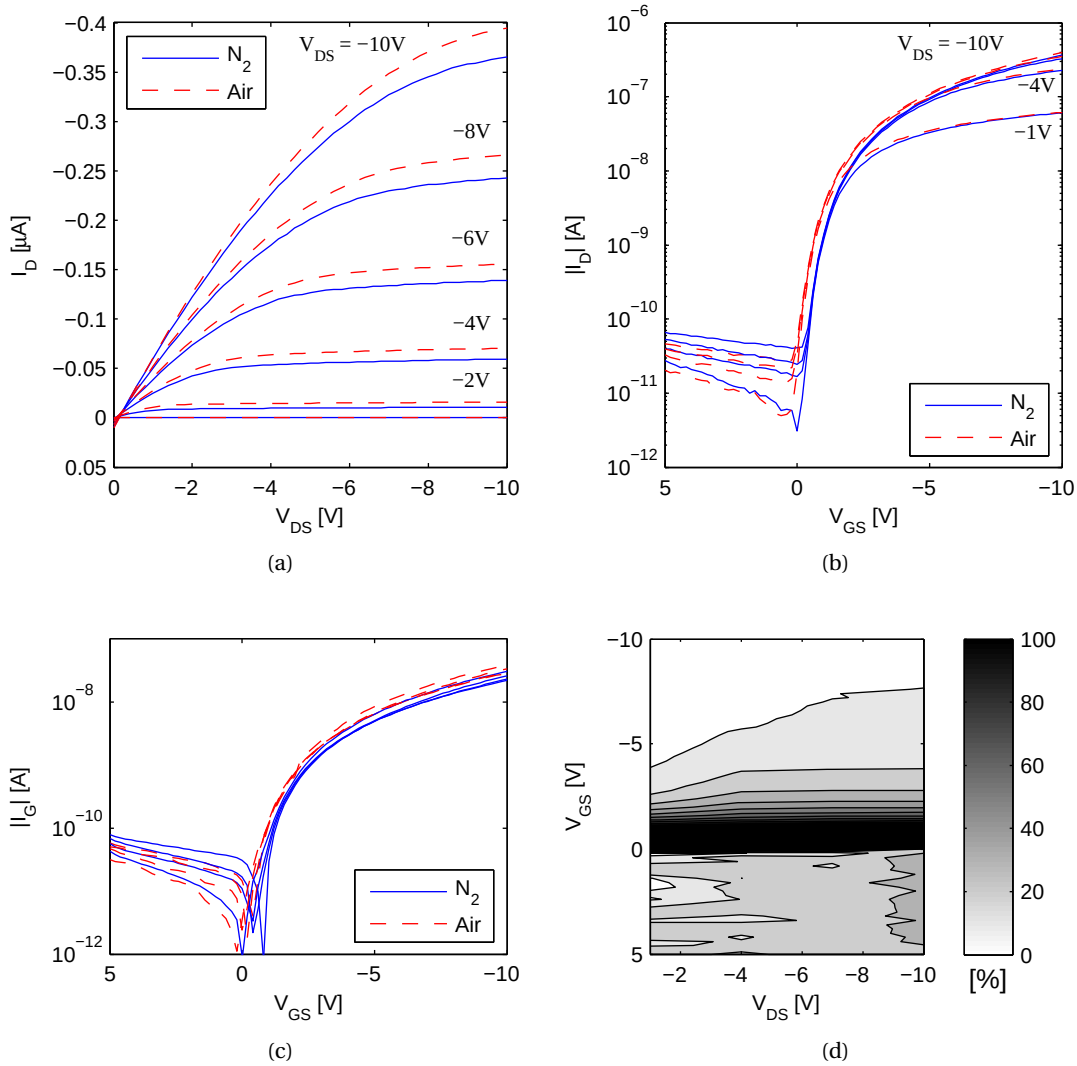
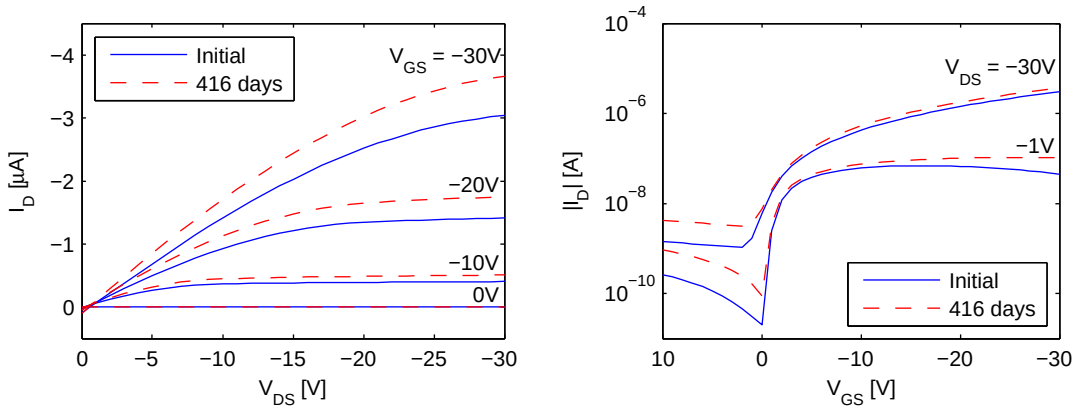


Figure 2.11: TG3 OTFT with $W/L = 200\ \mu m/20\ \mu m$ measured in inert atmosphere then in air. (a) Output characteristics, transfer characteristics of the drain (b) and gate (c) currents. (d) Relative error map of (b).

remains exactly the same. The only negative variation is the gate leakage which increases of 20%. However all these figures validate the air-stability of the TG3 technology and enable the possibility to perform temperature-dependent measurement at EPFL.

2.6.3 Shelf lifetime

The shelf lifetime characterizes how long a device can survive when not operated. To illustrate this point 13 TG3 OTFTs were measured for the first time on May 7th 2012. Then they were stored in air and measured again on June 27th 2013 (416 days after) and they were still operational as depicted in Figure 2.12. More details about the evolution of the performance parameters are shown in Figure 2.13.



(a) Output characteristics.

(b) Transfer characteristics.

Figure 2.12: BG3 OTFT with $W/L = 200\ \mu m/20\ \mu m$ measured on May 7th 2012 (Initial) and after 416 days on June 27th 2013.

The spread has increased for every performance parameter – except for $V_{T,sat}$ – as well as the gate leakage and the subthreshold swing. The OFF current has increased more than the ON current thus reducing the ON/OFF ratio.

The conclusion is that those TG3 OTFTs are stable even stored more than a year in air. This is an important feature for disposable devices such as quick diagnostic sensors. Indeed for those applications, the embedded OTFTs will be operated a short amount of time but they would have been stored beforehand waiting for their use.

The shelf-lifetime data of TG4 OTFTs are available in the next section to compare a stressed and an unstressed OTFT.

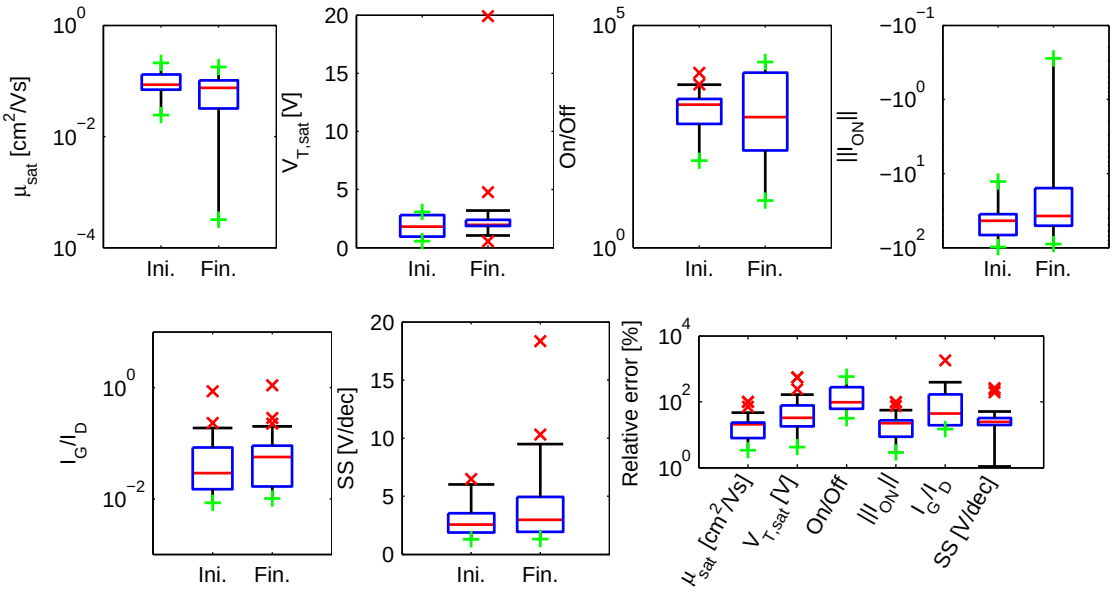


Figure 2.13: Performance parameters at the initial state (Ini.) and after 416 days (Fin.). (f) relative-error.

2.6.4 Stress lifetime

The stress lifetime characterizes how long can the device survive in operation. Several stressing methods exist such as the continuous bias stress [93], where the transistor is kept in the ON state, and the pulsed stress, applied in this section, which better represents the stress of an OTFT in a real circuit e.g. in an active-matrix (constant duty cycle). To perform this measurement the stressed OTFT is alternatively switched on and off for a given period of time and regurlarly the transfer and output characteristics are measured in order to track the performance parameters versus time. The procedure is depicted in Figure 2.14.

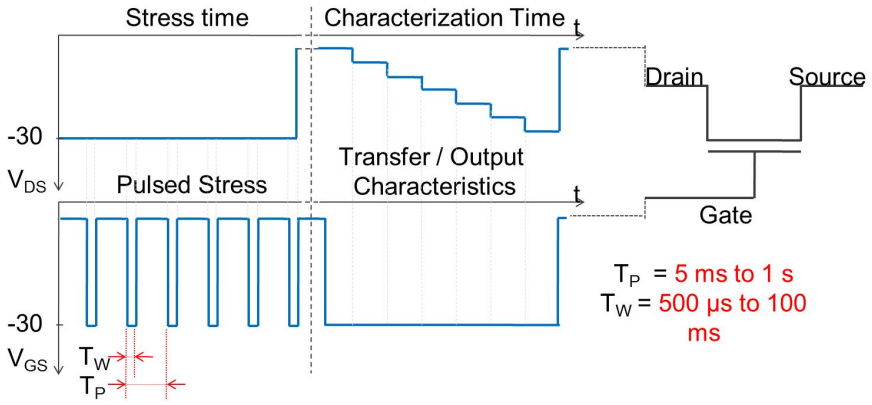
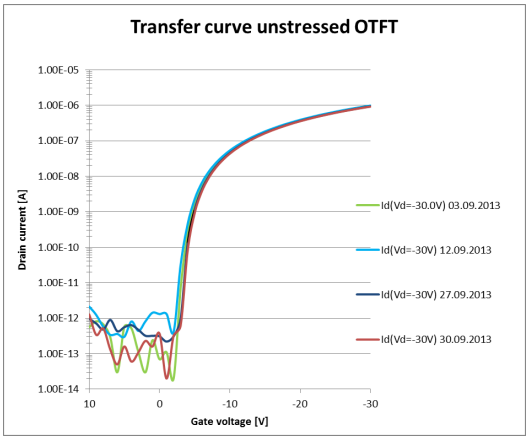


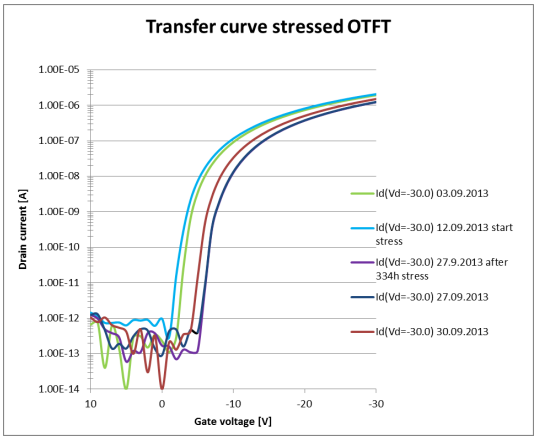
Figure 2.14: Stress-lifetime measurement: principle. The characterization step shown corresponds to the output and is measured in a quasi-static way.

An unstressed TG4 OTFT shows stable performance after one month stored in nitrogen environment (shelf lifetime), cf. Figures 2.15 and 2.16. Some figures of merit (field-effect mobility in saturation, threshold voltage and $I_{ON}L/W$) are plotted versus time in Figure 2.16. Concerning the stress lifetime, an OTFT was switched between the ON and OFF states at 50 Hz (minimum requirement for display applications) and withstand this stress performed during 15 days cf. Figures 2.15 and 2.16.

Note: both devices shown in these two figures were fabricated on August 29th 2013 while the different measurement dates are indicated in the figures.



(a) Shelf test: $W/L_{nom} = 2$ mm/90 μm.



(b) Stress test: $W/L_{nom} = 1$ mm/90 μm.

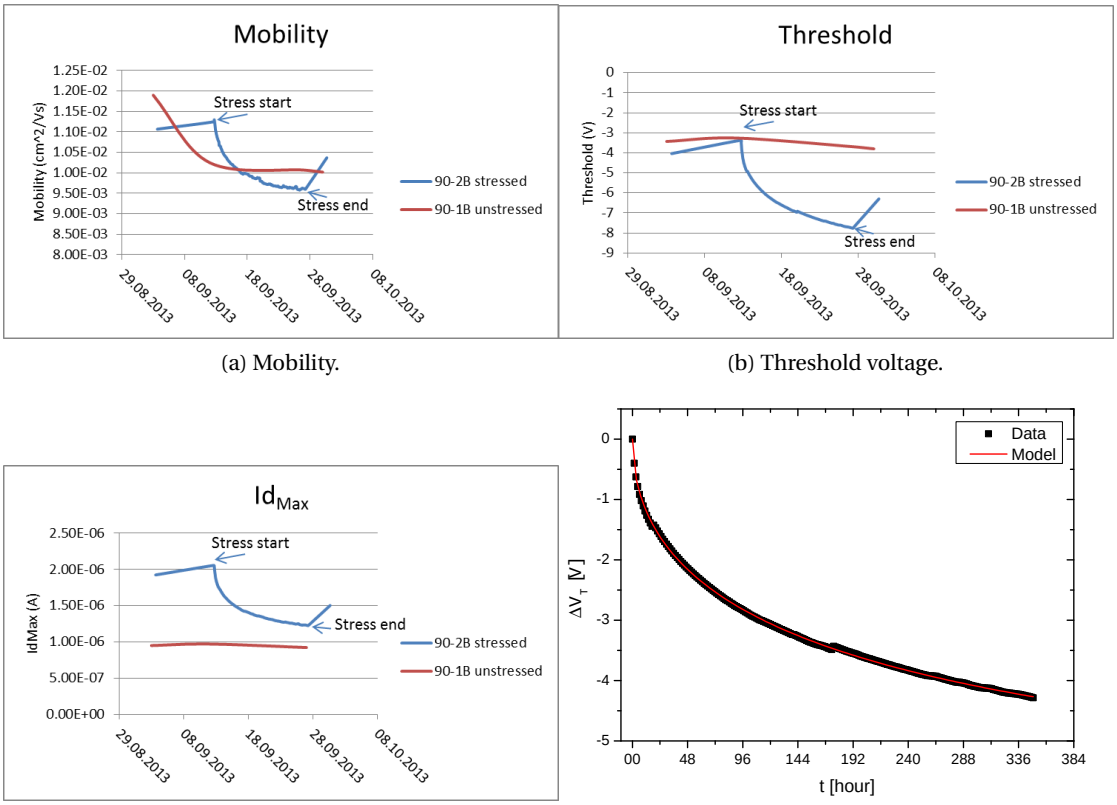
Figure 2.15: Shelf and stress lifetime measurement: transfer characteristics of TG4 OTFTs.

The mobility has slightly decreased (< 17%) and beside the threshold voltage (and thus the ON current), the other performance parameters have remained constant. Figure 2.16 also shows that the stressed OTFT started to recover from this stress stage with performance parameters evolving toward their initial value once the stress stops.

The threshold voltage shift is shown in Figure 2.16d and it appears that ΔV_T follows the empirical stretched-exponential model often reported [93, 102, 103, 104]:

$$\Delta V_T(t) = V_0 \left[1 - \exp\left(-\left(\frac{t}{\tau} \right)^{\beta} \right) \right] \tag{2.7}$$

With: $V_0 = V_T(\infty) - V_T(0) = -6.3$ V, $\tau = 11$h18min and $\beta = 0.50$. $V_T(0) = -3.3$ V is the initial threshold voltage which thus gives $V_T(\infty) = -9.6$ V. With a continuous bias stress, $V_T(\infty) = V_G$ [103] but here the observed difference is explained by the pulse mode where the OTFT recovers in a period of time defined by the pulse period and the duty cycle. The obtained value for β is compatible with the values reported in the literature: $0 < \beta < 1$ [104] and $\beta = 0.44$ for PTAA [103]. The relaxation time τ is thermally activated [103] and depends on the drain-source voltage [102], humidity [103] and the HOMO energy level of the semiconductor [104]. The lower τ, the faster the equilibrium is reached.



(a) Mobility.

(b) Threshold voltage.

(c) Normalized ON current.

(d) ΔV_T model.

Figure 2.16: Shelf and stress lifetime measurement of TG4 OTFTs: evolution of the performance parameters.

Beside this empirical model, Sharma *et al.* [104] reported a physical model based on a proton migration mechanism which explains the threshold voltage shift in both the stress and recovery phases. The threshold voltage shift is associated "with a reversible reaction in the organic semiconductor in which holes are converted into protons in the presence of water and a reversible migration of these protons into the gate dielectric" [104]. However the analytical model is not yet in a compact form as the empirical one.

2.7 Summary

Among the different electrical characterization methods introduced in this chapter, those available at CSEM ($I-V$, $C-V$, rise time & stress lifetime) are operational and can be performed automatically and at high throughput. This also stands for the developed data processing tools.

The twin technologies BG4 and BG5 (BGBC with X-PVP/PTAA) are demonstrated to be neither electrically stable nor air-stable confirming their low potential discussed in the previous chapter.

On the other hand TG3 (TGBC with BASF polymers) is demonstrated to be air stable and with a shelf lifetime above 416 days. The results of the temperature-dependent and rise time measurements are used in the next chapter. However further analysis of the obtained capacitance-voltage characteristics require to fabricate additional samples with different gate overlap and patterned semiconductor. Even if this technology cannot be used, at its current state to make circuits (dielectric not patterned), the material set as shown to have potential.

This show that the electrical characterization methods introduced in this chapter could bring new inputs to support the evaluation of a candidate technology.

The two last potential technologies identified in the previous chapter, BG6 (especially the submicron OTFTs) and TG4 (gravure-printed), were not available in this thesis for $C-V$, temperature-dependent, rise time and lifetime measurements. Therefore the analysis introduced in the next chapters will have to be undergone without these valuable inputs.

3 OTFT modeling

3.1 Introduction and state of the art

In this modeling chapter, the focus is set on compact models. A compact model is analytical but without differentials or integrals as possibly found in physical models. This feature allows the use of the model in Electronic Design Automation (EDA) tools and simulators. A compact model is not a finite element model and has relations that can be physically justified [105].

3.1.1 "Long-channel bulk MOSFET" model

The IEEE-1620 [71] definitions of the mobility and threshold voltage meant for OFET which were used in Chapter 1 come from the long channel bulk MOSFET model. They are recalled below.

Note: the following equations hold for a n-type transistor.

- Linear regime: $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$

$$I_{D,lin} = \frac{W}{L}\mu C_i \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \tag{3.1}$$

- Saturation regime: $V_{GS} > V_T$ and $V_{DS} > V_{DS,sat} = V_{GS} - V_T$

$$I_{D,sat} = \frac{W}{2L}\mu C_i \left(V_{GS} - V_T \right)^2 \tag{3.2}$$

- Subthreshold regime: $V_{GS} < V_T$

$$I_{sub\text{-}Vt} = I_{D0} \exp\left(\frac{\ln(10)}{SS} \left(V_{GS} - V_T \right) \right) \text{ where } I_{D0} = I_D(V_{GS} = V_T) \tag{3.3}$$

Using respectively μ_{sat} and $V_{T,sat}$ as μ and V_T in the above expressions gives the results depicted

in Figure 3.1 for a submicron OTFT.

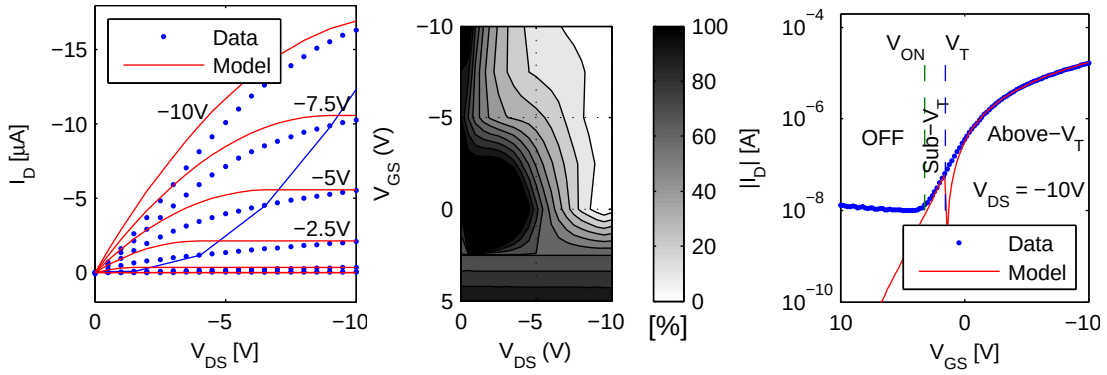


Figure 3.1: Experimental data of a submicron OTFT from BG6 ($W/L = 25\ \mu$m$/0.5\ \mu$m) and bulk MOSFET model. (a) Output characteristics ; the blue line denotes the saturation limit $V_{\mathrm{DS,\,sat}} = V_{\mathrm{GS}} - V_{\mathrm{T}}$. (b) Corresponding relative-error map. (c) Transfer characteristics in semi-logarithmic scale.

The output characteristics of Figure 3.1a shows that the MOSFET model globally overestimates the drain current for OFET, especially in the linear regime. This is particularly visible in the relative error map of Figure 3.1b where the relative error, $RE = (I_{\mathrm{Model}} - I_{\mathrm{Data}})/I_{\mathrm{Data}}$ is below 10% only for $V_{\mathrm{GS}} \leq 0$ V and $V_{\mathrm{DS}} \leq -9$ V. The difference in the linear regime can be related to contact resistances, an inherent issue to OTFTs. Contact resistances are studied in Section 3.3.

Whereas the MOSFET model actually saturates, a linear increase of the drain current is observed in the saturation regime for the given submicron OTFT. This behavior can come from a short-channel effect known as channel length modulation. Its implementation is performed in Sections 3.4.1 and 3.4.2 together with other short-channel effects.

For MOSFETs, the subthreshold current ideally decreases down to the detection limit of the characterization platform and thus flattens at this noise limit which is around 1 pA or below depending on the characterization equipment. In Chapter 1, this situation only occurs for TG4 (semiconductor patterned through gravure-printing). Thus for OFETs the OFF regime is generally defined as $V_{\mathrm{GS}} < V_{\mathrm{ON}}$ and the subthreshold regime is then defined as: $V_{\mathrm{ON}} < V_{\mathrm{GS}} < V_{\mathrm{T}}$. This is depicted in the transfer characteristics Figure 3.1c with $V_{\mathrm{T}} = V_{\mathrm{T,sat}}$. For OFETs, it can happen that $V_{\mathrm{ON}} \approx V_{\mathrm{T}}$ thus in this case, there is no need of a specific subthreshold model – examples are given in Section 3.4.1. The OFF current is modeled in Section 3.2.

Whereas the subthreshold regime itself is well reproduced in the example of Figure 3.1c, the transition with the above-threshold regime is poor. This topic is discussed in Section 3.4.3.

This introduction using a MOSFET model shows that many aspects of OTFTs need dedicated models. A set of such OTFT models is reviewed in the next section.

3.1.2 State of the art

Table 3.1: State-of-the-art OTFT modeling, part I: at the beginning of this thesis (2010). "Stats." refers to statistical model. "AC" refers to dynamic model with simulations only (S) or matching experimental data (✓). "PEM" indicates whether the parameter extraction method is given. "EDA impl." refers to the model implementation. "Circuits" indicates whether circuits (including inverters) are simply simulated (S) or matching experimental data (✓) in static/transient operation.

Year	Ref.	I_{OFF}	R_C	Sub-V_T	I_G	Stats.	AC	PEM	EDA impl.	Circuits
2003	[106]	-	-	-	?	-	-	N/A	ATLAS	-/-
2007	[107]	✓	✓	-	-	-	✓	[108]	Verilog-A	✓/S
2007	[109]	-	-	-	?	✓	✓	Fit	VHDL-AMS	✓/✓
2008	[110]	✓	✓	✓	-	-	-	[111]	SPICE	-/-
2009	[105]	-	✓	✓	-	-	-	[112]	?	-/-
2009	[113]	-	-	-	-	-	S	?	?	-/-
2009	[114]	✓	✓	-	-	-	S	[111]	SPICE	-/-
2009	[115]	-	-	-	-	✓	-	Fit	VHDL-AMS	S/S
2010	[116]	-	-	✓	-	-	S	?	SPICE	✓/-

A set of nine OTFT models reported up to 2010 (beginning of this thesis) are gathered in Table 3.1 to compare some of their features. The presence of the different aspects introduced in the previous section, namely the OFF current, the contact resistances and the subthreshold regime, can be thus assessed for each model. Any absence is not necessarily negative but needs to be cross-checked with the used experimental data: for example, the subthreshold regime is not always required as discussed in the previous section.

Among these nine models, three are not compact: Ref. [106] is a finite element model, Ref. [109] is a mathematical model and Ref. [115] is a behavioral model. The mathematical model from Ref. [109] is actually the only model which fulfills almost all criteria of the Model Quality Chart (MQC) [117]: it comprises a static model, a dynamic model, a statistical model, a hysteresis model, a noise model and a small-signal model. In addition, beside being only a mathematical model based on curve fitting, it predicts well the behavior of transistors as well as complex analog circuits such as a cascode amplifier or a differential amplifier thanks to its statistical component.

The behavioral model from Ref. [115] is actually the only other model validating the statistical criteria in Table 3.1. Jacob *et al.* from CEA-LITEN used the behavioral modeling suite called LYSIS (nowadays GREENLys[1] for organic electronics) from Infiniscale to model their OTFTs. A heuristic algorithm explores various function classes with different behaviors and complexities in order to minimize a quality-of-fit indicator that measures the difference between model and data [115]. I had the chance to test GREENLys and to give some feedback to the developers. A static model is automatically generated from a set of measured OTFT data in minutes or hours

[1] http://www.infiniscale.com/index.php?id=89

depending on the size of the dataset and of the computing power available. The generated model can then be exported to commercial EDA tools such as Eldo or Spectre to perform circuit simulation. However the model is only a purely mathematical expression thus without physical sense similarly to Ref. [109]. In addition the model itself is encrypted and can only be used as a black box within the software or by the EDA tools mentioned above. Thus the test case is not reported in this thesis.

Among the **compact** models listed in Table 3.1, one is commercially available: the Universal OTFT model (UOTFT) from Silvaco[2]. Its main contributors are B. Iñiguez (DEEEA, Universitat Rovira i Virgili) [110], S. Mijalkovic (Silvaco) [114] and A. Rankov (Cambridge Display Technologies) [118]. This SPICE model has been developed suitable for all analog, digital and RF circuit design. However one can read in Ref. [118] that the following points were described as future work: 1. Account for the bias dependent contact resistances, gate tunneling and effect of interface trap states, 2. Model a dynamic device behavior and 3. Handle aging and hysteresis of the OTFT characteristics within the model and the corresponding circuit design.

These future steps are also common to the other models: the gate leakage is indeed mostly neglected and only the compact model from Ref. [107] validates its dynamic model to experimental data ($C-V$ curves). This dynamic model and the others present in the table were developed using the charge oriented approach [119].

Four models out of the nine of Table 3.1 demonstrate static simulations of circuits (inverters) and three of them actually match the experimental data. Similarly three models out of nine demonstrate transient simulations of circuits (ring-oscillators but not only [109]) but only the one from Ref. [109] actually match the experimental data.

In this chapter, most of these aspects are screened on either the TG3 or the BG6 technology. The statistical part is mainly discussed in the next chapter. However the dynamic model and corresponding transient simulations are not covered in this thesis.

3.2 OFF current

The OFF current can be limited by the gate leakage when $|I_D| \approx |I_G|$ and $|I_S| \ll |I_D|$ (case A) or coming from bulk conduction when $|I_D| \approx |I_S|$ and $|I_G| \ll |I_D|$ (case B, as in Figure 3.2a). The gate leakage can also dominate the OFF current which actually corresponds to the case A when swapping I_D and I_S in the expressions above *i.e.* $|I_D| \ll |I_G| \approx |I_S|$. This means that the gate leakage mainly occurs at the source. This was already discussed for the different studied technologies in Chapter 1. More details about the gate leakage are given in Section 3.7.

[2] http://www.silvaco.com/products/analog/spicemodels/models/uotft/uotft.html

Dependence with the gate voltage

Looking at the experimental transfer curves in Chapter 1, the OFF current can be considered independent from the gate voltage at least for the following technologies: BG3, BG4, BG5, TG1, TG2, TG3 (confirmed in Figure 3.2a: flat drain current for $5V > V_{GS} > 0V$, and this for each V_{DS}) and BG6. Only the technologies on silicon substrate (BG1 and BG2) – thus with low interest – actually show a non-negligible gate voltage dependency. For TG4, the OFF current is actually below or equal to the noise level of the measurement platform.

At lower V_{DS}, the gate voltage dependency increases because of a higher parasitic influence of the gate leakage current. We thus still neglect the gate voltage dependency of the OFF current.

Dependence with the drain voltage

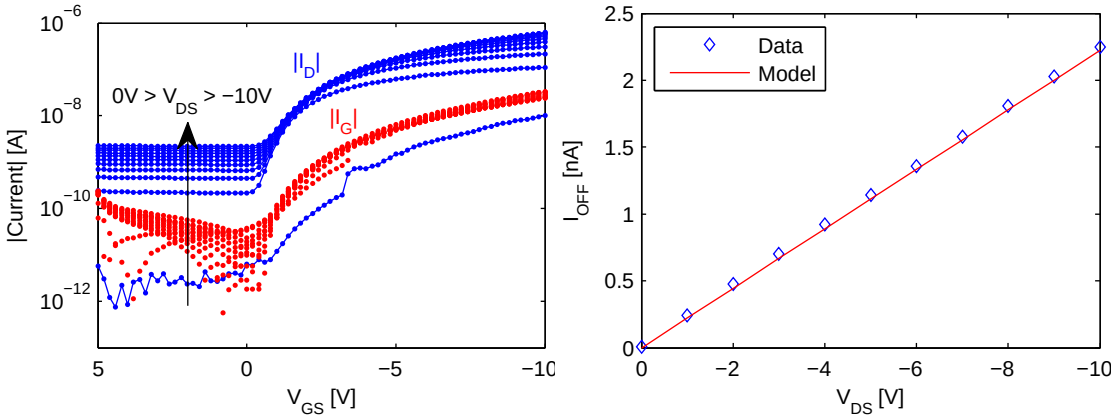


Figure 3.2: (a) Transfer characteristics in semi-logarithmic scale of a TG3 OTFT with $W/L = 400\,\mu m/20\,\mu m$ where $|I_{G,OFF}| \ll |I_{D,OFF}|$ ($V_{DS,step} = -1V$). (b) Linear fit of $I_{D,OFF}$ versus V_{DS}.

An ohmic behavior with respect to V_{DS} is mainly observed on the transistors reported in Chapter 1 but is also reported in Ref. [120]. This is illustrated with a TG3 OTFT in Figure 3.2b. Thus, I_{OFF} can be written:

$$I_{OFF} = \frac{V_{DS}}{R_{Bulk}} \tag{3.4}$$

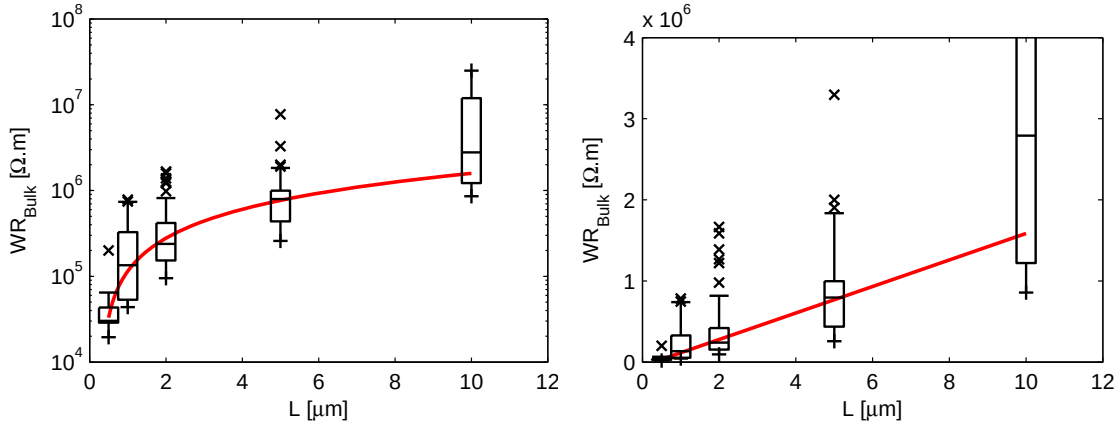
From these observations, a bulk resistor model of length L and cross-section $W\,t_{semiconductor}$ is selected in a first approximation for the transistor in the OFF regime:

$$R_{Bulk} = \rho_{Bulk} \frac{L}{W\,t_{semiconductor}} \tag{3.5}$$

This bulk resistor model works well however for short-channel lengths, a scaling-issue is

observed with respect to L. Indeed by directly using the median value obtained for the submicron OTFTs (BG6), we get $\rho_{\text{Bulk}} = 2.8$ kΩ.m which is 44% less than the value obtained in Figure 3.3. This can come from the increased importance of the contact resistance at shorter channel lengths: $R_{\text{OFF}} = R_{\text{Bulk}}(L) + R_{\text{contacts}}$. Contact resistances are discussed in the next section.

Additionally in the case A ($|I_{\text{D,OFF}}| \approx |I_{\text{G,OFF}}|$) the gate leakage disturbs the extraction of R_{Bulk} which requires I_G to be de-embedded beforehand. This is not performed in this section but discussed in Section 3.7.



(a) Semi-logarithmic scale.

(b) Linear scale.

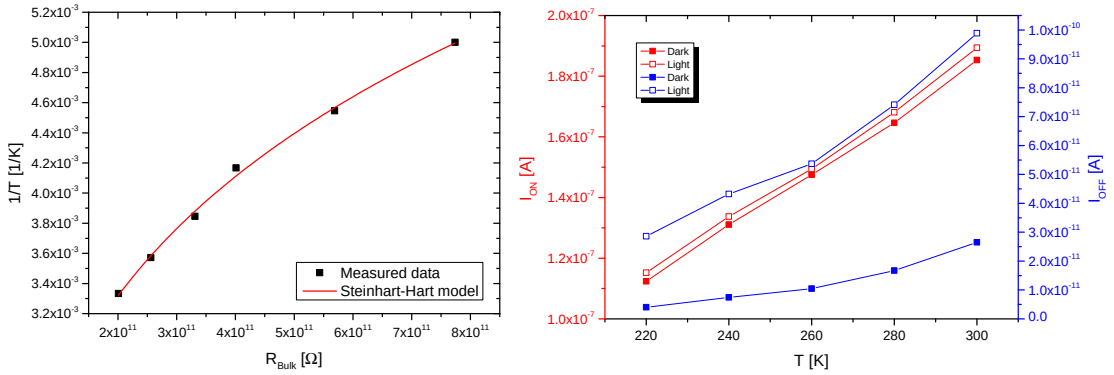
Figure 3.3: Scaling of WR_{Bulk} with respect to L of 103 BG6 OTFTs ($t_{\text{semiconductor}} = 30$ nm). The fit of the median values using Eq. 3.5 gives $\rho_{\text{Bulk}} = 6.4$ kΩ.m.

Dependence with the temperature

The behavior with respect to the temperature was assessed by using the measurement performed on a TG3 OTFT in Section 2.3. A bulk semiconductor should follow the model of Steinhart-Hart [121] in which the resistance R is linked to the temperature T as follows:

$$\frac{1}{T} = A + B\ln(R) + C(\ln(R))^3 \text{ with } A, B \text{ and } C \text{ constants (Steinhart-Hart coefficients).} \quad (3.6)$$

This is confirmed in Figure 3.4. This figure also shows the influence of light through the generation of photo-current. The OFF current increases more than the ON current thus the ON/OFF ratio decreases. This aspect has to be noted because all OTFT $I-V$ curves in the previous chapters were acquired in the dark. In addition both the OFF current and the ON/OFF ratio are key performance parameters in display applications where light is present. Since the characteristics of the used white light source (microscope) are unknown (power, spectrum...), this topic is not further discussed.



(a) (b)

Figure 3.4: (a) R_{Bulk} assessed to follow Steinhart-Hart model with the following coefficients: $A = 4.14 \times 10^{-2}$, $B = -2.71 \times 10^{-3}$ and $C = 1.85 \times 10^{-6}$. (b) Influence of temperature and light on the ON and OFF currents. TG3 OTFT with $W/L = 400\ \mu\text{m}/20\ \mu\text{m}$.

3.3 Contact resistances

Contact resistances are an inherent limitation to the performances of OTFTs due to the energy level mismatch between the organic semiconductor HOMO and the work function of the contact metal. There is indeed for example a potential contact resistance due to the P3HT-Au Schottky barrier of 0.3 eV, in the best case [47]. Studies about contact resistances in OTFTs are extensively reported in the literature [91, 122, 47, 123, 49] and contact effects themselves were the topic of Ph.D. thesis e.g. [92]. Thus, in this section, the focus is set on extraction methods rather than their physical analysis.

Several methods are available to extract the contact resistances such as the scaling approach [124] or a method based on the gradual channel approximation [125]. The most used is by far the transmission line method (TLM) [126] and is thus the starting point of this section followed by its modified version [127].

Note: the four mentioned extraction methods have been implemented in my modeling platform introduced at the end of this chapter.

Once extracted, the contact resistances can be modeled as: constant resistors [73, 107, 110], gate-voltage dependent resistors [122, 105, 127], transistors [128], a single diode [125], resistors and anti-parallel diodes [129] or a transistor coupled to a diode [110].

3.3.1 Transmission line method

The total resistance of a device is given by the sum of the contact resistances and the channel resistance as shown in Figure 3.5. The latter scales with the channel length.

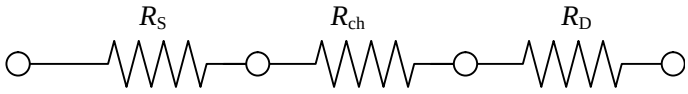


Figure 3.5: TLM for contact resistance of OFET

In Ref. [130], Sirringhaus *et al.* uses formulas developed for amorphous silicon TFTs [131]:

$$R_{ON} = \left(\frac{\partial I_D}{\partial V_{DS}}(L)\right)^{-1} = R_S + R_{ch}(L) + R_D \tag{3.7}$$

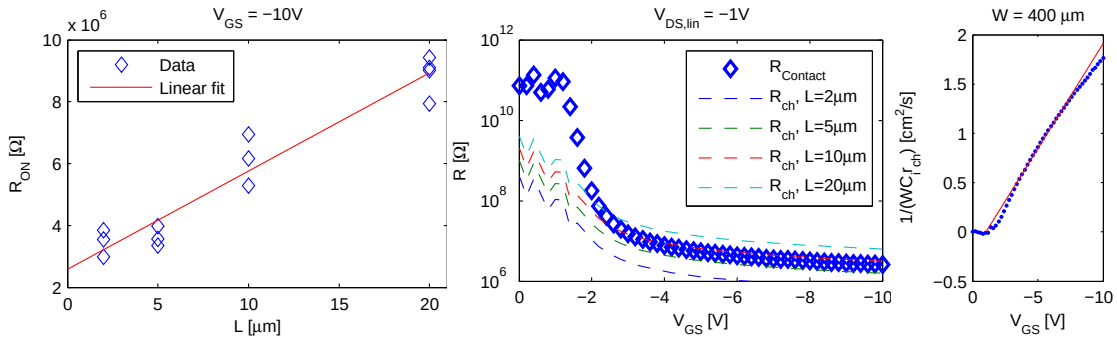
Assuming that the device is symmetrical, ($R_S = R_D = R_C/2$) further computations lead to [132]:

$$R_{ON} = r_{ch}L + R_C \quad \text{with} \quad r_{ch} = \frac{1}{W\mu_{FE,i}C_{ox}\left(V_{GS} - V_{T,i}\right)} \tag{3.8}$$

Where $V_{T,i}$ is the intrinsic threshold voltage and $\mu_{FE,i}$ is the field-effect intrinsic mobility. If the area of the contact remains the same and the channel length varies, a change of the channel resistance, R_{ch}, can be observed but the contact resistance, R_C, should be similar for all L, for a single V_{GS}.

$V_{T,i}$ is extracted from the $1/r_{ch}$ versus V_{GS} curve and $\mu_{FE,i}$ from the slope of this plot according to equation 3.8.

The whole extraction process is illustrated in Figure 3.6. Note: when multiple OTFTs have the same channel length, the average value of R_{ON} is taken to perform the linear fit.



(a) (b) (c)

Figure 3.6: (a) Linear fit of R_{ON} versus L at $V_{GS} = -10$ V and $V_{DS,lin} = -1$ V of 13 TG3 OTFTs with $W = 400$ μm. (b) Obtained R_C and $R_{ch} = r_{ch}L$ versus V_{GS}. (c) Linear fit to extract $\mu_{FE,i} = 0.213$ cm^2/Vs and $V_{T,i} = -1.04$ V according to Equation 3.8.

Influence of the channel width

The previous analysis is valid if the contact area is the same between the studied OTFTs. The influence of the channel width W is here studied by using transistors of the finger topology as available on the TG3 test structure chip (visible in Figure 1.30a). The contact resistances are extracted for each W-group – 50, 100, 200 and 400 μm – and compared in Figure 3.7a in order to assess the normalization by W. Indeed the contact resistances have to scale with $1/W$ as does R_{ON}.

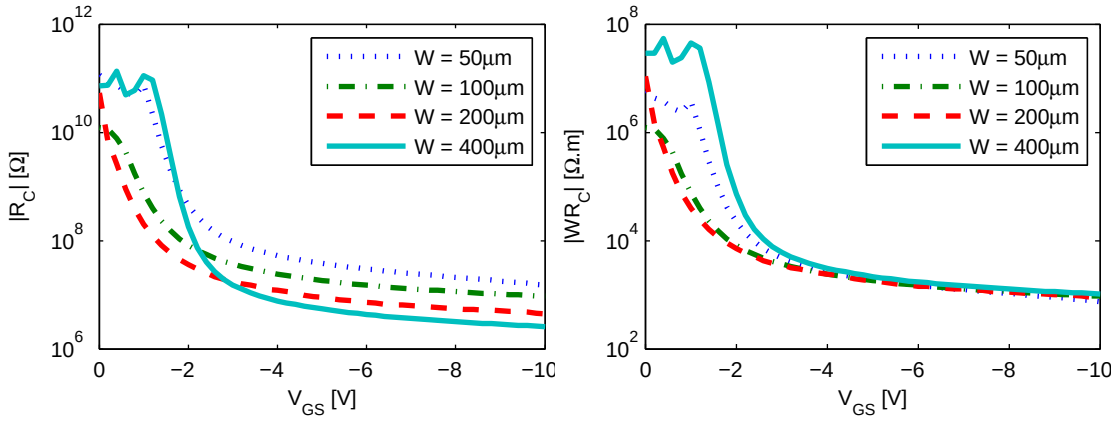


Figure 3.7: (a) R_C versus V_{GS} for different W ($\approx$ 13 OTFTs/W). (b) Normalization: $\|R_C\| = WR_C$.

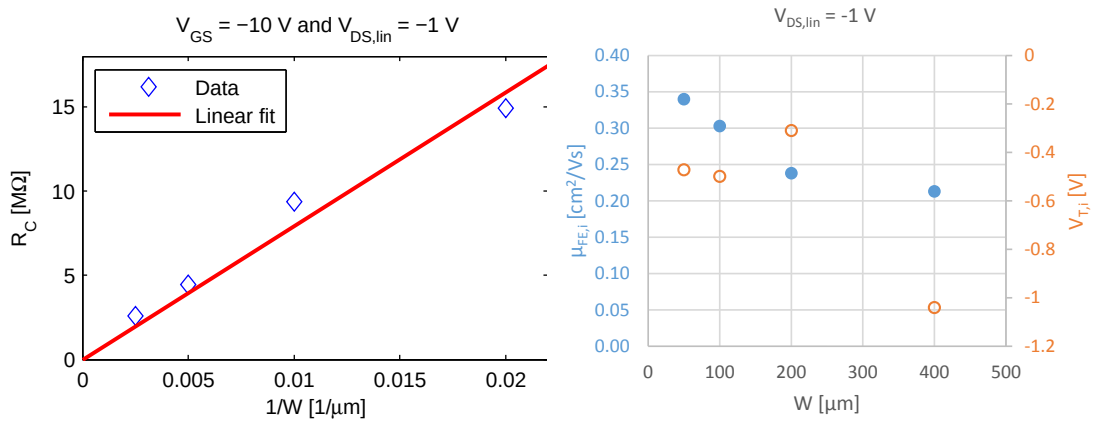
The WR_C curves of Figure 3.7b are superimposed especially for $V_{GS} \leq -3$ V assessing the normalization. Figure 3.8a also assesses the scaling.

In addition, whereas $V_{T,i}$ has no particular behavior, $\mu_{FE,i}$ seems to follow R_C with respect to W, see Figure 3.8b. It can be an artifact since the extraction quality of $\mu_{FE,i}$ degrades when W decreases.

Normalized contact resistances and gate leakage

The W-normalization allows using OTFTs with different channel width at the same time for the TLM extraction. Here all the OTFTs used in the previous paragraph (53) are combined to apply the TLM. The extraction is visible in Figure 3.9 and, as for Figure 3.6, when multiple OTFTs have the same channel length, the average value of WR_{ON} is taken to perform the linear fit.

As visible in Figures 3.9c and 3.6c, the $1/(WC_i r_{ch})$ curve giving $\mu_{FE,i}$ and $V_{T,i}$ has a non linear part at high $|V_{GS}|$. This looks similar to some extraction cases of the linear mobility μ_{lin}. Whereas for μ_{lin} this behavior was linked to the impact of contact resistances and gate leakage, here the contact resistances are de-embedded. Thus de-embedding the gate leakage could possibly correct this behavior. To do so, $I_{TFT} = (I_D - I_S)/2$ can be used instead of I_D in



(a) (b)

Figure 3.8: (a) $R_C(V_{GS} = -10V)$ versus $1/W$. (b) $\mu_{FE,i}$ and $V_{T,i}$ versus W.

Equation 3.7 to perform the TLM. This de-embeds the gate leakage under the following assumption: $I_{GS} = I_{GD} = I_G/2$ – more details in Section 3.7.

As visible in Figure 3.10b, de-embedding the gate leakage has indeed corrected the linear behavior and in addition yields the highest intrinsic mobility: $\mu_{FE,i} = 0.35$ cm^2/Vs.

From all the R_C versus V_{GS} curves seen in this section, it appears that only the OTFTs with $L = 20$ μm are not contact limited. This validates the hypothesis taken in Section 2.4.1 for the $C-V$-extraction of the mobility. Another common point to these curves is the critical channel length at which $R_C = R_{ch}$ i.e. $L_{critical} = R_C/r_{ch}$ and which is around 10 μm at $V_{GS} = -10$ V.

3.3.2 Modified transmission line method

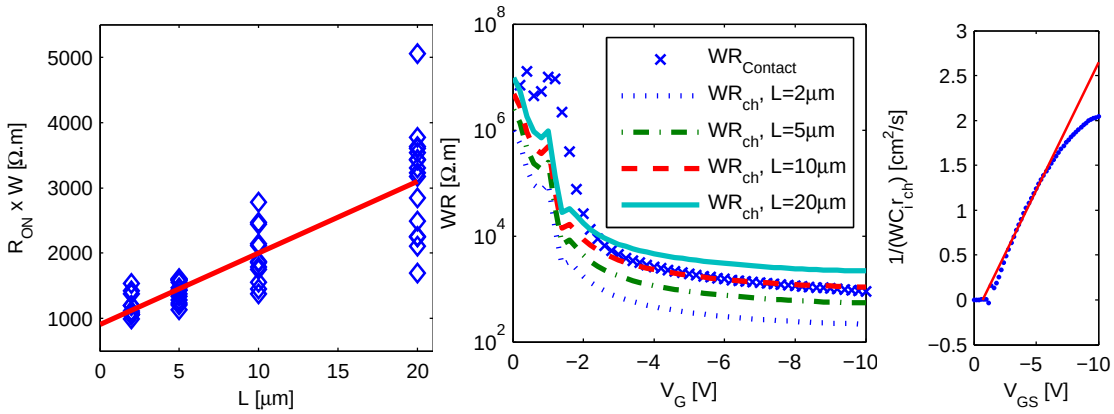
In this section, the modified transmission line method (M-TLM) proposed by Xu *et al.* [127] is introduced.

The M-TLM uses the same theoretical background as the conventional TLM (C-TLM) described in the previous section. The only difference resides in the linear fit performed to get R_C which basically uses the previous Equation 3.8 divided by L which once normalized by W gives:

$$\frac{WR_{ON}}{L} = Wr_{ch} + \frac{WR_C}{L} \tag{3.9}$$

The slope of WR_{ON}/L versus $1/L$ gives WR_C whereas for the C-TLM, WR_C was read at $L = 0$. The slope is well controlled by the OFETs of short L, where more dominant contact resistance gives a better linear fitting [127]. This method gives thus more weight to short channel OTFTs for the extraction of the contact resistance.

Furthermore, Xu *et al.* investigated theoretically the extraction error from C-TLM and M-TLM



(a) (b) (c)

Figure 3.9: (a) Linear fit of WR_{ON} versus L at $V_{GS} = -10$ V and $V_{DS,lin} = -1$ V of 53 TG3 OTFTs with different W. (b) Obtained WR_C and $WR_{ch} = Wr_{ch}L$ versus V_{GS}. (c) Linear fit giving $\mu_{FE,i} = 0.29$ cm^2/Vs and $V_{T,i} = -0.71$ V.

and they found out that the relative standard deviation of the contact resistances extracted by the M-TLM (14%) is much smaller than that in C-TLM (33%). This process is depicted in Figure 3.11. They concluded that the much less device-to-device variation in contact resistance results in more stable and more reliable contact resistance extraction [127].

The demonstrated robustness of the M-TLM makes it the chosen method to extract the contact resistances for this thesis. Figure 3.12 shows its application combined to the gate leakage de-embedding method used in the previous section. The intrinsic mobility increases further to $\mu_{FE,i} = 0.38$ cm^2/Vs.

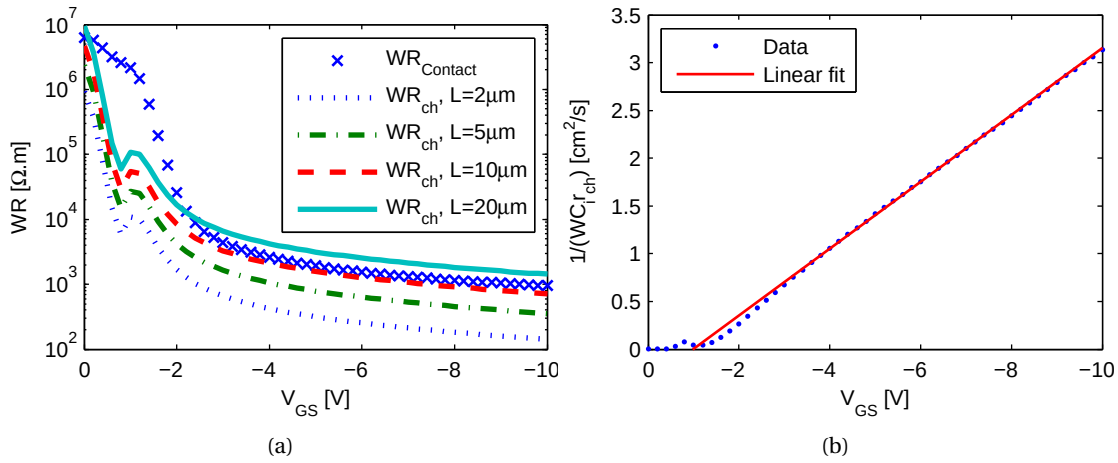
3.4 Drain current static model

The content of this section was published in [88] and its objective is to propose a static OTFT model valid for all operation regions and for most of the technologies described in Chapter 1 including the sub-micrometer OTFTs of BG6. The focus is thus set on the BG6 technology.

3.4.1 Level-1 model

In this section we use a DC model based on the so-called "TFT Generic Charge Drift model" (GCD) as described and derived in [105, Equation 8] coupled with the classic channel length modulation model [105, Equation 15] and the resistive leakage current model for the OFF regime described in Section 3.2. As shown in Equations 3.10 and 3.11, the DC model requires at this point only 5 parameters in addition to the design parameters L, W, and C_i.

Notes: $C_i = \epsilon_0 \epsilon_r / t_{dielectric}$ with, for BG6, $\epsilon_r = 3.8$ and $t_{dielectric} = 200$ nm. $t_{semiconductor}$ (for BG6,



(a) (b)

Figure 3.10: Same as Figure 3.9 after de-embedding the gate leakage. The linear fit of (b) gives $\mu_{\mathrm{FE,i}} = 0.35\ \mathrm{cm}^2/\mathrm{Vs}$ and $V_{\mathrm{T,i}} = -0.98\ \mathrm{V}$.

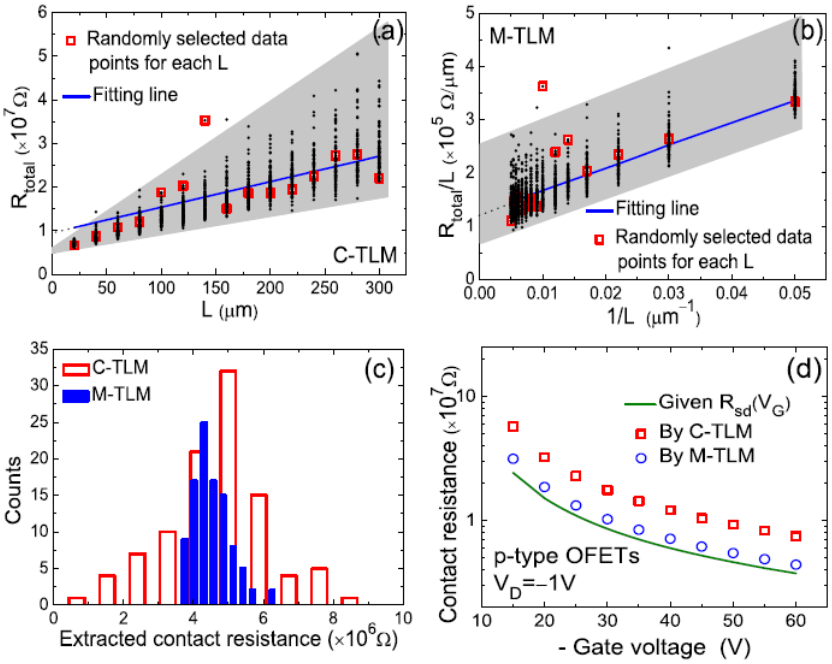
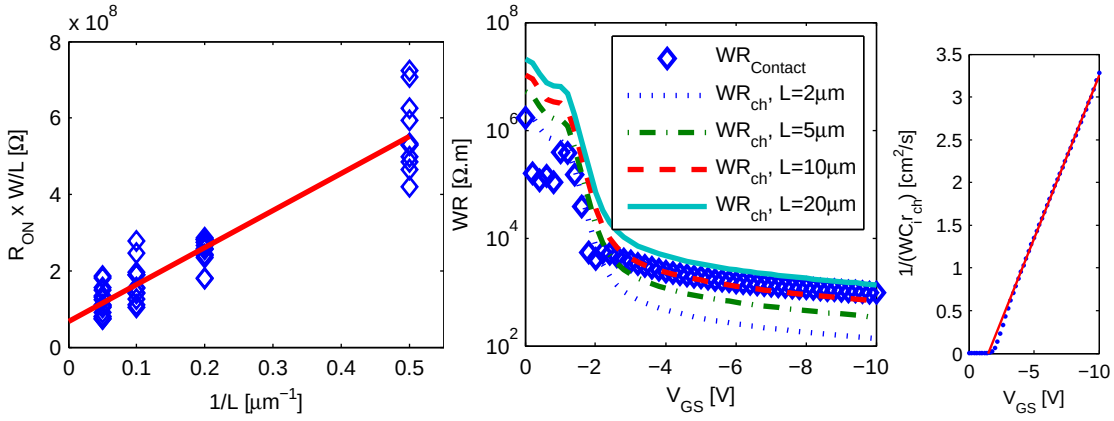


Figure 3.11: Modified Transmission Line Method. (a) and (b) is the linear regression at $V_{\mathrm{GS}} = -50\ \mathrm{V}$ of the random selected data points, for C-TLM and M-TLM extraction, respectively. The shaded region indicates the data dispersion region. (c) Histogram of 100 random extractions for the two TLM extractions. (d) An example of the contact resistances extracted by C-TLM and M-TLM, by using randomly generated mobility and threshold voltage. Adopted from [127].



(a) (b) (c)

Figure 3.12: M-TLM with de-embedded gate leakage. (a) Linear fit of WR_{ON}/L versus $1/L$ at $V_{GS} = -10$ V and $V_{DS,lin} = -1$ V of 53 TG3 OTFTs with different W. (b) Obtained WR_C and $WR_{ch} = Wr_{ch}L$ versus V_{GS}. (c) Linear fit giving $\mu_{FE,i} = 0.38$ cm^2/Vs and $V_{T,i} = -1.48$ V.

$t_{pentacene} = 30$ nm) used in the OFF current model comes back on purpose in the Level-2 model (Section 3.4.2). Also note that following equations are written for a n-type device.

$$I_D = I_{above} + I_{OFF} = I_{GCD}(1 + \lambda V_{DS}) + I_{OFF} \tag{3.10}$$

$$\begin{cases} I_{GCD,Lin.} = \frac{W}{L} C_i \frac{\mu_0}{\gamma+2} [(V_{GS} - V_{FB})^{\gamma+2} - (V_{GD} - V_{FB})^{\gamma+2}] \\ I_{GCD,Sat.} = \frac{W}{L} C_i \frac{\mu_0}{\gamma+2} (V_{GS} - V_{FB})^{\gamma+2} \\ I_{OFF} = \frac{V_{DS}}{R_{Bulk}} \end{cases} \tag{3.11}$$

V_{FB}, γ and μ_0 come from the simplified variable range hopping mobility model [24, 133, 134]: $\mu(V_G, x) = \mu_0 \left(\frac{V_G - V_{FB} - V_x}{V_{AA}}\right)^{\gamma}$ where x is the coordinate along the channel between Source and Drain and $V_{AA} = 1$ V is chosen to give a mobility dimension to μ_0. λ is the channel-length modulation parameter.

A high-throughput automated platform (visible in Section 3.8) was developed to apply the Parameter Extraction Method (PEM) which involves an iterative procedure as follows:

1. The H operator [73] is used in the saturation regime ($V_{DS} = -10V$) to get V_{FB}, γ and μ_0: $H_{I_{GCD}}$ to get V_{FB} and γ (Eq. 3.12 together with a linear fit) and $H_{I^2_{GCD}}$ [135] to get K (Eq. 3.13) and thus μ_0 (Eq. 2). I_{GCD} is obtained from Eq. 1 with $\lambda = 0$ for the first iteration.

2. λ is extracted from $g_D = \frac{\partial I_D}{\partial V_{DS}}$ (Eq. 3.14)

$$H_{I_{GCD}}(V_{GS}) = \frac{\int_{V_{FB}}^{V_{GS}} I_{GCD}(v_{GS})\, dv_{GS}}{I_{GCD}(V_{GS})} = \frac{V_{GS} - V_{FB}}{\gamma + 3} \tag{3.12}$$

$$K(V_{GS}) = \frac{2\gamma + 5}{(V_{GS} - V_{FB})^{\gamma+3}} I_{GCD}(V_{GS})\, H_{I^2_{GCD}}(V_{GS}) \tag{3.13}$$

$$\lambda(V_{GS}) = \frac{g_D\left(V_{DS,sat}\right) - R_{Bulk}^{-1}}{K(V_{GS} - V_{FB})^{\gamma+2}} \tag{3.14}$$

Equations 3.13 and 3.14 give gate-voltage-dependent K and λ, respectively, which are then averaged among V_{GS} in order to get constant values.

This PEM was applied to selected OTFTs and the results are shown in Figure 3.13 for each channel length (10 μm down to 0.5 μm, respectively). For the OTFT with $W/L = 500\,\mu\text{m}/10\,\mu\text{m}$ the obtained values for the model parameters are: $V_{FB} = -0.29$ V, $\gamma = 0.19$, $\mu_0 = 0.46$ cm^2/Vs, $\lambda = 15 \times 10^{-3}$ V^{-1} and $R_{Bulk} = 1.7$ GΩ.

The related model matching indicators plotted versus L in Figure 3.14a show that the model fits well with experiments: high determination coefficient (R^2) near 100% and low normalized relative mean-square deviation (NRMSD) near 0% while the relative error averaged on the whole V_D–V_G range (mean RE, 147 data points per OTFT) is below 20% for $L \geq 1\,\mu$m. However the matching quality degrades for the selected submicron OTFT.

On the other hand the extracted model parameters (e.g. R_{Bulk}) still depend on the channel length as shown in Figure 3.14b. Such dependence requires a set of transistors with different channel lengths in order to be modeled. This is performed by another PEM which takes the output of the Level-1 PEM and is thus referred in the following as Level-2.

3.4.2 Implementation of the short-channel effects and contact resistances: Level-2 model

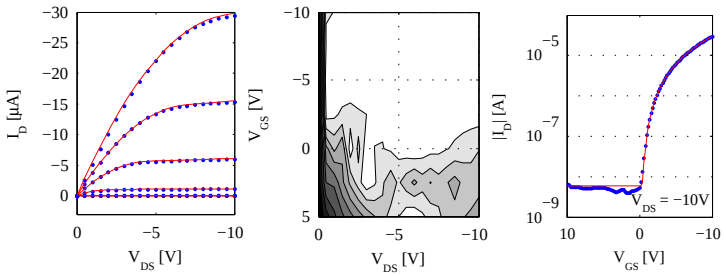
As discussed in Section 3.2, R_{Bulk} can be modeled in a first approximation as a resistor of length L and cross-section $W\,t_{Pentacene}$:

$$R_{Bulk}(L) = \rho_{Bulk} \frac{L}{W\,t_{Pentacene}} \tag{3.15}$$

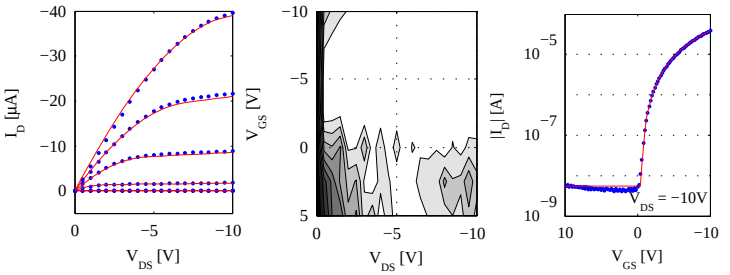
Thus:

$$W\,R_{Bulk}(L) = \rho_{Bulk} \frac{L}{t_{Pentacene}} \tag{3.16}$$

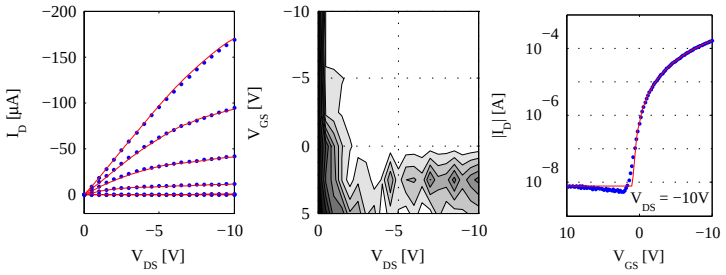
a) $W/L = 500/10$:



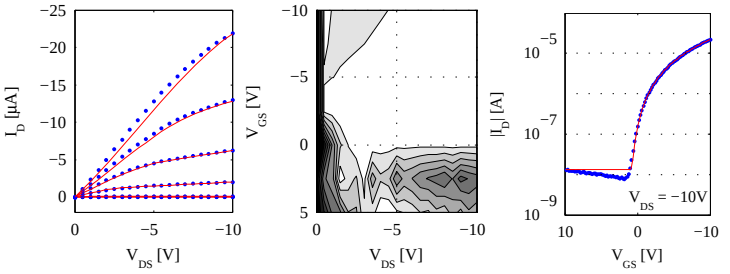
b) $W/L = 200/5$:



c) $W/L = 1000/2$:



d) $W/L = 100/1$:



e) $W/L = 25/0.5$:

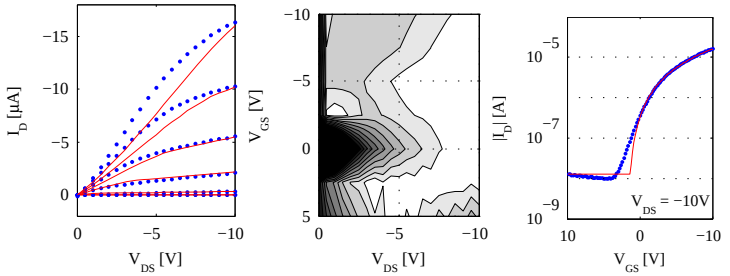


Figure 3.13: Level-1 PEM. From left to right: output characteristics, model (lines) vs experimental data (•), relative error (RE) map of the output characteristics (where white means $RE < 10\%$ and each gray level represents a 10% step) and transfer characteristics in logarithmic scale with model (lines) vs experimental data (•) for OTFTs with $L = 10$ μm down to $L = 0.5$ μm.

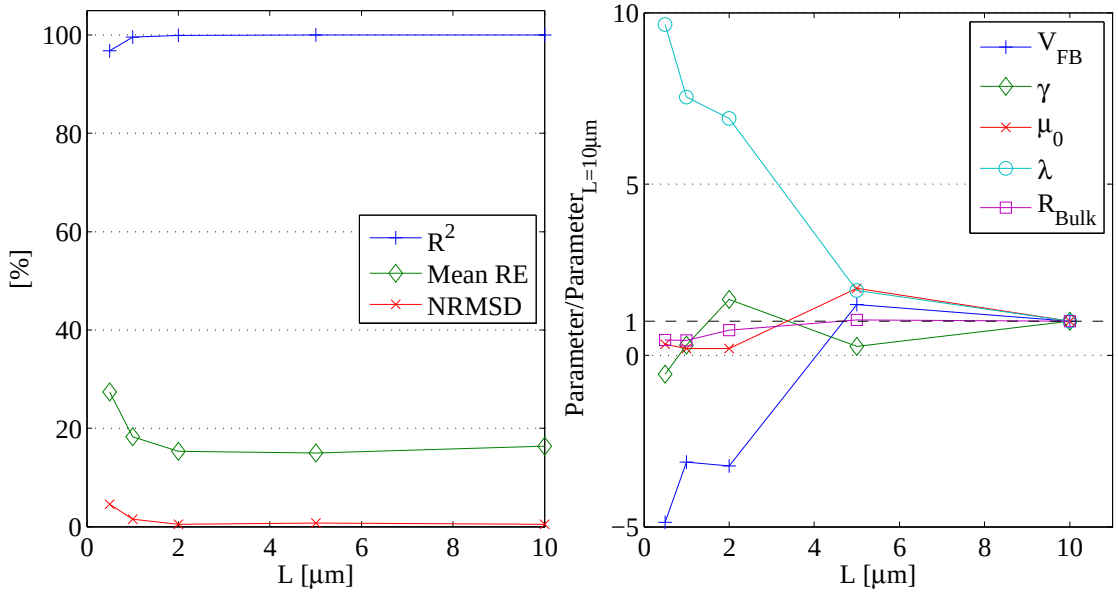


Figure 3.14: Level-1 PEM. (a) model matching indicators versus L: R^2, mean RE and NRMSD. (b) model parameters normalized by their value at $L = 10\,\mu$m versus L.

Plotting WR_{Bulk} versus L gives the Level-2 parameter ρ_{Bulk} knowing the design parameter $t_{\text{Pentacene}} = 30$ nm. This is illustrated in Figure 3.15. Note: the OTFTs selected to perform the Level-2 PEM are the ones visible in Figure 3.13 except the OTFT with $L = 2\ \mu$m which was excluded for the fit because of its outlier nature.

The fact that both λ and V_{FB} depend on L are related to short-channel effects previously observed and discussed for OTFTs [136, 137]. However, for the V_T-roll-off, a simplified expression used for Si-MOSFET [138] was chosen here for simplicity. Thus the following expressions were used:

$$\begin{cases} \lambda(L) &= \frac{\theta}{L+\Delta L} \\ V_{\text{FB}}(L) &= V_{\text{FB,Long}} - V_{\text{RO}} \exp\left(-\frac{L}{L_{\text{RO}}}\right) \end{cases} \tag{3.17}$$

From a best fitting procedure, we obtained: $\theta = 0.153\,\mu$m/V, $\Delta L = 0.5\,\mu$m, $V_{\text{FB,Long}} = -0.38$ V, $V_{\text{RO}} = -2.68$ V, $L_{\text{RO}} = 1.31\,\mu$m and $\rho_{\text{Bulk}} = 2.4$ kΩ.m. With drain-induced barrier lowering (DIBL), V_{RO} further depends on V_{DS} but we will intentionally neglect it.

At this point, the scaling of λ, V_{FB} and R_{Bulk} is implemented into the model. However it is well known that contact resistances do not scale and that their impact increases when the channel length decreases. Therefore, these will be extracted and added into the model in the

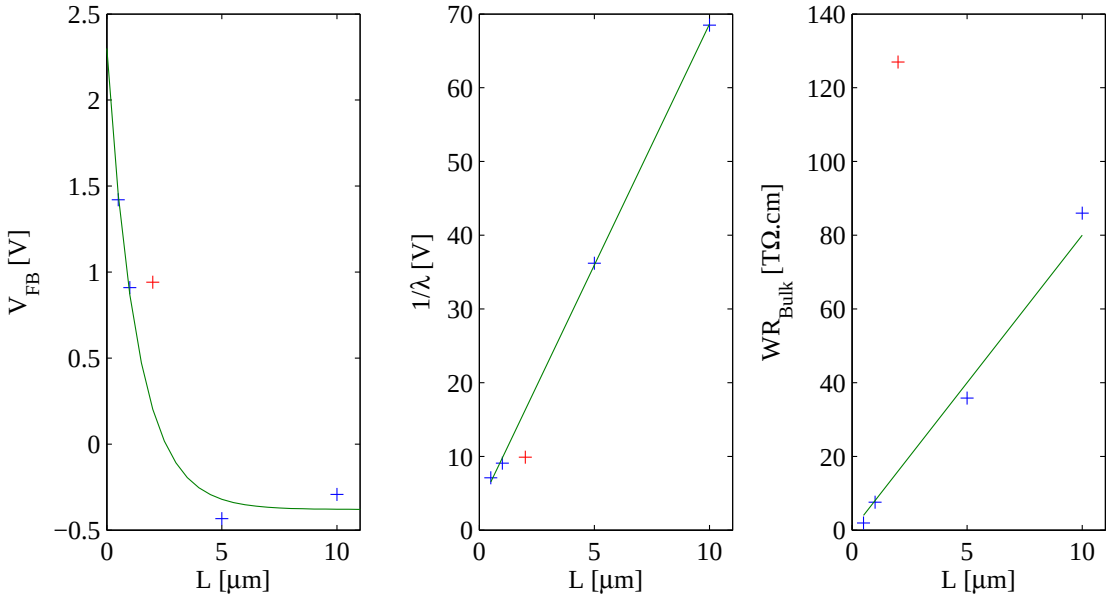


Figure 3.15: Level-2 PEM. Experimental data (+) used (blue) or ignored (red) for the corresponding fits (green lines).

next section.

The Modified Transmission-Line Method introduced in Section 3.3.2was applied to this set of OTFTs at $V_{DS} = -0.5$ V and the extracted contact resistance was fitted for $V_{GS} \leq -2.5$ V with the following empirical function, giving $r_{C0} = 41.4\ \Omega.m$ and $V_{C0} = 7.81$ V.

$$WR_{Contact}(V_{GS}) \approx r_{C0} \exp\left(\frac{V_{GS}}{V_{C0}}\right) \tag{3.18}$$

This pragmatic expression is less accurate than Xu's empirical one [127], Zaumseil's one developed for top-contact OTFTs [122] or Torricelli's one developed for ZnO TFTs [128], but it requires only two parameters and has no singularity.

Finally the model was implemented into Verilog-A with a module for the long-channel transistor (using the parameters from Eq. 3.17, $\gamma_{L=10\mu m}$ and $\mu_{0,L=10\mu m}$) and a module for the contact resistances ($R_S = R_D = R_{Contact}/2$ from Eq. 3.18). The simulations – run in Cadence®Virtuoso®Spectre®– shown in Figure 3.16 confirm that the Level-2 static model matches well the experimental data for the whole range of channel lengths.

Comparing the Figures 3.14a and 3.17 shows that the quality of the fit is lower than with the Level-1 model. However a single set of 10 model parameters is enough for all transistors instead of one set of 5 model parameters per transistor. The values of the Level-2 model parameters are gathered in Table 3.2.

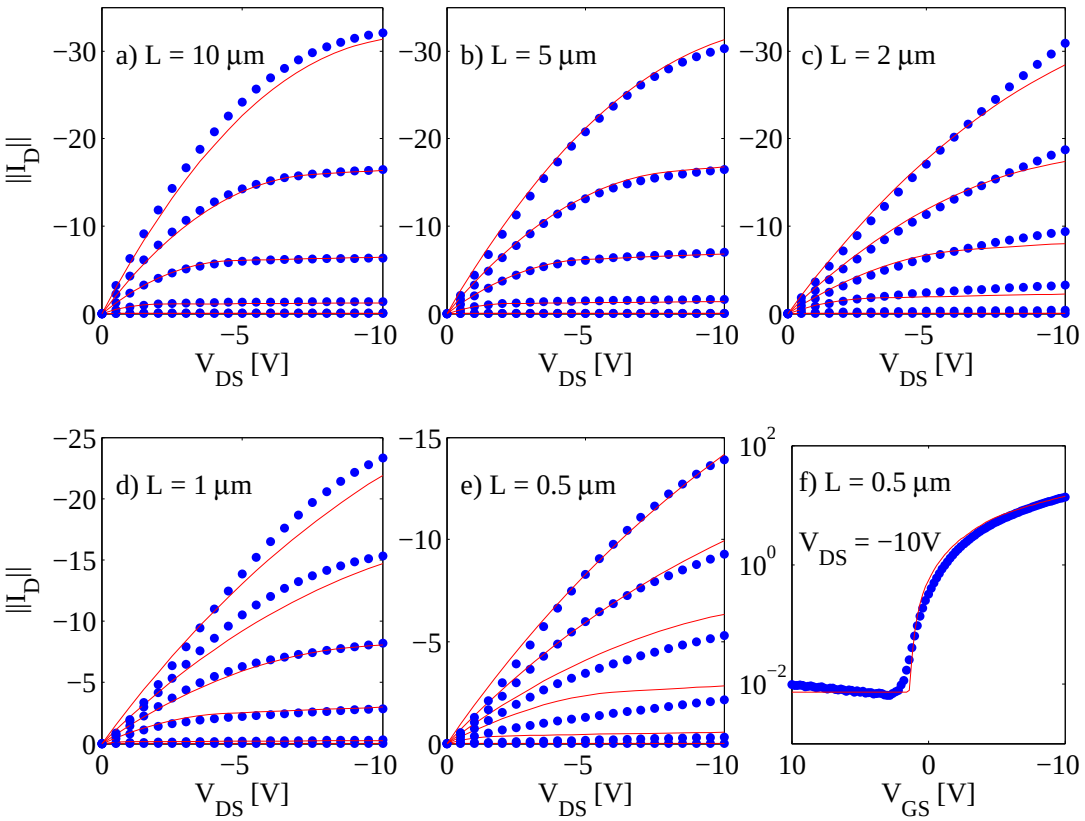


Figure 3.16: Normalized drain current $\|I_D\| = L/(WC_i) \times I_D$ versus voltage curves with experimental data (•) and Level-2 simulations (lines) of OTFTs with: a) and b) $W = 500\,\mu$m, c) and d) $W = 100\,\mu$m, e) and f) $W = 50\,\mu$m. $C_i = 17$ nF/cm^2 except for a) where $C_i = 23$ nF/cm^2 (sample with 150-nm-thin dielectric).

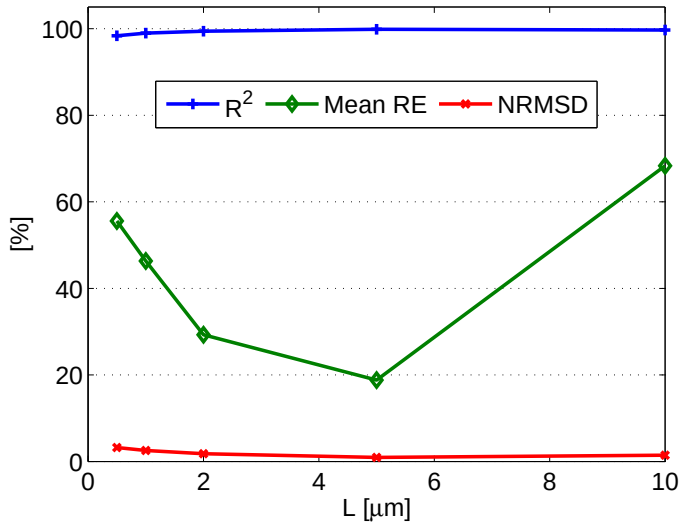


Figure 3.17: Model matching indicators versus L for the Level-2 model.

Table 3.2: Values of the obtained Level-2 model parameters.

μ_0 [cm^2/Vs]	γ	$V_{FB,Long}$ [V]	V_{RO} [V]	L_{RO} [μm]	θ [μm/V]	ΔL [μm]	ρ_{Bulk} [kΩ.m]	r_{C0} [Ω.m]	V_{C0} [V]
0.460	0.191	-0.38	-2.68	1.31	0.153	0.50	2.4	41.4	7.81

3.4.3 Implementation of the subthreshold regime: Level-3 model

The subthreshold regime has to be taken into account when a large mismatch is observed in this region between the model and the experimental data. A possible indicator is $\Delta V = |V_{FB} - V_{ON}|$: the larger the more needed is the subthreshold regime.

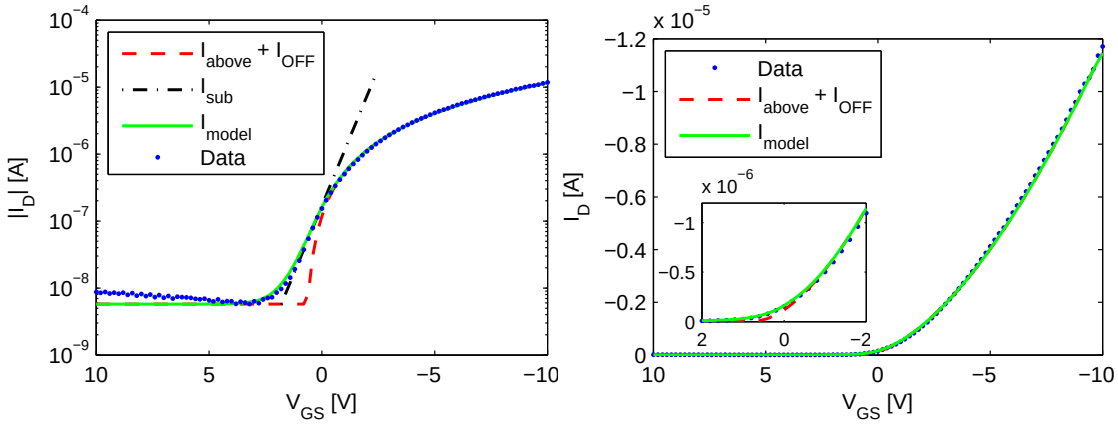
This is particularly true for the sub-micrometer OTFTs of BG6. Thus in this section only the BG6 sub-micrometer OTFTs are considered to model the subthreshold regime and combine it to the above-threshold model described in the previous section (I_{above} in Eq. 3.11). To do so, the subthreshold current model (I_{sub} in Eq. 3.19) and the transition method to connect it to the above-threshold model (cf. Eq. 3.20) both reported in [139] were chosen.

$$I_{sub} = I_{OFF} \exp\left(\frac{\ln(10)}{SS}\left(V_{GS} - V_{ON}\right)\right) \tag{3.19}$$

$$I_D = I_{above} \times \frac{1}{2}\left[1 - \tanh\left(B\left(V_{GS} - V_B\right)\right)\right] + I_{sub} \times \frac{1}{2}\left[1 + \tanh\left(B\left(V_{GS} - V_B\right)\right)\right] + I_{OFF} \tag{3.20}$$

In Eq. 3.19, SS is the subthreshold swing (the inverse of the subthreshold slope) and V_{ON} is the turn-on voltage which is defined as the voltage at which the subthreshold current crosses the off current, see [139]. In Eq. 3.20, B and V_B are empirical parameters tuning the transition between the two regimes. V_B is extracted as proposed in [139] and is *the voltage at which the vertical distance between I_{above} and I_{sub} is minimum* and B is obtained by non-linear fitting. This PEM including the subthreshold regime was added to the Level-1 PEM (without contact resistance nor L-dependent parameters). Once applied to a single submicron OTFT, the updated Level-1 model well matches the experimental data as shown in Figure 3.18.

In order to optimize the results when including the sub threshold model for submicron OTFTs with the above-threshold one, the value of the parameter $V_{FB,Long}$ was set to -1.13 V instead of -0.38 V in [88] (the reason is given in Section 4.4, Figure 4.12). Using the values of SS and V_{ON} extracted in Figure 3.18 for I_{sub} together with the values of the related I_{above}-parameters gathered in Table 3.2 gives $V_B = -0.2$ V. Finally the constraint $SS_{final} = SS_{parameter}$ (= 1.22 V/dec) leads to $B = 0.85$. Table 3.3 summarizes the parameters used for the implementation of the subthreshold regime while Figure 3.19 shows the good match with experimental data as well



(a) Logarithmic scale.

(b) Linear scale. Inset: zoom.

Figure 3.18: Transfer curve at $V_{DS} = -10$ V of an OTFT with $L = 0.5$ μm, $W = 25$ μm and simulations with Level-1 PEM without and with subthreshold regime model. Extracted parameters: $V_{\mathrm{FB}} = 0.67$ V, $\gamma = -0.33$, $\mu_0 = 0.17$ cm^2/Vs, $\lambda = 0.16$ V^{-1}, $R_{\mathrm{Bulk}} = 1.73$ GΩ ; $SS = 1.22$ V/dec, $V_{ON} = 1.80$ V, $V_B = -0.20$ V and $B = 2.94$.

as the improvement with respect to [88].

Table 3.3: Values of the Level-3 model parameters to implement the subthreshold regime in Figure 3.19.

$V_{\mathrm{FB,Long}}$ [V]	SS [V/dec]	V_{ON} [V]	V_B [V]	B [1/V]
-1.13	1.22	1.80	-0.2	0.85

3.5 Temperature dependency

In this section, the temperature-dependent measurement performed on a TG3 OTFT in Section 2.3 will be further analyzed. Nonetheless this field is extensively covered in the literature dealing with the study of charge transport mechanisms and the temperature dependency is included in the charge transport models used by the drain current models introduced in the previous section.

First the temperature-dependent drain and gate currents are plotted in Figure 3.20 versus the gate voltage for three drain voltages: $V_{\mathrm{DS}} = -0.1$ V, -1.1 V and -8.1 V. At $V_{\mathrm{DS}} = -0.1$ V, the gate leakage is significant and even larger than the drain current for $V_{\mathrm{GS}} < -4$ V whereas for the two other drain voltages, $I_{\mathrm{G}} \ll I_{\mathrm{D}}$. For this reason the analysis performed in the linear regime, which follow, will both consider $V_{\mathrm{DS}} = -0.1$ V and -1.1 V.

In terms of OTFT figures of merit, the ON/OFF ratio decreases when the temperature increases. The reason is that the ON current increases slower (linearly) than the OFF current (see Sec-

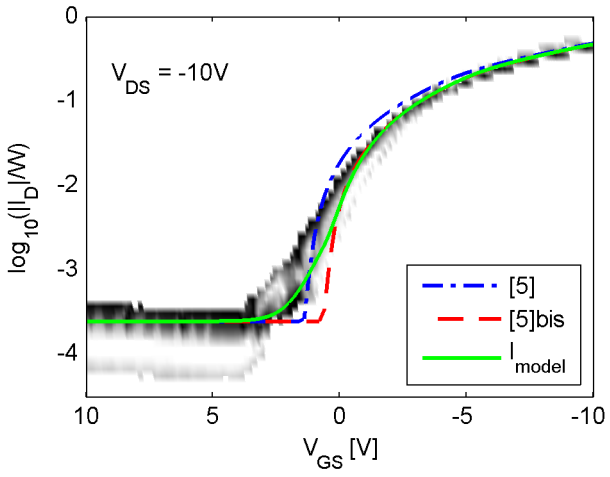


Figure 3.19: Normalized current in logarithmic scale for 8 submicron OTFTs and simulations. These OTFTs are represented by means of a grey scale density which reflects to the occurrence of the data. Level-2 model from Section 3.4.2 ([5]), with optimized $V_{\mathrm{FB,Long}}$ ([5]bis) and with the subthreshold regime (Level-3, I_{model}). The values of the parameters are listed in Tables 3.2 and 3.3.

tion 3.2) as depicted in Figure 3.21a. On the other hand, $I_{\mathrm{G}}/I_{\mathrm{D}}$ remains constant with respect to temperature meaning that the gate leakage increases as the drain current.

As for silicon MOSFETs, the subthreshold swing increases with the temperature. This is shown in Figure 3.21b at $V_{\mathrm{DS}} = -8.1$ V but also at $V_{\mathrm{DS}} = -1.1$ V. Linear fits provide the slope factor, n, since:

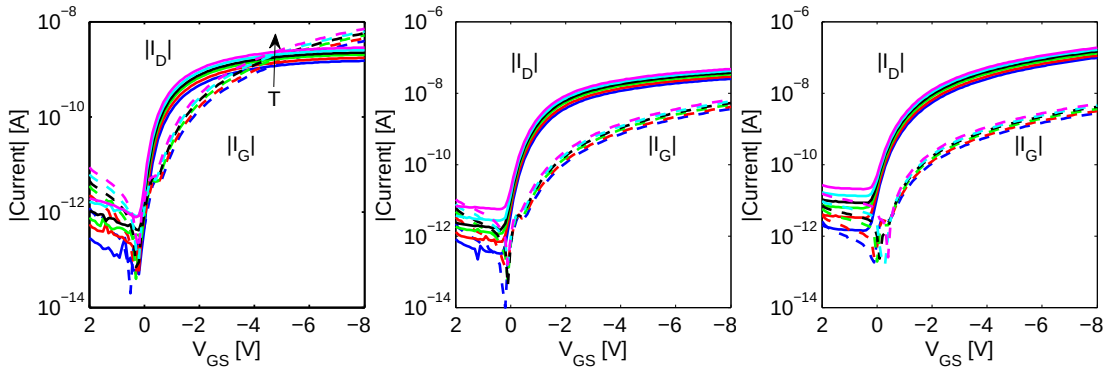
$$SS = \frac{nk_BT}{q}\ln(10) \tag{3.21}$$

At $V_{\mathrm{DS}} = -8.1$ V and -1.1 V, the obtained values are $n = 7.06$ and 5.04, respectively.

In a first step, the linear mobility was extracted with the standard linear fit at two drain voltages: $V_{\mathrm{DS}} = -0.1$ V and $V_{\mathrm{DS}} = -1.1$ V and compared with the standard saturation mobility in Figure 3.21c. As mentioned above, the gate leakage dominance explains the discrepancy observed at each temperature between the saturation and linear mobility extracted at $V_{\mathrm{DS}} = -0.1$ V.

Figure 3.21c shows that the saturation and both linear mobilities exhibit an Arrhenius-like behavior with activation energies $E_a = 31.6$ meV, $E_a = 32.6$ meV and $E_a = 30.8$ meV, respectively. The activation energy increases with the amount of disorder and the typical activation energy range for P3HT samples with a mobility around 0.1 $\mathrm{cm}^2/\mathrm{Vs}$ is 20 – 40 meV [123]. With the polymer semiconductor used for TG3 exhibiting such mobility values, the obtained value for the activation energy is thus validated.

In a second step, the linear mobility was calculated at each gate voltage for both V_{DS} values –



(a) $V_{DS} = -0.1$ V. (b) $V_{DS} = -1.1$ V. (c) $V_{DS} = -8.1$ V.

Figure 3.20: Drain and gate current versus gate voltage at different temperatures: 200K < T < 300K (20K step).

see Equation 1.1. Figures 3.22a and 3.22b both show than μ_{lin} increases as expected but then reach a maximum before decreasing. Since the decrease rate is much larger at $V_{DS} = -0.1$ V than at $V_{DS} = -1.1$ V, this phenomenon is again attributed to the gate leakage.

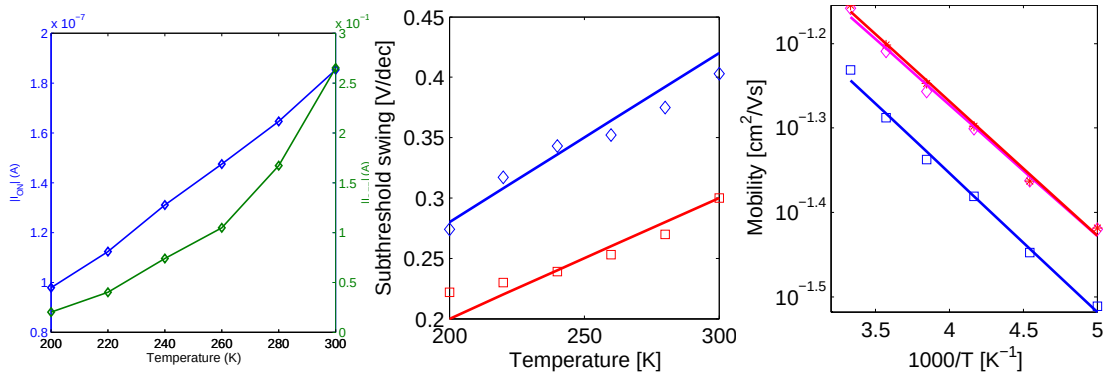
By considering only the first regime where μ_{lin} increases when plotting μ_{lin} versus $1/T$ at different V_{GS} in a semi-logarithmic scale, an Arrhenius-like behavior is also observed. A linear fit can extract the corresponding activation energy, E_a, which is plotted for each gate voltage in Figure 3.23.

3.6 Rise-time

The rise time measurement of TG3 OTFTs with different channel lengths and widths is shown in Figure 3.24a. Surprisingly the rise time does not decrease with shorter channel length as expected. Instead it increases.

The first hypothesis to explain this behavior is that the large parasitic overlap capacitance between the gate and the source and drain contacts could overwhelm the gain in speed of the intrinsic transistor channel. Since the large gate contact is the same for all OTFTs, the overlap area actually decreases when the channel length increases, as visible in Figure 3.24b. To quantify the importance of the channel area with respect to the overlap area, we define the relative channel area which is equal to the channel area over the total area (channel + overlap). The results, visible in Figure 3.24c, show that the relative channel area is below 3% for $L = 2$ μm and does not reach 20% for $L = 20$ μm which can confirm this hypothesis.

The second hypothesis to explain the rise-time behavior is that the spread of performance within these OTFTs affects the ideal and expected behavior. Since the transit frequency is proportional to the mobility, this parameter – μ_{sat} – is selected for this hypothesis and is plotted in Figure 3.24d. Correlations can be found with the rise-time behavior. Thus a first



(a) (b) (c)

Figure 3.21: (a) ON (⋄) and OFF (□) current, (b) subthreshold swing and (c) linear and saturation (+) mobilities versus temperature. (b) Subthreshold swing extracted at $V_{DS} = -8.1$ V (⋄) and -1.1 V (□) shown with corresponding linear fits. (c) Linear mobility extracted at $V_{DS} = -0.1$ V (□) and -1.1 V (⋄) shown with corresponding linear fits. TG3 OTFT.

proposal to normalize the rise-time is: $\| t_{rise} \|_1 = t_{rise} \mu_{sat}$. As visible in Figure 3.24e, the results show no specific behavior with respect to the channel length.

By combining these two hypothesis, a new normalization of the rise-time is proposed:

$$\| t_{rise} \|_2 = t_{rise} \mu_{sat} \frac{A_{ov}}{A_{ch} + A_{ov}} \tag{3.22}$$

$\| t_{rise} \|_2$, shown in Figure 3.24f, exhibits the expected behavior i.e. it increases with the channel length. In addition, the linear fit shown in Figure 3.24f (dash line) can then provide a semi-empirical model for the rise-time:

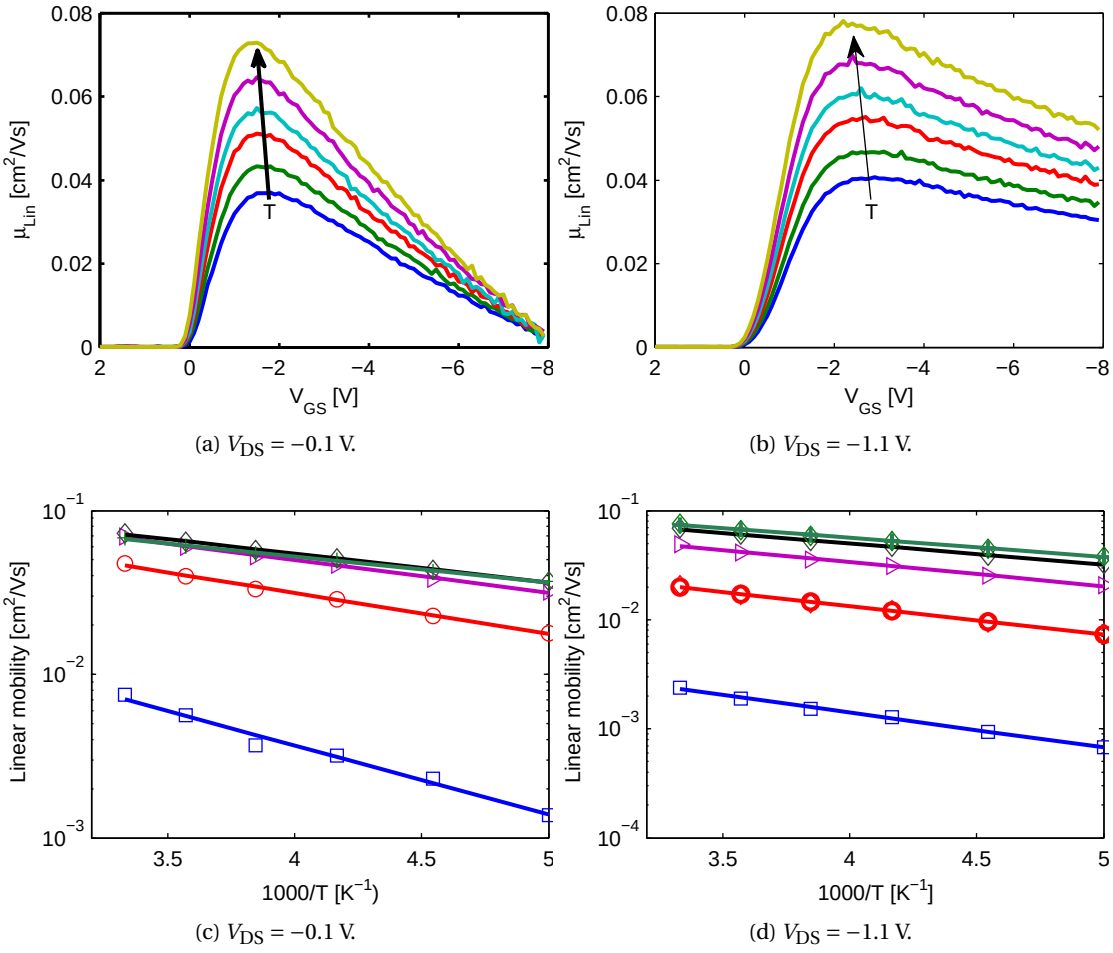
$$t_{rise} = \frac{0.0719\,(A_{ch} + A_{ov})}{\mu_{sat} A_{ch}} L \tag{3.23}$$

where, for TG3 transistor layout, $A_{ch} = WL$ and $A_{ov} = 2 \times 20 \times W + (450 - L - 2 \times 20) \times 50$ (in μm^2).

3.7 Gate leakage

The gate leakage current was neglected in the compact model introduced in this chapter as does most of the OTFT compact models reported so far, see Table 3.1. Knowing its maximum values in the ON and OFF regime is often enough to design circuits. It was however shown in this chapter and the previous ones that the gate leakage can disturb the parameter extraction procedure. Thus there is a need for de-embedding the gate leakage when it is not negligible.

The gate can leak to the source, I_{GS}, and to the drain, I_{GD}. The different relationships with the



(a) $V_{DS} = -0.1$ V. (b) $V_{DS} = -1.1$ V.

(c) $V_{DS} = -0.1$ V. (d) $V_{DS} = -1.1$ V.

Figure 3.22: (a)–(b): Linear mobility versus gate voltage at different temperatures: 200K $< T <$ 300K (20K step). (c)–(d): Arrhenius plot and associated linear fits at different gate voltages: $\square$: $V_{GS} = 0.0$ V, $\bigcirc$: $V_{GS} = -0.5$ V, $\triangleright$: $V_{GS} = -1.0$ V, $\diamond$: $V_{GS} = -1.5$ V and $+$: $V_{GS} = -2.0$ V.

transistor current, I_{TFT} (the intrinsic channel and contact resistances) are gathered below:

$$I_G = I_{GS} + I_{GD} = \alpha I_G + (1-\alpha) I_G \text{ with } 0 \leq \alpha \leq 1 \tag{3.24}$$

$$I_D = I_{TFT} - I_{GD} \tag{3.25}$$

$$-I_S = I_{TFT} + I_{GS} \tag{3.26}$$

The particular case where $\alpha = 0.5$ gives:

$$I_{TFT} = (I_D - I_S)/2 \tag{3.27}$$

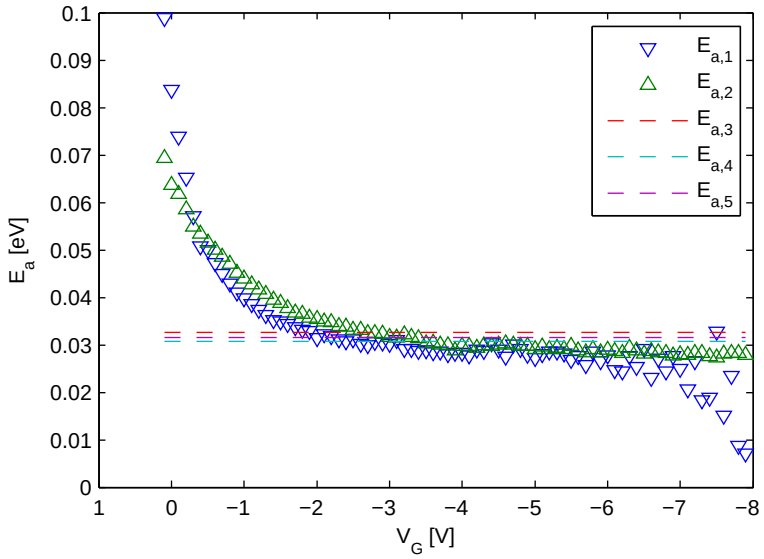


Figure 3.23: Activation energy versus V_{GS} calculated at $V_{DS} = -0.1$ V ($E_{a,1}$) and -1.1 V ($E_{a,2}$). Independent activation energy values calculated from the standard μ_{lin} (linear fit) extracted at $V_{DS} = -0.1$ V ($E_{a,3} = 32.6$ meV) and -1.1 V ($E_{a,4} = 30.8$ meV) as well as from the standard μ_{sat} ($E_{a,5} = 31.6$ meV). TG3 OTFT.

Equation 3.27 gives an easy way to de-embed the gate leakage but only under the assumption $\alpha = 0.5$ *i.e.* $I_{\text{GS}} = I_{\text{GD}} = I_{\text{G}}/2$. This assumption was not proven in this thesis but can be supported when there is no strong evidence of a privilege leakage contact. A counter-example is $I_{\text{OFF}} \ll I_{\text{G}}$ at low V_{DS} which means that the gate leaks to the source contact *i.e.* $\alpha \approx 1$.

Modeling effort can be spared by considering the worst case scenario *i.e.* where the gate leakage is the highest. In terms of drain voltage, this translates to considering $V_{\text{DS}} = 0$ V only *i.e.* $V_{\text{GS}} = V_{\text{GD}} = V_{\text{GC}}$.

At $V_{\text{DS}} = 0$ V, an observation common to the technologies shown in Figure 3.25 is that the gate leakage exhibits in semi-logarithmic scale an asymmetric "V" shape. When the transistor is OFF ($V_{\text{GS}} > V_{\text{ON}}$, for a p-type OTFT), the gate leakage seems ohmic. Then once the transistor is turned ON, the gate leakage seems to follow a power law which could be linked to a space-charge limited current (SCLC). In the OFF mode, this translates to:

$$I_{\text{G,OFF}} = \frac{V_{\text{GS}}}{R_{\text{GS}}} + \frac{V_{\text{GD}}}{R_{\text{GD}}} \underbrace{=}_{V_{\text{DS}}=0\text{ V}} \left(\frac{1}{R_{\text{GS}}} + \frac{1}{R_{\text{GD}}}\right) V_{\text{GS}} \tag{3.28}$$

Zaki *et al.* [129] have used this model with $R_{\text{GS}} = R_{\text{GD}} = R_{\text{L}}$ and where "*the value of R_L related to the contact area is typically very high (10^{14} μm^2) to reflect leakage currents in the order of 10 pA*" [129].

A space-charge gate leakage would read: $I_{\text{G}} \propto V_{\text{GC}}^{\delta}$ with $\delta = 3/2$ for the Child-Langmuir law and $\delta = 2$ for the Mott-Gurney law. However no common behavior was found for the technologies

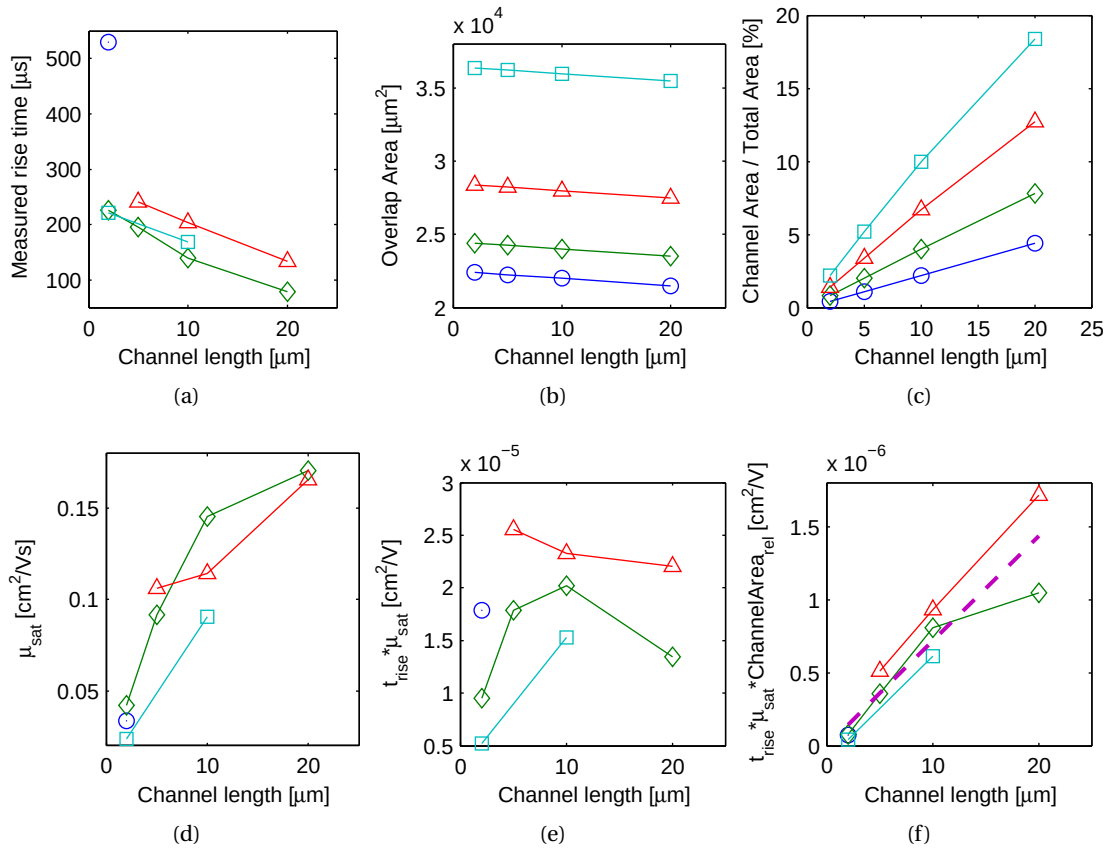


Figure 3.24: Rise time measurement and analysis for different channel widths: ◯ : $W = 50$ μm, ◇ : $W = 100$ μm, △ : $W = 200$ μm and □ : $W = 400$ μm.

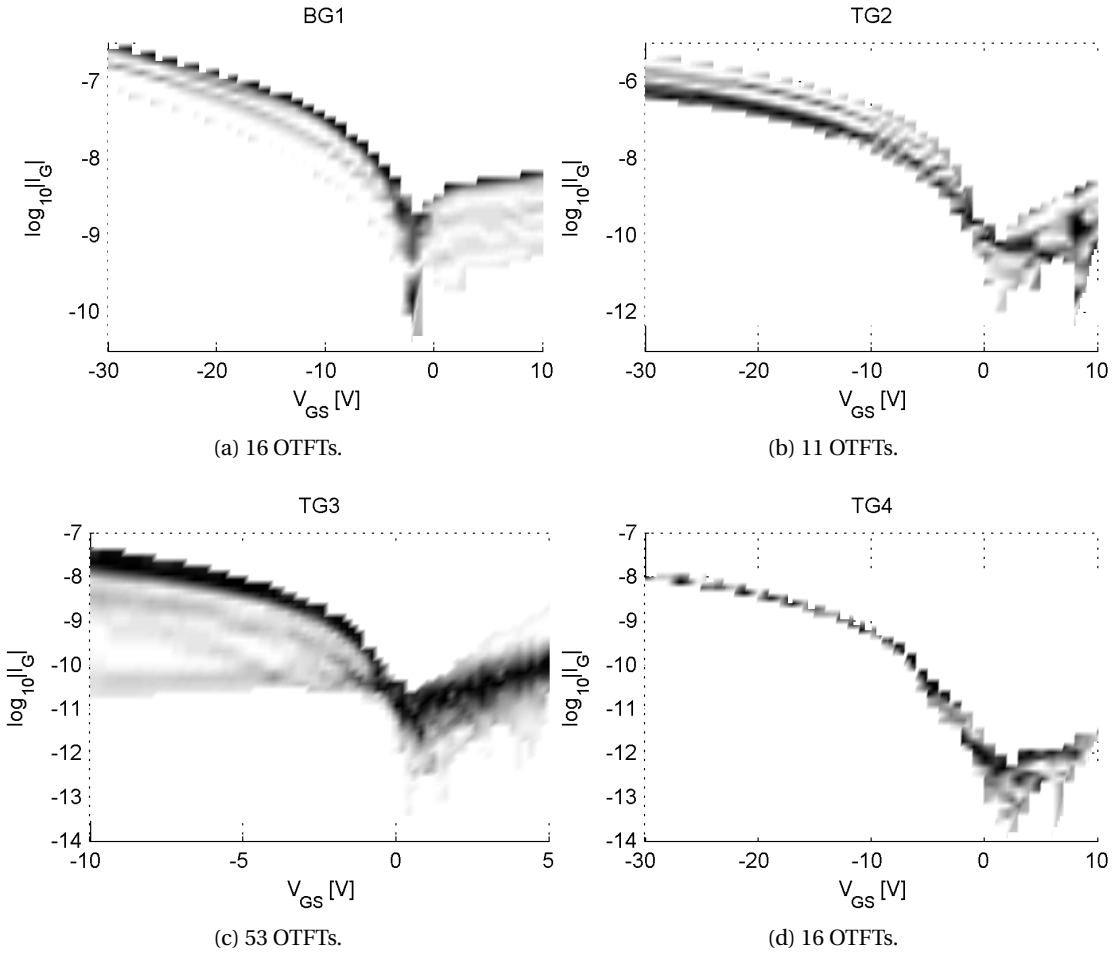
shown in Figure 3.25. Indeed the obtained values for the exponent δ vary from 1.92 (BG1) to 3.11 (TG4) – fits available in Appendix. Considering $I_G \propto (V_{GC} - V_T)^{\delta}$ instead does not exhibit a common behavior either: this time, δ varies from 1.45 (BG1) to 2.32 (TG3). Anyway this invalidates the use of a constant resistor R_L as in [129].

The empirical model by Xiong *et al.* [9]: $I_G \approx I_0 \left(\exp(V_{GC}/a) - 1\right)$ was also tested but without success. In those conditions, the modeling of the gate leakage was dropped.

3.8 Summary

The state of the art, at the end of this thesis, in terms of OTFT modeling is summarized in Table 3.4 which inputs are commented below.

Zaki *et al.* [129] used the model from Marinov [105] with contact resistances and its effective voltage overdrive used for the subthreshold regime and added anti-parallel diodes to deal with non-linear behavior in the linear regime. The source/drain-gate overlap capacitors were also



(a) 16 OTFTs.

(b) 11 OTFTs.

(c) 53 OTFTs.

(d) 16 OTFTs.

Figure 3.25: Gate leakage versus V_{GS} at $V_{DS} = 0$ V for different technologies shown in a density form. OTFTs with various channel lengths and widths.

added to simulate the dynamic behavior: $C_{gg} \approx 2C_{overlap} + (2/3)WLC_i$ and $C_{gs} = C_{gd} = C_{gg}/2$. This approach was unsuccessfully tested in this thesis to reproduce the behavior of BG6 ring-oscillators (explaining the "S" in the "AC" and "Circuits" columns). Moreover resistors were added to reflect the gate leakage current (as detailed in Section 3.7). This AC/DC model once implemented in SPICE allowed the transient simulation of a thermometer decoder and a good match was obtained with experimental measurement. A small-signal model was then developed and successfully confronted to experimental measurements in [144].

Torricelli *et al.* [141] proposed a DC model for pentacene OTFTs with two exponential functions describing the density of states: namely for tail and deep states, . This method allows taking into account the mismatch observed in the subthreshold regime. Following the same approach proposed for amorphous-silicon TFTs in [], the two regimes are combined as follows: $1/I = 1/I_{deep} + 1/I_{tail}$. It can be noted that the subthreshold regime itself is not exponential as for MOSFETs. This model was used by Raiteri *et al.* to design analog circuits such as a tunable

Table 3.4: State-of-the-art OTFT modeling, part II: at the end of the thesis (2013). "Stats." refers to statistical model. "AC" refers to dynamic model with simulations only (S) or matching experimental data (✓). "PEM" indicates whether the parameter extraction method is given. "EDA impl." refers to the model implementation. "Circuits" indicates whether circuits (including inverters) are simply simulated (S) or matching experimental data (✓) in static/transient operation. *Results published in [88, 140]

Year	Ref.	I_{OFF}	R_C	Sub-V_T	I_G	Stats.	AC	PEM	EDA impl.	Circuits
2011	[129]	-	✓	✓	✓	-	S	[112]	SPICE	?/✓
2012	[141]	-	-	✓	-	-	-	[112]	-	-/-
2012	[142]	-	✓	✓	-	✓	-	[143]	(Verilog-A)	✓/-
2013	[144]	-	✓	-	-	-	✓	?	?	-/-
2013	[139]	✓	✓	✓	-	-	-	[73]	SPICE	-/-
This thesis*		✓	✓	✓	-	✓	S	✓	Verilog-A	S/S

transconductor [145] and a synchronous rail-to-rail latched comparator [146]. The PEM of this model was implemented into my modeling platform ("T-C" in Figure A.12). Torricelli *et al.* [143] have then extended this model using Valletta's diode approach [125] to model contact effects. Abdinia *et al.* [142] used this latest version to design various circuits exhibiting a good match between simulations and measurements. Moreover Abdinia *et al.* [142] added the statistical dimension by running Monte-Carlo simulations of inverters.

Kim *et al.* [139] have proposed an advanced compact model for OTFTs based on the unified model and parameter extraction method (UMEM) [73, 110] which, among other new features, mainly extends it by adding the subthreshold-current model which was actually selected for this thesis. The OFF current is present but appears to be constant as well as the contact resistances. A review on OTFT compact models was also recently published by Kim *et al.* [147].

In this chapter we demonstrated that combining existing models into a DC model can successfully simulate the behavior of a broad range of OTFTs including the sub-micrometer OTFTs [88, 140]. In addition, a dedicated parameter extraction platform was developed in the framework of this thesis. More details about the developed tool are available in Appendix (Section A.3.1). Given that the device-to-device discrepancy affects the precision of the PEM, and therefore the model parameters, we will address this specific aspect in the next chapter through statistical modeling.

The outlook for OTFT modeling would be to implement the channel length dependency of the subthreshold swing related to short channel effects and develop a dynamic model.

4 Statistical modeling

4.1 Introduction

One of the reasons why OTFTs are not yet widely used in working circuits is their large spread of performance parameters such as threshold voltage and mobility. Indeed, a large variability occurs in both batch-to-batch and device-to-device scales. This makes the design of analogue/digital blocks particularly challenging. Therefore, a different approach is needed for the designer in order to compete with the before mentioned variability issues. In the following sections, this aspect will be investigated in order to bridge the gap between the measured device spread and circuit design.

In Section 4.2, different early technologies (BG1, BG2, BG3, TG1 and TG2) will be compared in a representation used for silicon MOSFET, the so-called g_m/I. An invariant will be identified and the route towards the related g_m/I design methodology will be discussed. This work was published in [148].

Then in Section 4.3, the Level-2 PEM introduced in the previous chapter will be performed in a statistical way. Indeed the Level-2 PEM requires to select OTFTs with different channel lengths. The selection process will be random whereas in Section 3.4.2 the OTFTs were selected arbitrarily. This statistical PEM will be applied to the sub-micrometer OTFTs from BG6 and discussed.

Finally in Section 4.4, another statistical approach, this time based on corner modeling, will be introduced and also applied to the sub-micrometer OTFTs from BG6. This work was accepted for publication in [140] and is currently in press.

4.2 Towards a g_m/I design methodology for OTFTs

In this section we show based on experiments that an invariant representation exists for various polymer-based solution processable organic thin film transistors (OTFTs). Despite the fact that this technology suffers from a non-negligible spread of parameters, all experimental

data exhibit low dispersion when represented in a g_m/I_D versus I_D diagram. This result is important for circuit design strategy based on the g_m/I_D representation, giving more insight into analogue design methodology. In addition, the g_m/I_D invariant can also be used to extract the gate voltage mobility dependence that is inherent to organic field effect transistor.

4.2.1 The g_m/I_D design methodology for OFETs

The g_m/I_D ratio characterizes the transconductance of a transconductor obtained for a given current level [149]. It can hence be used as a figure-of-merit (FoM) to compare the current-efficiency of different transconductors. Together with the inversion coefficient I_C defining the state of inversion of the channel, it can also be used to properly size transistors according to initial specifications such as gain, bandwidth, noise, etc. [149, 150, 151]. For silicon MOSFETS, the g_m/I_D characteristic versus the inversion coefficient has this unique property to remain invariant to process parameters (for long-channel devices) as shown in Figure 4.1.

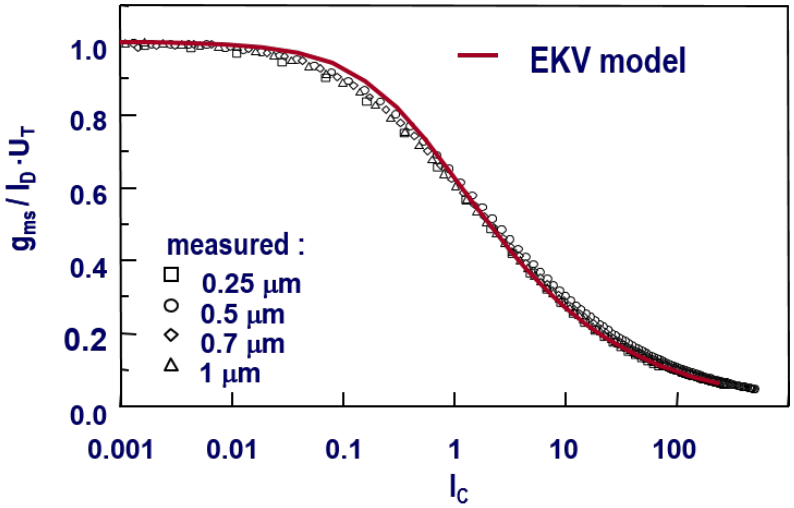
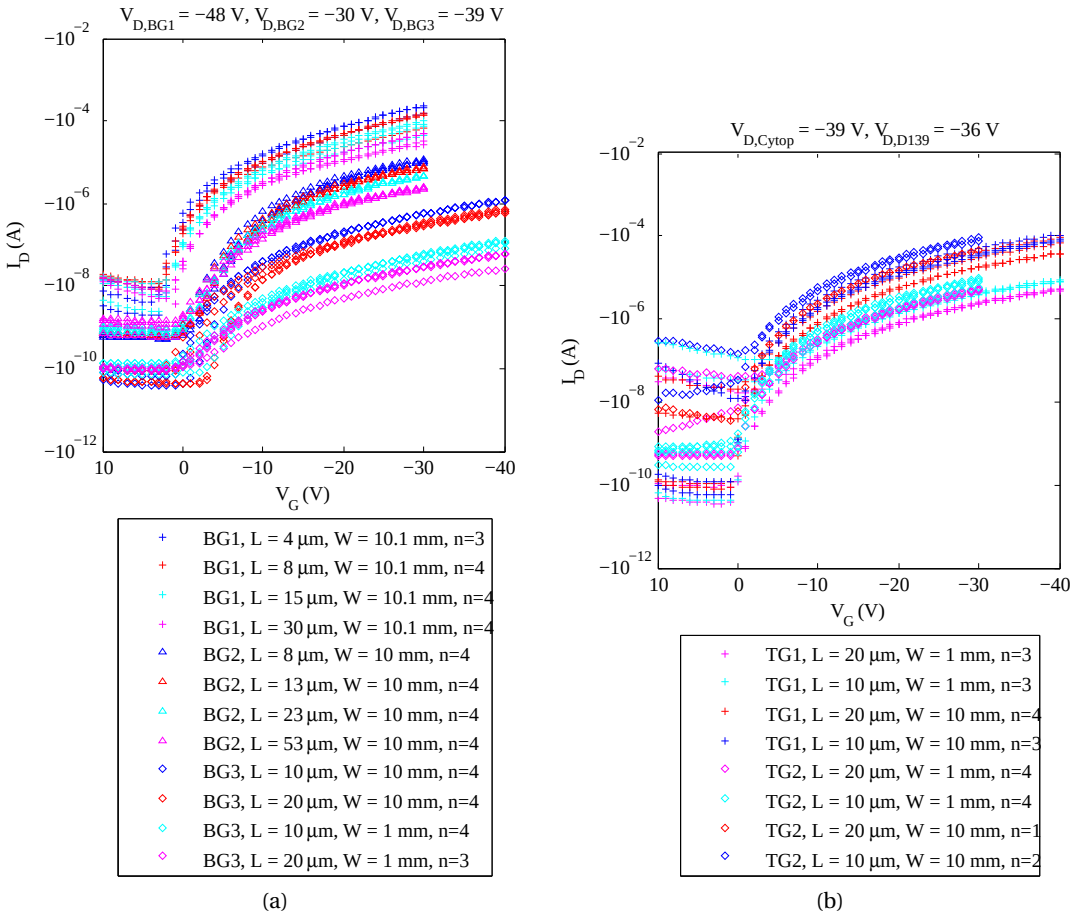


Figure 4.1: Typical g_m/I versus I_C diagram for silicon MOSFETs with different channel length. Adopted from [152].

This section investigates whether such an invariant property also exists for polymer-based OFETs, despite their different current transport mechanism. A few attempts have been done to analyze the g_m/I_D characteristics for small molecules OTFTs. In Ref. [68], Murmann et al. attempted a comparison of DNTT [153] OFETs with simulated 0.35 μm MOSFETs. But these did not bring a strong evidence for any kind of figure of merit that would deserve design in a large sense. To this purpose, we have extracted the g_m/I_D from measurements and tried to find a proper normalization current similar to the specific current used for silicon MOSFETs [149]. As will be shown later, this will also allow characterizing the mobility bias dependence.

The transfer characteristics in saturation regime are plotted in Figure 4.2 for the transistors used in this section. They are divided in two groups for readability reasons: bottom-gate and

top-gate transistors are plotted in Figure 4.2a and Figure 4.2b, respectively.



(a) (b)

Figure 4.2: Transfer characteristics in saturation regime of the different bottom-gate (left) and top-gate (right) OTFTs used for the g_m/I analysis. L: channel length. W: channel width. n: number of OTFTs plotted.

The transfer curves show that the studied samples exhibit distinct characteristics in terms of performances and V_{ON}, although four samples are made from the same semiconductor. This was already discussed in Chapter 1.

For a given set of identical transistors, e.g. "BG1, $L = 30$ μm, $W = 10.1$ mm, $n = 4$", Figure 4.2a reveals a spread of performance parameters on the very same substrate which is very problematic for circuit design using OTFTs.

The $g_m/|I_D|$ versus I_D characteristics are plotted in Figure 4.3. Each curve can be clearly decomposed in two asymptotes: one vertical dealing with OFF-currents, and one showing a slope close to the theoretical limit calculated in silicon MOSFETs, $\propto 1/\sqrt{|I_D|}$. This last point will be discussed in the next section.

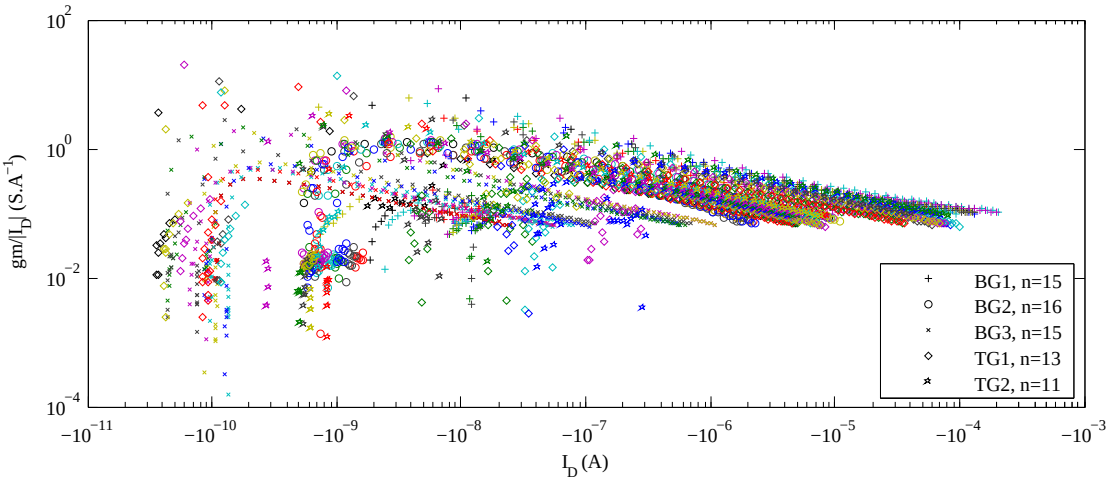


Figure 4.3: g_m/I_D versus I_D characteristics

4.2.2 Normalization of the g_m/I_D versus I_D characteristics

The classical silicon approach has been used to start normalizing the g_m/I_D characteristics using W/L which gathers and sorts group of curves per sample. Then C_i and a constant μ_{FE} have been added to compare samples together [149]. As a first step, the sample scale was considered *i.e.* the mean measured value of μ_{sat} was used as μ_{FE} for each sample. This already forms a common group of curves. Finally each value of μ_{sat} has been applied to the respective transistor.

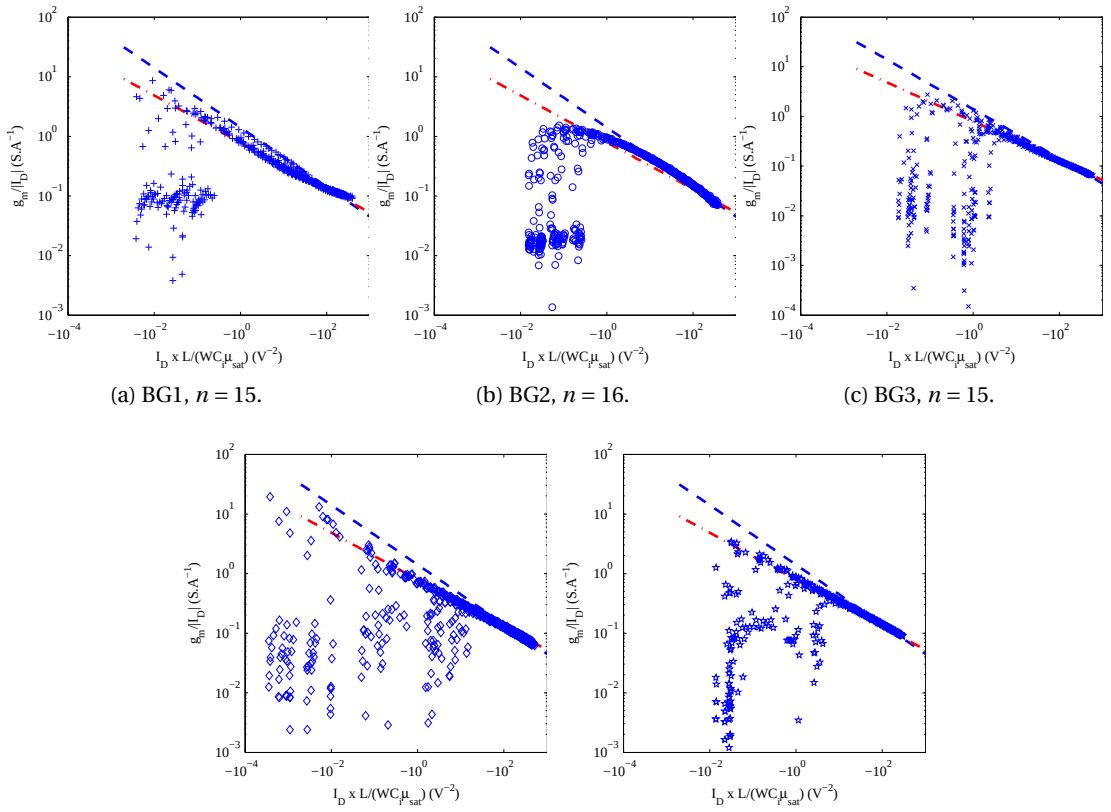
The result of this last step is plotted for each considered technologies in Figures 4.4a–4.4e. The resulting curves of other technologies are available in Appendix, Figure A.13.

4.2.3 Analytical discussion

As visible in Figure 4.5, some transistors and especially the TFTs on BG2 follow the ideal $|I_D|^{-0.5}$ asymptote accurately, however the asymptote of the majority of OTFTS tends to $|I_D|^{-0.4}$. At this point, we assume that this might be attributed to the gate-voltage dependence of the mobility, since this is indeed very peculiar to organic FETs. We will now discuss this point with the gate voltage dependent mobility part of the TFT Generic Charge Drift (GCD) model which was used in this thesis (Section 3.4.1). We are now going to extract the parameters μ_0 and γ of the power law description of the gate voltage dependent mobility using the asymptotic behavior of the normalized g_m/I_D representation in Figure 4.5. The asymptote writes:

$$\frac{g_m}{|I_D|} = 0.79 \left[I_D \frac{L}{W C_i \mu_{\text{sat}}} \right]^{-0.4} \tag{4.1}$$

The absolute value of the GCD drain current in the saturation regime (see Equation 3.11)



(a) BG1, $n = 15$. (b) BG2, $n = 16$. (c) BG3, $n = 15$.

(d) TG1, $n = 13$. (e) TG2, $n = 11$.

Figure 4.4: Normalized g_m/I_D diagram per technology. n: number of OTFTs plotted. Blue dashed line: $\propto |I_D|^{-0.5}$. Red dash-dotted line: $\propto |I_D|^{-0.4}$.

writes:

$$|I_{GCD,Sat.}| = \frac{W}{L} C_i \frac{\mu_0}{\gamma+2} |V_{GS} - V_{FB}|^{\gamma+2} \tag{4.2}$$

In other words, $g_m/|I_D|$ generally writes:

$$\frac{g_m}{|I_D|} = (\gamma+2)\left(\frac{W}{L(\gamma+2)} C_i \mu_0\right)^{\frac{1}{\gamma+2}} |I_D|^{\frac{-1}{\gamma+2}} \tag{4.3}$$

$$= (\gamma+2)\left(\frac{\mu_0}{(\gamma+2)\mu_{sat}}\right)^{\frac{1}{\gamma+2}} \left[|I_D| \frac{L}{W C_i \mu_{sat}}\right]^{\frac{-1}{\gamma+2}} \tag{4.4}$$

Comparing with (4.1), we deduce the mobility parameters: $\gamma = 0.5$ and $\mu_0 = 0.14\mu_{sat}$.

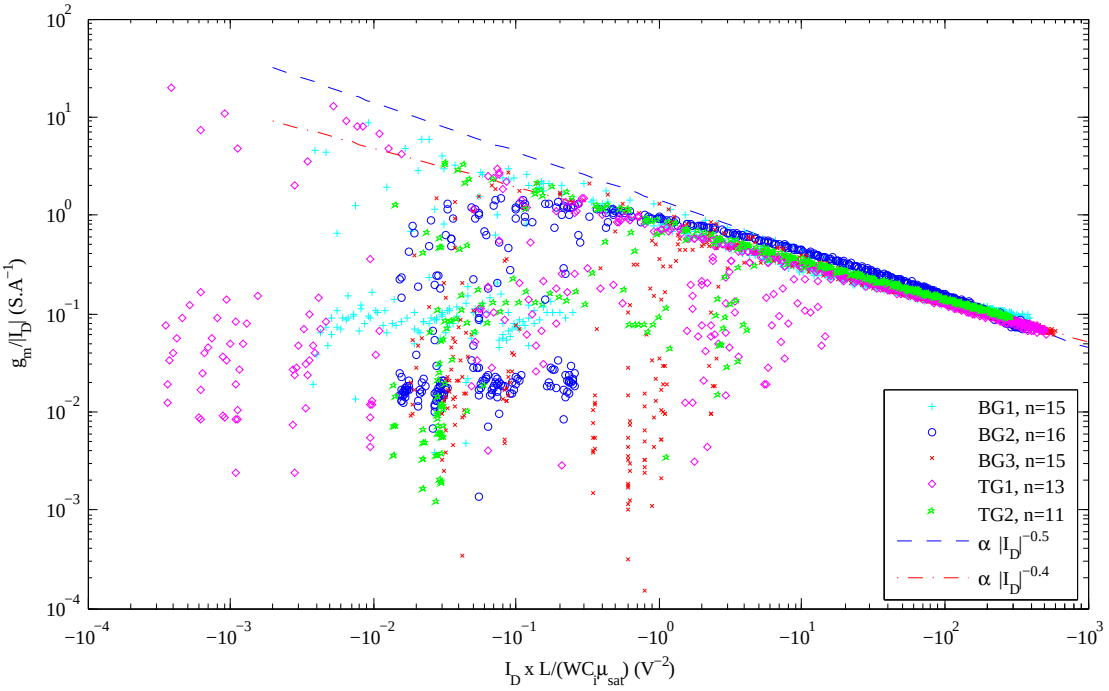


Figure 4.5: Normalized g_m/I_D versus I_D characteristics

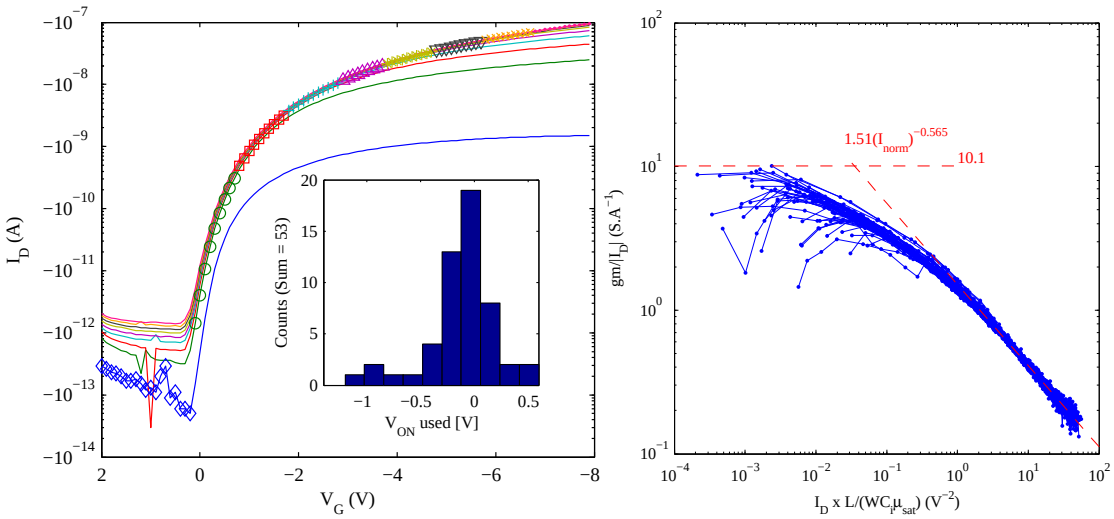
At this point we show experimentally that a quasi-invariant g_m/I_D characteristic exists for OTFTs based on both regioregular P3HT and PTAA polymer semiconductors. This stands for the above-threshold regime where we exhibited the corresponding asymptote. The observed slope was confronted to the ideal $|I_D|^{-0.5}$ MOSFET behavior. Next we will investigate on the second asymptote of the g_m/I_D diagram which, for MOSFETs, corresponds to the weak inversion regime.

4.2.4 Tracking the second asymptote

In this section the focus is set onto the exhibition and the study of the plateau corresponding, for silicon MOSFETs, to the weak inversion regime. This result is an additional step towards the g_m/I_D design methodology.

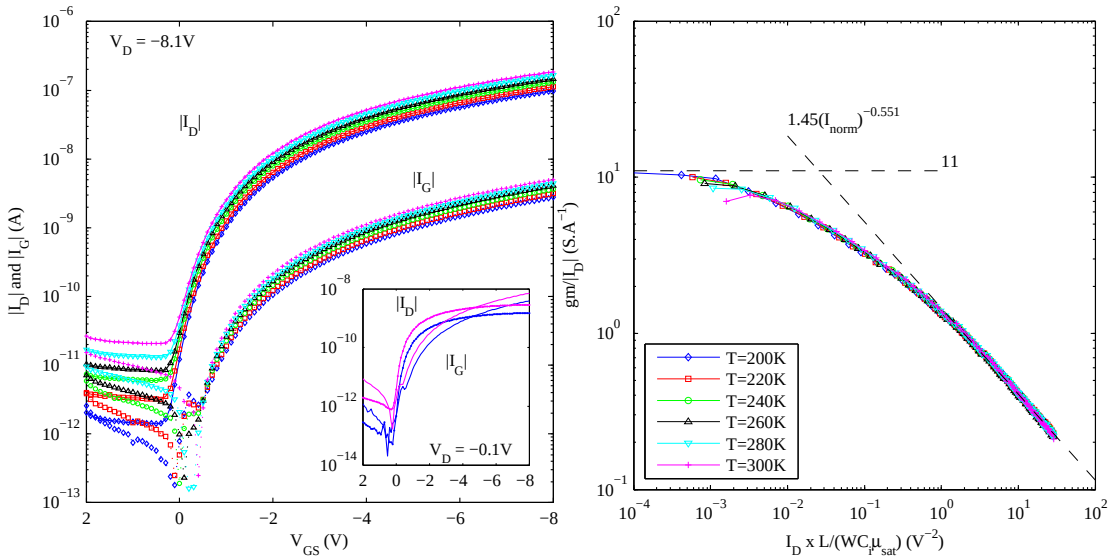
In order to plot the g_m/I_D diagram, the given OTFT has to be in the saturation regime. In the previous sub-section, this was performed by using the maximal available value for V_{DS}. However the OFF-current also increases with V_{DS} which, at $V_{DS,max}$, may prevent a proper observation of the subthreshold regime. On the other hand, at $V_{DS,min}$ the OFF current is minimum but the OTFT is not anymore in saturation.

The trade-off is to use a variable V_{DS} which for each V_{GS} is the first value at which $V_{DS} \geq V_{GS} - V_T$ (for a n-type OTFT). This process is illustrated in Figure 4.6a with V_T chosen to be V_{ON} which is by definition the closest point to the OFF current.



(a) Variable V_{DS} concept. (b) Updated g_m/I_D.

Figure 4.6: (a) Measured transfer characteristics at $T = 200K$ of a TG3 OTFT with $W/L = 400\ \mu m/20\ \mu m$ ($\diamond : V_D = -0.1V$; $\bigcirc : V_D = -1.1V$; $\square : V_D = -2.1V$; $+ : V_D = -3.1V$; $\triangle : V_D = -4.1V$; $* : V_D = -5.1V$; $\bigtriangledown : V_D = -6.1V$; $\times : V_D = -7.1V$; $\bullet : V_D = -8.1V$). (b) Normalized g_m/I_D diagram of 53 TG3 OTFTs obtained using the proposed method (at room temperature). Inset of (a): Distribution of the corresponding turn-on voltages.



(a) $I-V$ vs T. (b) g_m/I_D vs T.

Figure 4.7: (a) Measured transfer characteristics at $V_D = -8.1V$ at different temperatures ($\diamond : T = 200K$; $\square : T = 220K$; $\bigcirc : T = 240K$; $\triangle : T = 260K$; $\bigtriangledown : T = 280K$; $+ : T = 300K$). Inset: details for $V_D = -0.1V$ with $T = 200K$ and $T = 300K$. (b) Normalized g_m/I_D versus I_D diagram plotted using a variable V_D and at different temperatures.

Using this variable V_{DS} concept together with the condition $V_{GS} \geq V_{ON}$ (again for a n-type OTFT) to remove the OFF current leads to the updated g_m/I_D diagram visible in Figure 4.6b. There is a slight inflection of the curves and a plateau even appears for some OTFTs with an amplitude around 10. However the plateau is not well pronounced.

Then this method was applied to the temperature-dependent measurement recalled in Figure 4.7a and the temperature-dependent g_m/I_D diagram is visible in Figure 4.7b. The amplitude of the "plateau" decreases with the temperature as for MOSFETs but for MOSFETs, at 300K, the amplitude is 40. The observed lower amplitude could come from traps which catch mobile charges and thus weaken the free carrier dependence upon V_{GS}. The plateau amplitude could in theory be used to extract the subthreshold swing SS. Doing so at each temperature would lead to the slope factor n where $SS = nV_{\text{thermal}}\ln(10)$ with $V_{\text{thermal}} = k_B T/q$.

Even if a trace of the second asymptote was exhibited in this section, the plateau is less clear than for silicon MOSFET. In addition, the amplitude of this plateau was investigated but not understood. No link with the thermal voltage was found which differs from silicon MOSFET. A clear plateau combined with an explained amplitude could have led to the next step towards a g_m/I design methodology for OTFTs i.e analysis of the intersection of the two asymptotes in a similar way as for the EKV model.

Since this is not the case, other statistical analysis of the Level-2 model will be performed in the next sections.

4.3 Statistical PEM

4.3.1 Preparation of the set of parameters

As introduced in Section 3.4, the PEM extracts the model parameters in two steps. The first step estimates the Level-1 parameters i.e. μ_0, γ, V_{FB}, λ, R_{Bulk} – and optionally the Level-3 parameters for the subthreshold regime, not used in this section. The second step uses V_{FB}, λ, R_{Bulk} and the contact resistances to extract the Level-2 parameters: $V_{\text{FB,Long}}$, V_{RO}, L_{RO}, θ, ΔL, ρ_{Bulk}, V_{CO} and r_{C0}.

The Level-2 model takes into account the channel length dependency of some Level-1 parameters (e.g. V_{FB}) and the contact resistance. In order to perform the related PEM, transistors with different channel lengths are required. Thus with the device-to-device discrepancy generally observed with OTFTs, the transistor selection process will influence the results.

In Section 3.4.2, the Level-2 PEM was performed on a set of 5 BG6 OTFTs arbitrarily chosen, one transistor per channel length. In this section a more exhaustive approach will be studied focusing on the dataset of the technology BG6 including the sub-micrometer OTFTs.

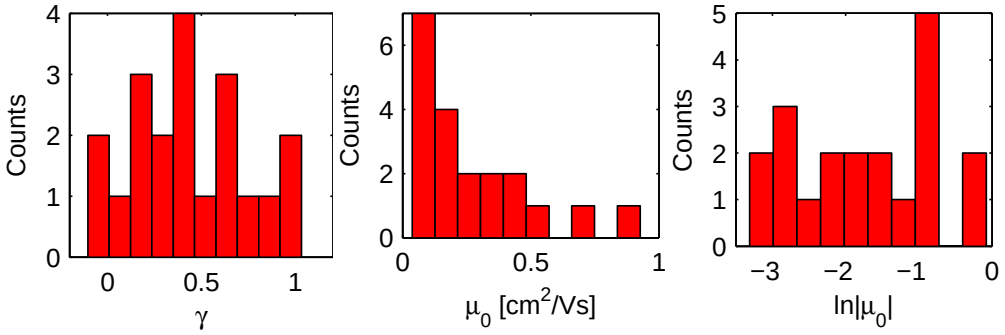
The dataset comprises 103 selected OTFTs coming from two samples having two dielectric gate capacitances $C_1 = 17$ nF/cm^2 and $C_2 = 23$ nF/cm^2 (150 nm dielectric). The geometric

details of these OTFTs are summarized in Table 4.1.

Table 4.1: Overview of the transistors dataset. Format: 'Sample C_1 ; Sample C_2'. 103 OTFTs in total: 68 OTFTs having $C_i = C_1$ and 41 OTFTs with $C_i = C_2$.

		Channel Length [µm]					
	OTFTs	0.5	1	2	5	10	**Total**
Channel Witdh [µm]	25	3;0					**3**
	50	3;0	5;1				**9**
	100		5;0	7;3			**15**
	200			7;3	6;8		**24**
	250	1;0			4;6		**11**
	500		4;0		4;5	3;3	**19**
	1000			6;0		3;5	**14**
	2500				1;1		**2**
	5000					0;6	**6**
	Total	**7**	**15**	**26**	**35**	**20**	**103**

The channel lengths of the BG6 dataset are: $L = 0.5, 1, 2, 5\&10\,\mu$m and the corresponding numbers of available OTFTs are: $n_{0.5} = 7$, $n_1 = 15$, $n_2 = 26$, $n_5 = 35$ and $n_{10} = 20$. This gives the number of sets of 5 OTFTs (one per channel length) which can be selected: $n_{0.5} \times n_1 \times n_2 \times n_5 \times n_{10} = 1.911$ million. The values of γ and μ_0 used in the Level-2 model are selected on the longest OTFT thus for these two parameters, there are only $n_{10} = 20$ possibilities which are depicted in Figure 4.8. For the other parameters, 100'000 random sets of 5 OTFTs were selected and the Level-2 PEM was applied for each set. The obtained distributions are available in the Appendix. The whole process took 1 hour 25 minutes[1] but it only represents 5% of the total amount of possible sets of transistors.



(a) $\overline{\gamma} = 0.44$, $\sigma_{rel} = 70.4\%$. (b) $\overline{\mu_0} = 0.27$ cm^2/Vs, $\sigma_{rel} = 90.6\%$. (c) $\overline{\ln \mu_0} = -1.72$, $\sigma_{rel} = 56.5\%$

Figure 4.8: Distributions of γ and μ_0 of the 20 longest ($L = 10$ μm) BG6 OTFTs (Level-1 PEM). (a) and (b) in linear scale and (c) in log scale.

Beside the calculation time, this process has another limitation: an additional filtering of the

[1] System: Matlab R2013a 64-bits, Windows 7 Entreprise, Intel i7 870 CPU, 2.93 GHz, 8 GB RAM

results has to be performed. Indeed its random nature mean that the selected OTFTs cannot always follow the expected behavior of the Level-2 sub-models which leads to meaningless values such as negative lengths or mega-volt voltages. Once filtered the distributions were fitted to a normal or log-normal distribution accordingly. The details are gathered in Table 4.2 and the results shown in Figure 4.9.

Table 4.2: Filtering range to refine the 100'000 runs and corresponding fitting distribution and their parameters. μ and σ are, for the normal distribution, the mean and the standard deviation whereas for the log-normal distribution they are the location parameter and the scale parameter, respectively.

Parameter	Range	Distribution	μ	σ	$\mu_\cap$	$\sigma_\cap$
γ	–	Normal	0.495	0.266	0.485	0.268
μ_0	–	Log-normal	-1.72	0.946	-1.79	0.916
$V_{\mathrm{FB,Long}}$	[-10;10]	Normal	0.079	0.762	0.094	0.559
V_{RO}	[-30;0]	Log-normal	0.566	1.26	0.568	1.02
L_{RO}	[0;1E-5]	Log-normal	-14.6	1.50	-14.3	1.49
θ	[0;1E-5]	Log-normal	-15.8	0.480	-15.7	0.427
ΔL	[0;1E-5]	Log-normal	-15.1	1.24	-15.3	1.28
ρ_{Bulk}	[0;6E4]	Log-normal	9.21	0.795	9.22	0.817
r_{C0}	[0;150]	Normal	48.8	24.3	52.7	21.1
V_{C0}	[0;100]	Log-normal	2.38	0.516	2.41	0.515

The filtering process used to get the distributions in Figure 4.9 removed different amount of transistor sets. The remaining ones are comprised between 68'380 (4.9e) and 100'000 (4.9g) out of 100'000.

The intersection of the 10 filtered sets – thus the 5-OTFT sets which fulfill all parameter range constraints, cf. Table 4.2 – gathers only 28'185 5-OTFT sets out of the 100'000 randomly selected. This additional filtering step refines the parameter distributions and thus slightly modify their corresponding μ and σ. The refined values are given in Table 4.2 as $\mu_\cap$ and $\sigma_\cap$. Thanks to this intersection set, the correlation between parameters can be studied. Figure 4.10 shows that μ_0 and γ are correlated, that $V_{\mathrm{RO}} - V_{FB,L} - L_{\mathrm{RO}}$ seem not to be correlated and that $\Delta L - \theta$ as well as $V_{C0} - r_{C0}$ may be correlated. This can be explained by the extraction process. For instance, for ΔL and θ, a random set of five OTFTs is selected and the obtained $1/\lambda(L)$-curve is linearly fitted in order to extract its slope and y-intercept which, at the end, give ΔL and θ at the same time. Thus correlations seem with this technique not easy.

4.3.2 Monte-Carlo simulations

By using the model parameter distributions of Table 4.2 (with μ and σ) and assuming that the parameters are uncorrelated, 200 Monte-Carlo runs of a single sub-micrometer OTFT were performed. The runs are visible in Figures 4.11a whereas comparison with the experimental data of 8 sub-micrometer OTFTs are shown in Figures 4.11b and 4.11c.

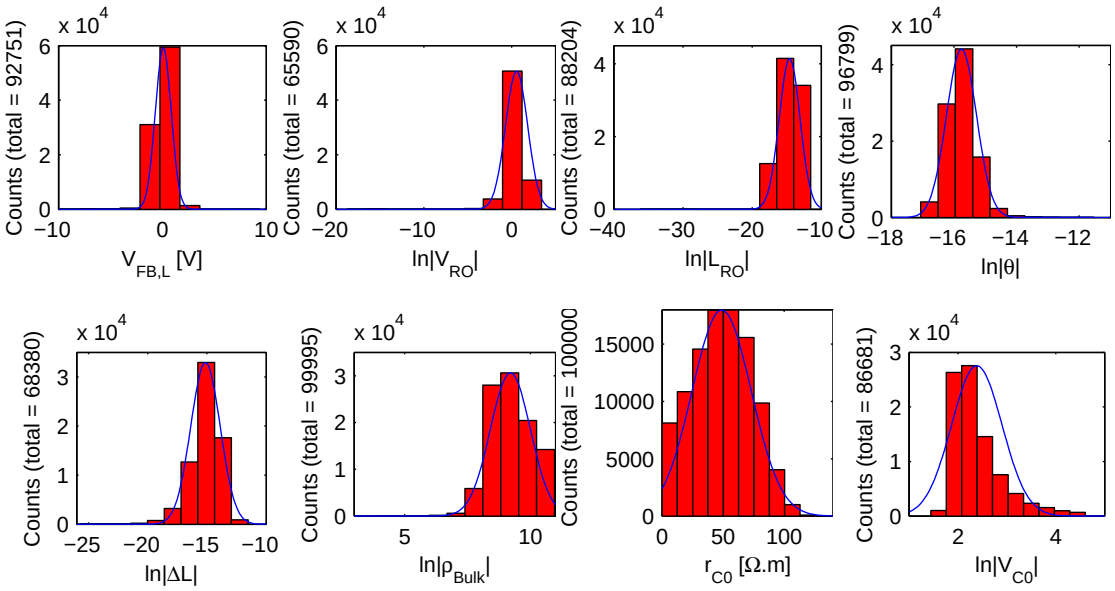


Figure 4.9: Filtered distributions of the Level-2 model parameters in linear or logarithmic scale obtained on BG6 OTFTs.

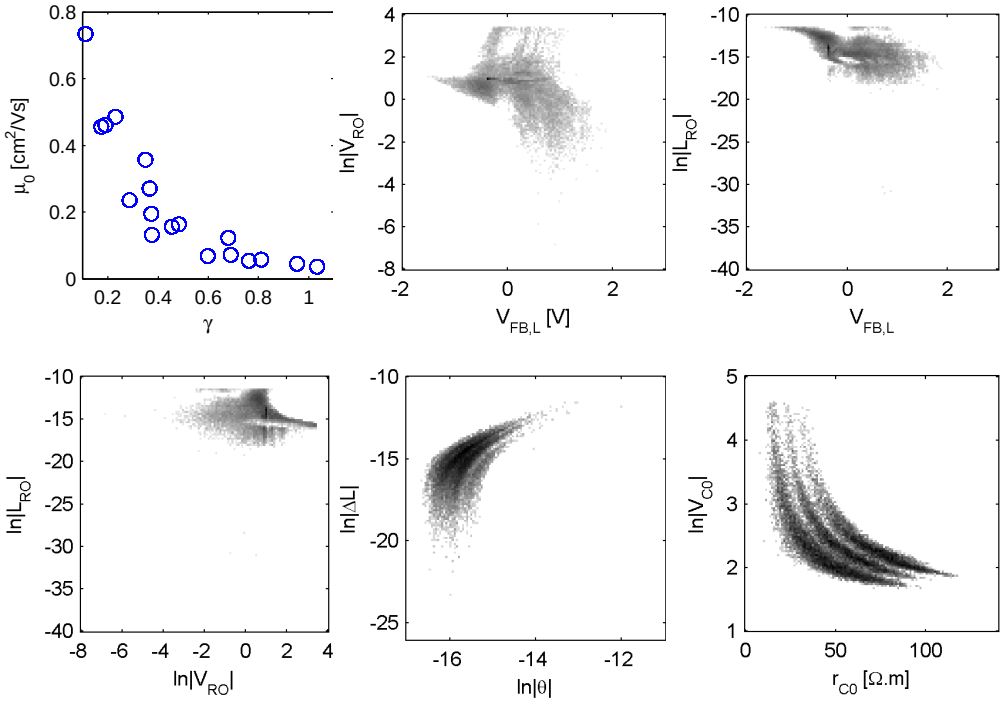
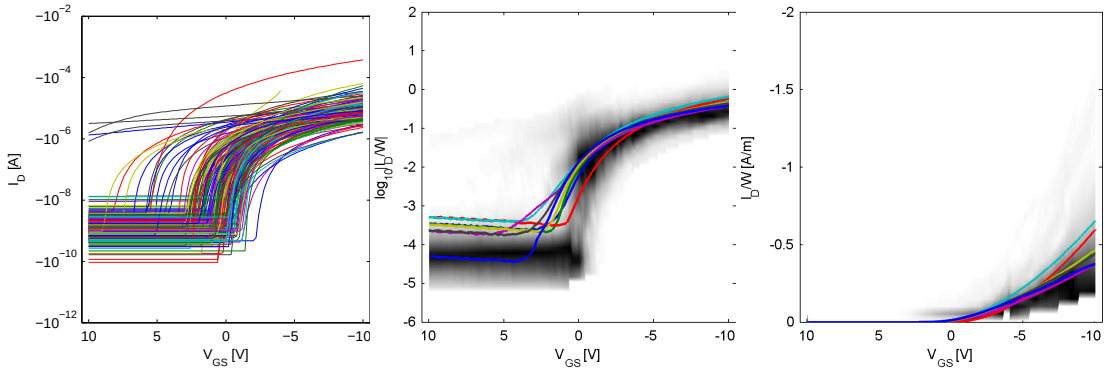


Figure 4.10: Correlations among the intersected filtered distributions of the Level-2 model parameters in linear or logarithmic scale. The grey scale evaluates the density of occurrence in a logarithmic manner, black meaning high density. Total: 28'185 sets of 5 BG6 transistors.



(a) (b) (c)

Figure 4.11: Results of the 200 Monte-Carlo runs with raw curves plotted in semi-logarithmic scale (a) and their density (b–c). Correlations with the experimental data of 8 sub-micrometer OTFTs from BG6 in semi-logarithmic (b) and linear (c) scales.

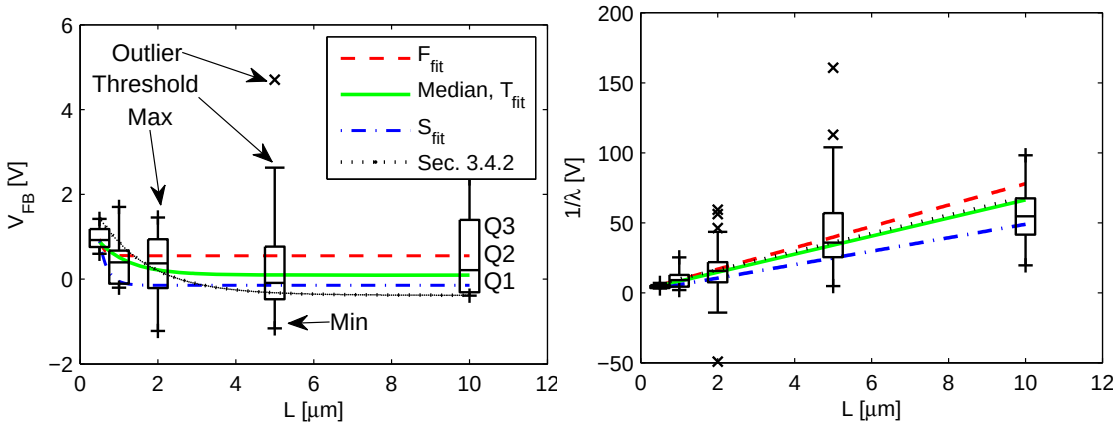
The experimental curves are located in the densest zones with the exception of the OFF regime where only one experimental OTFT out of seven lies in the densest zone. Whereas the results look promising one can note that the variations between runs are much larger than the largest one between experimental OTFTs. Thus this approach in addition to be time consuming may be too pessimistic. Both issues are solved in the next section.

4.4 Corner modeling: sub-micrometer OTFTs case study

In the semiconductor industry, process corners refer to the variations of process parameters (e.g. variations from nominal doping concentration) within which the circuit still must work. Three corners exist in the semiconductor naming convention: typical (T), slow (S) and fast (F). For a single transistor these corners can refer to the mobility or the threshold voltage and can be seen as three transistor profiles. In this thesis, this convention will be kept to define three OTFT corners which are exhibited below.

In the following, we will exploit the distributions of the first level model parameters obtained on the 103 OTFTs of BG6. For instance, by using the median value for μ_0 and γ obtained for $L = 10$ μm, the median values for SS and ρ_{Bulk} as extracted for $L = 0.5$ μm, and then combining these data with the median values obtained for V_{FB}, λ and the contact resistances when varying$L$, a "median set" of model parameters that defines the so called Typical (T) corner can be proposed. Then the parameters of the subthreshold regime – V_{ON}, V_B and B – are obtained as explained in Section 3.4.3.

To illustrate this process, the distribution of V_{FB} obtained for each channel length is represented versus L with box plots in Figure 4.12. The bottom side of the box holds for the first quartile ($Q1$), the inner-bar holds for the median ($Q2$), and the top edge is for the third quartile ($Q3$). The interquartile range $IQR = Q3 - Q1$ is used to detect outliers ($\times$) which are below $Q1 - 3/2IQR$ or above $Q3 + 3/2IQR$. The whiskers represent either these outlier thresholds ($-$) or the minimum/maximum value ($+$) if comprised within the outlier thresholds. The fit (Level-2 PEM) of the median data points of V_{FB} obtained with the Level-1 PEM versus L shows good agreement as shown in Figure 4.12 (Median, T_{fit}).



(a) (b)

Figure 4.12: V_{FB} versus L of 103 OTFTs with the corresponding fit used in Section 3.4.2 and in this section (F_{fit}, T_{fit} and S_{fit}). The value of V_{FB} obtained in Section 3.4.2is a maximum which explains why it was optimized in Section 3.4.3.

When all combined together the obtained T-corner matches quite well the data set as shown in

Table 4.3: Values of the Level-2 model parameters for the statistical S, T and F corners. $V_{\mathrm{FB,Long}}$ is here noted $V_{FB,L}$.

	μ_0 [cm^2/Vs]	γ	$V_{FB,L}$ [V]	V_{RO} [V]	L_{RO} [μm]	θ [μm/V]	ΔL [μm]	ρ_{Bulk} [kΩ.m]	r_{C0} [Ω.m]	V_{C0} [V]
S	0.126	0.317	-0.146	-11.07	0.211	0.208	0.175	3.4		
T	0.179	0.374	0.096	-1.46	0.803	0.155	0.275	2.8	25.5	12.1
F	0.270	0.483	0.553	-28.16	0.117	0.131	0.206	2.1		

Figure 4.13, where the T curves lie in the densest domains of experimental data. This result is actually valid for the whole range of channel lengths. To define the S and F corners, the whole process is repeated using chosen quantiles around the median. To illustrate this point, we used for V_{FB} and $1/\lambda$ the values of the 37.5 and 62.5 percentiles ("$Q1.5$" and "$Q2.5$") to apply this method and the resulting fits are shown in Figure 4.12 (S_{fit} and F_{fit}).

The values of the model parameters for the statistical S, T and F corners are gathered in Tables 4.3 and 4.4. (Note that the median values were kept for the contact resistances i.e. the S, T and F corners share the same parameters for the contact resistances).

Table 4.4: Values of the Level-3 model parameters for the statistical S, T and F corners.

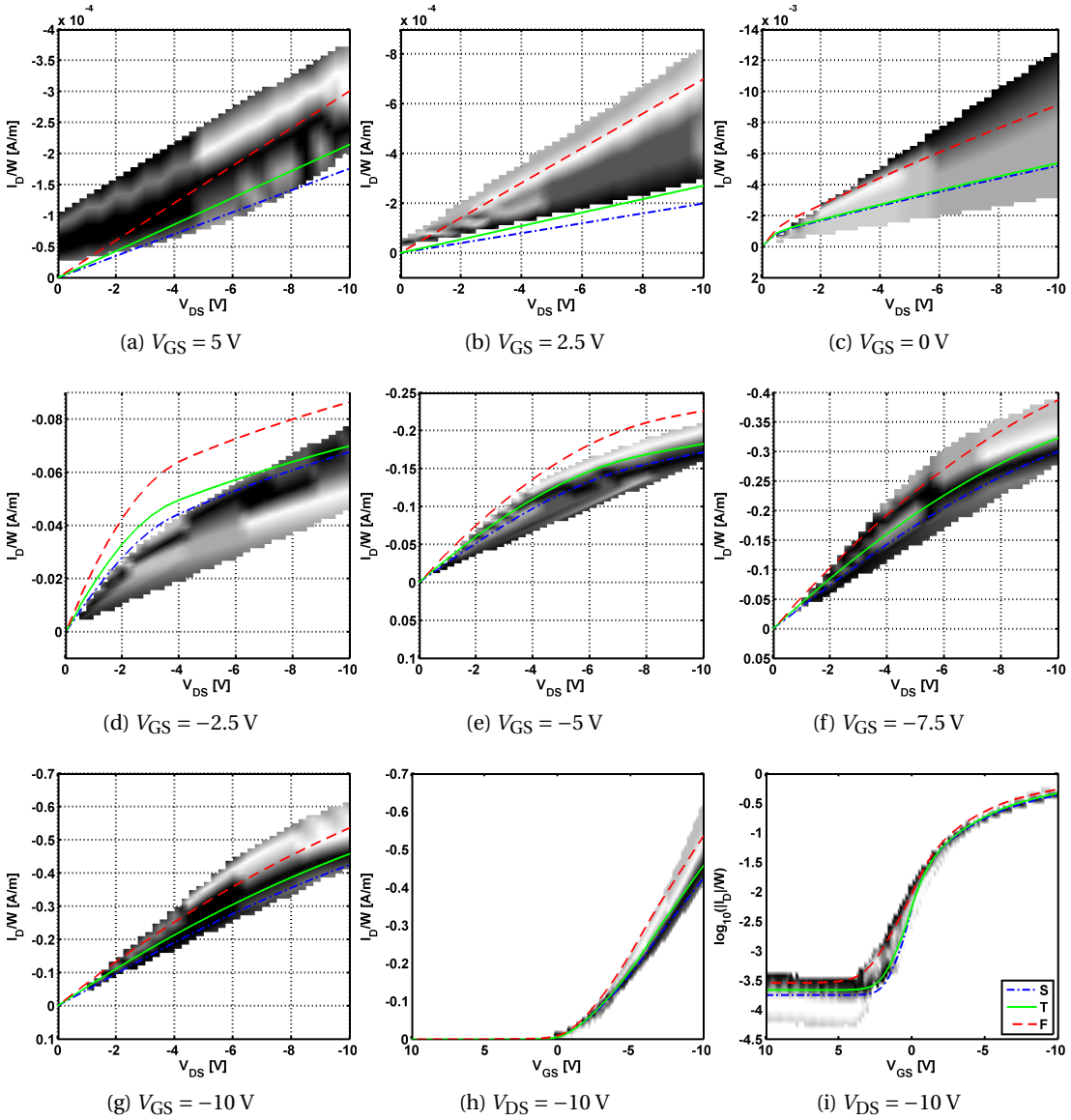
	SS [V/dec]	V_{ON} [V]	V_B [V]	B [1/V]
S	1.03	1.60	0	1.05
T	1.22	1.80	-0.2	1.00
F	1.74	2.80	-0.6	0.80

Figure 4.13 shows that the obtained S and F corners represent well the experimental data spread. These OTFT statistical corners will be used in the next chapter to simulate submicron zero-V_{GS} inverters.

4.5 Summary

In this chapter, a study of the g_m/I diagram was first performed. Whereas an invariant was demonstrated in the above-threshold regime and discussed, the exhibition of the second asymptote (plateau) was not conclusive. Thus the focus was set back on more traditional statistical analysis.

The statistical parameter extraction has screened 5% of the total amount of possible transistor sets in a reasonable time – which will not be the case of the whole screening. In addition, the meaningless results were further filtered out of the distributions of these 5%. Using the obtained parameter distributions, Monte-Carlo simulations of a sub-micrometer OTFT were able to reproduce the experimental OTFT data. However the simulated spread is larger than



(a) $V_{GS} = 5$ V (b) $V_{GS} = 2.5$ V (c) $V_{GS} = 0$ V

(d) $V_{GS} = -2.5$ V (e) $V_{GS} = -5$ V (f) $V_{GS} = -7.5$ V

(g) $V_{GS} = -10$ V (h) $V_{DS} = -10$ V (i) $V_{DS} = -10$ V

Figure 4.13: Output ((a)–(g)) and transfer ((h)&(i)) characteristics of the obtained statistical corners plotted together with the density of experimental data (8 submicron OTFTs). Red dashed line: F corner. Green line: T corner. Blue dash-dotted line: S corner.

the experimental one i.e. too pessimistic. In addition the Monte-Carlo simulations were run ignoring the correlations observed between some model parameters. Thus even if this approach works, it is time consuming and not robust.

Finally the corner modeling approach was able to define relevant statistical corners which can be implemented in a circuit simulator in an easier way than the Monte-Carlo parameters while having faster simulation time. This time the experimental OTFT data was successively reproduced.

5 Technology assessment through inverter simulations

In this chapter, the drain current static model introduced in the previous chapters and applied to the sub-micrometer OTFTs from BG6 is used to estimate the yield of a pair of zero-V_{GS} inverters. In the first section, we will adapt to our model a previously reported method by De Vusser et al. [154]. Secondly another approach based on statistical corner modeling will be introduced.

The content of this chapter has been accepted for publication in [140] and the corresponding article is currently in press.

5.1 State of the art: V_T-based method for yield estimation

The method reported in [154] allows estimating the yield of a chain of inverters by analyzing the worst case noise margin of two successive inverters in terms of threshold voltage deviations. De Vusser et al. assumed unipolar p-logic with zero-V_{GS} inverters whereas Bode et al. [155] extended the method for CMOS logic, and thus included complementary inverters as well. However the whole analysis in [154] is based on the classical MOSFET model. In this section, we will show a way to apply the same methodology with the current OTFT model.

5.1.1 Principle of the method

The worst case scenario identified in [154] happens when an inverter with a negative threshold voltage deviation for both the driver and load transistor is followed by an inverter with a positive threshold voltage deviation. In other words, for the first inverter: $V_{T1} = \text{mean}(V_T) - \Delta V_T$ for both driver/load OTFTs whereas for the second inverter: $V_{T2} = \text{mean}(V_T) + \Delta V_T$ for both driver/load OTFTs.

To follow the same approach and allow comparing our devices, the V_T mismatch (ΔV_T) proposed in [154] was applied to $V_{FB,Long}$ (see Eq. 3.17) but also, in a first approximation, to V_{ON} and V_B in order to keep I_{sub} matched with I_{above} and not to affect the subthreshold slope SS.

Table 5.1: Values of the model parameters. The nominal ("N") values correspond to the ones derived in Section 3.4.2(except $V_{FB,Long}$).The rows S, T and F are explained in Section 4.4.

	μ_0 [cm^2/Vs]	γ	$V_{FB,L}$ [V]	V_{RO} [V]	L_{RO} [μm]	θ [μm/V]	ΔL [μm]	ρ_{Bulk} [kΩ.m]	r_{C0} [Ω.m]	V_{C0} [V]
N	0.460	0.191	-1.13	-2.68	1.31	0.153	0.50	2.4	41.4	7.81
S	0.126	0.317	-0.146	-11.07	0.211	0.208	0.175	3.4		
T	0.179	0.374	0.096	-1.46	0.803	0.155	0.275	2.8	25.5	12.1
F	0.270	0.483	0.553	-28.16	0.117	0.131	0.206	2.1		

This additional approximation gives negligible deviation of about 0.8% on SS for corners with $\Delta V_T = \pm 0.5$ V.

In the next discussion, the OTFT corners are named according to the convention used in the semiconductor industry: typical (T), slow (S) and fast (F). For example, with $\Delta V_T = \pm 0.5$ V, we have $\Delta V_T(T) = 0$ V, $\Delta V_T(S) = -0.5$ V and $\Delta V_T(F) = +0.5$ V (for p-type transistor).

5.1.2 Method application

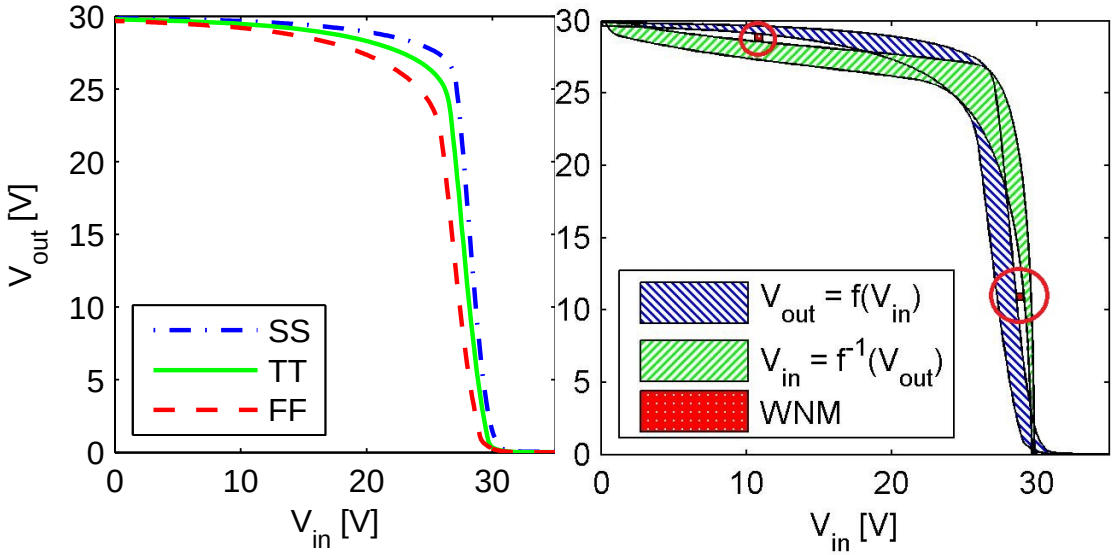
P-type zero-V_{GS} inverters with $L = 0.5$ μm, $W_{driver}/L = 50$ and $W_{load}/W_{driver} = 10$ were simulated in Cadence® Virtuoso® Spectre® at various supply voltages (V_{DD}) using the transistor model detailed in the previous section, together with the nominal model parameters listed in Tables 5.1 and 5.2. The worst case noise margin (WNM) of simulated inverters was extracted in the same way as in [154] with the algorithm from [78].

Table 5.2: Values of the model parameters for the subthreshold regime.

	SS [V/dec]	V_{ON} [V]	V_B [V]	B [1/V]
Fig. 3.19	1.22	1.80	-0.2	0.85
S	1.03	1.60	0	1.05
T	1.22	1.80	-0.2	1.00
F	1.74	2.80	-0.6	0.80

Figure 5.1 shows the simulation for SS, TT and FF inverters (the first letter denoting the driver transistor) at $V_{DD} = 30$ V (for clarity) with ΔV_T equal to the measured standard deviation $\sigma V_{T,sat} = 0.34$ V as in [154] i.e. $\Delta V_{FB,Long} = \Delta V_{ON} = \Delta V_B = 0.34$ V. The case SS-FF gives $WNM = 0.49$ V whereas the typical TT-TT case ($\Delta V_T = 0$ V) gives $WNM = 1.32$ V. Repeating the procedure with a slightly higher ΔV_T of 0.5 V gives $WNM = 0.24$ V. Plotting WNM versus ΔV_T gives a straigth line as reported in [154]. In our case where $V_{DD} = 30$ V, this reads:

$$WNM = 1.30 - 2.20|\Delta V_T| \tag{5.1}$$



(a) (b)

Figure 5.1: Left: Transfer curve of the TT inverter with $L = 0.5$ μm surrounded by the 2 corners FF and SS inverters. Right: Family of transfer curves according to theses corners and related WNM as in [6] at $V_{DD} = 30$ V with $\Delta V_T = 0.34$ V.

From the dependence of WNM on ΔV_T given in Equation 5.1 (essentially linear), a Gaussian distribution of V_T gives a Gaussian distribution of WNM whose mean is $\mu_{WNM} = 1.30$ V and standard deviation is $\sigma_{WNM} = \sqrt{2} \times 2.20\sigma_{VT}$ [154]. Because of the absolute value of ΔV_T in Equation 5.1, the right half of the Gaussian probability density function (PDF) is mirrored on the left half which doubles the PDF. Then the defect probability (P_D) of a pair of inverters resulting in $WNM < 0$ V, see [154], is obtained by calculating the normal cumulative distribution function of WNM for $WNM \leq 0$ V:

$$P_D = 2\int_{-\infty}^{0} \frac{1}{\sqrt{2\pi}\sigma_{WNM}} \exp\left(-\frac{(x-\mu_{WNM})^2}{2\sigma_{WNM}^2}\right) dx \tag{5.2}$$

The whole process is illustrated in Figure 5.2. With $\mu_{WNM} = 1.30$ V and $\sigma V_{T,sat} = 0.34$ V one gets $P_D = 22\%$ (at $V_{DD} = 30$ V). Thus k pairs of inverters have a probability $(1-P_D)^k$ [155] to work properly. Finally the 'circuit' yield of a chain of N inverters is given by $Yield = (1-P_D)^{N/2}$ (2 inverters per inverter pair). Results are shown for different supply voltages in Figure 5.3.

5.1.3 Results and method discussion

According to Figure 5.3, it seems almost impossible to get any working submicron digital circuit when biased at $V_{DD} = 10$ V. Even if the yield increases with the supply voltage, there is a

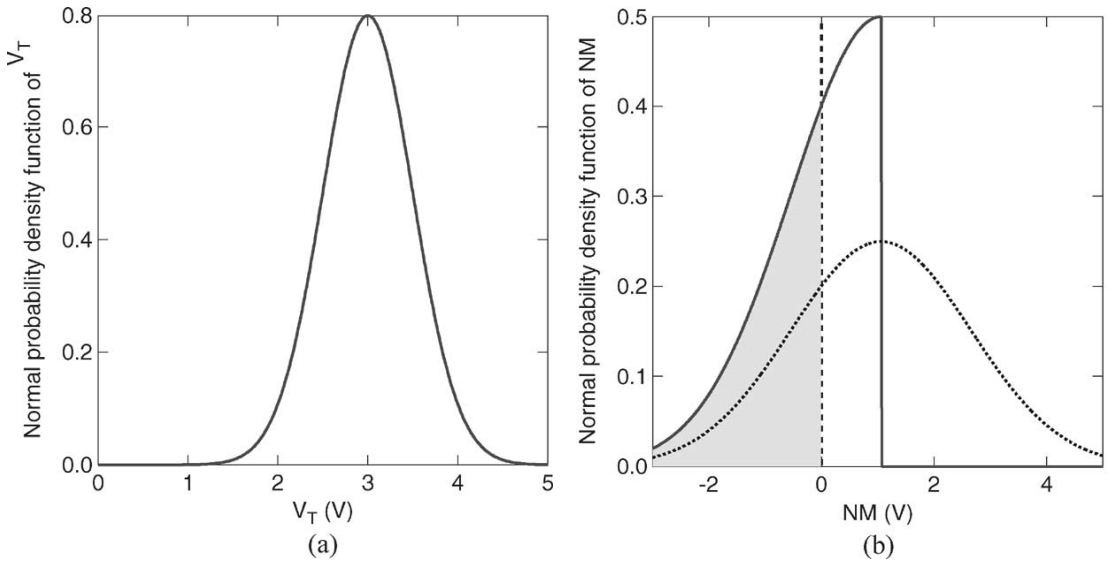


Figure 5.2: Example. (a) Gaussian probability density function of V_T with mean $\mu_{VT} = 3$ V and $\sigma_{VT} = 0.5$ V. (b) Dotted line represents the probability density function of WNM when Equation 5.1 would simply read $WNM = 1.06 - 2.26\Delta V_T$ (Gaussian with $\mu_{WNM} = 1.06$ V and $\sigma_{WNM} = \sqrt{2} \times 2.26\sigma_{VT}$). The solid line is the actual Gaussian probability density function of WNM, using $|\Delta V_T|$ rather than ΔV_T in 5.1). The gray area illustrates the defect probability ($WNM < 0$ V), as calculated in 5.2. Adopted from [154].

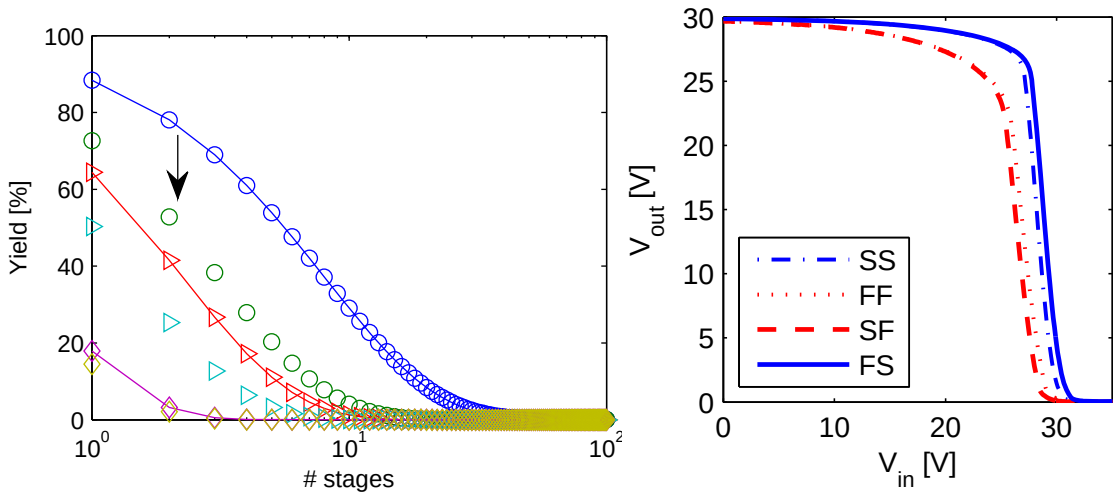
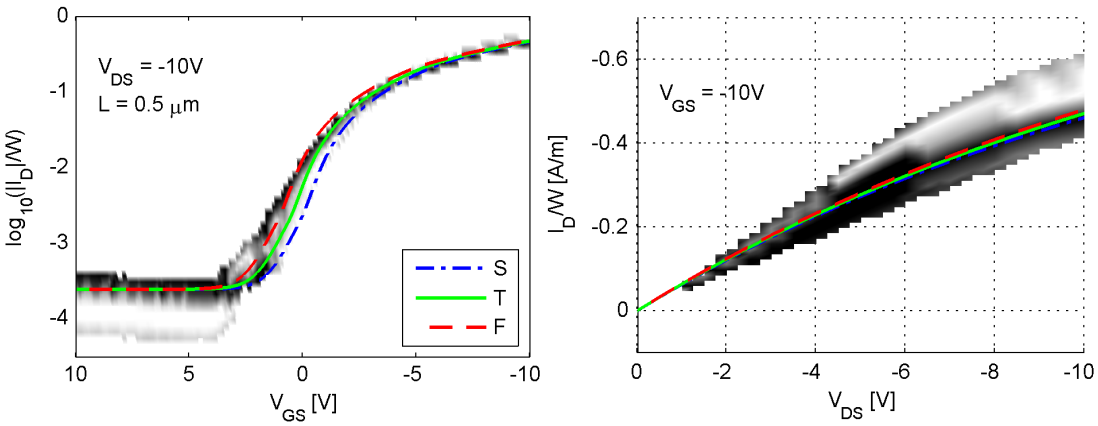


Figure 5.3: Circuit yield as a function of the number of submicron zero-V_{GS} inverters, calculated using $\sigma V_T = \sigma V_{T,sat} = 0.34$ V, for $V_{DD} = 30$ V (○), 20 V (▷) and 10 V (◇), and by considering SS-FF (symbols with line) or FS-SF (symbols only) as worst case scenario (inverters shown right).

physical limit in terms of current density and electric fields that the transistor can withstand. Still simulations show that, at V_{DD} = 30 V, the yield of a 10-stage circuit is below 29%.

Moreover two remarks can be made about these results:

1. SS-FF is actually not the worst case but FS-SF is, as shown in Figure 5.3. At V_{DD} = 30 V, the new relation is: $WNM = 1.34 - 3.87|\Delta V_T|$ and the yield decreases further, see Figure 5.3.
2. Even for a ΔV_T as high as ±0.50 V, the defined S and F corners are not able to account for the experimental spread neither of the ON-state currents nor of the spread measured in the subthreshold regime c.f. Figure 5.4.



(a) (b)

Figure 5.4: Normalized drain current vs V_{GS} (left) and V_{DS} (right). The corners S, T and F based on ΔV_T = ±0.50 V do not match well the current spread shown by the density of experimental points (8 submicron OTFTs).

Therefore, it seems that herein the actual definition of the corners is not appropriate to simulate the spread of OTFTs characteristics. Thus in Section 5.2 we will use the statistical corners defined in the previous chapter which give a better representation of the overall data spread.

Other remarks

The statistical PEM described in the previous chapter (Section 4.3) attributes a distribution to each model parameters. These distributions could be used for each OTFT of the inverter-pair to simulate a random set of inverter pairs and extract their noise margin. This will generate a distribution of the noise margin from which the defect probability can be obtained. However this work was not realized for this thesis. Indeed Monte-Carlo simulations of inverters – using an OTFT model whose parameters were varied – have already been reported [142, 10] as visible in Figure 5.5. Secondly the curve spread obtained for transistors in Section 4.3 was larger than the experimental data spread which would lead to a pessimistic evaluation.

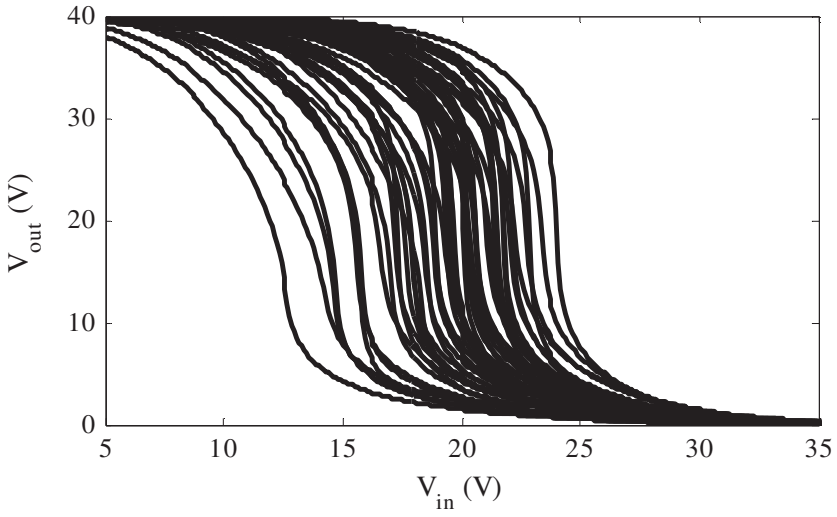


Figure 5.5: 50 Monte-Carlo runs of a CMOS inverter. Adopted from [142].

5.2 Proposed statistical method

5.2.1 Submicron zero-V_{GS} inverters

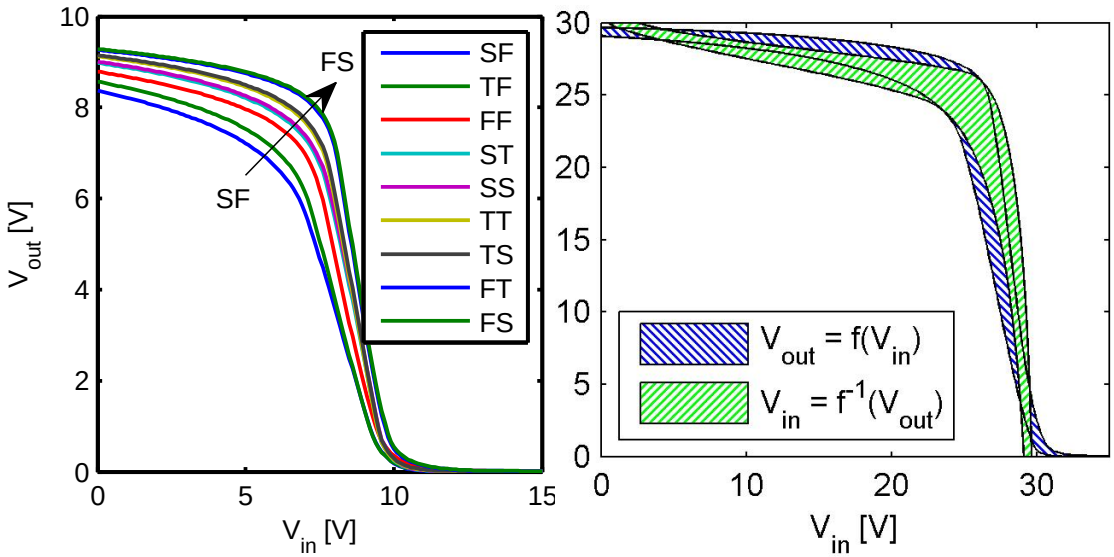
The simulations shown in Figure 5.6 highlight the results obtained for the 9 possible inverters built upon the S, T and F submicron OTFT statistical corners introduced in Section 4.4. As for the V_{T}-based analysis, the limiting corners are still represented by the FS and SF combinations. However there is no noise margin anymore for the worst case FS-SF at V_{DD} = 10 V, nor at V_{DD} = 30 V as visible in Figure 5.6 because the FS and SF inverters differ more from each other.

Next we will describe other methods to access P_D from these results since the one used in Section 5.1.2 is not applicable anymore.

5.2.2 Defect probability and electrical yield

From the 9 simulated corner inverters shown in Figure 5.6, 81 inverter pairs are possible. For each inverter pair, WNM was calculated and classified as "Pass" ($WNM > 0$ V) or "Fail" ($WNM \leq 0$ V). The result is shown in Figure 5.7 at different supply voltages.

From these $Fail$ results, two P_D candidate expressions were derived and follow.



(a) (b)

Figure 5.6: Left: simulated transfer curves of the 9 corner submicron inverters at $V_{DD} = 10$ V. Right: worst case SF-FS at $V_{DD} = 30$ V.

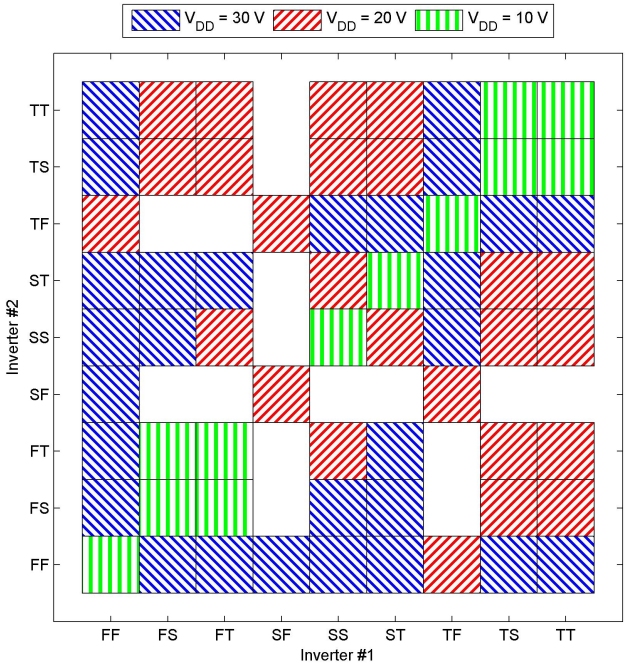


Figure 5.7: Schmoo plot of a chain of 2 inverters at different supply voltages. Hashed areas mean $WNM > 0$ V i.e. "Pass". Note: $Pass(10\ V) \subset Pass(20\ V) \subset Pass(30\ V)$.

P_D: expression #1

By its definition, P_D can be in a first step linked to $Fail$ as:

$$P_D = \frac{1}{81}\sum_{i=1}^{9}\sum_{j=1}^{9} Fail(i,j) = 1 - \frac{1}{81}\sum_{i=1}^{9}\sum_{j=1}^{9} Pass(i,j) \tag{5.3}$$

From Figure 5.7, 12 inverter pairs pass at $V_{DD} = 10$ V thus $P_D = 1 - 12/81 = 85\%$. At $V_{DD} = 20$ V and 30 V, we get $P_D = 53\%$ and 20%, respectively. Those values are close to the V_T-based ones (SS-FF case).

P_D: expression #2

An alternative way to express P_D, is to weight the different $Fail$ cases by the probability that a given failing inverter pair has to occur i.e:

$$P_D = \sum_{i=1}^{9}\sum_{j=1}^{9} P(INV_i, INV_j)\, Fail(i,j) \tag{5.4}$$

where $P(INV_i, INV_j)$ is the probability of occurrence of an inverter pair: $P(INV_i, INV_j) = P_{i,DL} \times P_{j,DL} = (P_{i,D}P_{i,L}) \times (P_{j,D}P_{j,L})$ ("D"-"L": Driver-Load OTFT).

About Equation 5.4:

- If $\forall\{i,j,k,l\} \in \{S,T,F\}^4, Fail([i,j],[k,l]) = 0$ then $P_D = 0$.
- If $\forall\{i,j,k,l\} \in \{S,T,F\}^4, Fail([i,j],[k,l]) = 1$ then, by associating "S" to 1, "T" to 2 and "F" to 3, one gets:

$$P_D = \sum_{i=1}^{3}\sum_{j=1}^{3}\sum_{k=1}^{3}\sum_{l=1}^{3} P_i P_j P_k P_l = \sum_{i=1}^{3} P_i \sum_{j=1}^{3} P_j \sum_{k=1}^{3} P_k \sum_{l=1}^{3} P_l \tag{5.5}$$

  Since by definition, $\sum_{i=1}^{3} P_i = 1$, thus $P_D = 1$ in this case.

In addition a link is also necessary between the OTFT corners used in the inverter pair and the spread of experimental data. Since the transfer curve of the inverter depends on the current characteristics of the driver and load OTFTs, we chose to define the probability to get a p-type OTFT of profile F, T or S from the experimental spread of the normalized ON-current, $\|I_{ON}\| = I_D(V_{GS} = V_{DS} = -10V)/W$, visible in Figure 4.13. The experimental mean ($\mu_{\|I_{ON}\|}$) and standard deviation ($\sigma_{\|I_{ON}\|}$) values were used in a Gaussian distribution to model in a first approximation the experimental spread of $\|I_{ON}\|$. The $\|I_{ON}\|$ values corresponding to the F and S corners – obtained with the corner parameters in Tables 5.1 and 5.2 – define 3 regions in the $\|I_{ON}\|$ distribution which we use to define the probability of occurrence of the respective corner.

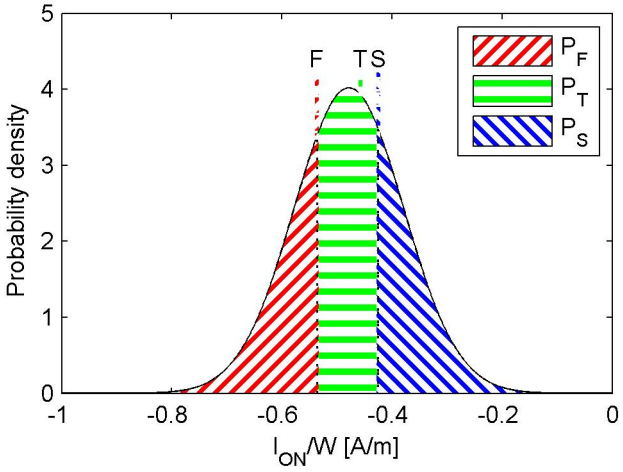


Figure 5.8: At $V_{GS} = V_{DS} = -10$ V, $\|I_{\mathrm{ON}}\|$ of the 3 statistical transistor corners and probability density assuming a Gaussian distribution ($\mu_{\|I_{\mathrm{ON}}\|} = -0.5$ A/m and $\sigma_{\|I_{\mathrm{ON}}\|} = 0.1$ A/m from the experimental data of 8 submicron OTFTs).

This is depicted in Figure 5.8 and we get $P_T = 43\%$, $P_F = 28\%$ and $P_S = 29\%$.

While Figure 5.7 shows $Pass(i, j)$ at different V_{DD}, the experimental data for P_T, P_F and P_S are, in our case, only available at $-V_{DS} \leq 10$ V, thus P_D can only be calculated at $V_{\mathrm{DD}} = 10$ V. We get $P_D = 82\%$ which is slightly lower (thus better) than with the expression #1 but it is still a quite high value which means a high probability of failure.

The subsequent electrical yield is plotted in Figure 5.9 and is compared to the yields obtained in Section 5.1 with the V_{T}-based corners at $V_{\mathrm{DD}} = 10$ V.

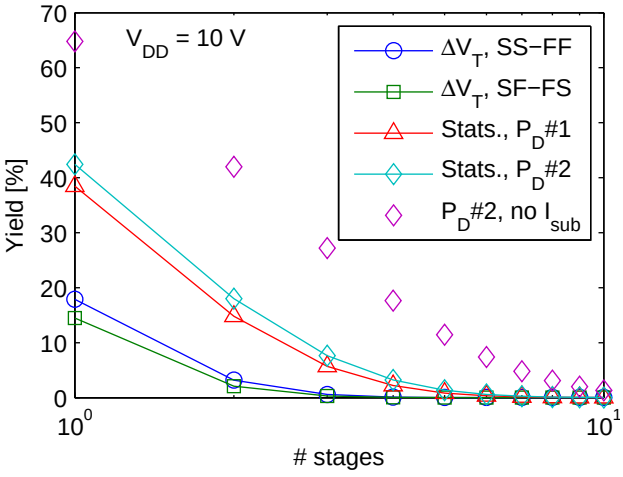


Figure 5.9: Summary of the electrical yields obtained at $V_{\mathrm{DD}} = 10$ V with ΔV_{T} and statistical corners. For the latter case, the electrical yield obtained with the model without I_{sub} ($I_{\mathrm{D}} = I_{\mathrm{above}} + I_{\mathrm{OFF}}$) is also shown.

5.3 Summary

In this chapter, the method developped by De Vusser et al., used to estimate yields of inverters chains based on the classic MOSFET model, was first adapted to the OTFT model developed in Chapter 3 which includes the contact resistance and the subthreshold regime. This gave a first quantitative assessment of the sub-micrometer OTFTs of BG6 and showed that they are not suitable yet for complex digital circuits.

Another advantage of this method is that it can be used to predict the evolution of the circuit yield with time. Indeed the stress lifetime tests studied in Section 2.6.4 have shown that the threshold voltage shifts with the stress time. In addition the empirical model of Equation 2.7 gives ΔV_T(time) which can finally be used as an input to this method to extract the circuit yield.

Secondly, a methodology based on the statistical corners developed in Chapter 4 was proposed. This approach gives higher yield than the V_T-based method but the yield values actually depend on the way the statistical corners are defined (here we chose $\|I_{ON}\|$) and on the definition of the associated probability (#1 or #2 cf. Figure 5.8).

Figure 5.9 also shows the yield dependence versus the transistor model itself, and more particularly how the yield can get overestimated when the subthreshold regime is ignored ($I_D = I_{above} + I_{OFF}$) when simulating submicron zero-V_{GS} inverters. Even with this overestimated value, the yield is below 10% with 6 stages of inverters. Considering or not the subthreshold regime has in our case an impact on the drain current at $V_{GS} = 0$ V which thus modify the current of the load transistor – biased in this way in the zero-V_{GS} topology.

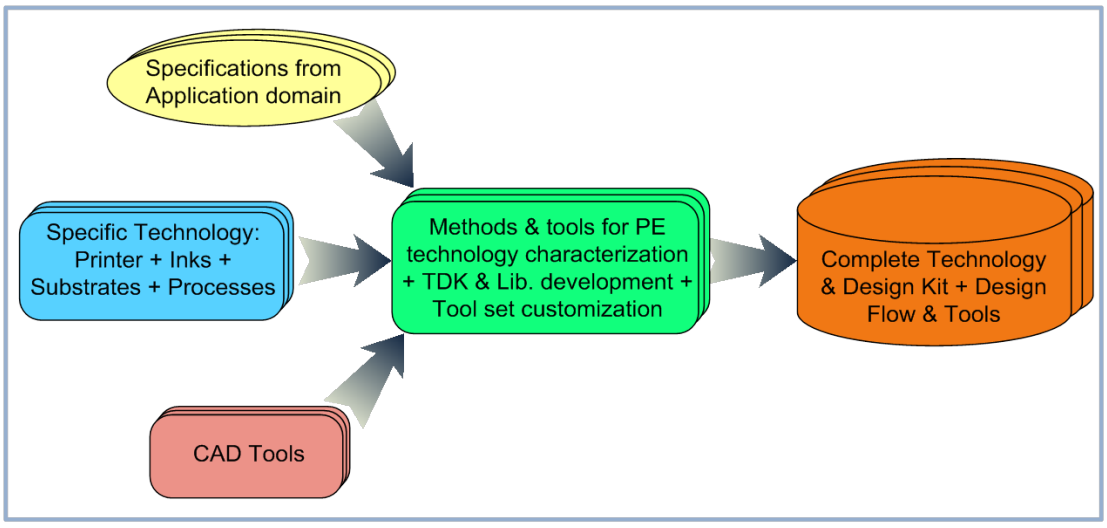


Figure 5.10: Next step: Technology & Design Kit (TDK). Adopted from TDK4PE's website.

The next step in the circuit implementation of a given organic/printed technology will be achieved by adopting a methodology similar to the silicon microelectronics one: using a

Technology and Design Kit (TDK) to abstract physics to a point where engineers could address physical design with sufficient certainty and great freedom for creativity. A TDK combines a set of design rules for a given technology and a library of standard design cells (layout and models implemented in standard EDA tools e.g. Cadence). The EU FP7 TDK4PE[1] project gathers 10 partners focusing on this topic.

This process was initiated for the technology TG4 in the last phase of this thesis in the framework of the EU FP7 COLAE[2] project.

[1] Technology & Design Kit for Printed Electronics, 2011-2014, grant agreement n°287682, http://www.tdk4pe.eu

[2] Commercialisation of Organic and Large Area Electronics, 2011-2014, grant agreement n°288881, http://www.colae.eu

6 Conclusion and outlook

The objectives of this thesis were to identify or give the methods to assess the different technologies used for organic circuits which are currently under development at CSEM, as well as to quantify their potential upon some targeted application as, for instance, digital circuits.

To this purpose ten OTFT platforms have been screened and their performance in terms of figures of merit have been discussed and compared in details. High throughput characterization and/or data analysis platforms have also been developed such as $I-V$, $C-V$, temperature-dependent, rise-time and stress lifetime.

Among these screened OTFT platforms, the self-aligned nano-imprinted technology demonstrated state-of-the-art characteristics for sub-micrometer OTFTs on 4-inch flexible substrates. This made this platform the most suitable candidate for developing the framework to answer to the second question: the potential evaluation. For that purpose, a set of more than 100 OTFTs with different channel lengths have been used to first develop a static model embedding almost all known electrical aspects of OTFTs and suitable for the sub-micrometer OTFTs. The parameter extraction method (PEM) has been automatized in a custom-made environment.

The device-to-device discrepancy often observed in OTFTs – and which is much larger than in typical MOSFETs – has been studied first introducing the g_m/I invariance and some novel statistical modeling methods. The latter allowed simulating sub-micrometer inverters on commercially available tools based on the developed model and parameter spread. Simulation results as input data in a proposed statistical method in order to evaluate the potential of the sub-micrometer OTFTs. The results have also been compared with another published methods, showing the improvement of our approach, especially regarding the impact of the subthreshold operation on the circuit yield. Whereas both approaches conclude that these sub-micrometer OTFTs are not mature enough to make complex digital circuits, the developed methodology is technology-independent and can spare the resources required for the circuit design, fabrication and characterization. Thus it may serve as a basis to characterize unipolar-logic printed electronics and can be further extended to complementary-logic circuits.

Most of the targeted value chain for this thesis was thus completed.

To sum up, the outcomes of this thesis are a high throughput characterization setups and related data analysis tools, the development of a static model valid for a broad range of transistor channel lengths including the sub-micrometer ones, an automated Parameter Extraction platform combined with a statistical methodology to evaluate the potential of a given technology for digital circuits.

Finally the first next envisioned step is to perform the whole set of (automated) characterizations and analysis on a given technology – which was not possible in this thesis due to the encountered issues with respect to the sample availability. The integration of the analysis reported in this thesis into the parameter extraction platform could then be followed up to further increase its throughput. From the dynamic point of view, there is still a need to validate the transit frequency measurement setup and compare the measured data with the values estimated in this thesis.

A Supplementary information

A.1 About technologies and designs

A.1.1 Additional test structures designs

This section gathers the test structure layouts which I have not designed.

- Figure A.1 is used for BG1. It comprises 16 OTFTs with common gate.
- Figure A.2 is used for BG3 and partially BG4. It comprises 24 OTFTs with patterned gate (usually ITO).
- Figure A.3 is used for TG1 and TG2. It comprises 16 OTFTs with patterned gate which is evaporated through a shadow mask.

A.1.2 Thinned X-PVP dielectric for BG4 and BG5

Two capacitor topologies are available on T1 and T3 layouts: the so-called D and E. In the E-case, the bottom electrode plate is larger than the top one and vice-versa for the D-case. More information is available in Figure A.4.

101 capacitors of both topologies coming from 10 samples of both BG4 and BG5 exhibit an average capacitance of 30.0 nF/cm^2 with a relative standard deviation, $\sigma_{\text{rel}} = \sigma_{\text{Ci}}/C_i$, of 16.9%. By only using the E-topology (54 capacitors), one gets 28.8 nF/cm^2 and 16.2%, respectively. The larger (uncontrolled) overlap of the D-type depicted in Figure A.4 explains the higher mean value as well as the slightly higher relative standard deviation.

Figure A.5 shows the mean and relative standard deviations for each of the 5 BG4 samples and 5 BG5 samples when considering both capacitor types or the E-type only. In addition Figure A.6 gives the distributions, mean, μ, and relative standard deviation, σ_{rel}, of BG4, BG5 and BG4+BG5 when again considering both capacitor types or the E-type only.

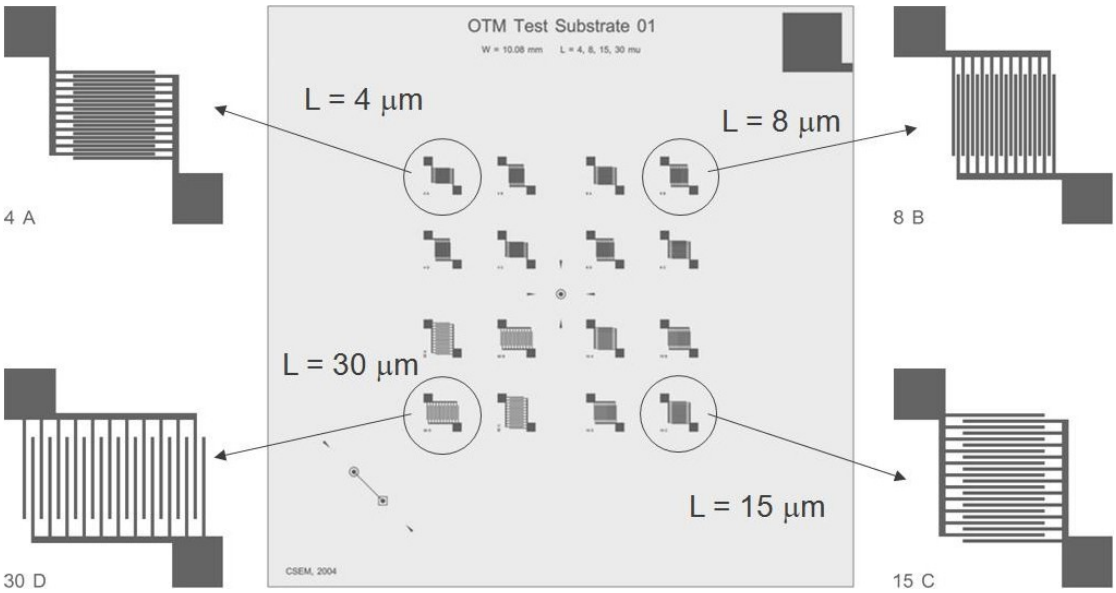


Figure A.1: 20 mm silicon screening platform.

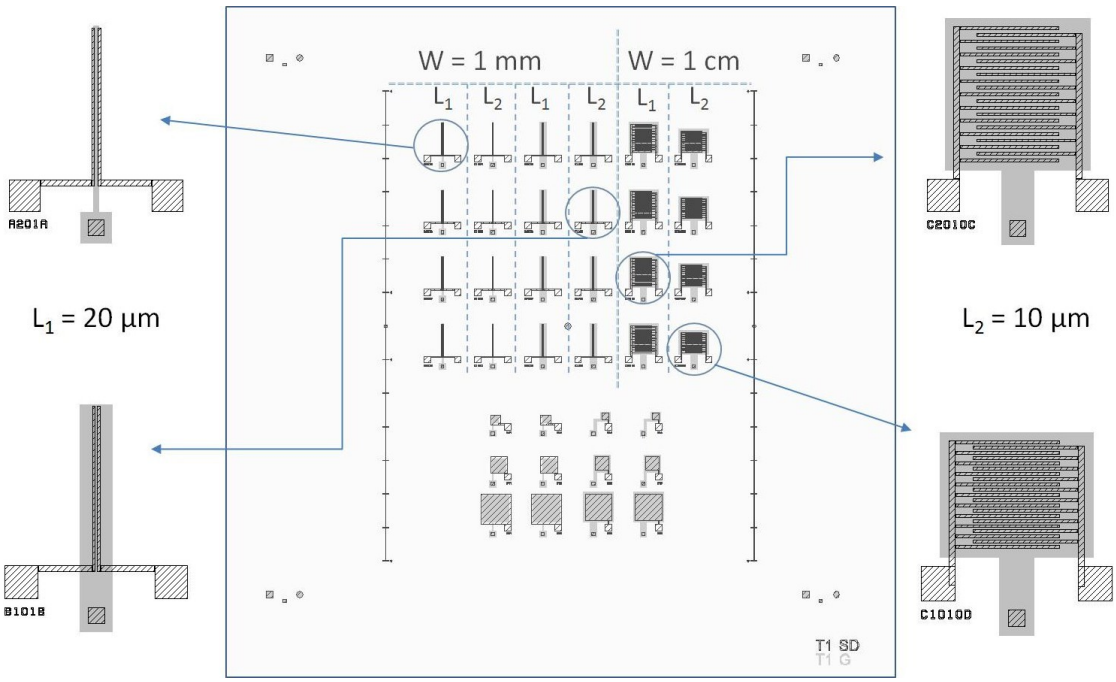


Figure A.2: BG3: test structure layout.

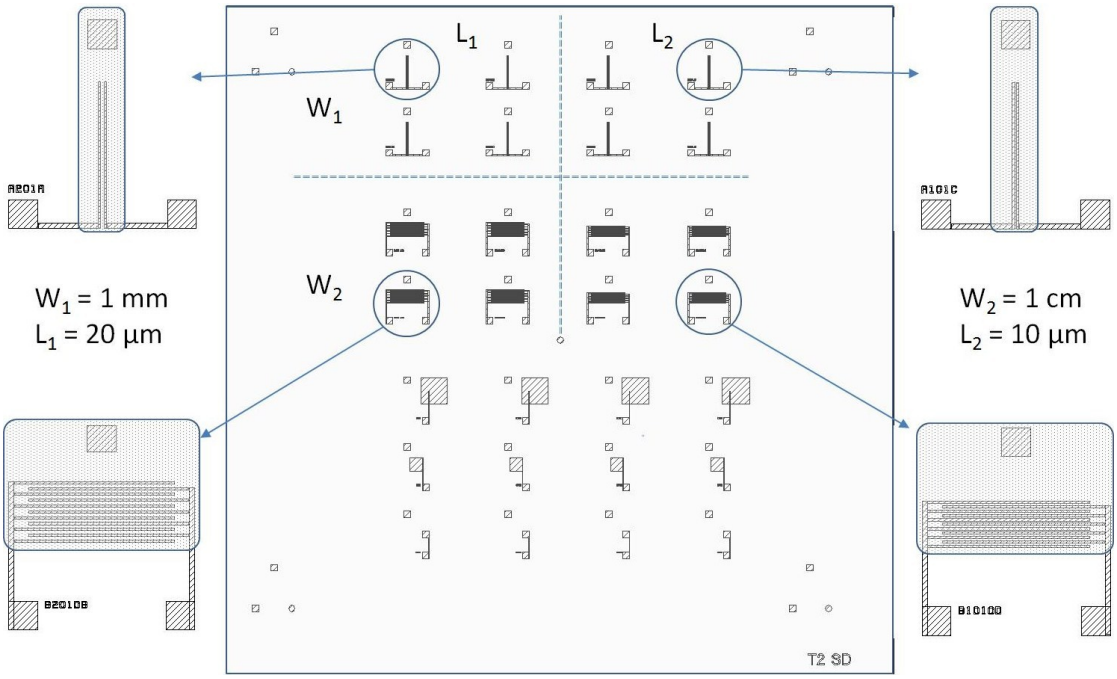


Figure A.3: Layout for TG1 and TG2

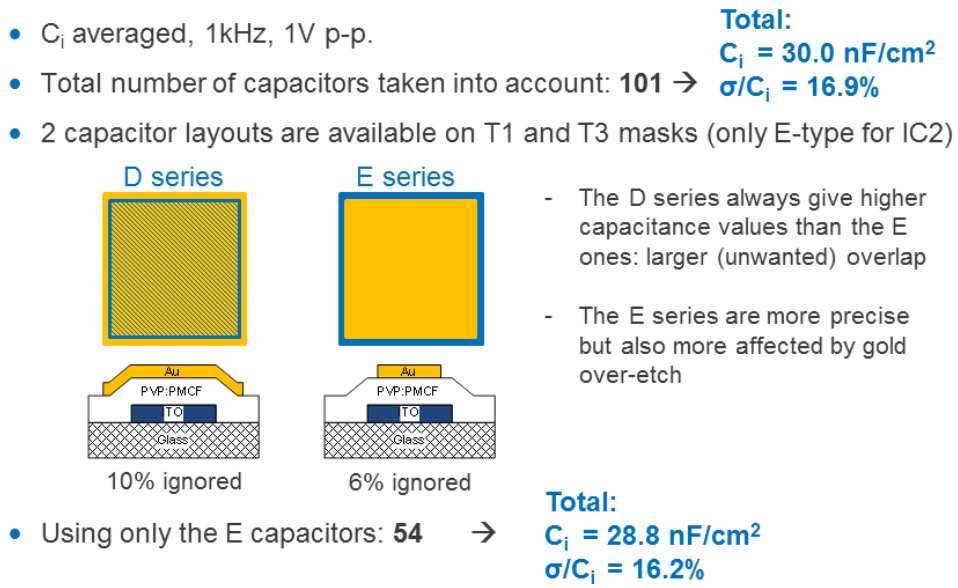


Figure A.4: Capacitors from BG4 and BG5: general information.

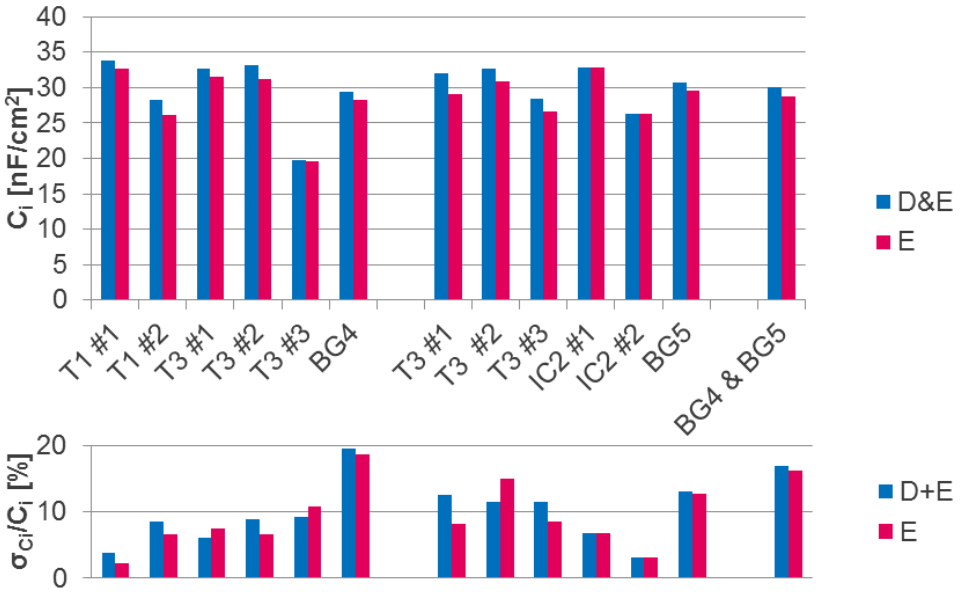
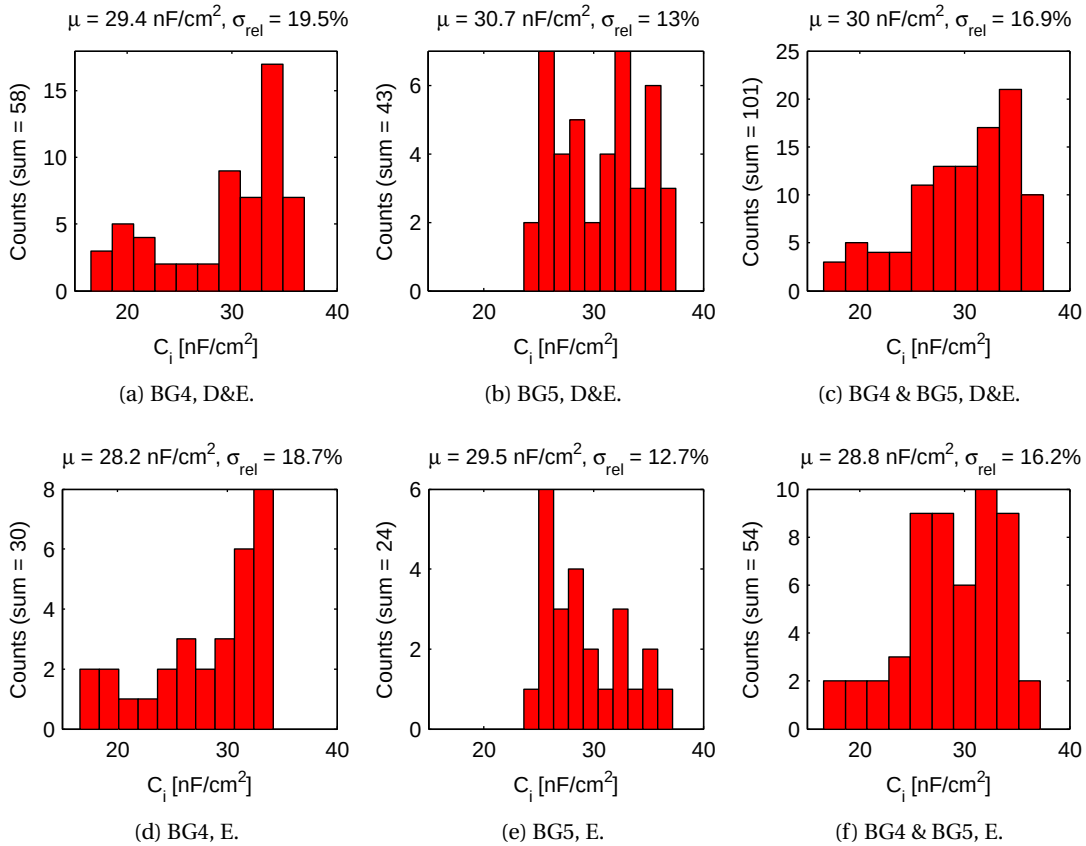


Figure A.5: Detailed average capacitances and relative standard deviations.



(a) BG4, D&E. (b) BG5, D&E. (c) BG4 & BG5, D&E.

(d) BG4, E. (e) BG5, E. (f) BG4 & BG5, E.

Figure A.6: BG4 & BG5: dielectric capacitance.

A $200 \times 200\ \mu m^2$ capacitor from BG4 was taken for additional $I-V$, $C-V$ and $C-f$ measurements. Results are shown in Figure A.7. The $C-V$ curves show that, for $f > 1$ kHz, 10.5 pF $< C <$ 10.7 pF over a voltage range of 25 V. At $V = 0.0$ V, the $C-f$ curve confirms this capacitance stability over the mentioned frequency range. Over 1 MHz, the coaxial cable capacitance becomes dominant.

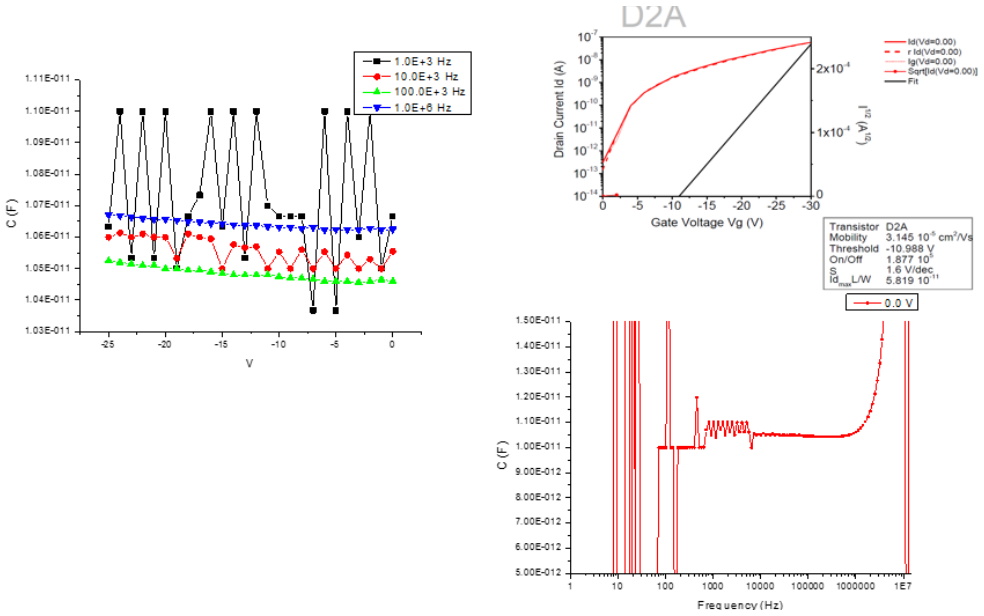


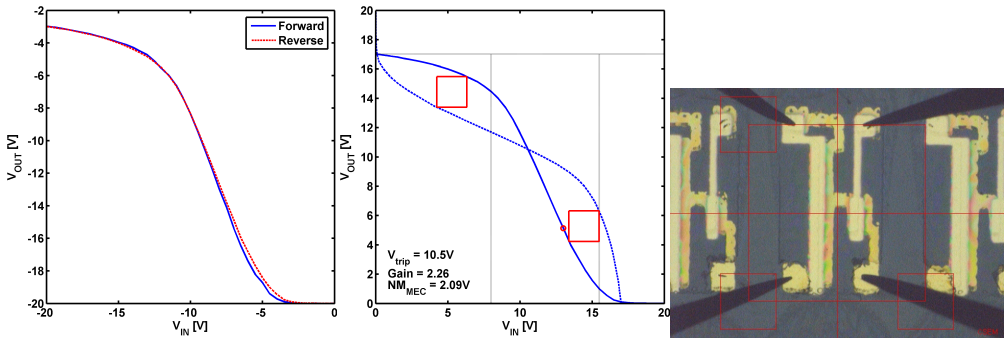
Figure A.7: Capacitor from BG4 with $C-V$, $C-f$ and $I-V$ measurement.

A.1.3 Source-drain/gate overlap area

For the following transistor layouts, the overlap area, A_{ov}, reads:

- T1_A: $A_{ov} = 2L_{ov}W$, with $L_{ov} = 10\ \mu$m.
- T1_B: $A_{ov} = 2W_{\text{finger}}W + (W_{\text{gate}} - L - 2W_{\text{finger}}W)W_{\text{access}}$, with $W_{\text{finger}} = 20\ \mu$m, $W_{\text{gate}} = 200\ \mu$m and $W_{\text{access}} = 40\ \mu$m.
- T3_A: $A_{ov} = W_{\text{finger}}(W + W_{\text{internal}})$, with $W_{\text{finger}} = 10\ \mu$m and $W_{\text{internal}} = 500\ \mu$m.
- T3_B: same as T3_A with $W_{\text{finger}} = 5\ \mu$m.
- IC2: $A_{ov} = W_{\text{finger}}(W/W_{\text{internal}} + 1)(W_{\text{internal}} + L_{ov})$, with $W_{\text{finger}} = 5\ \mu$m, $W_{\text{internal}} = 250\ \mu$m and $L_{ov} = 20\ \mu$m.
- TG1 and TG2 (finger OTFTs only): same as T1_B with $W_{\text{gate}} = 470\ \mu$m.
- TG3: same as T1_B with $W_{\text{gate}} = 450\ \mu$m and $W_{\text{access}} = 50\ \mu$m.
- TG4: same as T1_A with $L_{ov} = L_{ov,\text{design}} + L_{ov,\text{ink spread}} = 50 + 35 = 85\ \mu$m.

- BG6: $A_{ov} \approx 2L_{ov}(W + 2W_{\text{access}} + L)$, with $L_{ov} = 0.15$ μm and $W_{\text{access}} = 20$ μm. (only for the OTFTs shown in Figure 1.44).



(a) (b) (c)

Figure A.8: Typical characteristics of the best zero-VGS inverter from TG4. (a) raw measurement, (b) post-processed data. $V_{\text{DD}} = 20$ V, $L = 100/30$ μm (nominal, with ink spread) and $W_{\text{load}}/W_{\text{driver}} = 4$ and (c) micrograph. This results indicates a normally-ON load transistor therefore an outlier with respect to the experimental distribution (see Figure 1.40).

A.2 About electrical characterization

A detailed view of a typical Origin project generated by TP-10 is visible in Figure A.9. For that purpose, TP-10 actually calls the *OFET Suite* software I contributed to once the measurement is finished.

Demonstration $t_{\text{rise}} = \tau \ln 9$

The step response of a single stage low pass RC network is (input signal of V_i amplitude):

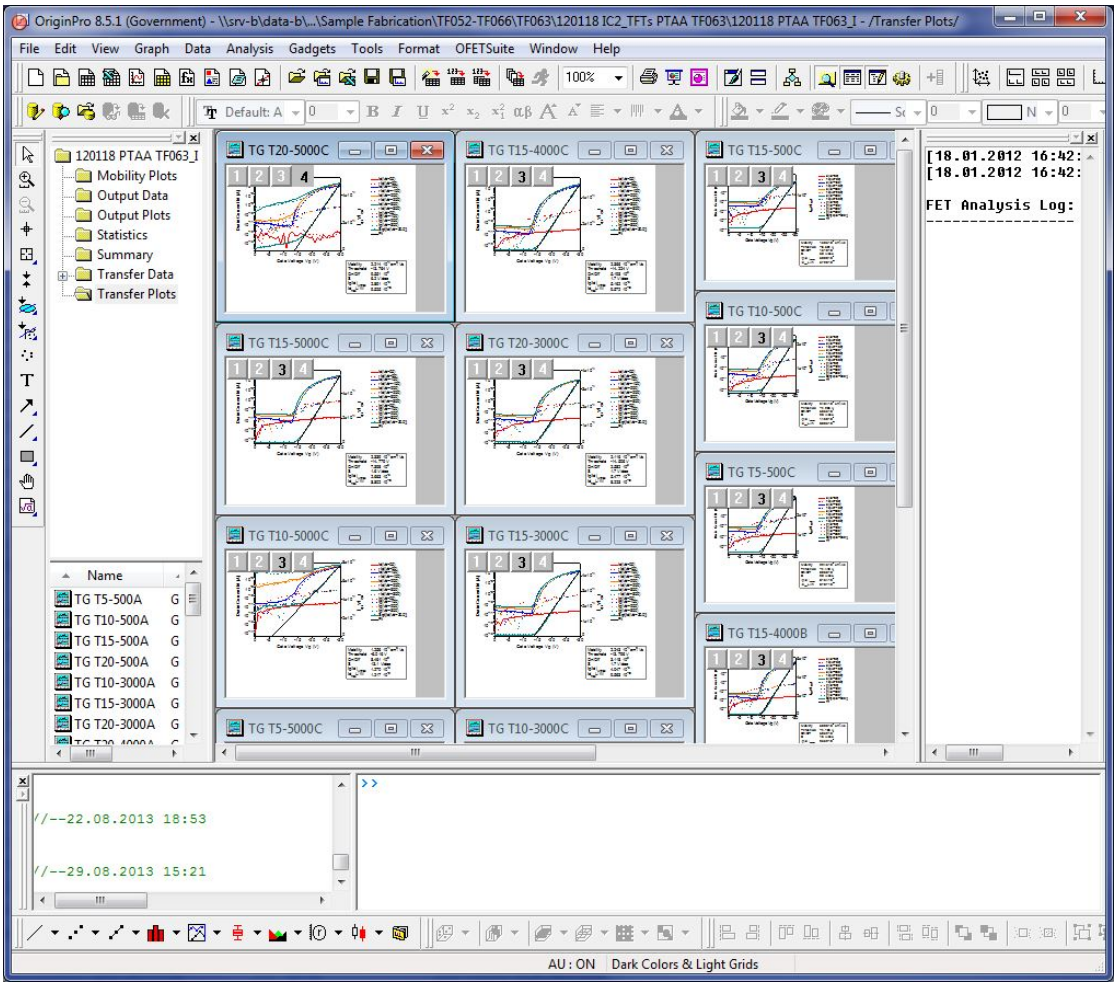
$$V(t) = V_i\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \tag{A.1}$$

Thus the time t to reach $V(t)$ is:

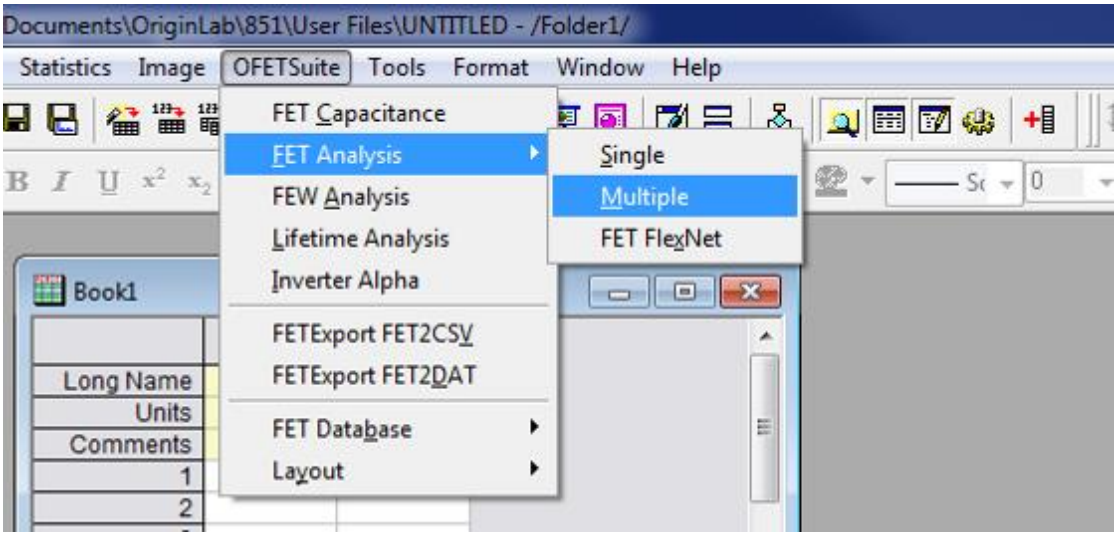
$$t = -\tau \ln\left(1 - \frac{V(t)}{V_i}\right) \tag{A.2}$$

Finally:

$$\begin{aligned} t_{\text{rise}} &= t_{90\%} - t_{10\%} && \text{(A.3)}\\ &= -\tau \ln(1-0.9) + \tau \ln(1-0.1) && \text{(A.4)}\\ &= -\tau \ln(0.1) + \tau\,(\ln(9) + \ln(0.1)) && \text{(A.5)}\\ &= \tau \ln 9 && \text{(A.6)} \end{aligned}$$



(a) Generated Origin project.



(b) OFET Suite.

Figure A.9: Generated Origin project and OFET Suite.

A.3 About OTFT modeling

Figure A.10 shows the results of the modified transmission line (M-TLM) contact resistance extraction on 5 selected OTFTs.

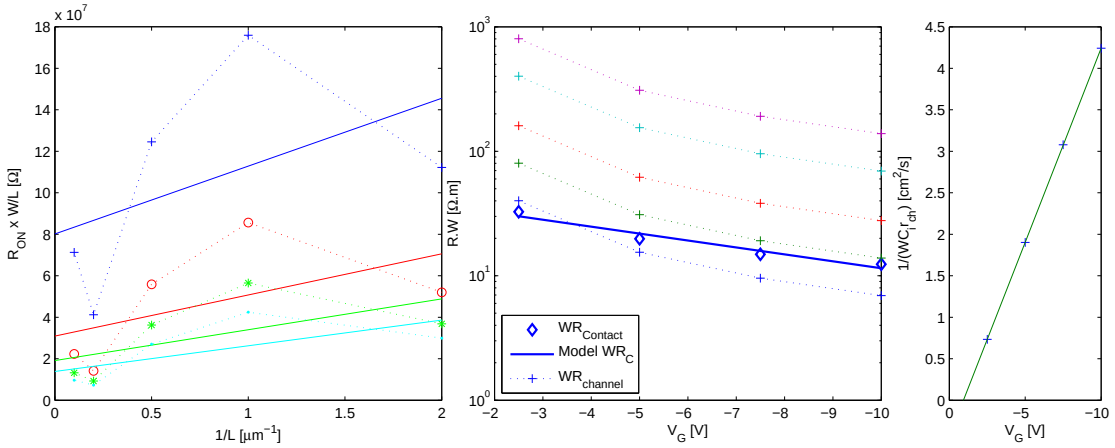


Figure A.10: M-TLM contact resistance extraction of BG6 OTFTs

Figure A.11 shows the gate leakage current versus the gate voltage for transistors of different OTFT platforms. The experimental data is fitted with two kinds of power law. Whereas the fits are quite representative, neither data nor obtained power law exhibit any kind of common behavior.

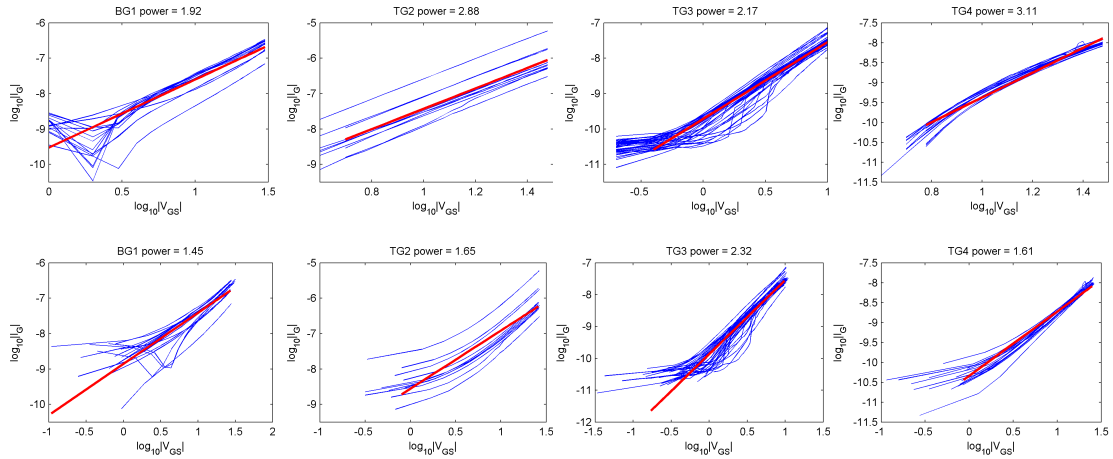


Figure A.11: Gate leakage versus V_{GS} at $V_{DS} = 0\,V$ and $V_{GS} < \min(V_{T,sat}, 0V)$ (p-type) in a log-log scale. Top row: data (thin blue lines) fitted to $I_G \propto |V_{GS}|^{power}$ (thick red line). Bottom row: data (thin blue lines) fitted to $I_G \propto |V_{GS} - V_{T,sat}|^{power}$ (thick red line). The obtained value of "power" is given in each graph. Number of involved OTFTs: 16 for BG1, 11 for TG2, 37 for TG3 and 16 for TG4.

A.3.1 Introduction to the modeling platform

A dedicated parameter extraction platform was developed in the framework of this thesis. Most of the PEMs described in Chapter 3 have been implemented: Level-1, partially Level-2, Level-3, TLM, M-TLM [127], I_{OFF} but also other published contact resistance models [124, 125] and PEMs such as UMEM [73] and the dual-exponential DOS model [141]. The developed tool depicted in Figure A.12 can import transistor data from different EU partners and acquisitions units (TP-10, EP6, $C-V$...), perform a set of user-defined analysis and generate on-demand dedicated PDF reports.

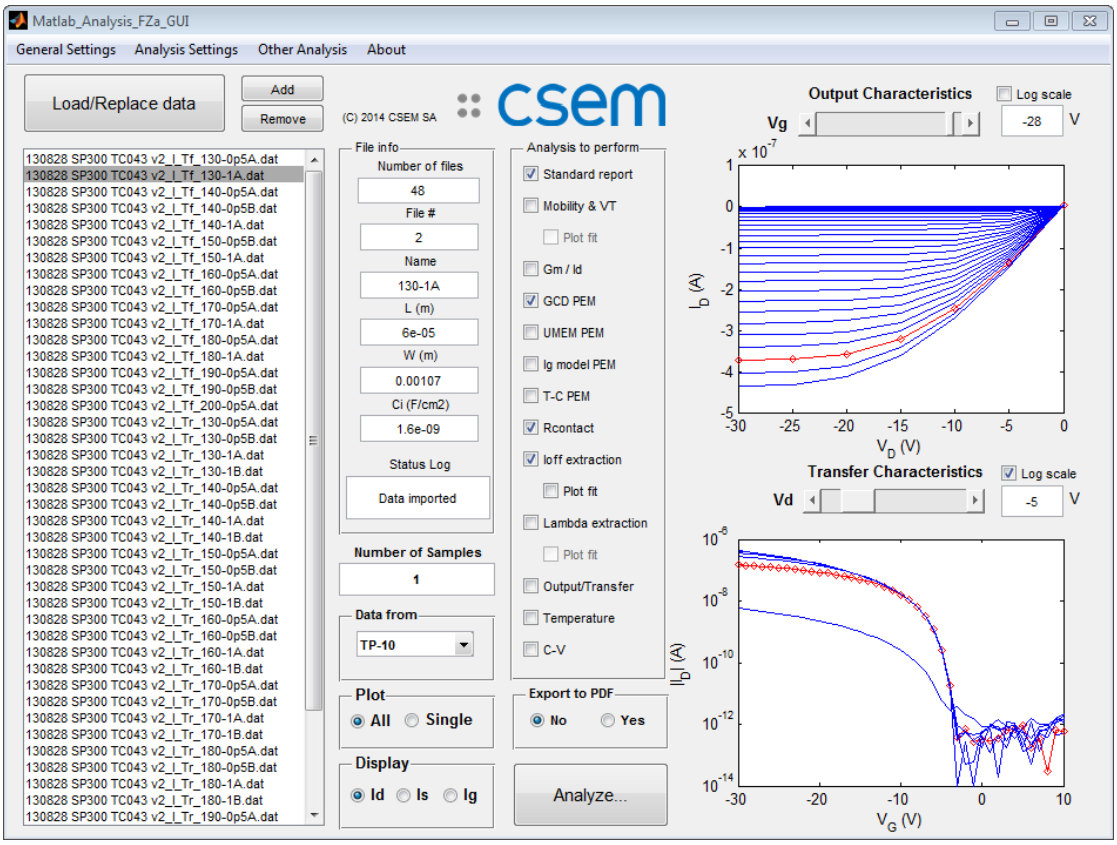


Figure A.12: Parameter extraction platform developed during this thesis.

A.4 About statistical modeling

A.4.1 Additional g_m/I curves

Figure A.13 shows that long-channel OTFTs, such as TG4's, are perfectly normalized which is not the case for BG6-s OTFTs including the sub-micrometer BG4-BG5 ones. This illustrates the limitation of this method which, as for silicon MOSFETs, is only valid for long-channel transistors.

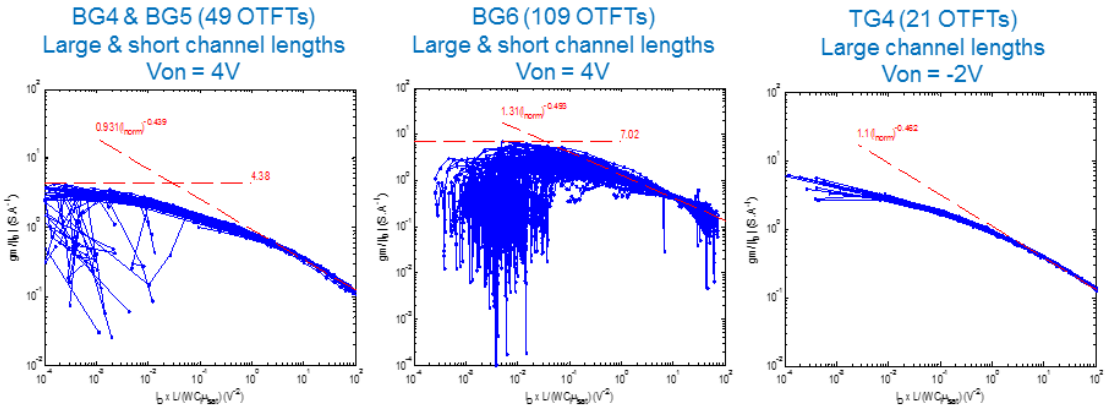
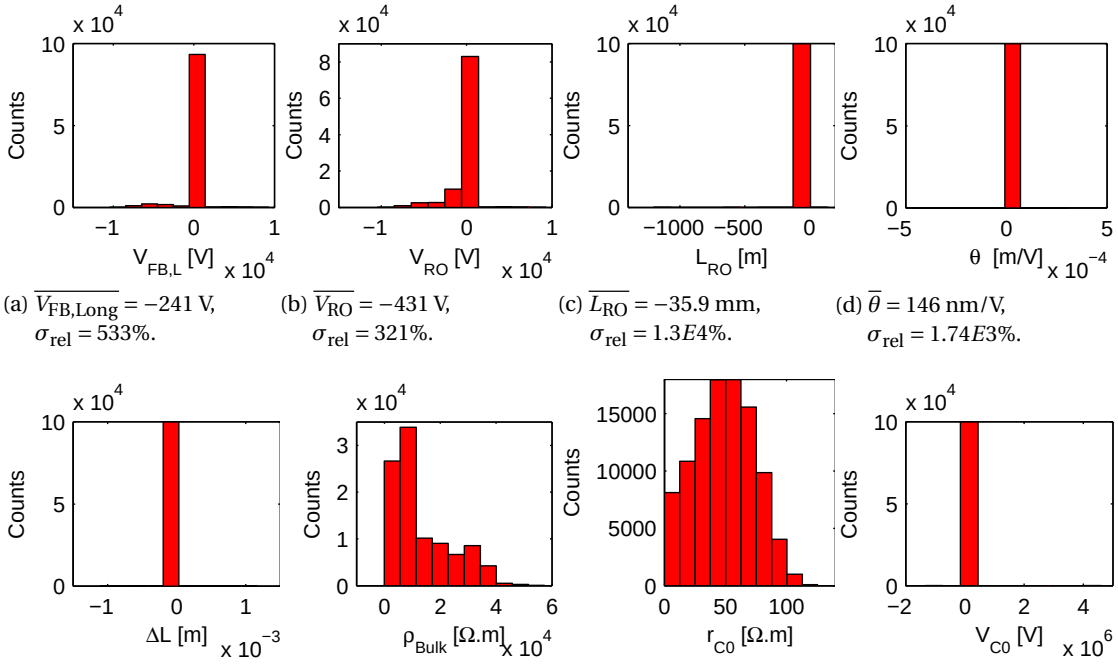


Figure A.13: Normalized g_m/I_D diagram per technology.

A.4.2 Statistical PEM: distributions of the 100'000 generated 5-OTFT sets

Figure A.14 shows the results of the Level-2 PEM performed on the 100'000 generated 5-OTFT sets (before filtering).



(a) $\overline{V_{\text{FB,Long}}} = -241$ V, $\sigma_{\text{rel}} = 533\%$.
(b) $\overline{V_{\text{RO}}} = -431$ V, $\sigma_{\text{rel}} = 321\%$.
(c) $\overline{L_{\text{RO}}} = -35.9$ mm, $\sigma_{\text{rel}} = 1.3E4\%$.
(d) $\overline{\theta} = 146$ nm/V, $\sigma_{\text{rel}} = 1.74E3\%$.
(e) $\overline{\Delta L} = 233$ nm, $\sigma_{\text{rel}} = 3.61E3\%$.
(f) $\overline{\rho_{\text{Bulk}}} = 13.5$ kΩ.m, $\sigma_{\text{rel}} = 77.8\%$.
(g) $\overline{r_{\text{C0}}} = 48.8$ Ω.m, $\sigma_{\text{rel}} = 49.7\%$.
(h) $\overline{V_{\text{C0}}} = 43.4$ V, $\sigma_{\text{rel}} = 3.51E4\%$.

Figure A.14: Raw distributions of the Level-2 model parameters in linear scale obtained on BG6 OTFTs. Total: 100 000.

B Acronyms and symbols

Table B.1: Acronyms and their definition.

Acronym	Definition
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor FET
OFET	Organic FET
OTFT	Organic Thin-Film Transistor
OSC	Organic semiconductor
CMOS	Complementary metal oxide semiconductor
PEM	Parameter Extraction Method
FoM	Figure of Merit
BG-BC	Bottom-gate bottom-contact
TG-BC	Top-gate bottom-contact
SAM	Self-assembled monolayer
INV	Inverter
R-O	Ring-oscillator
RE	Relative error
NRMSD	Normalized relative mean-square deviation
NM	Noise margin
WNM	Worst case noise margin
GCD	Generic charge drift
VRH	Variable range hopping
TLM	Transmission line method
M-TLM	Modified TLM

Table B.2: Symbols and their definition.

Symbol	Definition
μ	Charge carrier mobility [cm^2/Vs]; can also denotes an average
V_T	Threshold voltage [V]
V_{ON} or V_{to}	Turn-on voltage [V]
V_{FB}	Flat-band voltage [V]
σ	Standard deviation
R^2	Determination coefficient
ϵ_0	Electric permittivity of vacuum [$\approx 8.854 \times 10^{-12}$ F/m]
W	Channel width [m]
L	Channel length [m]
C_i	Dielectric capacitance [F/cm^2]
SS or S	Subthreshold swing [V/dec]
λ	Channel length modulation parameter [1/V]
P_D	Defect probability

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Publications

Journal articles:

- F. Zanella, N. Marjanović, R. Ferrini, F. X. Pengg, C. C. Enz, and J.-M. Sallese, "Sub-micrometer organic thin-film transistors: technology assessment through noise margin analysis of inverters," *IEEE Trans. Electron Devices*, (in press, 2014).
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