High-K Dielectric FinFETs on Si-Bulk for Ionic and Biological Sensing Integrated Circuits

THÈSE N^{O} 6134 (2014)

PRÉSENTÉE LE 2 MAI 2014

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DES DISPOSITIFS NANOÉLECTRONIQUES
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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ÉCOLE POLYTECHNIQUE
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Suisse
2014

Io, eterno studente
perché la materia di studio sarebbe infinita
e soprattutto perché so di non sapere niente.

Francesco Guccini

To all the beloved who made me smile during my Ph.D.

Abstract

Nanotechnology is a broad branch of science dedicated to the manipulation of matter featuring critical dimension below 100 nm. Despite the futuristic common mindset towards nanotechnology, anybody using an electronic device able of computing and processing data is using nanotechnology. Transistors, the smallest units of a microprocessor, have reached critical gate lengths in the tenths of nanometers. Lately, the idea of nanotechnology has been associated with small robots capable of exploring and operating within the human body. Though this type of technology may have to wait several years and overcome many obstacles, the idea does arise from several solid and proved emerging applications of nanotechnology in the field of life sciences.

Field-Effect Transistors (FET) based on Silicon Nanowires (SiNW) have emerged as promising candidates for a new generation of label-free real-time sensors for the detection of chemical and biological species. Many areas of science such as nanoelectronics, chemistry, physics, biology and medicine have been collaborating together in these recent developments. Despite SiNWs' potential has been largely proven and the knowledge of sensing mechanisms widely extended, mass-production and integration of such sensors has still to face many challenges.

The demonstration of a state-of-the-art FET sensor, compatible with CMOS Integrated Circuits, is addressed in this thesis. A *fully-depleted n-channel Fin Field-Effect Transistor* (FinFET) has been implemented as sensor in a liquid environment, according to the working principle of the Ion Sensitive Field-Effect Transistor (ISFET). Its vertical architecture and multiple gate control provide high stability and high signal-to-noise ratio. Moreover, such an architecture works under low applied voltages and currents, taking into consideration the power constraints of the semiconductor industry.

In this thesis, FinFETs with critical dimensions of the order of 30 nm have been designed, fabricated and characterized for their implementation as both circuit and sensing units in a microfluidic platform. A challenging fabrication process has been carried out on Si-bulk substrates where vertical transistors have been defined and then insulated by the so-called Si_3N_4 spacer technology. FinFETs featuring a metal-gate have been successfully characterized, showing excellent electrical properties in terms of subthreshold slope, SS= 72 mV/dec, and on-off current ratio, $I_{on}/I_{off} = 10^6$. These FinFETs have then been validated as pH sensors. Sensitivity close to the Nernst limit, S = 57 mV/pH, and high current variation at the readout, S_{out} = 60%, have been achieved. Long-term measurements have been performed over 4.5

days, demonstrating that stability and reliability are key-advantages of the FinFETs. The drift over time has been calculated to be $\delta V_{th}/\delta t = 0.13\,\mathrm{mV\,h^{-1}}$ with accuracy of 0.012 pH.
FimH protein has been successfully detected with a differential pair of FinFETs.

Finite Element Analysis (FEA) simulations have been performed to optimize the geometrical and electronic properties of the FinFETs. They have also proven to be a reliable tool for the calibration of fabrication steps, such as ion implantation and bulk wet oxidation. SPICE simulations, implementing analytical equations in Verilog-A, have been used to connect two or more devices together. A sensing common source amplifier, a ring oscillator and a pseudo-differential amplifier have been demonstrated.

Moreover, from the idea developed through circuit simulations, a device consisting of a metal-gate FinFET and a liquid-gate FinFET has been fabricated and demonstrated as sensing amplifying stage. If the sensing FinFET with liquid-gate is implemented as driver transistor and the metal-gate FinFET as load, the sensing variation at the input is amplified with a gain $A = \Delta V_{out}/\Delta V_{in} = 6.6$.
Low power consumption has been guaranteed for both single (tens of nW) and pair of FinFETs (few hundreds of nW), and without the use of a back-gate.

All devices feature an HfO_2 high-k gate dielectric. High-k oxides allow the continuous CMOS scaling process and they also provide the best sensitivity for pH applications. An electrical characterization based on HfO_2 MOS capacitor has been performed to investigate the impact of some fabrication factors on the oxide features. Good dielectric constant, $\varepsilon_{HfO_2} = 19$, high breakdown voltage, $V_{BD} = 14\,\mathrm{V}$, and negligible values of hysteresis have been achieved.

Keywords: Field Effect Transistor (FET) sensors, FinFET, ISFET, label-free sensor, nanoelectronics, pH sensor, biochemical sensing, Si-bulk, high-k dielectric, hafnium oxide, fully-depleted device, low power, Nernst limit, sensing integrated circuits, sensing common source amplifier, signal amplification, long-term stability.

Riassunto

La nanotecnologia è un ampio ramo della scienza dedicato alla manipolazione della materia con dimensioni critiche inferiori ai 100 nanometri. La Nanotecnologia non è una visione scientifica futuristica, chiunque usi un dispositivo elettronico in grado di calcolare e processare dati ne fa uso. Al giorno d'oggi, i transistors, gli elementi più piccoli di un microprocessore, hanno raggiunto dimensioni critiche di qualche decina di nanometro. Recentemente, il concetto di nanotecnologia è stato associato a quello di piccoli robot in grado di esplorare e di operare nel corpo umano. Questo dovrà aspettare qualche anno e sormontare molti ostacoli, ma l'idea sorge da concrete emergenti applicazioni della nanotecnologia alla biologia.

I transistor a effetto di campo (FET) basati su nanofili di silicio (SiNW) sono emersi come candidati promettenti per una nuova generazione di sensori label-free per il rilevamento in tempo reale di specie chimiche e biologiche. Molti settori scientifici come nanoelettronica, chimica, fisica, biologia e medicina hanno collaborato a questi recenti sviluppi. Nonostante il potenziale dei SiNW e le sempre piu diffuse conoscenze dei meccanismi di rivelazione, la produzione di massa e l'integrazione di questi sensori rimane confrontata a molte sfide.

In questa tesi, viene affrontata l'implementazione come sensore di un transistor all'avanguardia tecnologica e compatibile con circuiti integrati CMOS. Un fully-depleted n-MOS FinFET, viene qui dimostrato come sensore in ambiente liquido, sul principio di funzionamento dell'Ion Sensitive FET (ISFET). La sua architettura verticale ed il controllo dato da molteplici gate, sono in grado di fornire stabilità ed un buon rapporto segnale-rumore. Inoltre, una tale architettura funziona con basse tensioni di alimentazione e correnti, tenendo in considerazione i bisogni di basso consumo dell'industria dei semiconduttori.

In questa tesi, FinFETs con dimensioni critiche dell'ordine di 30 nm sono stati progettati, fabbricati e caratterizzati per essere implementati come unità circuitali e unità sensoristiche in una piattaforma microfluidica. Un laborioso processo di fabbricazione è stato condotto su substrati di silicio, sui quali i transistor verticali sono stati creati e isolati con spaziatori di Si_3N_4. I FinFETs con gate metallici sono stati caratterizzati per primi, dimostrando eccellenti proprietà elettroniche di Subthreshold Slope SS= 72 mV/dec, e un'ottimo rapporto di correnti on-off, $I_{on}/I_{off} = 10^6$. In seguito, è stato quindi dimostrato come questi FinFETs possano essere usati come sensori di pH. Sono state ottenute una sensibilità vicina al limite di Nernst, S= 57 mV/dec, ed un' alta variazione di corrente all'uscita pari al 60%. Una misura a lungo termine è stata condotta per un periodo di 4.5 giorni, dimostrando la stabilità e l'affidabilità

di questi FinFET. Sono state calcolate una deriva nel tempo di soli $\delta V_{th}/\delta t = 0.13$ mV/h con un'accuratezza di 0.013 pH.
La proteina FimH è anche stata rivelata per mezzo di una coppia differenziale di FinFET.

Le caratteristiche geometriche ed elettroniche dei FinFETS sono state ottimizzate grazie a simulazioni ad elementi finiti (FEA). Tale analisi si è rivelata essere uno strumento affidabile per la calibrazione di vari fasi del processo di fabbricazione come l'impiantazione ionica e l'ossidazione termica del silicio. Sono state effettuate anche simulazioni con SPICE, implementando equazioni analitiche scritte in Verilog-A, per collegare due o più FinFET, ottenendo quindi un'amplificatore common source, un ring oscillator, ed un amplificatore pseudo-differenziale con capacità di sensing.

In seguito a queste simulazioni è stato fabbricato un dispositivo composto da un FinFET con gate metallico e un FinFET con gate liquido e ne è stato dimostrato l'uso in quanto modulo di amplificazione. Implementando il FinFET con gate liquido come driver tranistor ed il FinFET con gate metallico come carico, la variazione all'ingresso è stata amplificata con un guadagno $A = \Delta V_{out}/\Delta V_{in} = 6.6$. La potenza totale dissipata è molto bassa, sia per un FinFET singolo (decina di nW) che per una coppia di FinFET (centinaia di nW), e non è stato fatto uso di back-gate.

Tutti i dispositivi fabbricati presentano un gate isolante ad alta costante dielettrica (high-k) in HfO_2 che consente non solo la compatibilità con la continua miniaturizzazione CMOS, ma anche una migliore sensibilità per applicazioni pH. Una caratterizzazione elettrica basata su condensatori MOS in HfO_2 ha inoltre permesso di definire l'impatto di vari fattori del processo di fabbricazione sulle caratteristiche dell'ossido. Sono quindi state ottenute una costante dielettrica $\varepsilon_{HfO_2} = 19$, una tensione di rottura dell'ossido $V_{BD} = 14\,\mathrm{V}$ e un'isteresi trascurabile.

Parole chiave: sensori Field-Effect Transistor (FET), FinFET, ISFET, sensori label-free, nanoelettronica, sensori di pH, sensori biochimici, Si-bulk, dielettrici ad alta costante dielettrica (high-k), ossido di afnio, dispositivi fully-depleted, basso consumo, limite di Nernst, circuiti integrati sensoristici, sensori ad amplificazione common source, amplificazione del segnale, stabilità a lunga durata.

Acknowledgements

I would first like to thank my advisor, Prof. Ionescu for giving me the possibility of undertaking this incredible journey into such advanced field of technology. Most of all, I would like to thank him for the chance of being involved in a valuable project such as Nanotera and participating to high level conferences in the field of sensors.

Thanks to all my present and former Nanolab colleagues. In particular, A. Bazigos, L. De Michielis, H. Guerin, E. Buitrago, W. Vitale, A. Biswas and M. Berthomé for being so patient with all my questions and doubts especially in the last year of my thesis. I. Buzzi and K. Jaymes for being there at the time and situations you don't expect them to be. Thanks to Prof. Sallese for receiving me every time I was getting lost in theoretical aspects. Thank to M. Halm and Prof. Gijs for being solid supports of the EDMI school.

The work here presented is the result of a long journey...

Everything started at CMi, where a wide team of valuable experts helped me to go through apparently insurmountable obstacles every day. In particular, I would like to thank P. Fluckiger for his capability of managing the cleanroom and D. Bouvet for an uncountable number of hours spent with me discussing the best technology solutions. Thanks to V. Ruhaut and A. Guillet for promptly assisting me with the Ritetrack and the AMS at anytime, and Claudia for her quick interventions outside the cleanroom. Thanks to all the CMi users, staff and ex-staff with whom I shared many technological issues and fun hours.
Thanks to A. Pezous for every time I scheduled and canceled the umpteenth hot phosphoric acid etching to be performed at CSEM, in Neuchatel.
In the south of France, the Ibs team helped me to get along with the challenge of Si-Bulk implantation.
Back to Switzerland, I would like to thank PSI and especially K. Bedner for the first RTAs. Even further... KTH in Sweden for other RTAs and in particular Prof. Östling and Prof. Hellström for the useful discussion on high-k dielectrics. ETHZ, and A. Stettler for the first bonding tests, G. Corradini at EPFL for many others.
Thanks to A. Mapelli for carefully dicing such small things and for not allowing me to give up in cleanroom when I really was going to.
Thanks to LPM and C. Jacq for the availability and allowing me to use their tools during the platform assembly.

Last stop at the University of Basel, where finally I could see my devices in action at the Nanoelectronics group. I would like to thank Prof. Schönenberger and Prof. M. Calame for allowing to me to collaborate so actively with their team. A big team, with whom I shared a lot of working (and not) hours: O. Knopfmacher, A. Tarasov, K. Bedner, R.L. Stoop and G. Navarra. A special thanks to M. Wipf for the experiments done together, for the long-term stability measurements and the endless phone conversations to explain me electrochemistry. Basel is also location of the BSSE department of ETHZ where I had the pleasure to work with P. Livi on circuit simulations, thanks also to Prof. Hierlemann who attentively corrected many pages of our Italian-English papers. Thank to P. Scarbolo for his great contribution to the oxide characterization and to make me discover Matlab (better late than never).
Thank to all of you for your cooperation who contributed so much in the realization of this work.

Thanks to Prof. L. Santorum, because he was the first one teaching me how much science is all around us and, most important, that not every question has an answer.
Thanks to Prof. V. Germano, because she taught me that if we stop smiling at children we stop smiling at our future.
Thanks to Prof. F. Pirri, Prof. M. Cocuzza and Prof. P. Allia for being such valuable resources of the (at the time) Physics Department of Politecnico of Turin and active promoters of the master in Micro and Nanotechnologies for Integrated Systems.

Thanks to my city, Turin, for hosting me so peacefully every time I was looking for comfort. Thanks to my mum Agnese for allowing me to be, sometimes, still a child and to my dad Pino to remind me to make fun of myself. Thanks to Mario, Marta and Daniele, simply, because you exist. Thanks to all my cousins and friends, Carola, Celeste, Diego, Andrea, Gianluca for the nice evenings full of laughs and their love, their children and parents, my grandma, you are all my friends. Thanks to Alice, Giada, Stefi, Simo, Ste, Raghu, Fazzo because no matter where we are and what we are going through, I know you'll always be there. Thanks to Alessandro for making me realize how many things seem, but they are not, impossible and giving me the love I have always dreamt of.

Lausanne, 10 Décembre 2013 Sara

Symbols and Abbreviations

Symbols or Abbreviation	Meaning
a	Ion Activity
A	Area
A/D	Analog to Digital
A_{pad}	Capacitance Area
A_v	Voltage Gain
AC	Alternating Current
Al	Aluminum
ALD	Atomic Layer Deposition
ANP	Acetic Nitric Phosphoric
Al_2O_3	Aluminum Oxide
$AlSi$	Aluminum-Silicon
BGA	Blood Gas Analyzer
BHF	Buffered Hydrogen Fluoride
C_a	Adsorption Capacitance
C_{acc}	Accumulation Capacitance
C_{dep}	Depletion Capacitance
C_{dif}	Diffuse Layer Capacitance
C_{DL}	Double Layer Capacitance
C_g	Oxide Gate Capacitance
C_{inv}	Inversion Capacitance
C_{it}	Interface-State Capacitance
C_{max}	Maximum Capacitance
C_{min}	Minimum Capacitance
C_{ox}	Oxide Capacitance
C_p	Parasitic Capacitance
C_s	Semiconductor Capacitance
C_{Si}	Silicon Capacitance
C_{Stern}	Stern Capacitance
CD	Critical Dimension
CF_4	Tetrafluoromethane

C_4F_8	Octafluorocyclobutane
CH_3COOH	Acetic Acid
Cl_2	Chlorine
$CMOS$	Complementary Metal–Oxide–Semiconductor
CMP	Chemical Mechanical Polishing
CP	Costant Power
CSA	Common Source Amplifier
$D_{etching}$	Si Etching Depth
D_{imp}	Implantation Depth
d_{NW}	Distance Between Fins
DC	Direct Current
$DELTA$	Depleted Lean-Channel Transistor
DG	Double Gate
DI	Deionized
$DRIE$	Deep Reactive Ion Etching
E_G	Energy Band Gap
E_{ref}	Reference Electrode Potential
E_S	Surface Transverse Electric Field
$E1$	Critical Electric Field, Phonon Scattering
$E2$	Critical Electric Field, Surface Scattering
EBL	Electron Beam Lithography
EDA	Electronic Design Automation
$ELISA$	Enzyme-Linked ImmunoSorbent Assay
EOS	Electrolyte-Oxide-Semiconductor
EOT	Equivalent Oxide Thickness
FEA	Finite Element Analysis
FET	Field Effect Transistor
FIB	Focused Ion Beam
$FinFET$	Fin Field Effect Transistor
G	Gibbs Energy
g_{ds}	Output Conductance
g_m	Trasconductance
GAA	Gate-All-Around
GAO	Gastric Acid Output
$GPIB$	General Purpose Interface Bus
H	Hydrogen
h_D	Driving Transistor Height
h_S	Sensor Height
h_{Si}	Si Body Height
H_{Fin}	Fin Heigth
H_{Ribbon}	Ribbon Heigth
HCl	Hydrogen chloride

$HClO_4$	Perchloric Acid
HF	Hydrogen Fluoride
HfO_2	Hafnium Oxide
HNO_3	Nitric Acid
H_2O	Water
H_2O_2	Hydrogen Peroxide
H_3PO_4	Phosphoric Acid
HR	High Resolution
H_2SO_4	Sulfuric Acid
HSQ	Hydrogen Silsesquioxane
I_b	Bond Ionicity
I_{bs}	Bulk to Source Current
I_c	Compliance Current
I_d	Drain Current
I_{d_0}	Initial Drain Current
I_g	Gate Current
I_{th}	Threshold Current
IC	Integrated Circuit
$ISFET$	Ion Sensitive Field Effect Transistor
k	Boltzmann Constant
K_a	Acid Dissociation Constant
K_b	Base Dissociation Constant
L	Length
l_B	Bjerrum Length
L_{Fin}	Fin Length
L_{imp}	Implantation Lateral Extension
L_{Ribbon}	Ribbon Length
l_{Si}	Si Body Length
La_2O_3	Lanthanum Oxide
$LPCVD$	Low Pressure Chemical Vapour Deposition
LR	Low Resolution
LTO	Low Temperature Oxide
$MG-FET$	Multi Gate FET
$MOCVD$	Metal Organic Chemical Vapor Deposition
$MOSCAP$	Metal-Oxide-Silicon Capacitor
$MOSFET$	Metal-Oxide-Silicon Field Effect Transistor
n_A	Acceptor Dopant Dose
N_A	Acceptor Dopant Concentration
N_D	Donor Dopant Concentration
n_i	Intrinsic Carrier Concentration
N_S	Surface Site Density
N_2	Nitrogen

NH_4OH	Ammonium Hydroxide
OH	Hydroxide
P	Power
P_{dep}	Depletion Load Power
P_{enh}	Enhancement Load Power
P_{Fin}	Fin Power
PCB	Printed Circuit Board
PDA	Post Deposition Annealing
$PDMS$	Polydimethylsiloxane
PEC	Proximity Effect Correction
$PGMEA$	Propylene Glycol Monomethyl Ether Acetate
PMA	Post Metallization Annealing
$POCl_3$	Phosphoryl Chloride
PSA	Prostate Specific Antigen
$PTFE$	Polytetrafluorethylen
pzc	Point of Zero Charge
q	Elementary Charge
Q_{ox}	Oxidation Quality Factor
Q_D	Depletion Charge
R_L	Load Resistor
R_{ds}	Source and Drain Resistance
R_{out}	Output Resistance
RCA	Radio Corporation of America
RIE	Reactive Ion etching
RTA	Rapid Thermal Annealing
S	Sensitivity
S/V	Surface to Volume Ratio
S_{out}	Readout Sensitivity
SE	Standard Error
SEM	Scanning Electron Microscopy
Si	Silicon
SF_6	Sulfur Hexafluoride
Si_3N_4	Silicon Nitride
$SiNW$	Silicon Nanowire
SiO_2	Silicon Oxide
SiO_x	IL Oxide
SOI	Silicon-On-Insulator
$SPICE$	Simulation Program with Integrated Circuit Emphasis
SS	Subthreshold Slope
T	Temperature
t_{bot}	Bottom Fin Thicness
T_{Fin}	Fin Thickness

t_{HfO_2}	Hafnium Oxide Thickness
t_{IL}	Interfacial Layer Thickness
t_{ins}	Insulator Thickness
t_{ox}	Oxide Thickness
T_{ox}	Oxidation Temperature
t_{shell}	Thickness of N-doped Triangular Shell
t_{Si}	Si Body Thickness
t_{SiO_2}	Silicon Oxide Thickness
t_{SiO_x}	IL Oxide Thickness
t_{spacer}	Si_3N_4 Spacer Thickness
T_{Ribbon}	Ribbon Thickness
t_{top}	Top Fin Thickness
Ta_2O_5	Tantalium Oxide
$TCAD$	Technology Computer Aided Design
TEM	Transmission Electron Microscopy
$TEMAH$	Tetrakis-Ethyl-Methyl-Amino-Hafnium
Ti	Titanium
$time_{ox}$	Si Oxidation Time
TiO_2	Titanium Oxide
UV	Ultraviolet
V_b	Back-gate Voltage
V_{BD}	Breakdown Voltage
V_{DD}	Supply Voltage
V_d	Drain Voltage
V_{ds}	Source to Drain Voltage
V_{FB}	Flat Band Voltage
V_g	Gate Voltage
V_H	Hysteresis Amplitude
V_{IH}	Minimum Input High Voltage
V_{IL}	Maximum Input Low Voltage
V_{in}	Input Voltage
V_{liq}	Liquid Voltage
V_{off}	Inverter OFF Voltage
V_{on}	Inverter ON Voltage
V_{out}	Output Voltage
V_{ref}	Reference Voltage
V_s	Source Voltage
V_{th}	Threshold Voltage
W	Width
W_{Ribbon}	Ribbon Width
x_{dep}	Depletion Width
x_{dmax}	Maximum Depletion Width

z_i	Ion Valence
ZrO_2	Zirconium Oxide

Greek Letters

Greek Letters	Meaning
α	Sensitivity Parameter
β	Surface Buffer Capacitance
β_e	Substrate Correction for EBL
ε_0	Vacuum Permittivity
ε_{HfO_2}	Silicon Oxide Dielectric Constant
ε_{ins}	Insulator Dielectric Constant
ε_{ox}	Oxide Dielectric Constant
ε_{Si}	Silicon Dielectric Constant
ε_{SiO_2}	Silicon Oxide Dielectric Constant
ε_{SiO_x}	IL Oxide Dielectric Constant
η_e	Density Correction for EBL
λ_D	Debye Length
μ_n	Electron Mobility
μ_0	Maximum Mobility
μ_S	Surface Mobility
ρ_i	Ion Density
σ	Standard Deviation
χ_{sol}	Surface Dipole Potential
Ψ	Oxide-Electrolyte Potential
Φ_M	Metal Work Function
Φ_{Si}	Silicon Work Function
ϕ_S	Surface Potential
ϕ_f	Fermi Potential

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1 Introduction: Narrowing the Gap between Nanoelectronics and Electronics for Sensing

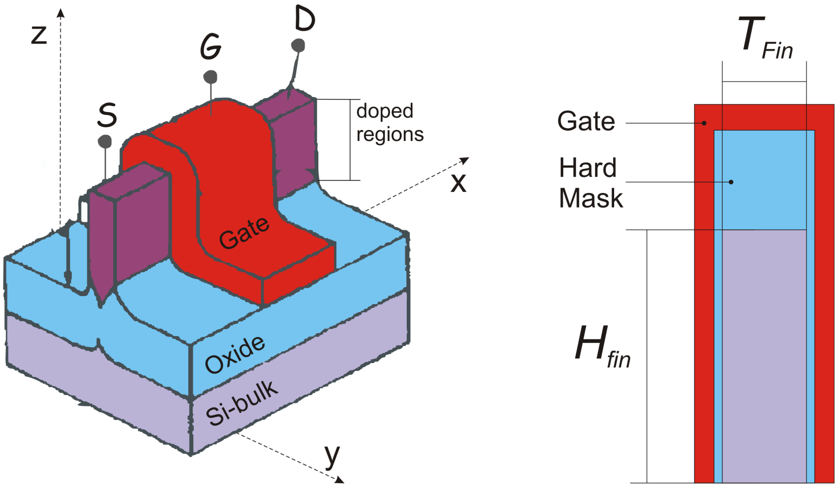
Field Effect Transistors (FET) based on Silicon Nanowires (SiNW) are emerging as ultrasensitive sensors for direct and label-free detection of chemical and biological species. Providing a quick response, durability, reliability and reproducibility of the fabrication process, they have become promising candidates competing with their mechanical and optical counterparts. Their potential has been widely demonstrated, but large-scale production and circuit integration are still challenging. The aim of this thesis is to create a more solid bridge between state-of-the-art nanoelectronics and the sensing field based on FET devices, looking forward to a definitive integration of sensing units in everyday electronic technology at the service of personal healthcare.

In this section, the main properties of a well-defined electronic device, namely the *n-channel fully depleted FinFET*, are introduced. Such architecture is recognized to be one of the best performing nanoelectronic device, thanks to the excellent electrostatic control provided by the multi-gate structure. The working principle of the ISFET is then presented together with a discussion on how the optimal performance of the FinFET could be an asset for the sensing field. The state-of-the-art related to SiNW sensing applications follows, focusing on the technology used to realize the SiNWs and their applications. The last sections describe the role of high-k dielectrics in CMOS scaling and in pH sensing applications, which are the main targets of this work.

1.1 Fin Field Effect Transistor in nanoelectronics

The first fabricated non-planar FET was proposed in 1989 as "fully DEpleted Lean-channel TrAnsistor (DELTA)" by Hisamoto et *al.* [1], as illustrated in Fig. 1.1a. The term Fin Field Effect Transistor (FinFET) was actually referring to the same DELTA structure but with an additional top hard-mask [2] used to avoid parasitic inversion at the corners, as shown in

Fig.1.1b. Commonly today and herein, the term FinFET is used also for the DELTA, that is technically the one implemented in this work. The DELTA and the FinFET are part of a group of transistors which can generally be referred to as multi-gate FETs (MG-FET) including double-gate (DG), triple and surrounding gate transistors [3]. These architectures have been developed to overcome the adverse effects that come along with CMOS scaling according to Moore's law [4] towards higher switching speeds and more densely integrated circuits. Some of the non-ideal effects have been identified as: (i) short-channel effects including voltage roll-off, (ii) drain-induced barrier lowering (DIBL), (iii) subthreshold slope degradation and (iv) non-negligible parasitic components [5]. Using a multi-gate architecture, a better control of the channel depletion is obtained with respect to a standard MOSFET and, most important, the influence of the drain electric field on the channel is reduced [6]. In the presented work, the FinFET length $L_{Fin} = 10\,\mu\text{m}$ is not directly subjected to the side effects of scaling but looking towards CMOS integration, the scaling compatibility is an indispensable feature. Moreover, the advanced channel control provided by the FinFET architecture will result in excellent sensor properties, as it will be shown in Chap. 5.



(a) DELTA [1]

(b) FinFET [2]

Figure 1.1: (a) Illustration of the DELTA [1] and (b) cross-section of a FinFET [2], as they were originally proposed.

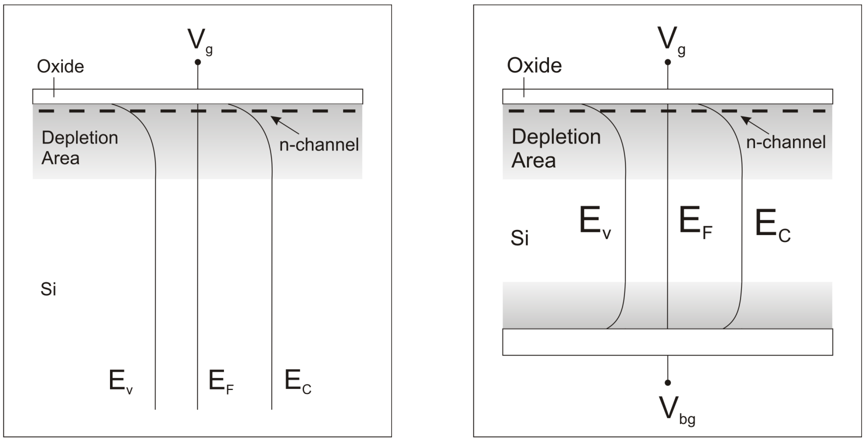
1.1.1 Full depletion in silicon thin-films

To better understand the advantages of the FinFET, it is worth to introduce the concept of full depletion of thin-films [5]. Figure 1.2 illustrates the band diagram of four different possible devices defined by the thickness of the silicon layer and the gate bias. It is important to notice that for a vertical thin-film, its dimension along the Y-axis (Fig. 1.1a) is, here, called "thickness" (T_{Fin}) and the one along the Z-axis is called "height" (H_{Fin}), avoiding the use of "width", commonly used in electronics for the dimension lying in a perpendicular plane with respect to the conduction direction. For an horizontal thin-film, the standard definition of width and silicon thickness applies. In this way, the term "thickness" always refers to the thinnest dimension which determines the condition of fully depletion. In Fig. 1.2 the following devices have been considered:

- Bulk MOSFET
- Thick-film on SOI
- Horizontal thin-film on SOI
- Vertical thin-film on SOI

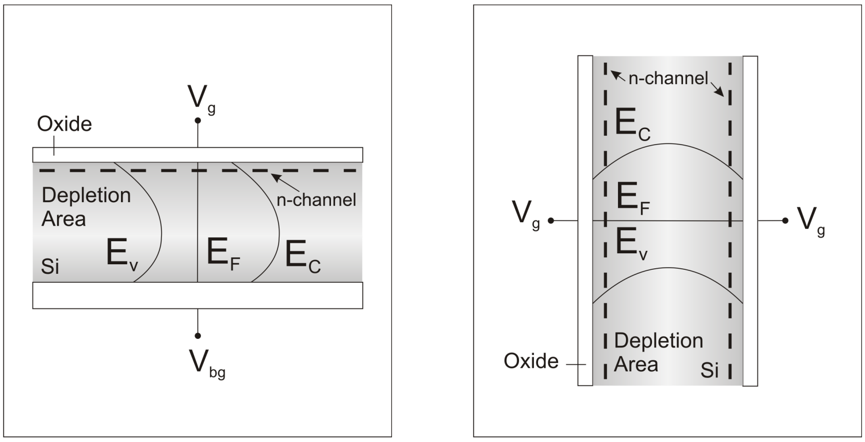
The SOI condition is assumed to be valid also for Si-bulk where a local insulation has been performed, as it has been done in the FinFET fabrication process presented in Chap. 3. The only difference may rise at the junction level that, in the case of SOI, they are completely separated from the bulk, while for the local SOI are still connected.

For a standard *bulk* device (Fig. 1.2a), the depletion zone (the region where the charge carriers



(a) Bulk

(b) Thick-film



(c) Thin-film

(d) FinFET

Figure 1.2: Distinction between bulk, thick- and thin-film: band diagram with depletion regions in a bulk (a), a thick-film (b), a thin-film with back-gate (c) and a FinFET (d).

have been repulsed away from the gate electric field) extends from the Si-Oxide interface to a maximum depletion width given by:

$$x_{dmax} = \sqrt{\frac{4\varepsilon_{Si}\phi_F}{qN_A}} \tag{1.1}$$

where ε_{Si} is the silicon dielectric constant, ϕ_F is the Fermi potential, N_A the channel doping and q the elementary charge. The Fermi potential ϕ_F for p-type silicon is given by:

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{1.2}$$

where k is the Boltzmann constant, T the temperature and n_i the intrinsic carrier concentration of silicon. The potential outside the depletion regions becomes linear in the bulk, known as body, characterized by a neutral space charge distribution.

For a *thick film*, the back-gate is biased to create another depleted (or accumulated) region. The silicon thickness becomes comparable to x_{dmax}, but the depleted regions are still divided by a portion of neutral silicon (Fig. 1.2b). Such a condition is defined **partial depletion** (PD). When the two depleted regions start to interact, i.e. x_{dmax} has become larger than the silicon film, the condition of **full depletion** (FD) applies and the device is referred to as *thin-film* (Fig. 1.2c). If the structure is rotated by 90° and a common gate controls the conduction on the vertical channels, the potential distribution is directly symmetric, which is the case for FinFETs (Fig. 1.2d). Moreover, for vertical structures the use of a back-gate is less needed, since almost the whole surface of the vertical structure is controlled by the front gate.

As for bulk MOSFET (Fig. 1.3a), the potential distribution $\Phi(x, y, z)$ inside the FinFET channel can be obtained by solving the Poisson's equation using the depletion approximation:

$$\frac{d^2\Phi(x,y,z)}{dx^2} + \frac{d^2\Phi(x,y,z)}{dy^2} + \frac{d^2\Phi(x,y,z)}{dz^2} = \frac{qN_a}{\varepsilon_{Si}} \tag{1.3}$$

For a double-gate device, $\frac{d\Phi}{dz} = 0$ [3], and the Poisson's equation becomes:

$$\frac{d^2\Phi(x,y)}{dx^2} + \frac{d^2\Phi(x,y)}{dy^2} = \frac{qN_a}{\varepsilon_{Si}} \tag{1.4}$$

An approximate solution of Eq. 1.4 can be found by assuming a parabolic potential distribution in the y-direction [7]. However, a more detailed solution should take into account the top gate of a FinFET as reported in [8], where a complex 3D analytical solution of the Poisson's equation is proposed, comparing the results to numerical solutions.

It is also worth mentioning how the threshold voltage V_{th} of a FinFET can be modified from the MOSFET equivalent one. The V_{th} is usually defined as the voltage at which strong inversion occurs. For a MOSFET it is expressed by [9]:

$$V_{th} = V_{FB} + 2\phi_F + \frac{qN_A x_{dmax}}{C_{ox}} \tag{1.5}$$

where V_{FB} is the flatband voltage equal to the workfunction difference between metal and silicon, $\phi_M - \phi_{Si}$, and C_{ox} is the gate capacitance per unit area (surface and oxide charges are neglected). The term $qN_A x_{dmax}$ represents the depletion charge Q_D.
In a fully depleted FinFET, Q_D is constant and it becomes [3]:

$$Q_{D_{Fin}} = q\frac{1}{2}T_{Fin}N_A \tag{1.6}$$

The above expression is valid as long as the thickness of the inversion layer is small with respect to the silicon film thickness. Also, for ultra-thin devices ($T_{Fin} \approx 10\,\mathrm{nm}$) more complex interactions should be taken into account, especially volume inversion [10].
The final gate and threshold voltage can then be expressed as:

$$V_g = \phi_S + V_{FB} + \frac{Q_{D_{Fin}}}{C_{ox}} \tag{1.7}$$

and, at threshold,

$$V_{th} = 2\phi_f + V_{FB} + \frac{Q_{D_{Fin}}}{C_{ox}} \tag{1.8}$$

where ϕ_S is the surface potential equal to $2\phi_f$ in strong inversion.
For pH sensing applications, the theoretical definition of V_{th} will not be used. The threshold voltage will be arbitrarily defined at constant I_{th} (Sec. 5.2.2), thus the use of Eq. 1.7 instead of Eq. 1.8 is more consistent.

1.1.2 Subthreshold slope for thin-film FETs

One of the most well-known feature of a FET device is the semi-logarithmic plot of the drain current I_d as a function of the gate voltage V_g, called $I_d(V_g)$ transfer characteristic, as illustrated in Fig. 1.3b. For $V_g < V_{th}$, one can define the subthreshold region, a region of particular interest for sensing applications. An explicit expression for the I_d in the subthreshold region for a double-gate thin-film is provided in [11]:

$$I_d = \frac{W}{L}\mu_n 4C_{Si}\left(\frac{kT}{q}\right)^2 (1 - e^{(-q/kT)(Q_D/8C_{Si})}) \cdot [1 - e^{-(qV_{ds}/kT)}] \cdot e^{q/kT(V_g - V_{FB} - [(Q_D/2)/C_{ox}] - 2\phi_f)} \tag{1.9}$$

where μ_n is the electron mobility, $C_{Si} = \epsilon_{Si}/t_{Si}$ is the capacitance per unit area associated to the silicon film, V_{ds} and V_g the voltage at the drain and gate contacts. The variation of the I_d current according to V_g in the subthreshold region is expressed by the subthreshold slope (inverse or the real slope of $I_d(V_g)$), defined as:

$$SS = \frac{\delta V_g}{\delta(log I_d)} = \frac{\delta V_g}{\delta \Phi_S} \cdot \frac{\delta \Phi_S}{\delta(log I_d)} \tag{1.10}$$

where $\frac{\delta V_g}{\delta \phi_S}$ is called body m-factor and it describes the coupling between the gate and the surface potential, while $\frac{\delta \phi_S}{\delta(log I_d)}$, known as n-factor is limited to a minimum value according to the Fermi-Dirac distribution. For a bulk MOSFET the subthreshold slope can further be expressed as:

$$SS = n \cdot m = \frac{kT}{q} \ln(10) \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) = 59 \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \mathrm{mV/dec} \tag{1.11}$$

where C_D and C_{it} are the capacitances associated to the depletion region and the interface trap states, respectively. The subthreshold slope is constant and independent from the drain and gate voltage. An ideal FET device has a subthreshold slope of SS_0 =59 mV/dec at room temperature (300 K). The full-depletion condition allows thin-film to get closer to the ideal value. In first approximation, the variation of the depletion charge with the front gate is, in fact, $\delta Q_D / \delta V_g = 0$, meaning that $C_D \approx 0$ and the subthreshold slope approaches its theoretical limit [12] with $m = 1$:

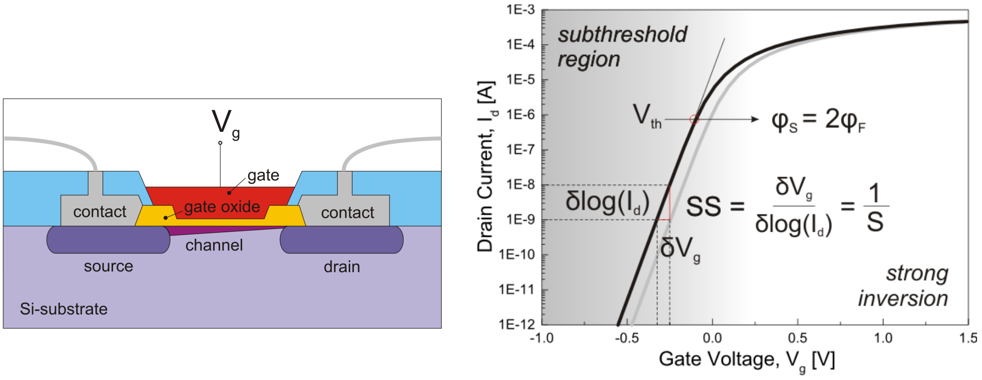
$$SS \cong \frac{kT}{q} \ln(10) \equiv SS_0 \tag{1.12}$$

which is valid for small thicknesses ($t_{Si} < x_{dmax}$) [5] and neglecting the interface traps. Under scaling, the subthreshold slope of a thin-film device with the same parameters of a bulk device or thick-film will be steeper. In turns, in the subthreshold regime any variation of gate voltage δV_g is perfectly coupled to the surface potential ϕ_S, giving rise to an equal increase. In a real device, the theoretical limit is never reached due to the presence of traps at the Si-Oxide interface.

In [13], the subthreshold slope limit is derived starting from the Fermi-Dirac distribution which describes the distribution of particles (fermions) obeying the Pauli exclusion principle. In the next section, Sec. 1.2, dedicated to the ISFET, an equivalent limit will be introduced for the change of surface potential caused by the variation of charge in an electrolyte solution.

1.2 Ion Sensitive Field Effect Transistor

Ion Sensitive Field Effect Transistors (ISFET) were first developed in the 1970s, as an alternative to the glass electrodes for pH and ion measurements. In comparison to a MOSFET, the gate electrode is replaced by a reference electrode immersed in an aqueous solution in contact



(a) MOSFET (b) $I_d(V_g)$

Figure 1.3: (a) Cross-section of a planar MOSFET and (b) $I_d(V_g)$ characteristic for a thin-film with t_{Si}=100 nm and definition of subthreshold slope.

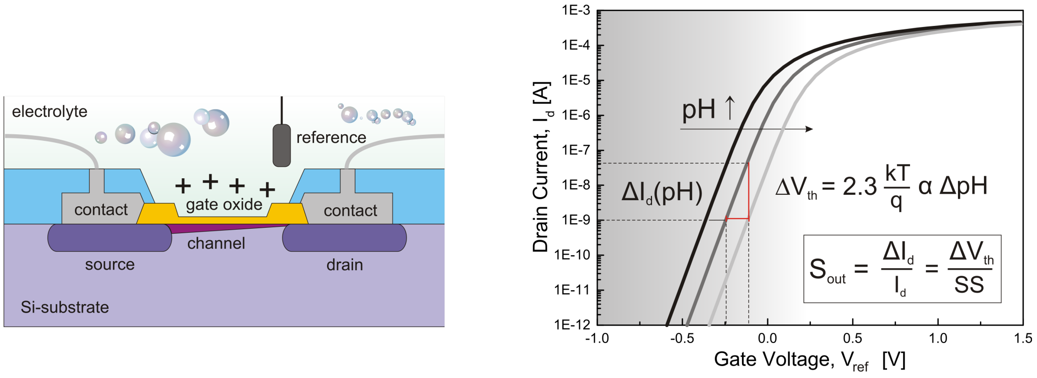
with the gate oxide, as illustrated in Fig. 1.4a. The potential at the silicon surface is then function of the reference electrode and the amount of charges present in the solution as long as their contribution is not negligible at the ISFET surface. With respect to Eq. 1.7, additional contributions should be considered [14]:

$$V_g = E_{ref} - \Psi + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_D}{C_{ox}} + \phi_S \tag{1.13}$$

and, at threshold,

$$V_{th} = E_{ref} - \Psi + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_D}{C_{ox}} + 2\phi_f \tag{1.14}$$

where E_{ref} is the potential of the reference electrode, Ψ is the chemical potential at the solution-oxide interface, χ^{sol} is the surface dipole potential of the solvent (usually constant), Φ_{Si} is the work function of the silicon which has been separated from the Φ_M of the metal gate now included in E_{ref} and ϕ_S is the surface potential at the Si-Oxide interface which will finally determine the $I_d(V_g)$ transfer characteristics, always according to Eq. 1.9 for a double-gate thin-film. It is important to notice that Ψ and ϕ_S are both surface potentials but they refer to two different interfaces in series. Any chemical variation in the solution modifies Ψ, which in the case of pH can be expressed as $\Psi(pH)$, but it can depend on any other electrical charges related to other ions or biological entities (DNA, proteins). The contribution of Ψ is linearly added to ϕ_S, meaning that the electronic properties of the FET expressed by the $I_d(V_{ref})$ relation are not modulated by Ψ but only shifted by a $\Delta\Psi$. Viceversa, $\Delta\Psi$ is independent from the electronic and geometrical properties of the FET and it is exclusively controlled by the surface chemistry of the gate oxide. As illustrated in Fig. 1.4b, a change in Ψ will result in a change of the ISFET threshold voltage ΔV_{th}, which can be measured by sweeping the reference electrode or by monitoring the I_d value at fixed V_{ref} value.



(a) ISFET

(b) $I_d(V_{ref})$

Figure 1.4: (a) Cross-section of a planar ISFET and (b) $I_d(V_{ref})$ characteristic for a thin-film with t_{Si}=100 nm and definition of threshold voltage variation, ΔV_{th}, and readout sensitivity, S_{out}.

1.2.1 The Nernst limit in pH sensing applications

It has been mentioned that a $\Delta\Psi$ occurs at the ISFET surface due to a chemical modification in the bulk solution if such a variation is transduced from the solution to the gate oxide surface. Such a modification can be related to any chemical or biological species containing a certain amount of charge able to reach the sensor surface. The modification of the pH in a solution is the most straightforward experiment because the gate oxide does not need any functionalization and it can be continuously repeated. The pH is a measure of the acidity or basicity of an aqueous solution and it is equal to:

$$pH = -\log_{10}(a_{H^+}) = log_{10}\left(\frac{1}{a_{H^+}}\right) \tag{1.15}$$

where a_{H^+} is the activity, or effective concentration, of H^+. The relation between $\Delta\Psi$ and the change of pH is established by:

$$|\Delta\Psi(pH)| = \frac{\ln(10)kT}{q}\alpha\cdot\Delta pH_B \longrightarrow \alpha\cdot 59mV/pH \tag{1.16}$$

with

$$\alpha = \frac{\beta}{\beta+1} \tag{1.17}$$

where β symbolises the surface buffer capacitance (Sec.1.4.2) and ΔpH_B is the pH change in the bulk solution. Eq. 1.16 is usually referred to as Nernst equation or Nernst limit. This relation derives from the proton concentration difference caused by the potential between the bulk solution of the oxide surface [15, 16]. According to Boltzmann statistics that can be used as approximation to Fermi-Dirac statistics in the classical regime, the proton concentration is:

$$a_{H_S^+} = a_{H_B^+} exp \frac{-q\Psi_0}{kT} \tag{1.18}$$

or

$$pH_S = pH_B + \frac{q\Psi_0}{(2.3kT)} \tag{1.19}$$

where S and B denote surface and bulk. In turns, such potential difference arises from the surface reactions occurring at the oxide surface necessary to reach the electrochemical equilibrium. Specific surface sites, called amphoteric sites, are responsible for the chemical reactions. According to their density, specific for each oxide, the parameter α will approach the unit. Assuming oxides with $\alpha = 1$, Eq. 1.16 shows its maximum Nernstian sensitivity reaching 59 mV/pH, while for oxides having $\alpha < 1$, a sub-Nernstian response is expected. Only an ideal coupling between the solution and the device through the sensing oxide, expressed by α, can guarantee the maximum change in the solution to be transduced to the device and being read out in terms of threshold voltage variation ΔV_{th}.

Equations 1.16, 1.18 and 1.19 have been derived specifically for pH, but the Nernst equation actually refers to a more general relation between the potential and the Gibbs free energy ΔG of the overall reaction [17], as the Boltzmann statistics applies for general material particles. The Nernst limit also applies for all types of ions as Na, Cl, K, through $pK_a = -\log_{10} K_a$ instead of the pH, where K_a is the acid dissociation constant.

In Tab. 1.3 many works based on SiNWs related to both pH and salt sensing applications are reported.

1.2.2 Fundamental models of the EOS interface

This section cites the fundamental models that followed one another in history, modelling the extremely complex Electrolyte-Oxide-Silicon (EOS) system. When an object (metals, alloys, semiconductors, insulators) is immersed in an electrolyte, a potential is set up across the two phases, at the object/electrolyte interface. The more common terminology in electrochemistry is that a double layer is set up at the interface. All models aim at the description of this Electrical Double Layer (EDL) [18]:

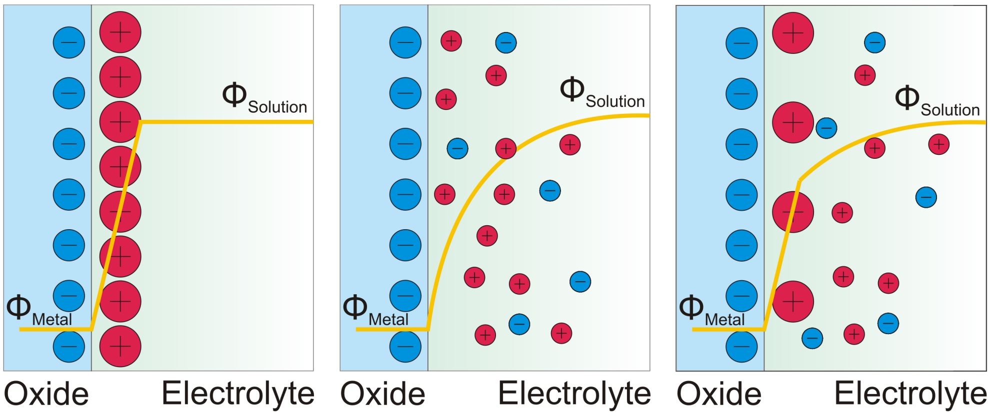
- **Helmholtz**: The earliest model of the EDL is usually attributed to Helmholtz, who mathematically treated the EDL as a capacitor. In this model, a single layer of ions, known as the *surface charge layer*, is adsorbed at the surface of an object, as illustrated in Fig. 1.5a. The remaining counterions in the bulk solution do not contribute to the potential difference $\Phi_{surface} - \Phi_{solution} = Q/C$ and the surface charge potential is linearly dissipated from the surface to the bulk.
- **Gouy-Chapman**: Gouy and Chapman proposed independently the idea of a *diffuse dou-*

ble layer [15, 19] to interpret the capacitive behaviour of a surface/electrolyte interface. The solution contains an excess of charge which is equal in value to that on the solid state surface but, due to their large-radius, a single layer of these charges will not be enough to screen the electric field. The ions in the solution are therefore electrostatically attracted, but the attraction is weak and counteracted by the random thermal motion. This finite width of charges gives rise to an exponential electrostatic potential drop within this layer as shown in Fig. 1.5b. However, this model considers the ions as point charges. As a consequence, it overestimates the capacitance, causing unrealistic high concentrations of ions near the surface.

- **Stern**: Stern [20] provided an adjustment to the previous model, introducing the concept that ions cannot approach the surface closer than their ionic radius. Such a distance has been called the Outer Helmoltz Plane (OHP) [21]. Close to the surface an ion depletion region gives rise to a constant capacitance, known as Stern capacitance with typical value of 20 µF cm^{-2} [22, 23]. The total differential capacitance is then made up of two components, the Stern and diffuse layer contributions in series:

$$C_{DL} = \frac{C_{dif}C_{Stern}}{C_{dif} + C_{Stern}} \tag{1.20}$$

where C_{dif} is mainly determined by the ionic strength.



(a) Helmoltz (b) Gouy-Chapman (c) Stern

Figure 1.5: Illustrative view of EOS models: (a) Helmoltz theory with large radius ions forming a surface charge layer opposite to the oxide charge layer assumed to be negative due to the presence of O^{-} groups, (b) Gouy-Chapman model (c) Stern theory with both diffusion and constant contributions.

Several other contributions to the total potential drop have also been developed [24] such as (i) specific adsorption of ions onto the surface (Gouy-Chapman-Stern-Graham model), (ii) non-specific adsorption, (iii) polarization of solvent and (iv) surface complexation. However, their effects can generally be neglected.

1.3 A common parameter for the limit of FET devices in pH sensing applications

In the previous sections, the classic physical limit that neither a MOSFET nor an ISFET can overcome has been introduced. For a MOSFET such a limit specifically translates to one decade of current, 59 mV/dec, whilst for an ISFET to one decade of H^+ concentration, 59 mV/pH. The transduction of the pH variation in the solution, ΔpH_B through the sensor surface into a surface potential change $\Delta\Phi$ is the *intrinsic sensitivity* of the sensor. Such a sensitivity can be read out by monitoring the variation of the threshold voltage of a FET, $\Delta V_{th} = \Delta\Phi$ or, alternatively, the drain current ΔI_d, at fixed V_{ref}. For the latter case, the two physical limits of the MOSFET and the ISFET can be merged together into a common parameter describing, at the same time, the quality of the surface transduction and the readout capability of the FET device. Throughout the whole thesis, this parameter will be called *readout sensitivity*, S_{out}, and it will be equal to the relative drain current variation before and after a change in the solution. The parameter S_{out} can be developed as follows:

$$S_{out} = \frac{\delta I_d}{I_d} = \frac{\delta I_d}{\delta V_g} \cdot \frac{\delta V_g}{I_d} = \frac{\delta I_d}{I_d \cdot \delta V_g} \cdot \delta V_g = \frac{\delta \ln(I_d)}{\delta V_g} \cdot \delta V_g = \frac{\delta V_g}{SS} \Rightarrow \frac{\Delta V_{th}}{SS} \tag{1.21}$$

In details:

- For a surface oxide featuring at least full coupling with $\Delta pH_B \Rightarrow \frac{\Delta V_{th}}{SS} = S_{out} \leq 1$
- For a FET device featuring at least the ideal $SS_0 \Rightarrow \frac{\Delta V_{th}}{SS} = S_{out} \leq 1$
- For a FET device with fully responsive surface oxide and ideal $SS_0 \Rightarrow \frac{\Delta V_{th}}{SS} = S_{out} = 1$

The S_{out} parameter can be defined for all types of chemical and biological sensing applications with the difference that each one of them will provide a specific ΔV_{th}, subjected to different physical principles. Moreover, S_{out} involves all the information necessary to characterize a FET sensor. The subthreshold slope includes all electronic properties of a transistor such as doping, silicon width and gate length, interface states, thickness and dielectric constant of the gate oxide. Furthermore, S_{out} can be written as:

$$S_{out} = \frac{\Delta V_{th}}{SS} = \frac{g_m}{I_d} \cdot \Delta V_{th} \cdot \ln(10) \tag{1.22}$$

where $\frac{g_m}{I_d}$ is the transcoductance-to-current ratio which is used in analog IC design [25, 26]. On the other hand, the threshold voltage variation always provides the transduction capability of the sensor surface.

1.4 High-k dielectrics

In this section, another important element of the presented work, i.e. HfO_2, is introduced. Such an oxide is part of the group of oxides called "high-k". First, the role of high-k dielectrics in microelectronics and their fabrication challenges are described. Later, the influence of different oxides on pH sensing is also discussed. Despite the fact that it is not common to talk about high-k dielectrics for pH sensing applications, it is not a coincidence that HfO_2 represents one of the best option for both fields. Commonly, the term high-k describes a bulk property, while, on the other hand, pH sensing is a surface phenomenon. A physical correlation between bulk and the surface is, indeed, traceable.

1.4.1 Advantages of high-k oxides in electronics

The increase of the calculating capacity of electronic devices has been realized with the continuous miniaturization of MOS transistors. The transistor scaling process has not only increased the package density of integrated circuits, but it also improved the circuit speed. According to Moore's law [4], the number of transistors within integrated circuits doubles approximately every two years and the Semiconductor Roadmap provides the factor scaling of each design parameter. How much the scaling can continue over time is not defined. However, the limits were envisaged to be in lithography, but it turns out that materials have also strict constraints to be taken into account. In the scaling process, the thickness of SiO_2, which has been used for more than 40 years, has shrunk to as little as five atomic layers (1.2 nm). These very thin layers brought along many disadvantages such as:

- Too high leakage current through direct tunneling, resulting in energy waste and a build-up of heat;
- Reduction of the breakdown voltage and the oxide reliability;
- Control growth and uniformity of such small thicknesses.

As a solution, new gate oxides with physically thicker layer but higher permittivity started to replace SiO_2:

$$C_{ox} = \frac{\varepsilon_0 k A}{t_{ox}} \tag{1.23}$$

where ε_0 is the vacuum permittivity, k the relative permittivity, A the capacitance area and t_{ox} the oxide thickness. Intel announced the integration of hafnium-based high-k dielectrics in conjunction with a metallic gate for the 45 nm node in 2007. However, such a replacement entails many difficulties and loss of many advantages. Indeed, the SiO_2, except when it becomes too thin, is an excellent material, with few electronic defects, excellent interface, high thermal stability and high band offset with Si. All these properties are physically and chemically connected with the low permittivity and, moving towards an higher dielectric constant, it involves losing such privileges. Moreover, the choice of a high-k oxide should take into account [27,28]:

- Enough high dielectric constant to be used for a reasonable number of years;
- Large band offset with Si (E_G is inversely proportional to ε);
- Thermodynamic and kinetic stability;
- No reaction with Si and the metal gate;
- Good interface with Si, low lattice mismatch and similar thermal expansion coefficient;
- Few electrically active defects in its bulk;
- Negligible CV hysteresis.

The static dielectric constant and the band gap of some interesting high-k dielectrics are reported in Tab. 1.1 [29]. Considering the constraints listed above, HfO_2, ZrO_2 and La_2O_3 are the most promising candidates. Al_2O_3 and Si_3N_4 provide, in fact, a too low k-value to be implemented for several years, while TiO_2 and Ta_2O_5 have a too small energy band offset with Si. La_2O_3 has a higher k-value and band offset than HfO_2, but it has been found to be highly hygroscopic, meaning that it attracts and holds water molecules from the surrounding environment. HfO_2 and ZrO_2 are very similar in their electronic structure. Zr and Hf have both 8 oxygen neighbours and each oxygen has 4 Zr/Hf neighbours. All the parameters usually used to describe an oxide are the result of this intrinsic electronic nature. Low-k oxides, as SiO_2, are in fact characterized by a prevalence of covalent bonding with a low coordination number. On the other hand, high-k are characterized by ionic bonding with high coordination number [30]. Such a difference is not only the origin of the different bulk permittivity but it has also a large impact on the concentration of defects. The SiO_2 network, in fact, is much more able to relax, to rebound dangling bonds and remove defects, providing an excellent interface with Si. Finally, the analysis of the thermodynamic stability has revealed that ZrO_2 is actually unstable and reacts with Si and Poly-Si [31], leaving HfO_2 as the preferred high-k oxide.

Table 1.1: High-k dielectrics

Oxide	K	Gap[eV]	CB offset[eV][1]
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8
Ta_2O_5	22	4.4	0.35
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
La_2O_3	30	6	2.3
TiO_2	80	3.5	0

---

[1] Conduction Band offset

1.4.2 Advantages of high-k oxides in pH sensing applications

In Sec. 1.2, the working principle of the ISFET has been introduced. It has been pointed out that the FET intrinsic sensitivity to pH depend on the chemical reaction happening on the gate oxide in contact with the electrolyte solution. Since the first applications of the ISFET, it was observed that according to different oxides a different sensitivity and linearity was observed. The sequence SiO_2, Si_3N_4, Al_2O_3 and Ta_2O_5 provides a increasing sensitivity and linearity [14]. According to most recent results, HfO_2 should be added to such sequence. The site-binding theory first developed by Yates *et al.* [32] and the site-dissociation model by Van den Berg *et al.* [23] provide a complete explanation of the correlation between the interfacial potential at the oxide-electrolyte interface and the H^+ concentration in the electrolyte. Each oxide provides on its surface a certain number of hydroxyl groups (OH), described by the surface density N_S. It can be assumed that only this type of site is present for the mentioned oxides [33]. Hydroxyl groups behave as punctual sites, where the chemical reaction takes place when the concentration of H^+ changes in the solution. Therefore, considering a general oxide with A-OH sites, each hydroxyl group can be neutral, donate (acidic reaction) or accept (basic reaction) a proton from the solution, as depicted in Fig. 1.6. The mechanism for the oxide surface is described by the site-binding model [33,34], and it is based on the principle of the achievement of the equilibrium between the surface potential Ψ_0 and and H^+ ion concentration in the bulk of the solution. The equations that describe the equilibrium between the surface OH groups and H_S^+ located near the surface are:

$$\mathrm{A{-}OH} \xrightleftharpoons{\mathrm{K_a}} \mathrm{A{-}O^-} + H_S^+ \tag{1.24}$$

$$A - OH + H_S^+ \xrightleftharpoons{\mathrm{K_b}} \mathrm{A{-}OH_2^+} \tag{1.25}$$

where K_a and K_b are the equilibrium constants.
According to the number of surface sites N_S and the surface reactivity, K_a and K_b, the same variation of pH will result in a different ΔV_{th}, specific to the type of oxide. These informations are contained in the parameter called β, already mentioned in Eq. 1.17, and it can be further defined as:

$$\beta = \frac{2q^2 N_S (K_a K_b)^{1/2}}{kTC_{DL}} \tag{1.26}$$

where C_{DL} is the differential double-layer capacitance, mainly determined by the ion concentration of the bulk solution via the corresponding Debye length [35]:

$$\lambda_D = \frac{1}{\sqrt{4\Pi l_B \Sigma_i \rho_i z_i^2}} \tag{1.27}$$

where l_B is the Bjerrum length, Σ_i is the sum over all ion species, and ρ_i and z_i are the density and valence of ion species. The Debye length represents the length scale beyond which charges are electrically screened, due to the exponential decay of the electrostatic potential. In the experiments, λ_D and C_{DL} are minimized by keeping the solution ionic strength to a low value. However, for H^+ and salts, being very close to the oxide surface, it rarely represents an obstacle, while for biological sensing, where long chain of functionalization may be needed, λ_D plays a crucial role. Assuming a reasonable ionic strength, the parameter β, associated to a specific oxide, becomes the only parameter which determines the $\Delta\Psi_(pH) = \Delta V_{th}(pH)$ relation. High values of β corresponds to higher ΔV_{th}. It has been determined that $\beta_{SiO_2} = 0.14$ and $\beta_{Al_2O_3} = 4.8$ with $N_S = 5 \times 10^{14}\,\mathrm{cm}^{-2}$ and $N_S = 8 \times 10^{14}\,\mathrm{cm}^{-2}$, respectively [19]. Upon certain conditions, an oxide expressing the Nernstian sensitivity is not sensitive to salt concentration [14, 36] assuring high linearity from one pH value to another. Table 1.2 summarizes the pH response expected from some common insulators used for ISFET together with the dielectric constants, value of ionicity and coordination number [37]. It can be noted that combining the pH response with the dielectric constant a certain order is present: the higher the dielectric constant the higher the pH response. The connection may arise from the level of ionicity, which in turn is connected to the coordination number, which expresses how many oxygen neighbours a central atom (Si, Hf) has. As previously mentioned, high-k dielectrics are characterized by a high level of ionicity I_b which at the surface will turn into a higher density of hydroxyl groups and higher pH sensitivity. Such a consideration cannot be extended for higher dielectric constant like TiO_2, since the pH response is limited by the Nernst limit while the dielectric constant does have a similar physical limit. In [38], the difference in sensitivity for the same material is commented as "due to varying oxygen content in the layers", which is in agreement with our general remark on the ionicity. The presented considerations are aimed at pointing out the connection between the bulk properties of high-k dielectrics and the surface properties of pH responsive materials. The connection of high-K to high-pH response is a good overlap in the perspective of merging modern Integrated Circuits and pH sensors. In

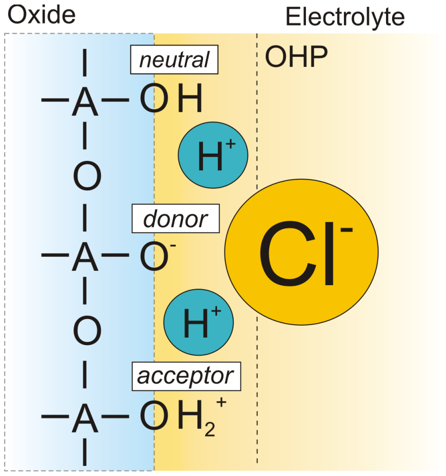


Figure 1.6: Site-dissociation model with amphoteric sites and Outer Helmoltz Plane (OHP) in evidence.

the case of Si_3N_4, a similar principle applies as explained in [39].

It is also important to notice that the pH sensitivity is not only important as quantity. The stability and linearity of the ΔV_{th} is also extremely important. In Chap. 5, non fully pH-responsive FinFETs are shown unstable and prone to time drift (Sec. 5.3.1), as it has been studied also in [36, 38]. The use of HfO_2 is therefore highly recommended for the fabrication of FinFETs due to the crossroads of the following properties: (i) fully compatibility with the scaling rules of CMOS microprocessing, (ii) highest pH response and (iii) good perspective of stability and linearity.

Table 1.2: Sensing properties of high-k dielectrics

Oxide	K	ΔV_{th} [mV/pH]	I_b	Coordination
SiO_2	3.9	35-41 [38, 40, 41]	0.45	4
Si_3N_4	7	46-55 [38, 39]	0.47	4
Al_2O_3	9	52-58 [19, 36, 38]	0.57	4 and 6
Ta_2O_5	22	56-58 [24, 42]	0.61	6 and 8
HfO_2	25	57[2]-59 [43]	0.68	8

1.5 Motivations for using FETs in sensing applications

After the first pioneering works dating back to the 70's and 80's, the implementation of nanotechnology for biological and chemical applications started to emerge again after the begin of the new century. The progress of microfabrication, the continuous miniaturization of MEMS, the evolution of the MOSFET into MG-FETs and especially the possibility to access such fields at the research level, have surely played the most important role in such an upswing.

Sensing devices are not exclusively FETs. On the contrary, many sensing applications of the last decade are based on microcantilevers [44, 45], quantum dots [46], mass spectroscopy [47, 48], atomic force microscopy [49], quartz crystal microbalance [50, 51] and surface plasmon resonance [52, 53]. Recently, carbon nanotubes have also been used for biosensing [54, 55]. Microcantilevers and mass spectroscopy are the most sensitive techniques. However, they both require the use of quite complex instrumentation or optical components in order to readout the signal. They eventually are a great instrument for overcoming new detection limits and discover new biological patterns but their integration in healthcare systems is much more a challenge with respect to FETs.

Generally, label-free sensors provides the following advantages with respect to traditional label sensing, such as ELISA (Enzyme-Linked ImmunoSorbent Assay):

- Better real-time detection;
- More direct output and less chemical interference;
- Reduced manufacturing cost;
- More single-user oriented, towards personal home point of care;

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[2] value obtained from this work

- Higher specificity and detection sensitivity.

With respect to other label-free sensors, FETs can provide the following advantages:

- Best real-time detection, only surface-binding is needed for the signal transduction;
- Cheapest manufacturing cost;
- Mechanical durability;
- Resistance to the environment;
- Reliability over time;

Moreover, a label-free n-channel fully depleted **FinFET** can be advantageous as sensor because of its high channel control which entails:

- In terms of **Performance**:
  - Steep subthreshold slope upon scaling, i.e. high readout sensitivity;
  - Stability and repeatability;
  - Noise robustness;
- In terms of **Integration**:
  - CMOS scaling compatibility;
  - Direct integration with electronic readout within monolithic CMOS chip;
  - No need of a back-gate;
  - Unique architecture for both sensors and circuit transistors;
- **Low power consumption**.

One can also mention the high Surface-to-Volume Ratio of SiNWs (S/V), as done in many general reviews [56, 57]. However, the concept of S/V should not be misinterpreted. If a metallic wire is compared to a silicon wire, the concept can be applied straightforward. The current in the first one, in fact, flows in the whole volume surrounded by its surface, while in the semiconductor the current is confined in few nm below the surface, occupying a smaller volume. Instead, in the comparison between semiconductor devices, as a planar ISFET and a SiNW, the definition of S/V becomes more subtle, since it may not be worth to talk about "volume", being the current always confined. A high S/V is a property which holds true for FET devices in general and not specifically to SiNWs.

For *ionic* sensing applications, where the charge particles are uniformly distributed in the solution, a smaller device is not expected to be intrinsically more sensitive. However, it has been mentioned how the geometry and smaller dimensions of a device improve the electronic performances. An advanced electronic device, as the FinFET, could be considered a better sensor, not because of a higher intrinsic sensitivity but for its compatibility with integration and better readout of the sensing event. For *biological applications*, where the biological entity is confined and extremely small in a large volume, the discussion is more complex. Generally, for such applications, the size of the species to be sensed being comparable to the SiNW probe represents an asset for the signal transduced to a macroscopic instrument, as shown by many excellent works (see Tab. 1.3). However, this concept may rely only on the fact that the comparison of similar signal amplitude is more convenient than its opposite and it may be contradicted by the implementation of advanced Integrated Circuits (ICs) and their functions (differential, mixing architectures).

1.5.1 State-of-the-art of SiNWs for sensing applications

In this introductive state-of-the-art two fields of classification are considered: technology and application. The electronic and sensing performances will instead be compared in Chap. 6, focusing on pH sensing, which is the main experimental application of the FinFETs. Tab. 1.3 collects the most important works related to SiNWs for sensing applications. The classification regarding the technology field is organized as follows:

- **Technology approach:**
  - Top-Down (TD): it consists in removing material from an initial substrate (e.g. silicon wafer) until structures are created;
  - Bottom-Up (BU): small items (e.g. atoms or molecules) are assembled to create a larger device.
- **Silicon substrate:**
  - Bulk: single-crystal piece cut and polished from larger single-crystal ingots;
  - SOI: it consists of two silicon pieces separated by an insulator layer (usually SiO_2).
- **Architecture:**
  - FinFET: H_{Fin}/T_{Fin} at least > 1;
  - Ribbon FET: $W_{Ribbon}/T_{Ribbon} > 1$, including trapezoidal and triangular shape where $W_{bottom} > T_{Ribbon}$;
  - ISFET: standard bulk MOSFET;
  - Trigate FET: $W_{Fin}/T_{Fin} \approx 1$;
  - GAA: circular wire.

Looking at the technology field the following remarks on the previous works can be done:

- **Technology approach**: Despite the larger number of devices fabricated according to a top-down approach, some works are also based on SiNWs produced by a bottom-down approach, which is usually based on the wire synthesization starting from molecular precursors. Despite the high quality and reduced size of the NWs, bottom-up manufacturing is not compatible with CMOS integration, which is the main focus of this work.
- **Type of substrate**: Almost the totality of the cited works are based on SiNWs fabricated on SOI substrate, since it is faster and it involves less electronic issues. Today, the choice between SOI and Bulk relies more on strategic manufacturing choices than electronic performance advantages. Providing a reliable alternative on Si-bulk to the many existing sensing devices on SOI is an important objective addressed in this thesis.
- **Architecture**: Most of the available devices are based on Ribbon-like structures, which are practical structures to be patterned on SOI substrates. As mentioned in Sec. 1.1 and

as it will be also shown by simulations in Sec. 2.1.1, FinFET may provide advantages from the electronic point of view.

Moreover, it can be pointed out that the most similar device with respect to our (FinFET on Si-bulk) is the work of Ahn *et al.* [58]. The difference is that the exploited sensing surface in [58] is only the top side of the FinFET while the body is embedded and controlled by lateral gates. As well explained in their other work [59], the independent lateral gates are used for amplification, which here it has been achieved by connection of two FinFETs (Sec. 5.3.4). The double-gate vertical FinFET structure is fully immersed in the solution and the potential is controlled exclusively by the potential in the solution.

Table 1.3: State-of-the-art of SiNWs for sensing applications: Technology and Application

Reference	Technology	Application
This work	TD, Bulk, FinFET	pH
Microsens SA [60]	TD, Bulk, ISFET	pH, ions
Abe et al. [61]	TD, Bulk, ISFET	pH, ions
Lee et al. [62]	TD, SOI Ribbon FET	pH
Park et al. [63]	TD, SOI, Ribbon FET	pH, ions
Yoo et al. [64]	TD, SOI, Ribbon FET	pH
Kim et al. [65]	TD, SOI, Trigate FET	pH
Ahn et el. [59]	TD, SOI, Trigate FET	pH
Ahn et el. [58]	TD, Bulk, Buried FinFET[3]	anti-AI
Vu et al. [40]	TD, SOI, Ribbon FET	PSS, PAH[4]
Cui et al. [66]	TD, SOI, NA	pH, ions
Tarasov et al. [36]	TD, SOI, Ribbon FET	pH, ions
Chen et al. [67]	TD, SOI, Ribbon FET	pH
Zhang et al. [68]	TD, SOI, Trigate FET	ssDNA[5]
Li et al. [69]	TD, SOI, Trigate FET	ssDNA
Hahm et al. [70]	BU, SOI, GAA	ssDNA
Stern et al. [71]	TD, SOI, Ribbon FET	pH, IgG and IgA[6]
Zheng et al. [72]	TD, SOI, NA	PSA[7]
Kim et al. [73]	TD, SOI, Ribbon FET	PSA
Li et al. [74]	BU, SOI, GAA	PSA
Wang et al. [75]	BU, SOI, GAA	ATP[8]
Zhang et al. [76]	TD, SOI, Ribbon FET	Dengue virus
Chiang et al. [77]	TD, SOI, Ribbon FET	H5N2 virus
Patolsky et al. [78]	BU, SOI, GAA	Influenza A virus

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[3] only the top side of the FinFET is exploited for sensing, the lateral sides are controlled by metallic gates

[4] Polyelectrolyte multilayers

[5] single-stranded DNA

[6] antibodies

[7] cancer marker

[8] Adenosine triphosphate

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2 TCAD Simulations for the Design and Integration of FinFETs

In this chapter, FEA and SPICE simulations are used for the optimization of the FinFET parameters and to identify advantageous circuit connections of two or more FinFETs. The term TCAD stands for Technology Computer Aided Design, which groups softwares modelling device fabrication (Process TCAD) and operation (Device TCAD). TCAD may also include the creation of compact models, which are mathematical equations of semiconductor devices used in analog circuit simulators, as SPICE, meaning Simulation Program with Integrated Circuit Emphasis. However, SPICE is usually considered as part of EDA, Electronic Design Automation, rather than TCAD. SPICE is, in fact, based on analytical expressions, while TCAD is commonly based on FEA, Finite Element Analysis, which is a numerical technique for finding approximate solutions of differential equations.

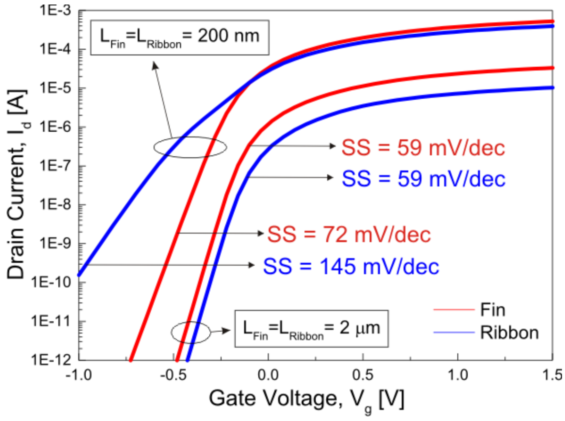
2.1 FinFET design considerations by FEA TCAD simulations

FEA simulations have provided valuable guidelines for the definition of the first fabricated devices. In the first part of this section, a FinFET is compared to a Nanoribbon under scaling conditions. In the second one, a partially gated FinFET is simulated according to different electronic parameters. FEA simulations have also been used for the fabrication process, as it will be described in Chap. 3.

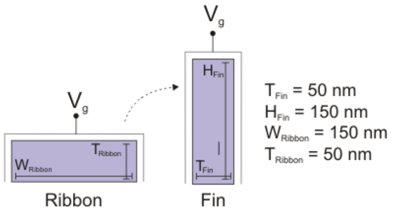
2.1.1 Scalability of FinFETs versus Nanoribbons

In Chap. 1, the advantages of FinFETs in terms of channel control have been discussed. Many works based on ribbon-like structures for sensing applications have also been cited. In Fig. 2.1b a Ribbon and a Fin are defined according to their typical features. A Ribbon is usually defined by a width W_{Ribbon}, on the horizontal direction, and by a thickness T_{Ribbon} on the vertical direction. A Fin is defined, in this work, according to its thickness T_{Fin} on the horizontal plane and height H_{Fin} on the vertical one. For both, thickness is related to the smallest dimension. The following dimensions: $T_{Ribbon} = 50\,\text{nm}$, $W_{Ribbon} = 150\,\text{nm}$, $T_{Fin} = 50\,\text{nm}$ and

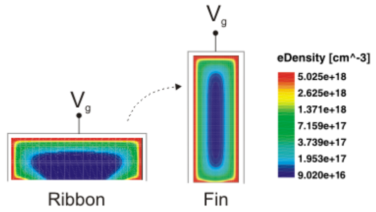
$H_{Fin} = 150\,\text{nm}$ were considered for assuring a condition of full-depletion of both devices [1]. The two devices were simulated by a FEA software (Sentaurus Device, Synopsys 2009.C). The parameters set in the simulations were: a low level of doping of the p-type channel, i.e. $N_A = 10^{16}\,\text{cm}^{-3}$ (boron), high level for source and drain $N_D = 10^{20}\,\text{cm}^{-3}$ (phosphorus) and thin SiO_2 layer, $t_{SiO_2} = 5\,\text{nm}$. Moreover, for both devices a length of $L_{Fin} = 2\,\mu\text{m}$ was defined. Considering these parameters, combined with the fully-depletion condition, both SiNWs reached the maximum ideal subthreshold slope $SS = 59\,\text{mV/dec}$, as shown in Fig. 2.1a.



(a) $I_d(V_g)$ for a Fin and a Ribbon



(b) Structure



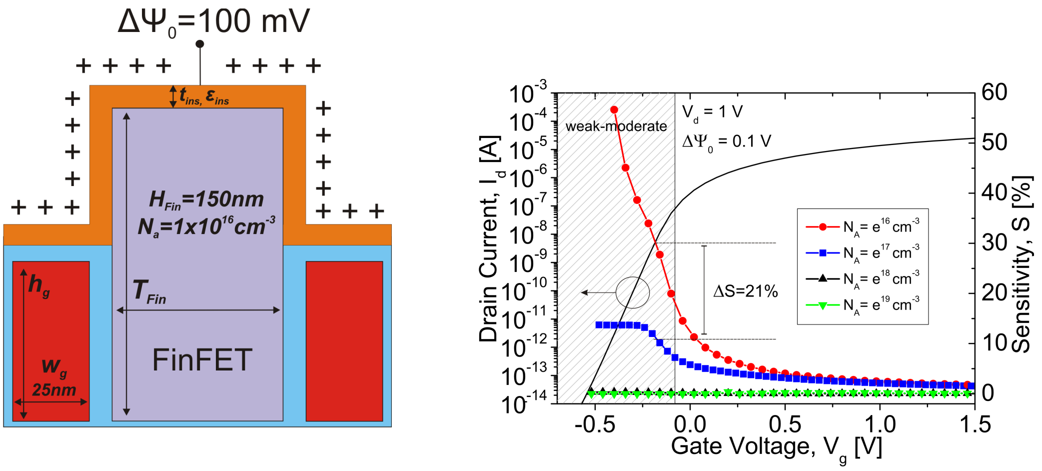
(c) Electronic density

Figure 2.1: Scalability of Fin versus Ribbon: (a) simulated $I_d(V_g)$ when their L_{Fin} and L_{Ribbon} are scaled down from $2\,\mu\text{m}$ to 200 nm and subthreshold slope values; (b) geometrical dimensions and (c) electronic density for the simulated Fin and Ribbon.

Later, the length of the Fin and the Ribbon was reduced. As previously introduced, reducing the distance between source and drain implies a degradation of the FET performances. When L_{Fin} approaches 500 nm, the effect on the subthreshold slope starts to be visible and at $L_{Fin} = 200\,\text{nm}$ it has worsened to $SS = 145\,\text{mV/dec}$ for the Ribbon and $SS = 75\,\text{mV/dec}$ for the Fin, as it is possible to see in Fig. 2.1a. This example shows how the FinFET properties are better preserved as the device features are scaled down, while other devices encounter higher performance degradation due to their architecture. Figure 2.1c shows a cross-section of both devices with a color gradient indicating the electronic density. The devices are considered not suspended, meaning that the bottom side is in contact with an isolated floating surface (e.g. the SiO_2 BOX for SOI wafers). In the Fin structure, the higher electron density, responsible for the conduction, is almost surrounding the whole Fin perimeter while for the Ribbon it is clear that the bottom has a charge density almost two orders of magnitude lower. Such a potential distribution is what causes the degradation of the Ribbon when the channel potential approaches the potential applied at the source and drain. On the other hand, the potential in the Fin channel acts as a shield. In case of suspended structure devices (Gate-All-Around, GAA), the potential distribution would be the same. The application of a back-gate potential could also provide more similar charge density in the compared devices, but such a potential should be compliant with the integration of other transistors and with power constraints. The parameters used for the Fin are considered valuable to be implemented in the fabrication process, since they can provide the steepest subthreshold swing and they are reasonable from the fabrication point of view. The only dimension that is not taken into account is $L_{Fin} = 2\,\mu\text{m}$. Other electronic parameters have been investigated in the next section.

2.1.2 Hybrid partially gated FinFET

FEA simulations have also been performed on a partially gated structure [2], as illustrated in Fig. 2.2a. The structure consists of a FinFET with two vertical N+ Poly-Si side-gates, a p-type Si body, N+ source and drain and an insulator top layer. The top part of the device is exposed to the environment, while the bottom part is embedded. For its double function, this FinFET can be defined "hybrid". This architecture can be used as a more compact circuit element where a sensor and a driver transistor are used together for achieving specific circuit functions. The top part of the architecture is used as sensor while the bottom as standard transistor. The two components work in parallel, as it will be demonstrated in Sec. 2.2.1. For such reason, the parameters analyzed here are also valid considering the Fin sensor independently for the bottom part.



(a) (b)

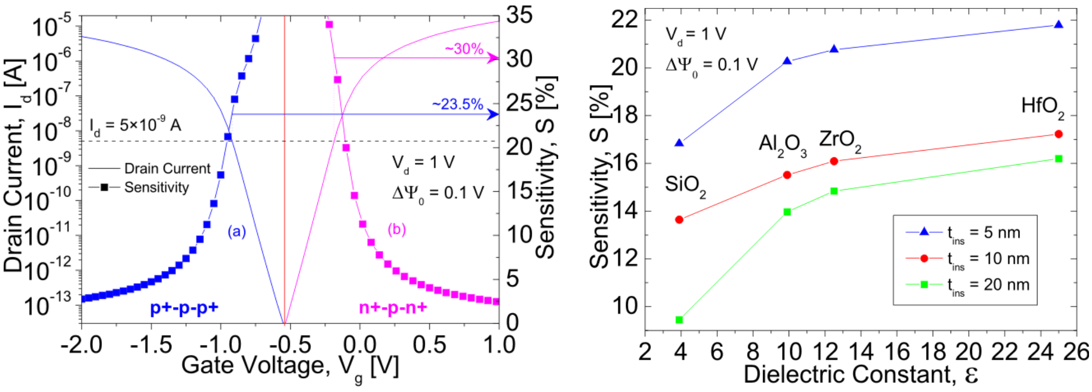
Figure 2.2: FEA simulation of a partially gated FinFET: (a) cross-section of the structure; (b) simulated $I_d(V_g)$ and sensitivity for different channel doping values.

The body of the device is fully depleted with the same geometrical dimensions defined in the previous section, i.e. $T_{Fin} = 50\,\text{nm}$ and $H_{Fin} = 150\,\text{nm}$. The sensing environment is modeled by an external potential, $\Delta\Psi_0 = 100\,\text{mV}$, applied on the top surface and the reference potential is set to $V_{ref} = 0\,\text{V}$. The gate voltage was swept between $V_g = -0.5\,\text{V}$ and $V_g = 1.5\,\text{V}$ at $V_d = 1\,\text{V}$. With this choice of electrodes, the current at the drain I_d is iteratively computed by solving the Poisson's equation through out the wire cross-section. A doping and transverse field dependent mobility model was used. The readout sensitivity is defined as the relative variation of current due to the difference of external potential, $\Delta I_d / I_{d0}$ where I_{d0} is the current before applying the potential shift. The $I_d(V_g)$ transfer characteristic of the hybrid device is plotted in Fig. 2.2b on the left y-axis, while on the right y-axis the sensitivity is plotted according to different channel doping concentration, for $10^{16}\,\mathrm{cm}^{-3} < N_A < 10^{19}\,\mathrm{cm}^{-3}$. The FinFET response is not negligible only for $N_A = 10^{16}\,\mathrm{cm}^{-3}$ and $N_A = 10^{17}\,\mathrm{cm}^{-3}$, with an improvement $\Delta S = 21\%$ for the lower doping value. Since the subthreshold slope becomes less step with increasing the doping concentration, it is expected to observe a drop in the sensitivity. This confirms $N_A = 10^{16}\,\mathrm{cm}^{-3}$ to be a good choice for the fabricated device. However, as it will be presented in Sec. 5.1.1, a higher doping will result better, since the bulk (which could not be simulated here) will result to be too leaky and not controllable for such doping. Low doping concentrations and subthreshold regime have already been indicated as optimal conditions for high response [3], but it is important to point out that this is strictly connected to the FET subthreshold slope.

A p-MOS transistor was compared to an n-MOS transistor. For the last one, the sensitivity improves of $\Delta S = 6.5\%$, as reported in Fig. 2.3a. As previously mentioned, this is again connected to the improvement of the subthreshold slope. It has been reported, in fact, that a n+-p-n+ device has lower subthreshold swing values compared to an equivalent p+-p-p+ device [4]. Based on the simple concept of capacitance, $\delta Q / \delta V = \varepsilon_{ins} / t_{ins}$, the effect of the top insulating layer on the readout sensitivity was also simulated. Different simulations were performed reducing the thickness and increasing the permittivity of the insulator which separates the FinFET from the external environment. The best response was reached for 5 nm of HfO_2, as shown in Fig. 2.3b. This is in agreement with the choice of a fully-responsive oxide for the highest ΔV_{th}. Finally, grouping the best geometrical and electronic properties, the sensor output can be estimated for different external potentials, each of them associated to a specific chemical or biological type of sensing [5]. Cancer markers, as prostate-specific antigen (PSA), or proteins in general, are ones of the less charged biological entities. On the other hand, DNA strands contain a large number of electrons, resulting in a relevant threshold voltage shift.

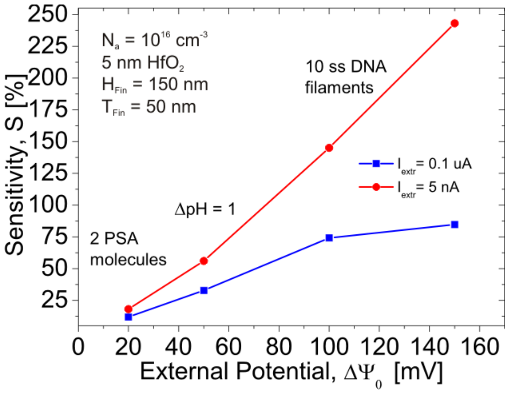
2.2 Low power sensing circuits by EDA simulations

This section presents different circuit architectures that combine sensing and signal readout functions [6]. The basic building block is the FinFET, as previously introduced, implemented both as sensor and metal gate transistor. The hybrid partially gated FinFET is proposed as a compact device enabling the integration of digital gates with biosensing capabilities. In order to explore different designs through Electronic Design Automation (EDA) simulations, each device has been modeled using equations written in Verilog-A. An important, yet neglected issue is, in fact, an efficient readout of the sensor output signal, which is normally rather weak and noisy. Sensors are typically individually addressed. Few complex readout circuits, fabricated in CMOS technology, have been previously proposed [7] and used [8], but mostly for planar ion-sensitive FETs (ISFETs). These complex circuits, however, have usually been



(a) Accumulation versus enhancement FET

(b) Gate oxide impact



(c) Current level impact

Figure 2.3: FEA simulations for a partially gated FinFET: (a) comparison between a n+-p-n+ and p+-p-p+ FinFET; (b) impact of the gate oxide on the sensitivity; (c) impact of the current level for different type of sensing applications.

developed independently from the sensors and are externally connected to the sensing units, limiting the potential performance of the overall sensing system. The approach of integrating both, the sensor and readout circuits on the same substrate, is here explored, taking into account the constrains of low power consumption. All proposed topologies in this section rely only on n-channel FinFETs.

2.2.1 From 3D FEA to 2D device analytical models

The sensing circuits are composed of three different FinFET-based electronic units as illustrated in Fig. 2.4: a sensor (1A), a transistor with surrounding metal gate (2A) and a partially gated transistor, with its top surface exposed to the liquid and the bottom driver transistor with a embedded metal gates (3A). The first row of Fig. 2.4 shows a 3D sketch of the three devices, whereas the second row shows the 2D cross-section perpendicular to the y-coordinate. The three devices are all fully depleted and can be modeled as symmetric FinFETs: V_{ref} is the voltage applied to the liquid solution through a reference electrode, V_{liq} is the total potential applied to the liquid including the ionic potential and V_g is the gate voltage for the transistor with metal gate. Each device was previously simulated using three-dimensional FEA simulations. Herein, Verilog-A models for the DG-MOSFET [9] have been modified and calibrated to match the previous simulations.

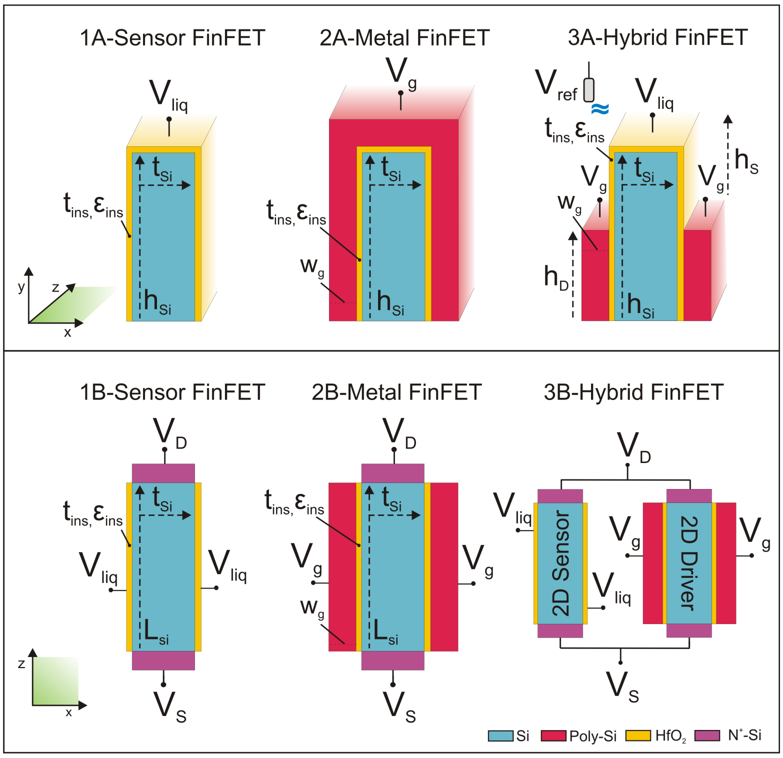


Figure 2.4: A) Fin cross-sections of the 3D devices: (1A) liquid gate sensing FinFET, (2A) metal gate DG-FinFET, (3A) FinFET sensor with embedded transistor; B) cross-sections perpendicular to the z-direction for the 2D equivalent structures (1B, 2B, 3B).

The electrical behavior of a MOSFET can be described according to the parabolic potential approximation simplifying the geometry from three to two dimensions [1]. For the devices 1A and 2A, the three dimensional structure can be easily reduced to a two dimensional equivalent by assuming the electric field along the y-direction to be uniform and then multiplying the output current, I_d, by the device height, h_{Si}. The total height is calculated as the sum of the real device height plus half of the top surface, t_{Si}. On the other hand, the electric field along the y-direction of the device in Fig. 2.4 (3A) is not uniform and it is controlled by two independent gate voltages (i.e., the top sensing part exposed to the liquid and the bottom driving part with a metal gate). Device 3A is then treated as a parallel combination of its two components. Such approximation allows each part to be reduced to a two-dimensional structure with independent gates, V_g and V_{liq}, and the output current is multiplied by the height of the driving transistor and the sensor, respectively. This evaluation can also be applied to other sensors that incorporate both, a sensing and a biasing or driving part. The demonstrations of

these assumptions will follow in the next sections.
The impact of including the top corners in the total device height was first verified. The new height, h^*_{Si} is:

$$h^*_{Si} = h_{Si} + 0.5 \cdot t_{Si} \tag{2.1}$$

as shown in the equivalences of Fig. 2.5

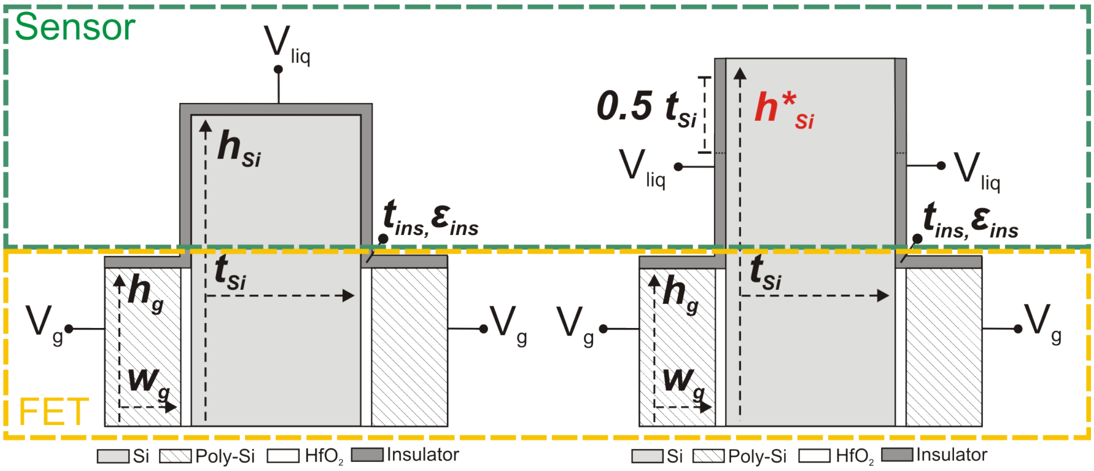


Figure 2.5: Fin cross-section of the 3D original hybrid FinFET structure (left) and cross-section of the device with top corners included in the total height (right).

Being the device 3A the more complex, it is the one described in details. Taking into account that the FinFET sensor is its top part and the FinFET transistor its bottom part, the results can be applied, respectively, to the two independents components 1A and 2A. Additionally, without applying a pH-dependent potential, V_{liq} and V_g correspond to one another and they can both be referred to as V_g. Figures 2.6a and 2.6b shows that the simplification concerning the top corners is valid. Looking at the $I_d(V_g)$ characteristics of Fig. 2.6a, an average current variation of only 5% in the subthreshold region is observed between the structures with and without top corners. In the saturation region, the difference increases to 10%. The measurements will be conducted by biasing the devices in the subthreshold region, making even more reasonable the approximation. A similar result was obtained with the $I_d(V_d)$ characteristics (Fig. 2.6b) where a mismatch of about 15% was observed at $V_g = 1.5$ V. The top corners play then a significant role only for a high level of inversion. With this approximation, all structures can be modeled by 2D equations, with two remaining variables, t_{Si} and l_{Si}. The total current was calculated in function of the total gate height h_{Si}, independently from the FinFET being a sensor or a drive transistor. For the hybrid device, the two regions, the sensing top part and the driver bottom one, can be considered independent and their current contributions can be added as for two parallel devices, as shown in Fig. 2.6c. This evaluation can also be applied to other sensors that incorporate both a sensing and an embedded driving part.
After verification of the correspondence between structures A e B of Fig. 2.4, the equivalence

Table 2.1: FinFET parameters implemented in analytical models as reported in [9]

		Default value
Design parameters		
L	Channel length	1E-4 cm
W	Channel width	15E-6 cm
TS	Channel thickness	50E-7 cm
TOX	Oxide thickness	5E-7 cm
TPOLY	Poly-Si thickness	35E-7 cm
Technological parameters		
EPOX	Oxide dielectric constant	22E-13 cm^{-2}
NSS	Interface charge density	0
NA	Channel doping concentration	5E16 cm^{-3}
GT	Material gate	1 (poly gate)
Fitting parameters		
M0	Maximum mobility	1800 cm^2/Vs
E1	Critical field-phonons	5E6 V/cm
E2V	Critical field roughness	5E7 V/cm
VSAT	Saturation velocity	0.9E7 cm/s

between the outputs of the 3D FEA simulations, generated by Sentaurus, and the 2D simulations, generated by Virtuoso, should be proven. Each components, in fact, can be simulated by the Verilog-A code proposed in [9], based on a model for symmetric DG-MOSFETs. The blue curve in Fig. 2.7a shows the first $I_d(V_g)$ characteristic obtained by the implementation of the Verilog-A code when only geometrical parameters were modified. It is evident that it is necessary to go further in the modification to provide a good match. Table 2.1 summarizes the geometrical and fitting parameters that have been modified according to the FEA simulations. Design and technological parameters were modified according to the FinFET specifications for the fabrication process. The channel length l_{Si} is set to 1 µm for the initial matching with FEA simulations, where the channel length is limited by the available meshing points. In reality and for the next circuit simulations, this length will be 10 µm. The interface charge density N_{SS} has been set to 0 since it is not taken into account in the FEA simulations. The maximum mobility M_0 and the carrier velocity saturation V_{SAT} have been matched with the parameters extracted from Sentaurus. The fitting parameters $E1$ and $E2V$ have been modified by repeated simulations towards a good match: their values result higher with respect to [9] meaning that the surface mobility,μ_S, is overall less affected:

$$\mu_S = \frac{\mu_0}{1 + \overline{\frac{E_S}{E1}}^{P1} + \overline{\frac{E_S}{E2}}^{P2}} \tag{2.2}$$

where μ_0 is the maximum mobility value, $E1$ is the critical electric field for phonon scattering, $E2$ is the critical electric field for roughness scattering, E_S is the surface transverse electric field, $P1$ and $P2$ are exponential fitting parameters of different weight according to the most relevant contribution (phonon or surface scattering). After the proposed modifications of the fitting parameters a good mach is achieved, as shown by the red curve of Fig. 2.7a. To validate the new parameters a good match in terms of $I_d(V_d)$ is also provided, as shown in Fig. 2.7b. Upon modifications, the code described in [9] is accurate enough to simulate the FinFETs in SPICE. In order to introduce the sensing effect, it is assumed that every ionic or biological event can be described as a charge accumulation on the sensor surface, resulting in a surface potential modification and subsequently in a threshold-voltage shift with a corresponding output current change. The surface potential variation as a function of pH can be expressed as [10]:

$$\Psi(pH) = 2.3\frac{kT}{q}\alpha(pH_{pzc} - pH) \tag{2.3}$$

where, k is the Boltzmann's constant, T is the temperature, q the electrical charge, pH_{pzc} is the pH-value at the point of zero charge and α is a dimensionless sensitivity parameter that varies between 0 and 1, depending on the intrinsic buffer capacity of the oxide surface. The oxide implemented here is HfO_2, whose pH_{pzc} is 7.5, and $\alpha = 1$, since this oxide typically shows a pH response close to the Nernst limit of 59 mV/pH [11]. Equation 2.3 has been previously experimentally verified through TCAD simulations as shown in [12]. In the circuit simulations, it is implemented as a voltage generator in series with the reference electrode V_{ref}. This modeling approach is also valid for other biosensing events, as long as they can be approximated by a surface potential change. For example, proteins or DNA fragments binding to a functionalization layer on top of the sensor can induce such a surface potential change, as it has been demonstrated in [5, 13]. By introducing the additional voltage drop given by Eq. 2.3 into the Verilog-A code, the output characteristics of the FET sensor can be simulated for different pH values. In the inset of Fig. 2.8a, the $I_d(V_{ref})$ curve of the device 1A of Fig. 2.4 was simulated for different pH values. For $pH > pH_{pzc}$ the net charge on the surface is negative, reducing the absolute value of the threshold voltage, V_{th}, for an n-channel device. For $pH < pH_{pzc}$ the surface charge is positive increasing the absolute value of V_{th}.

2.2.2 A sensing common source amplifier

Based on the promising results presented above, new circuits based on the same FinFET architecture as both sensor and standard transistor have been investigated. Fig. 2.8a shows the schematic of a common-source amplifier, where the active transistor is the FinFET 1A of Fig.2.4, and where the load is implemented using a 200 kΩ resistor, R_L. Fig. 2.8a shows the output characteristics of such an amplifier. The output voltage is plotted for different pH values as a function of the voltage applied through the reference electrode, V_{ref}. When $V_{ref} < V_{th}$ the transistor has no conducting channel, $I_d \approx 0$ and, since there is no potential drop across R_L the output voltage is $V_{out} = V_{DD}$. When the input increases above V_{th}, the transistor turns on and goes into the saturation region. The output voltage is given by:

$$V_{out} = V_{DD} - I_d \cdot R_L \tag{2.4}$$

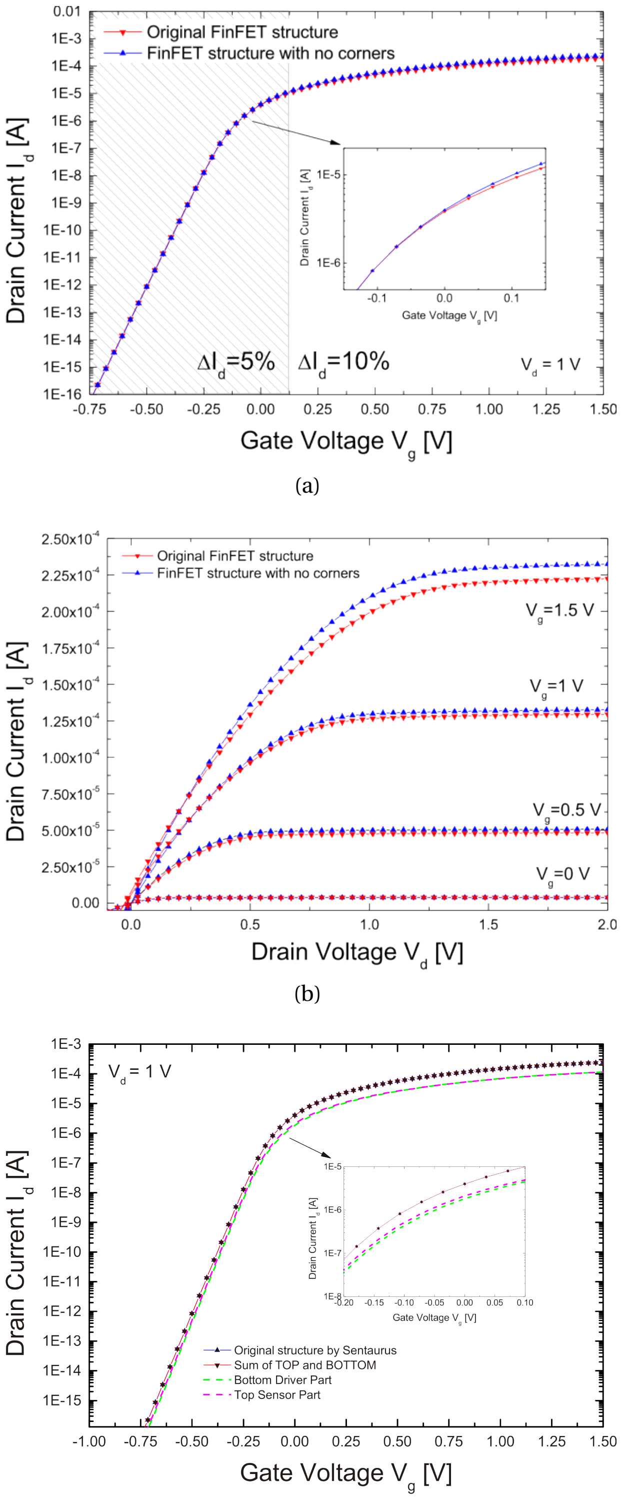
The curve $V_{out}(V_{ref})$ shift is due to the variation of the threshold voltage, ΔV_{th}, of the sensing FinFET, as previously discussed. Such a shift corresponds to 59 mV/pH and it is amplified by the circuit if a proper reference voltage is applied to the liquid environment. Choosing an appropriate reference voltage to be applied to the liquid is an important step. In fact it can be seen in Fig.2.8a that a shift in the curve will not provide any change in the output voltage if the liquid voltage is fixed either at V^1_{ref} or V^2_{ref}. At $V_{ref} = V^*_{ref}$, a ΔV_{out} of 300 mV/pH can be achieved, which is five times more than the input signal ΔV_{th} . This simple architecture thus provides both sensing and amplification functions. In first approximation, the gain, A_v, can be defined as:

$$A_v = \frac{\Delta V_{out}}{\Delta V_{th}} \approx -g_m \cdot R_L \tag{2.5}$$

where g_m is the sensing FinFET transconductance and R_L is the load resistance. Higher gain can therefore be achieved by increasing either g_m or R_L. A higher g_m can be accomplished by increasing the fin height, h_{Si}, or decreasing the fin length, L_{Si}. However, due to fabrication process constraints, the fin height is limited to 150 nm, while the fin length to a maximum of 500 nm. Figure 2.8b shows A_v according to different R_L values: for higher R_L, $\Delta V_{out}/pH$ increases, reaching a maximum value of 1.35 V/pH for a liquid voltage $V_{ref} = -100\,\text{mV}$ and $R_L = 1.5\,\text{k}\Omega$. The V_{ref} value was previously chosen according to the amplifier onset voltage, in order to optimize the linearity. By changing R_L, the amplifier onset voltage also changes, meaning that V_{ref} should be changed accordingly. This is also the reason why $\Delta V_{out}/pH$ starts decreasing after reaching a maximum value. For each biasing condition, i.e., for each value of V_{ref}, it is then possible to define a R_L, which maximizes the $\Delta V_{out}/pH$ or, viceversa, for a fixed R_L it is possible to choose the best biasing point. Anyway, implementing the load with a resistor is not an efficient solution in terms of integration. A resistance in fact can be thousands of times larger than a MOSFET and the fabrication process would require more lithography steps. The load resistor R_L is thus replaced by a metal FinFET (device 2A of Fig. 2.4) by connecting its gate to the power supply, V_{DD}, so that it is always biased in the saturation region and does behave as a resistor. In this case, the gain is given by:

$$A_v = \frac{\Delta V_{out}}{\Delta V_{th}} \approx \frac{g_{m1}}{g_{m2}} \tag{2.6}$$

which can be reduced to the ratio L_2/L_1 considering that both the sensing and the load FinFETs have the same oxide material, thickness and height. Fig. 2.9a shows the output voltage of the amplifier with active load as a function of time for three pH changes between 6.5 and 9.5. V_{DD} was increased to 3 V in order to have a higher output swing, meaning a larger measurable pH range. The red curve features a L_2/L_1 ratio three times higher than that of the blue curve, showing an increase in ΔV_{out} of roughly 300 mV (with a suitable V_{ref} chosen as explained above). The gray curve shows how an incorrect bias point can lead to a much smaller $\Delta V_{out}/\Delta V_{th}$, even when a large L_2/L_1 ratio is adopted. With the metal FinFET connected as an enhancement-mode load, a gain of $A_v = \Delta V_{out}/\Delta V_{th} \approx 17V/V$ is obtained for FinFETs featuring a length ratio $L_2/L_1 = 30$ and $A_v = 12V/V$ for $L_2/L_1 = 10$. It is important to stress that the good linearity of the transduction from ΔpH to ΔV_{out} is directly correlated to the circuit input–output characteristics. In literature, FET ionic sensors are usually biased in the depletion region, which does not provide a linear current change according to the surface potential variation. Moreover, the use of a single sensor in the linear region would not provide a significant current change due to a poor subthreshold slope.



(a)

(b)

(c)

Figure 2.6: Simulations of single devices for 2D modelling: (a) $I_d(V_g)$ and (b) $I_d(V_d)$ characteristics simulated in SPICE for the approximation of no-corners between the devices of Fig. 2.5; (c) $I_d(V_g)$ characteristics simulated in Sentaurus for the hybrid FinFET considered as monolithic device and as sum of its bottom and top parts.

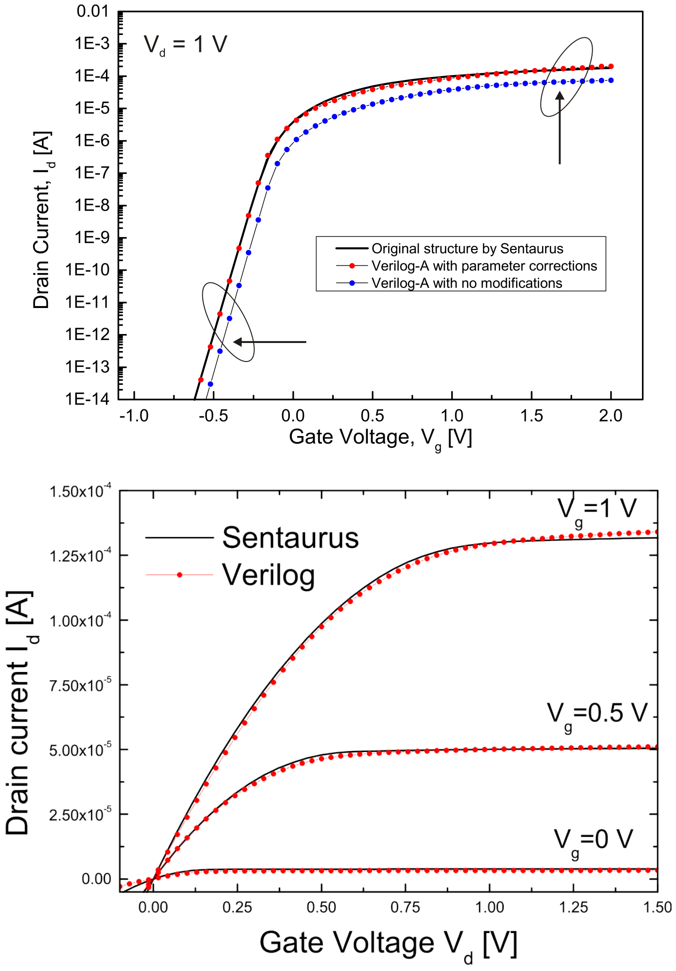
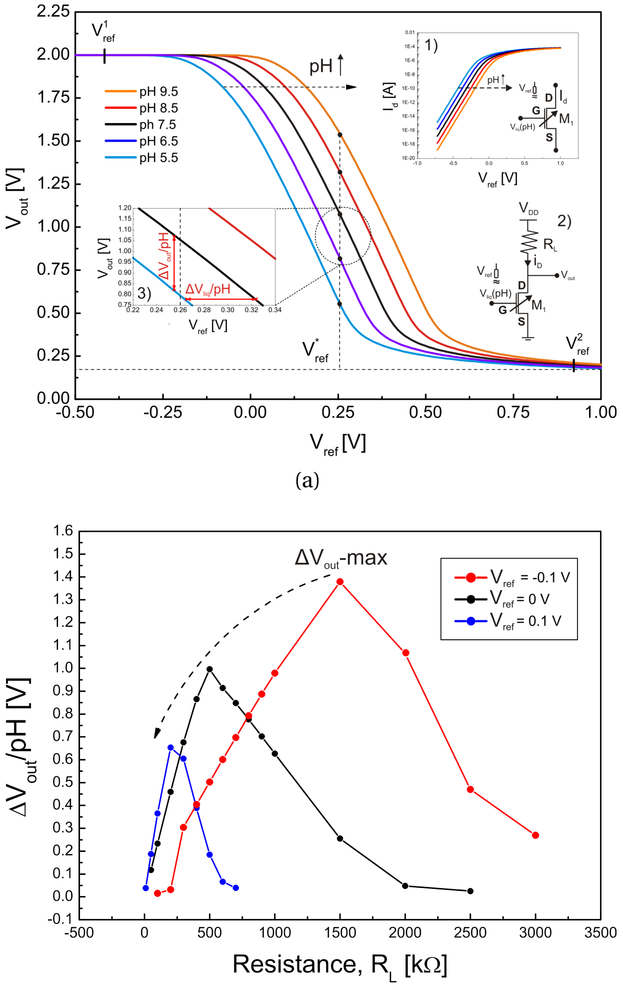


Figure 2.7: Comparison between 3D FEA and 2D SPICE simulations: (a) $I_d(V_g)$ and (b) $I_d(V_d)$ for the FinFET simulated by the FEA software and in SPICE by analytical equations.



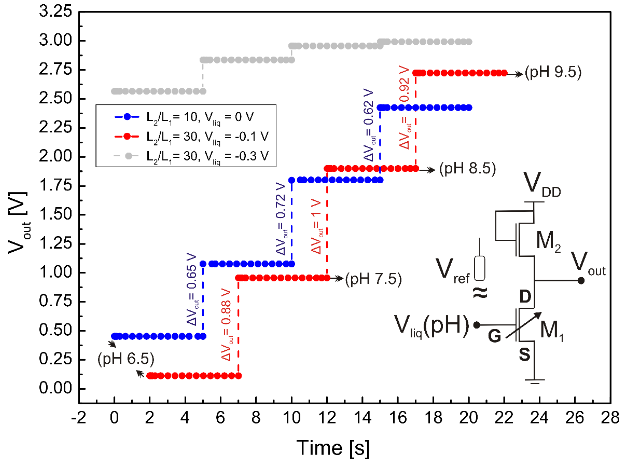
(a)

(b)

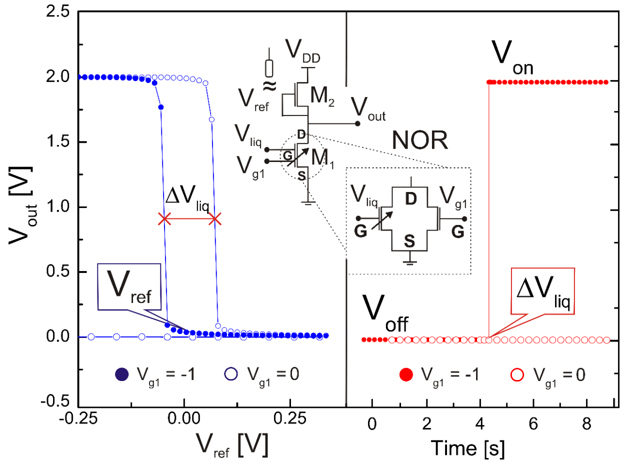
Figure 2.8: Sensing common source amplifier realized with a resistor: (a) V_{out}, as a function of the liquid voltage through V_{ref}; $V_{out}(V_{ref})$ shifts according to different pH values: (1) $I_d(V_{ref})$ curve for different pH values of a single FinFET sensor; (2) circuit schematic of the common-source amplifier with resistive load R_L; (3) detail of $I_d(V_{ref})$ to show $\Delta V_{out}/pH$ with respect to $\Delta V_{liq}/pH$; (b) $\Delta V_{out}/pH$ for different load resistance values, R_L, according to different biasing conditions.

2.2.3 A sensing NOR gate

The circuit in Fig. 2.9a can be modified by connecting the metal FinFET as a depletion load, as shown in the schematic of Fig. 2.9b. This is achieved by connecting the FinFET gate and source terminals together. Using a depletion-mode load offers two main advantages: (i) the output voltage can be equal to V_{DD} (and it is not limited to $V_{DD} - V_{th}$, as for the enhancement-mode load) and a steeper ON–OFF transition can be achieved even with a smaller L_2/L_1 ratio. A further modification of such a circuit can be implemented by substituting the FinFET sensor with the compact hybrid device 34 of Fig. 2.4. This circuit implements an n-MOS NOR logic gate. When the voltage at the metal gate, V_{g1}, is set to 0 V the driving transistor is turned on and forces the output voltage to zero independently of the status of the sensing transistor. When the voltage on V_{g1} is instead set to -1 V, the circuit behaves as a logic inverter whose



(a) Enhancement-load



(b) Deplition-load

Figure 2.9: Sensing common source amplifiers based on two n-MOS components: (a) V_{out} as a function of time with the sensor FinFET as active transistor for four different pH values, different fin length ratios and different biasing points; in the inset, circuit schematic of the common-source amplifier with n-MOS transistor connected as enhancement load; (b) NOR logic gate with voltage output, $V_{out}(V_{ref})$ on the left, and as a function of time, on the right, implemented with a hybrid FinFET as active transistor and a depletion-mode FinFET as load (center inset).

characteristics are shown in Fig. 5.11. The graph in the left part demonstrates a complete ON–OFF transition: by setting V_{ref} close to the inverter slope onset, a sensing event modelled as $\Delta V_{liq} = 70\,\text{mV}$ is enough to trigger a transition from $V_{off} = 0$ V to $V_{on} = 2$ V. An additional margin of roughly 50 mV is taken into account in order to compensate for drift in the solution. Then, ΔV_{liq} is set equal to 120 mV. In terms of ionic concentration such a value corresponds to a change of at least 2 pH units. While in biosensing applications, it is consistent with surface potential variations due to the binding of a DNA strand or of a specific protein [5]. The result is presented in the right graph of Fig. 2.9b, where the output voltage is plotted as a function of time. After 4 seconds, a ΔV_{liq} = 120 mV is applied simulating the sensing event. The circuit output switches from the OFF to the ON state.

Such a configuration can detect whether a specific analyte is present in the solution, which is complementary to the one shown in Fig. 2.9b, suitable for quantitative measurements. Both amplifying stages have been demonstrated to be highly effective for the readout of a sensing event, when the sensor is implemented as a driver transistor and the standard metal transistor as a load. The gain in amplification cannot be exploited, if the two functions are interchanged. The circuit would then be a simple voltage-readout stage as described in [14]. Another advantage of this circuit is that V_{g1} can be used to turn off the sensor. This might be useful if one envisions complex systems with many sensors with different functionalizations. In such configuration, only the sensors needed for a specific measurement could be turned on, so that the power consumption could be reduced, and the signal readout would not affect nor be affected by the other sensors. More generally speaking, the hybrid device has the advantage of being able to sense an analyte and to provide a certain amount of DC current to the circuit, e.g., a biasing current. This does not have any effect on the sensitivity but can be an important feature for more complex circuit architectures, such as the ring oscillator or the differential amplifier described in the next section.

2.2.4 A sensing ring oscillator and pseudo-differential amplifier

This section shows how the devices that have been presented so far can be combined in order to achieve superior readout characteristics. Through combination of several devices, a sensing circuit can be realized, where the entire circuit behaves as a sensor. There are two main advantages of this approach: (i) the responses of the individual devices are summed up, which results in an enhanced sensor response, and (ii) non-idealities of single devices can be compensated. Fig. 2.10 shows the first proposed circuit, which consists of a three-stage ring oscillator whose oscillating frequency depends on the pH, i.e. on the voltage drop at the sensor surface. This is achieved with the inverter scheme shown in the inset of Fig. 2.10: the FinFET 2A of Fig. 2.4 is used as the driving transistor while the hybrid DG-FinFET 3A is connected as load. The compact device in our implementation provides the driving part, i.e., the part featuring the metal gate, as a depletion-mode transistor load, while sensing part modulates the current flowing through the inverter. The time needed to charge the capacitances in between the inverters is then changed, affecting the oscillating frequency. Fig. 2.10 shows the output frequency with a good linearity between pH 2 and 10 and $\Delta f \approx 16\,\mathrm{MHz/pH}$. A similar circuit was presented in [15], where, however, very high operating voltages (> 50 V) were used, which are prohibitive to any implementation with standard Si-based ICs. The design proposed here relies on a power supply of 2 V and includes only six n-channel transistors.

Fig. 4.10a shows another circuit: a pseudo-differential amplifier. Two hybrid DG-FinFETs constitute a pseudo differential pair. One is used for sensing, i.e., its surface is chemically

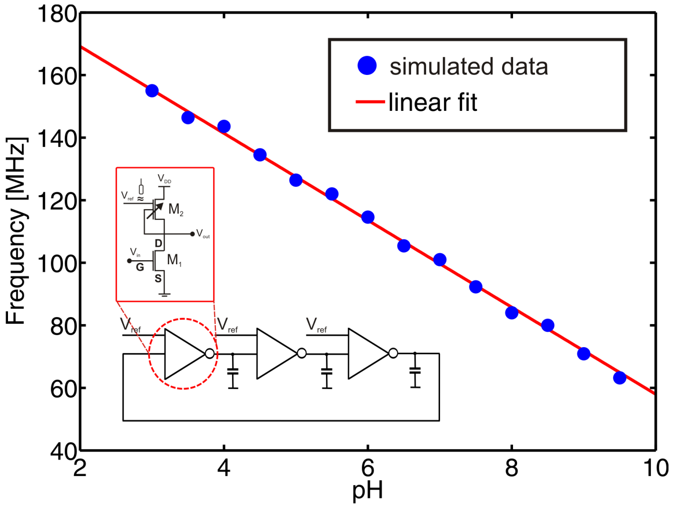


Figure 2.10: Sensing ring oscillator: oscillating frequency of the ring oscillator versus pH and ring oscillator schematic shown in the bottom left schematic.

active, and the other one is used as a reference, i.e., its surface is passivated. Two FinFETs are then used as loads. As an example, the surface of the sensing FinFET could be modified so as to be sensitive to a specific protein, while the surface of the reference FinFET would be inert. This way, a differential measurement can be carried out, alleviating common variations due to temperature or solution drifts. The gate of the driving part of the hybrid DG-FinFET can be connected to the output implementing an amplifier stage as shown in the insets of Fig. 4.10a with a gain directly proportional to h_S/h_D, where S and D denote sensor and drive. The simulation results in Fig. 4.10a show that a gain of 6 dB can be achieved (for the same V_{ref}) just by changing the ratio between the sensing part and the driver part in the hybrid DG-FinFET in the design phase. The graph of Fig. 2.9a shows that higher gains, i.e. 25 dB, can be achieved using a uniform sensing FinFET as driving transistor instead of a hybrid DG-FinFET. However, it should be noted that the linear range is increased when using the hybrid device. Fig. 4.10a shows good linear behavior between pH 5 and 10.5, whereas in Fig.2.9a (where the sensing FinFET is used) the linear range goes from pH 6.5–9.5.

2.3 Doping strategies for triangular nanowires

In the last section of this chapter, an additional implementation of TCAD FEA simulations for boosting sensing devices is proposed. The results of this section were elaborated in the initial phase of the research concerning the FinFET design. Despite these results have not resulted in a practical implementation they are important for understanding how the electronic and sensing properties of a semiconductor devices are reciprocally interwoven [16].

Two different triangular SiNWs have been studied and compared: device A consists of a uniformly doped p-type body, while device B consists of a p-type core surrounded by an n-type layer, as illustrated in Fig. 2.12. The thickness of this layer is $t_{shell} = 20\,\text{nm}$. The common

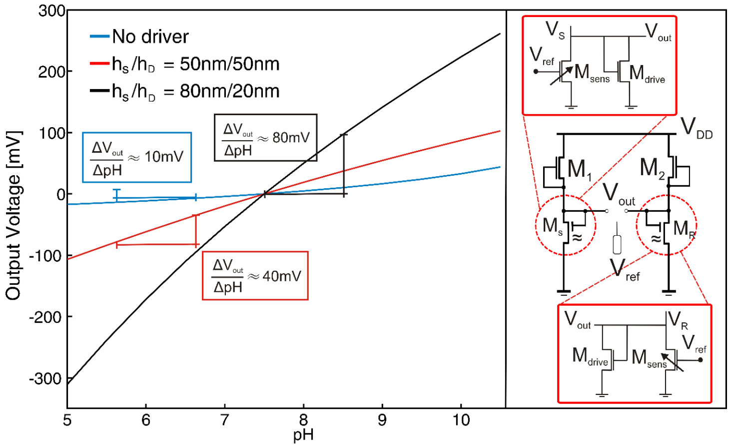


Figure 2.11: Sensing differential amplifier: simulation of the output voltage of the pseudo-differential amplifier for different h_S/h_D ratios (compared to the output with no driving transistors), and schematic (right) of the pseudo-differential amplifier with the equivalent circuit of the hybrid device.

parameters of the two devices are: p-type core doping $N_A = 10^{17}\,\mathrm{cm}^{-3}$ (boron), n-type shell doping $N_D = N_A = 10^{18}\,\mathrm{cm}^{-3}$ (phosphorus), contact doping $N_D = 10^{20}\,\mathrm{cm}^{-3}$ (phosphorus), nanowire length $L = 1\,\mu\mathrm{m}$, SiNW cross-section side $L = 120\,\mathrm{nm}$. Both devices are covered by a 10 nm thick layer of HfO_2. As both structures can be fabricated as suspended NWs [17], the whole surface is exploited for sensing. In order to compare the two devices, the device readout sensitivity, S_{out}, is defined as the relative drain current variation, $S_{out} = |\Delta I_d|/I_{d0}$ where ΔI_d is the drain current difference after applying a $\Delta V_g = 50\,\mathrm{mV}$ and I_{d0} is the highest current value before the surface potential shift. As previously discussed, the readout sensitivity is directly connected to the reference electrode biasing point, when operating in non-equilibrium conditions. On the contrary, the intrinsic device sensitivity, i.e. the threshold voltage shift ΔV_g, is fixed. As reported in Chap. 5, the threshold voltage shift achieved with HfO_2 is $\Delta V_g = 56\,\mathrm{mV}$, so our assumption is correct. The two devices are fully-depleted, thus the model described in Chap. 1 applies. The transfer characteristics of the two devices is shown in Fig. 2.13a, the

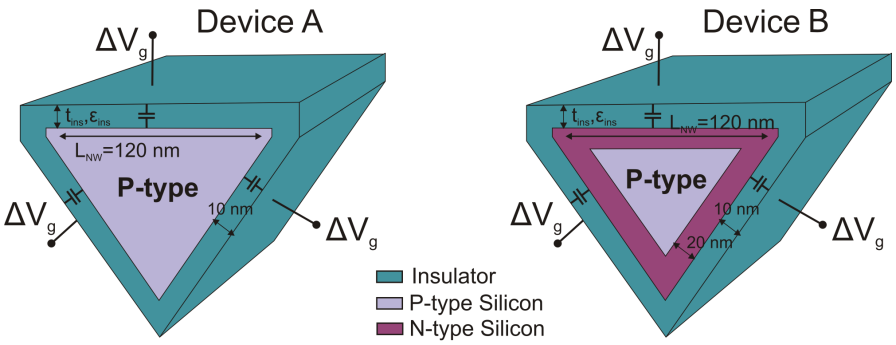
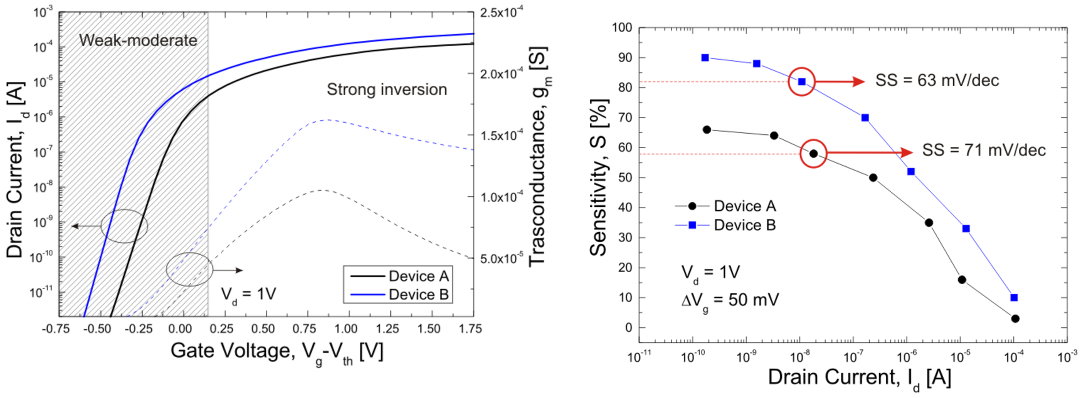


Figure 2.12: Triangular SiNWs: device A consists of a uniformly doped p-type body, while device B presents a p-type core with an implanted n-type shell of 20 nm depth.

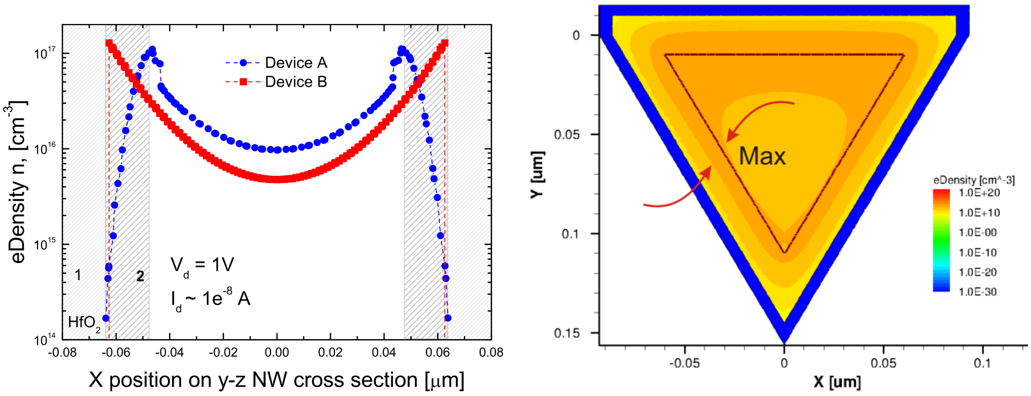
gate voltage is reported as $V_g - V_{th}$. Looking at the $I_d(V_g)$ curve it is not possible to perceive a difference in the subthrehsold slope of the two devices. Indeed, according to the charge density inside the SiNWs, small Subthreshold Slope (SS) differences exist, and they can be exploited for a higher readout sensitivity. The gate voltage around the triangular wire is fixed at different bias, simulating the biasing point of the reference electrode. The sensitivity is plotted in Fig. 2.13b for both devices. The sensitivity of the n-shell device is always higher with respect to the uniformly doped device. Since the punctual SS is higher, it is expected to have a higher readout sensitivity. The physical mechanisms behind a high subthreshold slope for the n-shell doped device may be extremely complex, especially in presence of nanoscaled fully-depleted devices with important corners [18]. In order to correctly model the observed behaviour a deeper simulation study should be performed, taking into account quantum mechanics corrections as proposed in [18]. However, an important feature of such a mechanism can be identified. Looking at the electronic density of the SiNW cross-section along a XY-plane, the maximum electronic density for device A is located close to the surface, while for device B is located at the n-shell/p-core interface. This comparison is proposed in Fig. 2.14a where the electron density is plotted according to the x-depth as illustrated in the SiNW cross-section of Fig. 2.14b. The two electronic densities have been obtained for an equivalent I_d value of current. The space charge distribution, which comes from the doped n-shell and its lower concentration at the surface, can be assumed at the origin of the slope enhancement. This application of FEA simulations can be implemented on already existing devices to make them more amenable to sensing applications.



(a) $I_d(V_g)$

(b) Sensitivity of triangular SiNWs

Figure 2.13: (a) $I_d(V_g)$ transfer characteristic of device A and device B plotted as function of $V_g - V_{th}$ at $V_d = 1\,\text{V}$; (b) extracted sensitivity for device A and B according to I_d values defined at different biasing of V_g.



(a)

(b)

Figure 2.14: Electron density of triangular SiNWs: (a) carrier density at the cross section when both devices reach a drain current approximately of $I_d = 100\,\text{nA}$; (b) cross-section along Z-axis of the triangular wire of device B visualizing the electron density.

2.4 Summary

This last section summarizes all the results achieved by *simulations* of FinFETs implemented as both sensor and circuit units.

- **Technical outcomes**:
  - *Parameters validated by FEA simulations:*
    - Device architecture: n-channel fully depleted FinFET;
    - Geometrical dimensions: $T_{Fin} \leq 50\,\text{nm}$ and $H_{Fin} \leq 150\,\text{nm}$, so that $H_{Fin}/T_{Fin} \geq 3$;
    - Gate oxide: HfO_2, with $5\,\text{nm} \leq t_{HfO_2} \leq 10\,\text{nm}$;
    - Channel doping: $N_A \leq 10^{16}\,\text{cm}^{-3}$;
    - Source and Drain doping: $N_D \geq 10^{20}\,\text{cm}^{-3}$.
  - *Results of SPICE simulations:*
    - Common source amplifier: $A_v = \Delta V_{out}/\Delta V_{th} = 17$, i.e. 25 dB (enhancement-load mode):
    - Common source switch: $\Delta V_{off-on} = 2\text{V}$ for a $\Delta V_{th} = 120\,\text{mV}$, i.e. 24 dB (depletion-load mode);
    - Ring oscillator: $\Delta f(pH) = 16\,\text{MHzà/pH}$.
- **Main contributions to the field**:
  - Definition of a well-defined electronic unit, the FinFET, as a dual-purpose device: sensor and circuit component;
  - Demonstration, through SPICE simulations, of how the connection of a sensor, connected as driver, and metal gate FET, connected as load, can achieve threshold voltage variation amplified up to 1 V/pH;
  - Demonstration of a sensing switch for the qualitative analysis of solutions, i.e. presence or not of a chemical species in the solution;
  - Merging of electronic stages with the sensing principle:
    - NOR gate: for enabling or disabling single SiNW in multiple sensing array;
    - Ring oscillator: for frequency dependence on sensing events;
    - Pseudo-differential amplifier: for differential measurements with tunable gain.

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3 Technological Development of FinFETs for Sensing Applications

The FinFETs described in Chap. 2 were fabricated according to a top-down approach on silicon bulk substrate. As previously presented in Tab. 1.3, the majority of works related to SiNWs for sensing applications have been implemented on SOI wafers and very few examples are available for Si-bulk.

Here, the FinFET fabrication process is described. After a concise overview, the chapter includes the technological strategies of the main steps which have led to a reliable and reproducible process. The use of softwares to assist and correct the most critical steps and parameters is also described. The fabrication aimed to achieve several goals:

- The realization of the FinFETs on Si-bulk wafers;
- A specific and reproducible geometry of the FinFETs, as expected for SOI wafers;
- The implementation of an high-k dielectric oxide as sensing gate oxide;
- The characterization of the electronic components prior to the microfluidic platform assembly.

The basic steps of the cleanroom fabrication process were established according to prior works [1, 2] developed at the Nanoelectronic Devices Laboratory, EPFL. The device fabrication was realized at the Center of MicroNanoTechnology (EPFL-CMi), while the microfluidic platform assembly was realized at the Nanoelectronics group of the University of Basel in collaboration with the Paul Scherrer Institute.

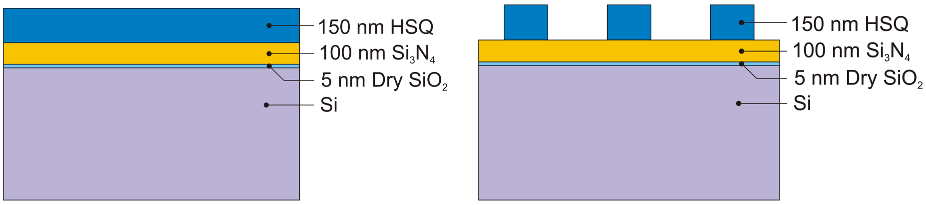
3.1 Overview of the process flow

The device fabrication was performed at EPFL-CMi. More details on the cleanroom can be found in App. A. The key features of the process are:

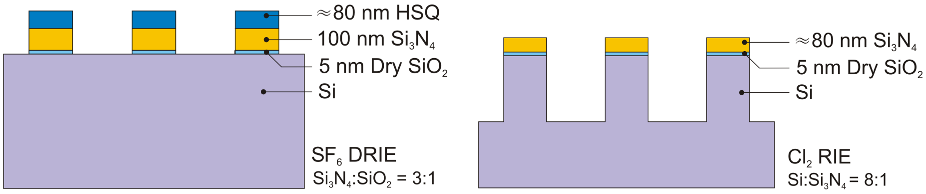
- **Technology:** Silicon bulk
- **Total number of steps:** 86, from e-beam lithography to wire bonding
- **Total number of masks:** 7, among these 3 are virtual layouts and 4 are Chromium masks

- **Critical steps:**
    1. Calibration of the e-beam lithography in order to achieve $T_{Fin} \approx 20\,\text{nm}$
    2. Local oxidation for the electrical insulation of the FinFETs from the Si-bulk
    3. Reliable SU-8 coverage
- **Main cleanroom techniques:**
    1. E-beam and UV lithography
    2. LPCVD, wet and dry oxidation, ALD, sputtering
    3. DRIE, RIE, wet etching, CMP
    4. SEM, FIB, TEM, mechanical profilometers, spectroscopic ellipsometer and reflectometer
- **Support softwares:**
    1. Sentaurus Process by Synopsis;
    2. Layout BEAMER by GenISys.

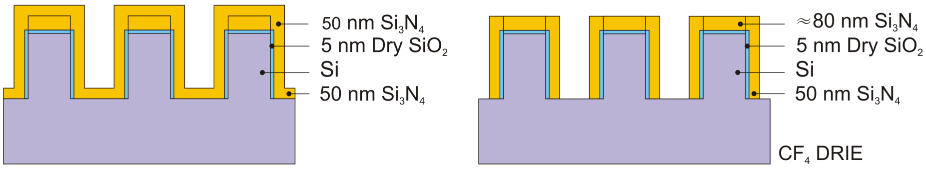
The whole fabrication process can be simplified as shown in Fig. 3.1. The starting substrate was a p-type silicon wafer, single side polished, with a resistivity of 0.1-0.5 Ohm.cm, a diameter of 100 mm and a thickness of 525 µm. The process started with an electron beam lithography (EBL) step, followed by four photolithography masks. The EBL step was realized by exposure of hydrogen silsequioxane resist (HSQ), deposited on a Si_3N_4/SiO_2 hard mask (Fig. 3.1a). Subsequently, the patterned HSQ (Fig. 3.1b) was transferred into the Si_3N_4 mask by SF_6 based Deep Reactive Ion Etching (DRIE, Fig. 3.1c) and into the Silicon substrate (200 nm) by Cl_2 based RIE (Fig. 3.1d). 50 nm of Si_3N_4 (Fig. 3.1e) were deposited by Low Pressure Chemical Vapor Deposition (LPCVD) and etched to form the so-called Si_3N_4 spacers (Fig. 3.1f). Later, after an additional Si RIE (Fig. 3.1g), 300 nm of SiO_2 were grown by wet oxidation, detaching and isolating the vertical fins from the bulk (Fig. 3.1h). Such local oxidation, assisted by Finite Element Analysis (FEA), allowed to achieve fin width ranging from 15 to 40 nm and $H_{Fin}/T_{Fin} \geq 3$. The Si_3N_4 spacers were then removed by hot phosphoric acid (performed at CSEM, Neuchatel) and source and drain pads were implanted with phosphorous at 25 keV with $n_A = 2 \times 10^{15}\,\text{cm}^{-2}$ as dose, creating n-channel device with n+ contacts (Fig. 3.2a). The fin surface was then exposed by Dip Hydrofluoric (HF) acid (Fig. 3.1i) to guarantee the fin to be maximally exposed but preventing the SiO_2 etching under the fin. The whole wafer was then covered by 8 nm of HfO_2 deposited by Atomic Layer Deposition (ALD, Fig. 3.1j). Vias of $3{\times}3\,\mu\text{m}^2$ were created by Ar ion milling, and the devices were connected with $AlSi_{1\%}$ lines to $250{\times}250\,\mu\text{m}^2$ pads at the edge of each die (Fig. 3.2b). For FinFETs aimed at the electrical characterization an $AlSi_{1\%}$ metal gate was also deposited. Chemical Mechanical Polishing (CMP) and a backside metallization were performed for a good chuck contact. This concluded the main process flow. The packaging process for the liquid environment continued the process, after verification of the device electrical quality. SU-8 openings were patterned next to the FET sensing channels to prevent the contact between liquid and the metal connections. Finally, the wafer was diced, each die was glued into a chip carrier and connected by Au wires. In the following sections, the technological development of the main fabrication steps is exposed in chronological order, from e-beam lithography to the chip-carrier assembly.



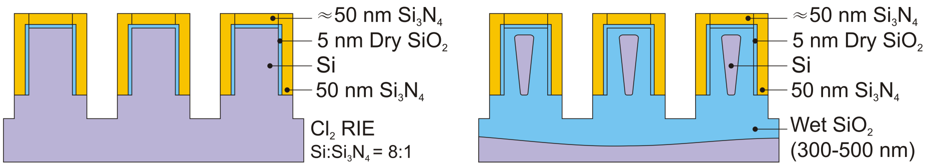
(a) Starting substrate (b) E-beam Lithography



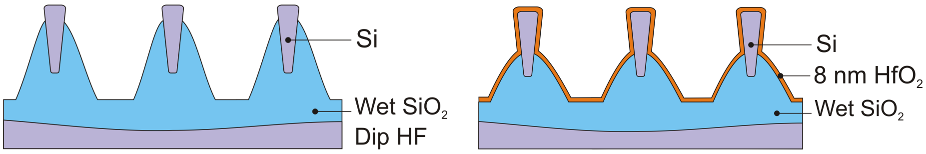
(c) Hard mask transfer (d) Vertical fin definition



(e) Spacer deposition (f) Spacer definition

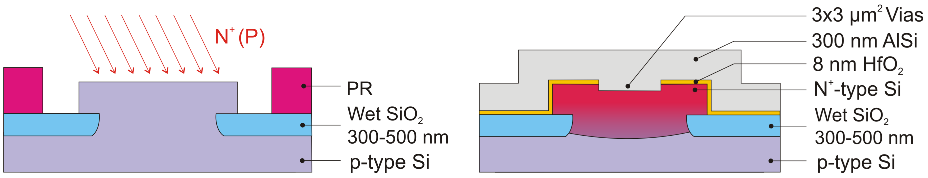


(g) Si-bulk exposure (h) Wet oxidation



(i) Fin exposure (j) HfO_2 deposition

Figure 3.1: Simplified process flow: cross-section drawings of FinFETs.



(a) Source and drain implantation

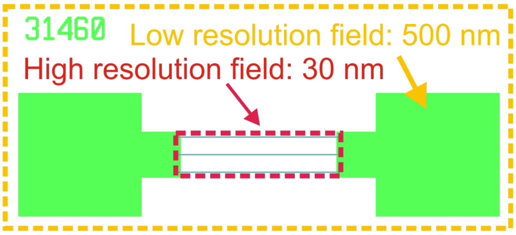
(b) Metallization

Figure 3.2: Simplified process flow: cross-section drawings of contact pads.

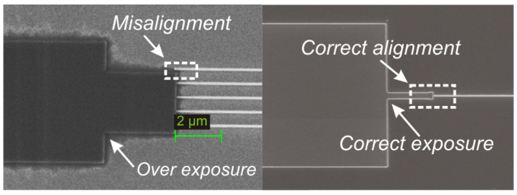
3.2 E-beam lithography for sub-20 nm resolution

The EBL system at CMi (Vistec, EBPG5000ES) is capable of writing sub−10 nm features and placing structures on a substrate with an accuracy of less than 20 nm. The results are however extremely dependent on the type of resist and the parameters chosen for the e-beam writing during the data conversion.

The e-beam layout strictly defines the FinFET structures from the beginning to the end of the process. The layout is composed of two resolution sub-layouts: high resolution (HR) for the definition of the fins with a critical dimension (CD) of 30 nm and low resolution (LR), for the connection pads, the alignment marks and testing structures with a CD of 500 nm, as illustrated in Fig. 3.3a. The layout overlapping and the correct merging of the two resolution data sets, allow to avoid any misalignment problem as shown in Fig. 3.3b. The resist used is a 150 nm thick layer of HSQ, which was dispensed manually and spin coated at 3500 rpm.



(a)



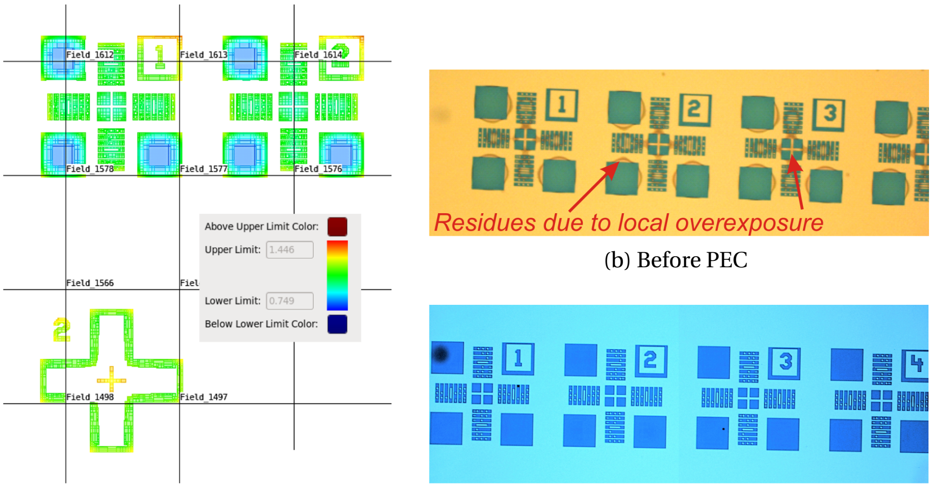
(b)

Figure 3.3: (a) Layout of a three wire FinFET with the two resolution fields set during the data conversion for the vertical fins and pads; (b) EBL testing procedure: misalignment of the two resolution fields and overexposure of big areas (left) and correct exposure and alignment (right).

The EBL parameters have been set after a dose test where a wide range of exposure doses has been tested for both fins and pads. The final parameters are:

- **Resolution**: 3 nm (HR) and 50 nm (LR), calculated as one tenth of CD;
- **Dose**: 2000 μC cm^{-2} (HR) and 700 μC cm^{-2} (LR), defined after the dose test;
- **Current**: 10 nA (HR) and 150 nA (LR), set for the best resolution but limited by the total exposure time.

The final frequency, from one pixel to another when writing a pattern, is 6.5 MHz (HR) and 2 MHz (LR) for a total writing time of about 25 minutes per wafer.
Later, the introduction and calibration of a Proximity Effect Correction (PEC) software (GenISys, Layout BEAMER) allowed to improve the alignment marks which, having a higher pattern density with respect to the SiNWs, resulted slightly overexposed. The PEC software has been calibrated with the parameter $\beta_e = 33$, which takes into account the silicon substrate, and the parameter $\eta_e = 0.6$ for the correction level connected to the pattern density. This software not only provides advantages in term of dose distribution but it also optimizes the total writing path, which was reduced to about 18 minutes, after the so-called "data healing". Figure 3.4 shows the improvements at the alignment mark level and the elaborated distribution dose by the PEC tool, where the colour gradient corresponds to the factor of multiplication of the constant starting dose.



(a) Dose distribution by PEC

(b) Before PEC

(c) After PEC

Figure 3.4: (a) Example of the graphical output after the PEC data adjustment and conversion where the colour legend is the new dose distribution which was originally constant; alignment marks (b) before the introduction of the PEC with traces of overexposure and (c) after the correction with spotless areas.

3.3 Wet and dry etching optimization

This section describes the main etching recipes used in the fabrication process. Particular attention is given to the etching procedures that have been optimized for the involved materials.

This mostly concerns the dry etching sequence after the e-beam lithography, which allows the fin fabrication without any additional photolithography masks.

3.3.1 Si_3N_4 etching based on SF_6 for T_{Fin} definition

Silicon nitride dry etching is commonly performed using fluorine gases such as Sulfur Hexafluoride, SF_6, or Tetrafluoromethane, CF_4, in presence of O_2 or H_2 [3]. By using SF_6 it is possible to obtain a recipe with a good selectivity with respect to HSQ which at high exposure doses is chemically similar to SiO_2 [4]. This way the HSQ mask can be completely transferred into the Si_3N_4 hard mask (Fig. 3.1c)) by DRIE (Alcatel, AMS200 DSE). To obtain such selectivity the power supplied to the chuck should not exceed 10 W. The etching rates obtained are then:

- **Si_3N_4**: 210 nm/min
- **SiO_2**: 77 nm/min
- **Si**: 3 µm/min

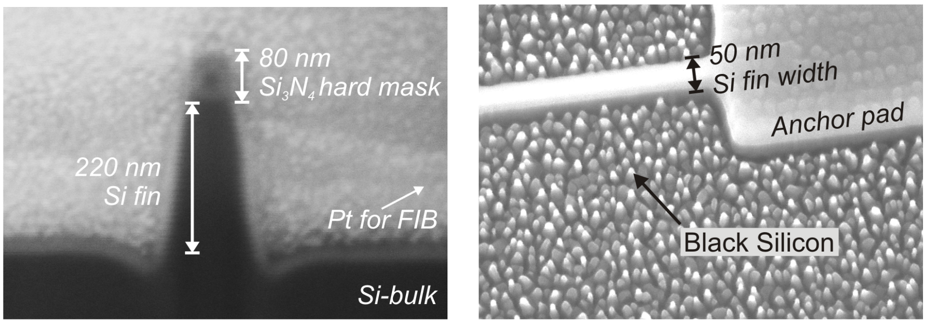
A final selectivity of $Si_3N_4 : SiO_2 = 3 : 1$ is achieved. An etching time of 32 seconds also guarantees the removal of the few nanometers of SiO_2 under the Si_3N_4. For this purpose, it is more recommended to continue running a recipe based on SF_6 rather than CF_4 or CF_4F_8. The reaction between fluorocarbons and SiO_2 may, in fact, result in the formation of polymers, especially for short etching times. Such polymers can then act as a stopping layer and cause etching time variations for the following etching steps. It is nevertheless important to etch even few nm of SiO_2 to facilitate a smooth vertical silicon etching step afterwards. The SF_6 recipe is extremely stable and it did not need frequent calibration.

3.3.2 Vertical Si etching based on Cl_2 for H_{Fin} definition

Reactive ion etching (STS, Multiplex ICP) based on Cl_2 was used to transfer the patterned Si_3N_4 hard mask into the Si substrate, (Fig. 3.1d and 3.5a) and to expose part of the Si substrate in preparation of the local oxidation (Fig. 3.1g and 3.6b). The standard recipe provides the following etch rates:

- **Si**: 360 nm/min
- **Si_3N_4**: 75 nm/min

for a selectivity of $Si : Si_3N_4 = 5 : 1$. The optimal vertical fin height has been found to be at least 200 nm, as shown in Fig. 3.5a. The recipe is also used after the spacer creation to vertically expose the Si-bulk to the oxidation (Fig.3.6b). This etching depth should not be less than 150 nm, otherwise the quality of the local bulk oxidation would be compromised. The etching time was set to 32 seconds but later the recipe exhibited a slower etching rate of 290 nm/min. Differently from the previous recipe, a constant etching rate monitoring was needed to adapt the etching time from batch to batch. Silicon etching in presence of oxide residues from previous steps may lead to the formation of unwanted and uncontrolled black silicon as



(a)

(b)

Figure 3.5: Si fins etched by RIE: (a) SEM picture obtained by FIB cross-section of a fin with Si_3N_4 top mask and (b) SEM top picture of unwanted black Si after RIE.

shown in Fig.3.5b.

3.3.3 Si_3N_4 etching based on C_4F_8 for spacer creation

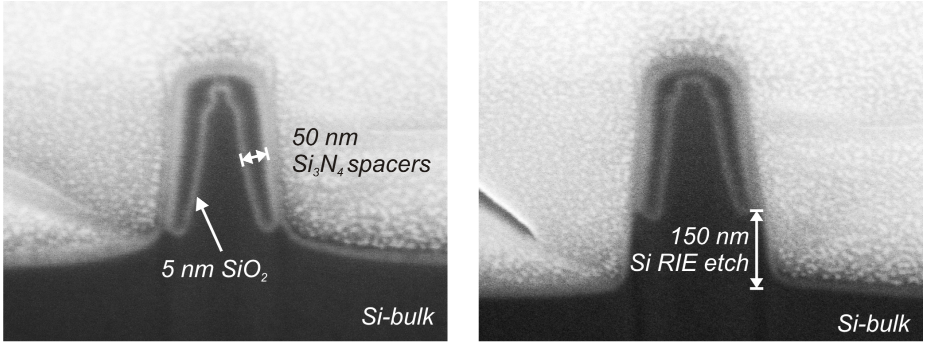
After the vertical fin etching, 50 nm of Si_3N_4 were deposited by LPCVD to form the Si_3N_4 spacers. After the deposition, the nitride needed to be anisotropically removed from the bottom, as shown in Fig. 3.1f and 3.6a. The isotropic deposition and the previous remaining Si_3N_4 mask on top of the fins allow a homogeneous encapsulation around the fin (Fig. 3.1e). The previous Si_3N_4 etching recipe based on SF_6 is not suitable for this particular etching because:

- The spacer etching needs to be anisotropic in order not to consume the nitride on the fin sidewalls. On the contrary, the recipe based on SF_6 is quite isotropic, especially because of the low chuck power;
- The etch rate should be slower in order to be more accurate on the etching time and avoid an over-etching which would reduce the spacer thickness;
- The etching time should include a small over-etching time, otherwise, if any Si_3N_4 remains, the oxidation would not take place. At the same time, the recipe should stop with a certain selectivity at the Si bottom, which is etched too fast by SF_6.

For these reasons C_4F_8 is a much better choice with respect to SF_6. The initial recipe was optimized in terms of chuck power. A final Si_3N_4 etching rate of 135 nm/min at 40 W was obtained. The etching time is then set to 25 seconds and the result is shown in Fig. 3.6a, where it is possible to observe how the etching precisely ends at the bottom of Si.

3.3.4 Fin surface exposure by dip HF

After the definition of the vertical fins and the creation of the spacers the Si substrate was oxidized by wet oxidation (Sec. 3.4) and source and drain were ion implanted (Sec. 3.5), leaving



(a) Si_3N_4 DRIE (b) Si RIE

Figure 3.6: Si_3N_4 spacers: (a) SEM cross-section of a vertical fin with Si_3N_4 spacers etched by DRIE down to the Si bottom and (b) additional Si etching to optimize the wet oxidation.

the fins covered by thermally grown SiO_2 and Low Temperature Oxide (LTO). Before the HfO_2 ALD, the SiO_2 needs to be completely removed from the fin surface. For this purpose a wet etching by dip HF was performed. A wet HF acid solution with dilution 1:50 was prepared with 80 ml of HF(50%) in 4 L of DI water and adding 4 mL (0.1%)of wetting agent FC-93. This chemical recipe is commonly called "dip" HF because its use is recommended for fast wafer immersion to remove the native oxide, usually prior to the metallization step. The wetting agent FC-93 allows the liquid to enter in small vias. In addition to this standard treatment, it was used in this process to expose the fin surface. Its slow etching rate allows to control the oxide etching with high precision, so that the fin surface can be exposed as much as the oxide is not removed from its bottom. The complete fin detachment from the underlying SiO_2 is discouraged, since water stiction problems have been observed in the first fabricated fins. This is mainly due to the extremely high L_{Fin}/T_{Fin} ratio which should be reduced in order to consider suspended structure. For this reason, dip HF has been preferred to the buffered HF (BHF) which has an etching rate at least ten times higher. The test procedures revealed the following etching rates:

- **SiO_2**: 7 nm/min
- **HfO_2**: Not observed

After a 8 minute etching the fins resulted properly exposed (Fig. 3.7). It is important to leave a certain amount of SiO_2 underneath the fins. It was calculated that a RCA cleaning procedure removes an additional 10-15 nm of SiO_2, which has to be taken into account. During the calibration, the etching has been stopped and verified at different stages by FIB, recalculating the remaining etching time (Fig. 3.7.b). No etching rate was observed for HfO_2 during an etching time of about 30 minutes. However, it is known that HfO_2 is etched by HF, but the etching rate is very low, especially at low concentration [5]. The described wet etching recipe was also used for removing the native oxide from the vias prior to the metallization, and it is then important to guarantee that no high-k material is removed from the device channels.

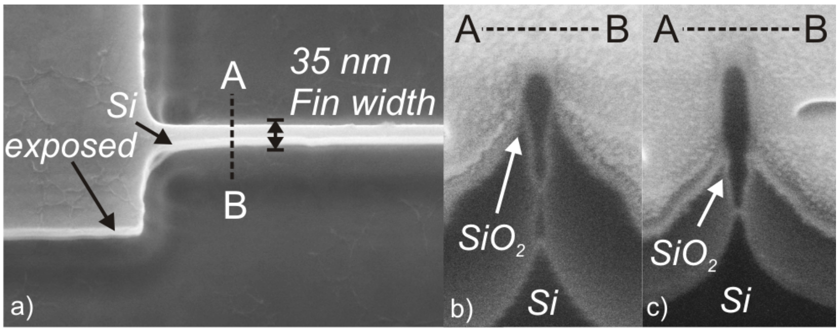


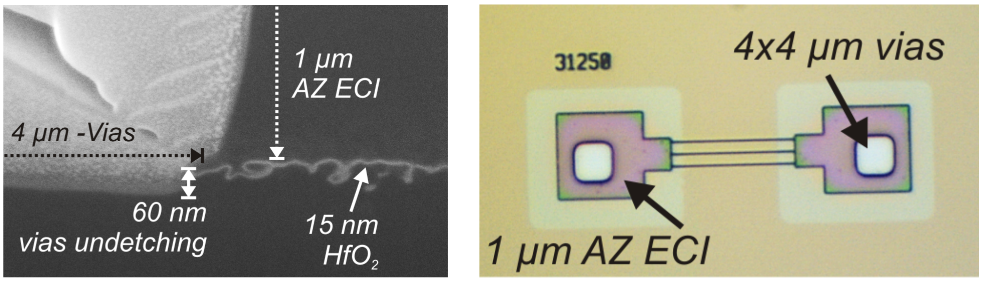
Figure 3.7: Fin exposure by dip HF: (a) SEM top view of a 35 nm width fin with Si surface cleared from SiO_2, (b) FIB cross-section at A-B section showing a Si fin after 5 minutes of dip HF and (c) after 7 minutes.

3.3.5 Vias etching by Ar ion milling

Ar Ion Milling is used for the HfO_2 etching to create the contact vias. This physical etching guarantees slow etching rates for all materials. The aim of the via etching is to remove the high-k dielectric oxide deposited by ALD after the fin surface exposure. A small over-etching into silicon is highly recommended. The testing procedure provided the etching rates:

- **HfO_2**: 13 nm/min
- **LTO**: 33 nm/min
- **Si**: 30 nm/min

For the 10 nm thick HfO_2 an etching time of 2 minutes was set. This recipe is also recommended with respect to other wet procedures in case of other oxides. If the vias apertures are quite small (≈ 3 µm) and the solution does not contain any wetting agent, they risk not to be etched due to the hydrophobicity of the photoresist. The etching rate of the photoresist (AZ ECI, 1 µm) is negligible for the set etching time. It is recommended to execute the recipe at low temperature, i.e. 0 °C, to limit the photoresist overheating during the etching.



(a) (b)

Figure 3.8: Vias etching:(a) SEM picture obtained by FIB cross-section during vias etching testing by Ar ion milling and (b) optical picture of fins after vias creation still in presence of photoresist.

3.4 Oxidation of Si-bulk aided by FEA simulations

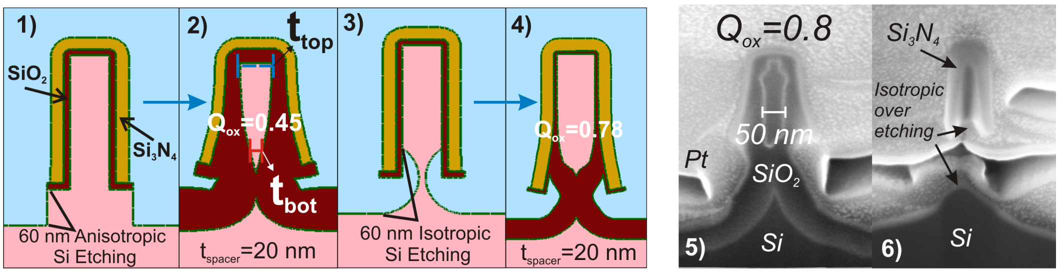
The Si fin thermal wet oxidation is one the most critical steps of the process flow. In this section, a combined FEA simulation-fabrication approach is presented for its calibration and optimization. Although the Si_3N_4 spacer technology for Si oxidation has already been validated as a reliable process [6], an overall investigation on the key parameters of such process was not yet accessible. The code (Sentaurus Process 2009.C) simulates the following fabrication steps : (i) Si fin patterning and vertical etching, (ii) SiO_2/Si_3N_4 deposition and etching, (iii) Si isotropic or anisotropic etching and (iv) wet/dry oxidation. The code is accessible at App. B. The oxidation is essential for the isolation of the fins and no other practical alternatives can replace this local insulation. Nevertheless, it is an aggressive process, especially in this specific case where a very small portion of silicon is protected by the Si_3N_4 spacers with respect to total oxidized surface. Moreover, the fin thickness $T_{Fin} \approx 50\,\text{nm}$ is three orders of magnitude higher than the fin length $L_{Fin} \approx 10\,\mu\text{m}$, making the formation of wreckage points quite easy, due to the concentrated stress.
The wet oxidation is usually performed at high temperature, between 950 °C and 1050 °C, which allows the following reaction between silicon and water vapour to take place:

$$Si + 2H_2O \Rightarrow SiO_2 + 2H_2 \tag{3.1}$$

Approximately, for the oxide growth of thickness t an amount of Silicon equal to $0.44t$ will be consumed. The oxidation depends on many variables, each having a significant impact on the final result. Some of those variables, e.g. gas flow, temperature ramps and chamber pressure were set in the FEA code according to the fabrication facility (Centrotherm furnaces). Other variables, e.g. the Si_3N_4 spacer thickness, t_{spacer}, the SiO_2 interfacial layer, t_{IL}, the duration of the Si oxidation, $time_{ox}$ and temperature T_{ox}, have been investigated through simulations. The quality of the resulting structures was defined as Q_{ox}, an index of quality of the vertical sidewalls equal to the ratio t_{bot}/t_{top} where t_{top} is the top fin thickness as defined by EBL, and t_{bot} is the fin thickness estimated at distance of $H_{Fin} = 150\,\text{nm}$ from t_{top}. The goal is to be able to reproduce the quality of SOI equivalent structures which would have a $Q_{ox} = 1$.

3.4.1 Results and comparison with fabrication

A Si isotropic etching prior to the oxidation as an alternative to the common anisotropic etching (Fig. 3.9a.1 versus 3.9a.3) can achieve a significant improvement of Q_{ox}. The isotropic etching results, in fact, in very sharp sidewalls after oxidation, as shown in Fig. 3.9a.4 versus 3.9a.2. An improvement from $Q_{ox} = 0.45$ to $Q_{ox} = 0.78$ was estimated. For the fabricated device, $Q_{ox} = 0.8$ was calculated for the Si exposure by isotropic etching (Fig. 3.9b.5). However, such isotropic etching can easily result in a complete fin over-etching making the oxidation impossible, as shown in Fig. 3.9b.6. This phenomenon was observed at minimum etching time and low chuck power too. The recipe instability may be due to the formation of polymers, as mentioned in Sec. 3.3.1, or to a particular condition of the reaction chamber. As a consequence,



(a) (b)

Figure 3.9: FEA simulations for wet oxidation: (a) Process simulation outputs: (1) anisotropic Si etching and (2) corresponding oxidation with $Q_{ox} = 0.45$; (3) isotropic Si etching and (4) corresponding oxidation with $Q_{ox} = 0.78$; (b) SEM images of fin cross-section obtained by FIB: (5) result after isotropic etching with a $Q_{ox} = 0.8$ and (6) over-etching problem due to the isotropic etching.

even if a higher quality result was demonstrated for the isotropic etching, both in simulation and in fabrication, its reliability made the anisotropic etching still preferable.

The t_{IL} has a similar impact as the type of etching, the smaller its thickness the higher the Q_{ox}. This thin SiO_2 layer underneath the Si_3N_4 is deposited to reduce the stress between Si and Si_3N_4, thanks to its intermediate liquid phase before the glass solid phase.

In case of multiple wires a minimum distance, $d_{NW} = 1.5\,\mu m$, was determined to guarantee a uniform etching and oxidation without the use of dummy structures, independently from the position of the wire.

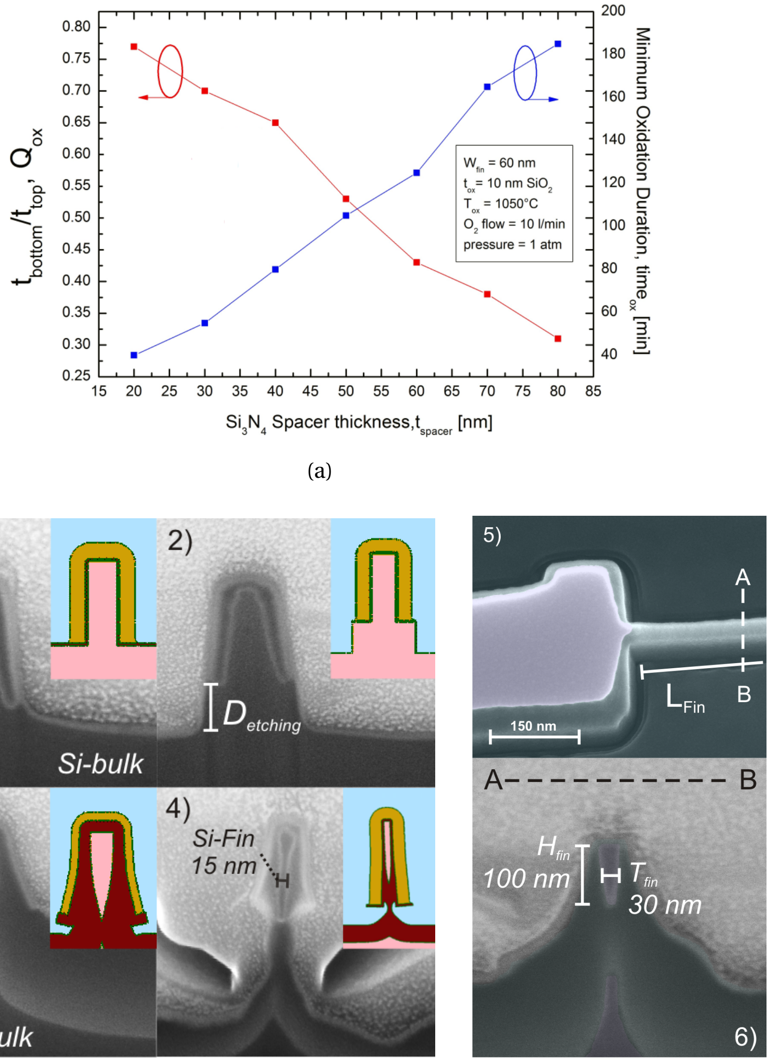
The graph of Fig. 3.10a shows the impact of t_{spacer}: when the thickness is reduced from 80 nm to 20 nm, Q_{ox} improves from 0.3 to 0.8. A possible explanation is that the oxidation time required to insulate the body becomes longer with thicker t_{spacer}, as also shown in the graph, giving more time to the water vapor or oxygen to consume the Si at the bottom of the fin.

The optimized simulated parameters have been used to fabricate different structures and to verify the agreement between simulations and fabrication. The parameters are summarized in Tab. 3.1.

Table 3.1: Optimized parameters for wet oxidation

Optimized parameters		Value
d_{NW}	Distance between SiNWs	1.5 µm
t_{spacer}	Spacer thickness	50 nm
t_{IL}	IL oxide thickness	5 nm
t_{ox}	SiO_2 thickness	350 nm
$D_{etching}$	Si etching depth	100 nm
T_{ox}	Oxidation temperature	1000 °C

The final oxidation time was set directly according to the temperature and targeted oxide thickness. Figure 3.10b shows the comparison of the simulated structures with respect to the fabricated ones. After the calibration, a good agreement was obtained, meaning that the



(a)

(b)

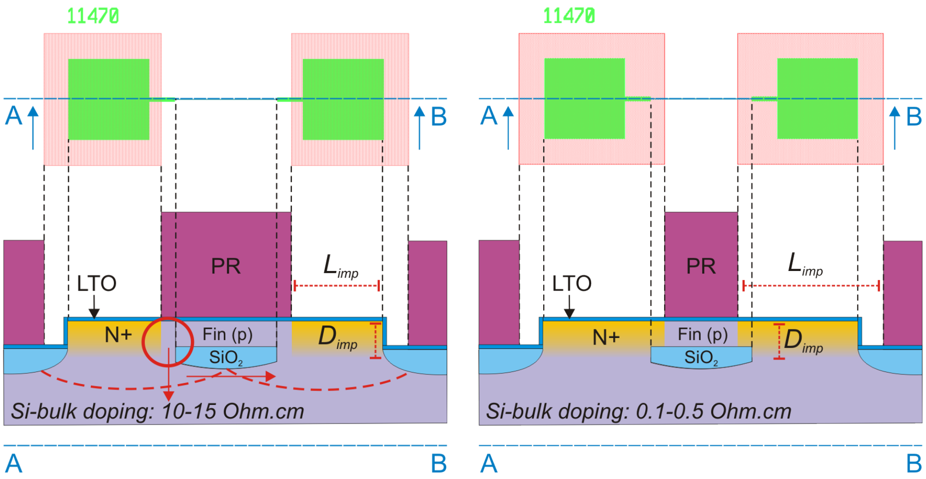
(c)

Figure 3.10: Wet oxidation at different process steps: (a) variation of Q_{ox} and $time_{ox}$, according to t_{spacer}; (b) SEM cross-sections of fins at different process steps: (1) vertical fins with Si_3N_4 spacers, (2) Si exposure by RIE, (3) fins after wet oxidation with SiO_2 between the Si fin and bulk, (4) smallest fin width (13 nm); all insets show the results of simulated processes; (c) fin after oxidation: (5) SEM top view and (6) cross-section of a fin after Si_3N_4 removal.

presented simulations are a reliable tool to design different oxidation configurations and to verify the impact of the change of one variable. This is finally proved by the equivalence of Fig. 3.10b.4 where a sub-15 nm T_{Fin} with $Q_{ox} \approx 0.8$ was first simulated with the optimized parameters and then fabricated in excellent agreement with the simulations. The final dimensions of the fabricated device are $16\,\text{nm} \leq T_{Fin} \leq 40\,\text{nm}$, and $50\,\text{nm} \leq H_{Fin} \leq 120\,\text{nm}$, with H_{Fin}/T_{Fin} always higher than 3. The different T_{Fin} were fabricated starting from $50\,\text{nm} \leq T_{Fin} \leq 90\,\text{nm}$ patterned with EBL, while the different H_{Fin} are a result of a different consumption rate according to the different T_{Fin}. Structures with starting $T_{Fin} \leq 60\,\text{nm}$ were completely oxidized or they did not survive the end of the process. Structures with starting $T_{Fin} \geq 80\,\text{nm}$ resulted still attached to the bulk. Additional tests were performed to evaluate the differences between wet and dry oxidation but no effect was observed on the structures, both in simulation and fabrication. A certain fragility for the longer fins has been identified, mostly in correspondence with the smallest thicknesses, but no correlation was found with respect to the type of oxidation. A future replication of this process should take into account the reduction of L_{Fin} to fabricate more resistent structures.

3.5 Source and drain implantation

Source and drain implantation is an important step for the fabrication process on Si-bulk, since the creation of proper n+ wells, and in turn p-n junctions, is crucial to limit the electron conduction only in the fin channels, avoiding parasitic paths through the bulk. If this step is not attentively carried out, the function of the bulk oxidation, i.e. electrical insulation, is ineffective. Figure 3.11a shows possible leakage current paths which have been observed in the initial non-optimized layouts, while Fig. 3.11b shows the final layout, which has led to the optimal devices. As shown in Figs. 3.11 there are three parameters which have to be taken into account:



(a) Non optimized layout

(b) Final optimized layout

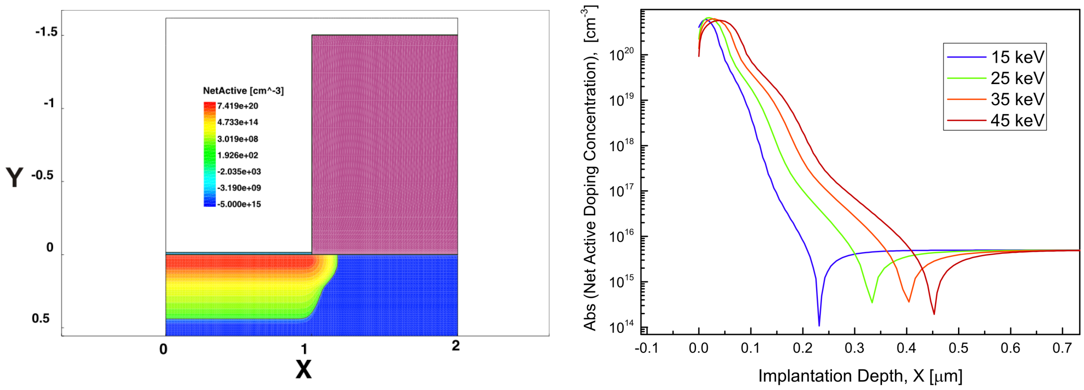
Figure 3.11: Layout strategies: (a) first layout which resulted in leaky devices and (b) optimized layout with no available path for parasitic currents.

1. **Implantation depth**, D_{imp}: it should cover the whole FinFET height but it should not exceed the SiO_2 depth in order to prevent the dopant diffusion under the fin channels. The D_{imp} has been targeted to be about 300 nm.
2. **Implantation lateral extension**, L_{imp}: it should not be limited to the fin-pad connecting section as shown in Fig. 3.11a. Such areas are in fact thicker than the fin thickness

and the oxidation cannot penetrate underlying the Si_3N_4 spacers, leaving a p-type region still connected to the bulk allowing parasitic currents. To avoid that, the regions which are still connected to the bulk should also be doped to create a complete reverse bias p-n junction able to force a unique current flow into the fin channel. The implantation lateral extension has then been extended beyond the fins, as shown in Fig. 3.11b.

3. **Substrate doping**: the p-n junctions created at the interface of the n+ wells and the silicon substrate work properly only for the doping substrate $N_A \approx 1 \times 10^{17}\,\mathrm{cm}^{-3}$. For lower doping concentration $N_A \approx 5 \times 10^{15}\,\mathrm{cm}^{-3}$, the implanted regions undergo punchthrough, a condition where source and drain depletion region merge together causing an uncontrolled current flow and a bad FET operation.

An additional constraint for the implantation is represented by the mask implantation material, needed to screen the whole substrate except from the source and drain areas. Two excellent materials which are conventionally used are SiO_2 and Si_3N_4, but the removal procedure after implantation is not compatible with the SiO_2 grown in the previous steps. It is unreliable to predict how SiO_2 and Si_3N_4 are affected by the implantation and, in turns, to calibrate the etching procedure without affecting the underneath oxide and the Si fins. The photoresist material AZ ECI was then chosen as implantation mask. It is recommended that the thickness of the mask should be at least three times thicker than the implantation depth. Since the target depth is approximately 300 nm, the resist thickness was set to 1.5 µm. Considering all the described constraints, the implantation parameters were simulated by the same FEA tool used for the Si-bulk oxidation. Figure 3.12a shows the simulated substrate after implantation and Rapid Thermal Annealing (RTA), while Fig. 3.12b is the implantation profile for the chosen dose $n_a = 2 \times 10^{15}\,\mathrm{cm}^{-2}$ for different implantation energies.



(a) (b)

Figure 3.12: Example of ion implantation simulations (dose: $n = 2 \times 10^{15}\,\mathrm{cm}^{-2}$): (a) Si substrate after implantation and 10 second annealing with 1.5 µm photoresist as implantation mask; (b) net active concentration profile along the x-axis according to different implantation energies.

The final parameters which were used for the implantation are:

- **Ion species**: Phosphorous - Standard n-type dopant for source and drain implantation.

It can be chosen over arsenic for its smaller mass and wider gaussian implantation distribution, useful for a uniform doping along H_{Fin}.

- **Dose**: $n_A = 2 \times 10^{15}\,\mathrm{cm}^{-2}$ - The value was obtained according to the simulations for a dopant concentration at the surface $N_A \geq 1 \times 10^{20}\,\mathrm{cm}^{-3}$ for ohmic contacts. Higher doses would have also been acceptable, but the maximum implantation current is limited to 100 µA. Higher doses are then only possible by increasing the implantation time, which is not recommended, especially in presence of photoresist.
- **Energy**: 25 keV - The value was obtained according to the simulations to reach an implantation depth included between 300 and 400 nm, as it is possible to observe in Fig. 3.12.
- **Tilt Angle**: 7° - Standard tilting angle used in CMOS fabrication so that ions hit the wafer obliquely, avoiding channeling [7].
- **Rapid Thermal Annealing (RTA)** : 10 seconds, 1000 °C - High activation, reduced diffusion and low defect density are reported for these parameters [8,9]. The annealing was performed in an Ar ambient with a temperature ramp of 115 °C/s.

The implantation was performed at Ion Beam Services in Peynier, France, while the RTA has been performed, in the first place, at Paul Scherrer Institute (PSI) at Villigen, Switzerland and, for the last batches, at the Royal Institute of Technology at Stockholm (KTH), Sweden.

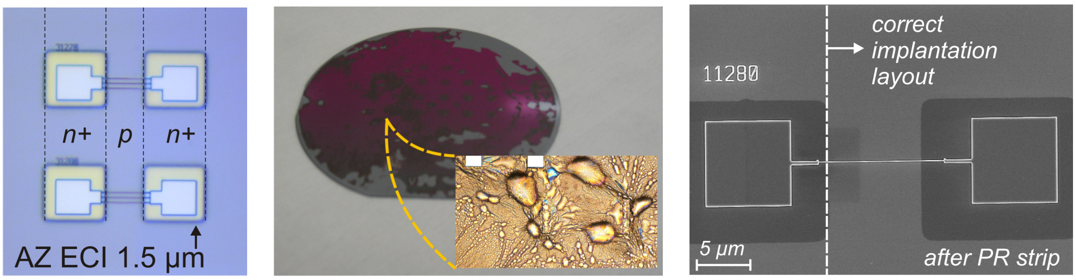
3.5.1 Photoresist removal after ion impact

Before the wafers can be processed with RTA, they need to be cleaned from any organic material. Since the photoresist has been highly overheated during the implantation, its removal cannot be performed in an unique step, as for standard lithography. The direct use of a hot liquid remover (Shipley, Remover 1165) at 75 °C was not able to remove the top hardened photoresist residues, as it is possible to observe in Fig. 3.13b. The correct procedure to totally remove the photoresist is to perform a 20 minute O_2 plasma and then proceed with the Remover 1165. A longer O_2 plasma, i.e. 1 hour, can also achieve a good result, but long ion cleaning are not always recommended for channel exposed devices.

The same procedure was performed in the case of photoresist removal after dry etching by Ar ion milling.

3.6 Photolithography techniques

Each photolithography step of the fabrication process included the fabrication of the corresponding Chromium mask realized by an optical pattern generator based on a fast LASER scanner (Heidelberg, DWL200). The masks were first virtually realized by the layout editor (Tanner EDA, L-Edit) and then converted to a compatible format to allow the transfer to the cleanroom. Before the mask data stream conversion and transfer, the writing parameters were set according to the configuration mode and the wanted resolution. The layout masks were transferred on 5 inch Cr blank mask plates with the following configurations:



(a) (b) (c)

Figure 3.13: Ion implantation photoresist mask: (a) implantation areas according to the final optimized layout; (b) photoresist after implantation processed by immersion in a liquid remover; (c) SEM picture after the correct procedure to remove the implanted photoresist with no residues.

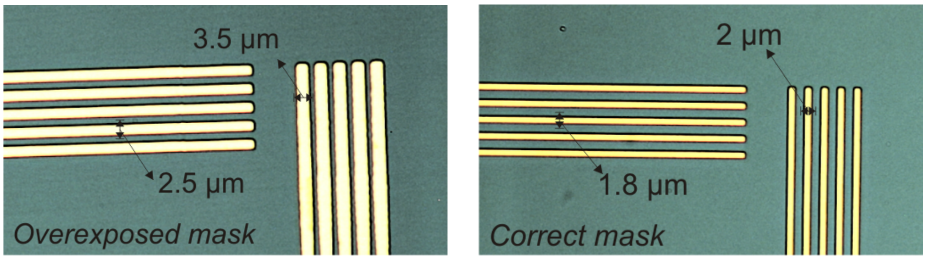
- **DIO 4.04**: Gaussian spot size of 0.8 µm (4 mm head), 4 beams, LASER Diode (λ=405 nm) for the *Implantation* mask;
- **KRY 4.04**: Gaussian spot size of 0.8 µm (4 mm head), 4 beams, Krypton gas LASER (λ=413 nm) for the *SU-8* mask;
- **KRY 2.04**: Gaussian spot size of 0.8 µm (4 mm head), 2 beams, Krypton gas LASER (λ=413 nm) for the *Vias* and *Metal* masks.

The configuration choice was done according to the layout critical dimension and density of features. The mask photoresist was then developed (Süss, DV10), the Chromium was etched for 90 seconds in an $HClO_4$ based bath and the remaining photoresist removed (Technistrip, P1316). Simple structures designed on the layout aimed at verifying the resolution after the mask writing. An optical inspection of the test structures as shown in Figs. 3.14 is important to verify the quality of the fabricated mask. A higher tolerance can usually be accepted (Fig. 3.14a) but since the required precision of all the photolithography steps for the FinFET process is demanding, each mask should aim at its best output (Fig. 3.14b). According to the status of the source, a calibration of the laser power may be needed.

All the photolithography steps were realized with a unique type of AZ ECI positive photoresist with different thicknesses (1, 1.5 and 2 µm). The resist was coated (Ritetrack, 88 Series) on a HMDS-treated substrate and exposed in hard contact mode (Suessmicrotec, MA6). Examples of optimized exposure times for Si and SiO_2 are:

- AZ ECI 1 µm: 7.5 s, used for the *vias* mask;
- AZ ECI 1.5 µm: 10.5 s, used for the *implantation* mask;
- AZ ECI 2 µm: 9.5 s, used for the *metallization* mask.

The cleanroom humidity, the quality of the photoresist coating and the exposure tool status substantially affect the exposure times. Every photolithography step was carried out together with an exposure test taking into account at least ±4 second variation with respect to the last used value. Moreover, the exposure time for aluminum substrates is strongly affected. Al



(a) Overexposed mask test (b) Correct exposed mask test

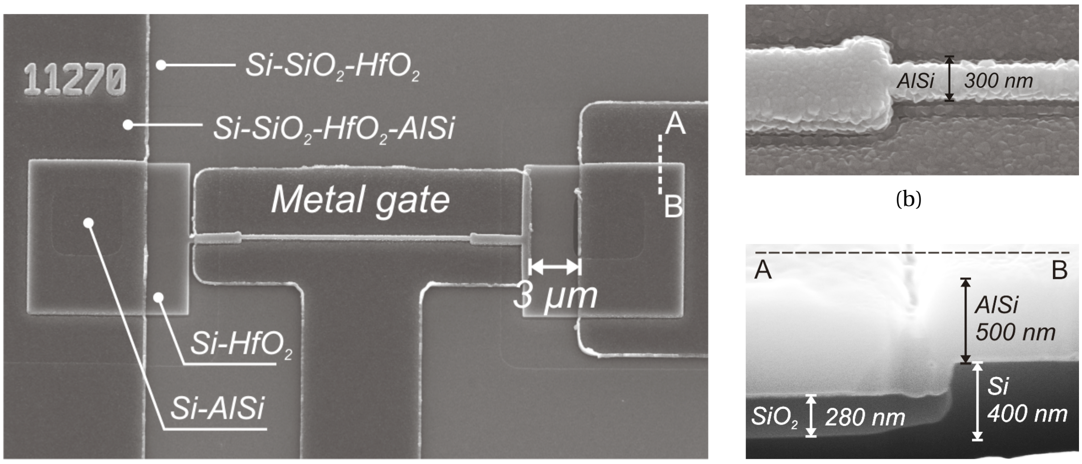
Figure 3.14: Chromium mask test with expected thickness and distance lines of 2 µm: (a) overexposed mask with bigger effect on the vertical lines; (b) correct exposure mask for the critical dimension of 2 µm.

has, in fact, the highest material reflectance in the UV (90%), much higher than polished Si (60%) [10]. The exposure times for Al substrates is usually found to be at least 4 seconds less than for Si substrates.

After exposure, the resist was automatically developed (Ritetrack, 88 Series) and removed by a combination of liquid remover and plasma.

3.6.1 Lift-off for device contacts

A lift-off procedure is used for the metal contacts in order to preserve the device channel from aggressive etching and metallic contamination. Usually, a lift-off process is obtained by a double photoresist (LOR and AZ1512HS), which limits the metal deposition on the vertical resist walls. Despite the numerous tests, it was not possible to achieve the desired resolution of 3 µm with the bi-layer lift-off. Such resolution was required for the metal gates which are in the same layout layer as the connections, in order to avoid an additional mask and a further level of misalignment. The resolution is otherwise achieved with a single photoresist layer (AZ ECI 2 µm), whose compatibility was also tested with respect to the sputtering deposition of 500 nm thick $AlSi_{1\%}$ layer. Such metal, available only by sputtering, is chosen for its 1% content of Si which is used to prevent the Al diffusion into the Si at the vias interface. After the metal deposition, the wafer was left overnight in a bath containing a liquid remover at 70 °C. Additionally, the lift-off can be triggered by the use of a low intensity ultrasonic bath. The final result is shown in Fig. 3.15. The deposited layer is extremely conformal with resolution down to 1.5 µm and neither lines nor corners were affected by the unusual lift-off process. A curing annealing was finally realized at 500 °C for 15 minutes in a N_2 ambient. The metal gate devices can then be tested and, upon successful characterization, as it will be shown in Chap. 5, the process can continue for the realization of the liquid interface.



(a) (b) (c)

Figure 3.15: Lift-off process: (a) SEM picture of a metal gate FinFET with different layer stack; (b) detail of a metallized SiNW and its anchor pad; (c) cross-section at A-B showing the oxidized surface and the pad still connected to the bulk.

3.6.2 SU-8 microfluidic channels

SU-8 is a negative photoresist conventionally used for 3D structures which require high resolution and high aspect ratio thick resists. Its high epoxy content promotes strong adhesion to many different types of substrates and makes the material highly UV sensitive. Because of its aromatic functionality and highly cross-linked matrix, it is also chemically very inert and temperature stable [11]. Even though high aspect ratio structures are not needed in our process, all the other features match the requirements for the insulation layer which should prevent any contact between Al and the liquid. Not only could the potential applied to a metal contact in a liquid environment cause water electrolysis, but Al is also toxic, meaning that a good sealing should be achieved.

The SU-8 coating and patterning can be considered a small fabrication process apart, due to the numerous steps and its complexity. It can be summarized as follows:

- **Coating and soft bake**: Spin coating and baking parameters were calibrated according to the targeted thickness, in this case 2 µm. The spinning speed was set to 1176 rpm and baking time at 130 °C for 1500 seconds. A 15 minute O_2 plasma before the coating is important to prevent adhesion problems after the first soft bake.
- **UV exposure and development**: The SU-8 photolithography was quite affected by the presence of Aluminum. Many SU-8 residues and distorted aperture shapes were observed mainly next to the metal lines. Due to the reflecting power of the metal lines the exposure time needed to be quite short. An exposure time of 2 seconds in constant power modality (CP) was found to be the optimal parameter for the highest resolution. After a baking step of 15 minutes at 100 °C the SU-8 was developed in PGMEA for 1 minute involving the use of ultrasounds at low intensity. The result, shown in Fig. 3.16, is independent from the Al proximity and the SU-8 is completely removed also in the

narrower corners.

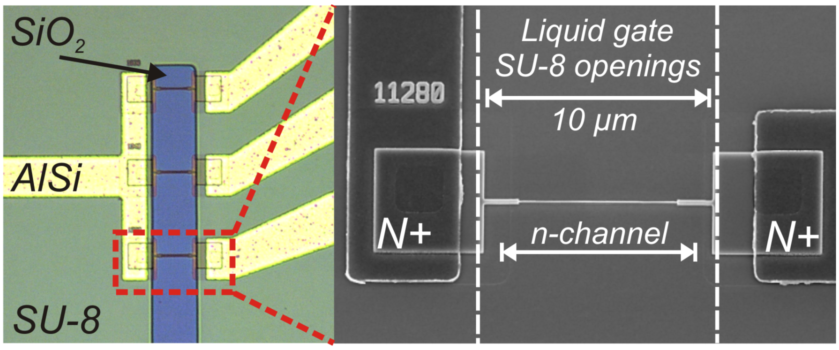
- **Bake-out**: The resistance of the SU-8 was tested after development in different acetone based solution. Once the SU-8 is exposed and developed it should not be possible to dissolve it except with a particular type of chemicals. Nevertheless, a lift-off of the resist was observed in a remover bath, indicating an adhesion problem. The resistance of the layer was also tested by adhesive tape which easily removed the SU-8. Since the SU-8 should stand many hours in an ionic solution, the adhesion needed to be improved. After several tests, a post development bake at 150 °C for 15 minutes made the SU-8 adhesion to the substrate irreversible. Neither the remover at 70 °C nor the tape could detach the resist. This final bake is usually defined bake-out since it is supposed to eliminate any solvent left in the resist. All the baking steps were realized with temperature ramps of 2 °C/min.

The SU-8 patterning is the last critical alignment to be performed. If the microfluidic openings are not perfectly aligned with respect to the device channels the liquid will not be in contact with the p-type regions and the devices will not work, since a non conductive region will divide the n+ source and drain regions from the active channel. Figure 3.16a shows one of the first layouts where the implantation regions (violet area in the optical image) were extremely close to the SU-8 openings with a margin of approximately 1.5 µm. This made the alignment quite critical and laborious. To obtain a good result it was necessary to expose separately the two halves of the wafer. In fact, the wafers resulted bent after the oxidation and, in turn, the alignment marks were less precise towards the center. Taking into account the intrinsic misalignment of the exposure tool and the oxidation bending the layout was adapted in order to have a larger margin of error and not to perform the exposure twice. In Fig. 3.16b it is possible to observe that the distance between the openings and the n-channel has been increased to 5 µm on each side. At the same time the metal lines have also been modified since there should be no risk that the SU-8 apertures leave the metal exposed to the liquid.

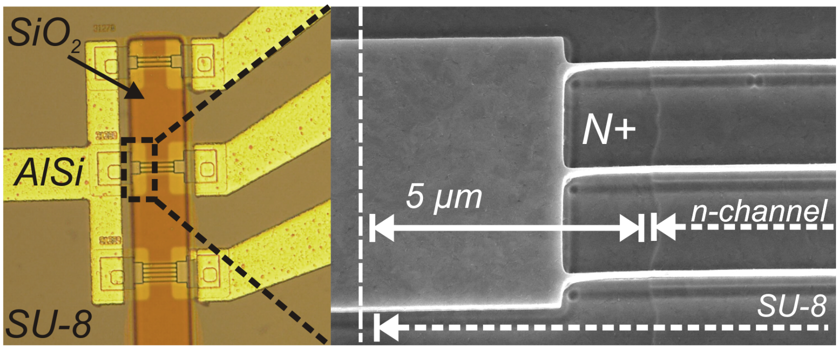
3.7 Wafer layout

The wafer layout is composed of 24 dies. For all the devices, the fin width varies between 50 and 90 nm; after oxidation, it results approximately between 15 and 40 nm. The FinFET length's range is from 8 to 12 µm. Single, three or five parallel wires have been fabricated for each geometrical parameter. Different types of devices are available, all located at the die corners for optimization of the metal connections, as shown in Fig. 3.17a:

1. **Liquid gate FinFET** (sensor): the conduction channel is exposed to the liquid environment through the SU-8 microfluidic channels (Fig. 3.17b). Being n+-p-n+ devices, it is possible to characterize them only by contact with the liquid and a reference electrode.
2. **Metal gate FinFET** (standard transistor): a metal gate allows the device characterization prior to the complex microfluidic platform packaging (Fig. 3.17c).
3. **Two-component amplifier**: connecting one metal gate FinFET and one FinFET sensor



(a) SU-8 openings with small misalignment margin



(b) SU-8 openings with optimized misalignment margin

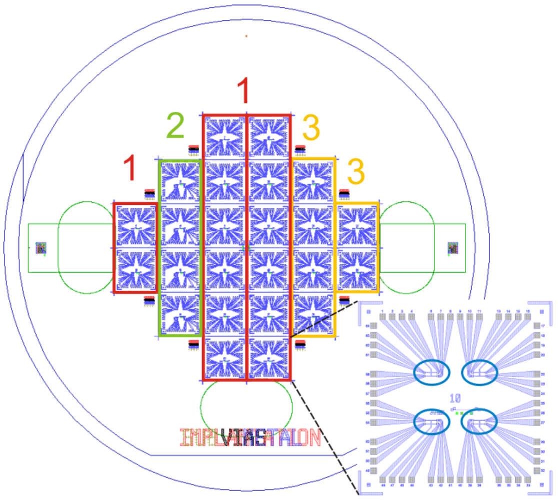
Figure 3.16: Final fabricated FinFETs with SU-8 openings: optical and SEM images of (a) single SiNW FinFET with small misalignment margins and (b) multiple SiNW FinFET sensors with larger superposition of the SU-8 openings and implantation areas.

> it is possible to realize an amplification stage where the sensing variation is amplified at the output. Both enhancement and depletion load amplifier have been realized. Also in this case, in the same die, testing architectures with only metal gate FinFETs are available.

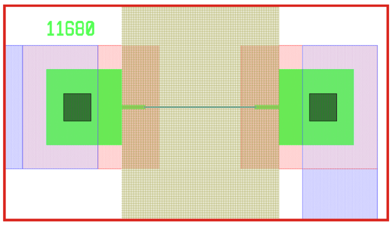
In Figs. 3.17b and 3.17c, five masks can be distinguished: *green* for the definition of the fins, *red* for the implantation areas, *black* for the vias, *blue* for the metal contacts and *golden* for the SU-8 openings.

3.8 Chip-carrier assembly

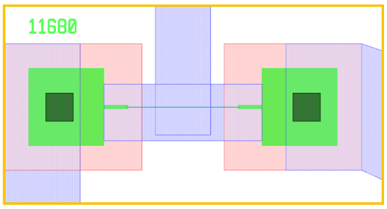
After the SU-8 coverage, a 10 µm thick layer of photoresist was deposited on the wafer frontside to perform a Chemical Mechanical Polishing (CMP, Steag Mecapol, E460) on the backside. The CMP was needed to remove all the material deposited on the back side of the wafer and assure a good ohmic contact. The CMP was in fact followed by the deposition of other 500 nm of AlSi. Without removing the photoresist, the wafer was diced (Disco, DAD-321) and each die was glued to a 64 pin chip carrier by an electroconductive glue (Epotecny, E212), which



(a) Complete FinFET wafer layout



(b) Liquid gate FinFET



(c) Metal gate FinFET

Figure 3.17: Wafer layout and available devices: (a) wafer overview according to the different available devices; (b) liquid gate FinFET sensor and (c) metal gate FinFET

was subsequently polymerized at 120 °C for 15 minutes. The AlSi pads of each die were finally connected to the chip carrier gold pads by ball bonding of Au wires with a 25 µm diameter. Figure 3.18 shows the final assembly with all packaging components and devices. This section ends the fabrication process at EPFL, whereas the microfluidic channels will be described in Chap. 5.

3.9 Summary

This last section briefly summarizes the most important achievements of the *fabrication* of FinFETs.

- **Technical outcomes**:
  - Well-defined vertical FinFET with the following properties:
    - N-channel, fully depleted devices
    - $16\,\text{nm} \leq T_{Fin} \leq 40\,\text{nm}$, $3 \leq H_{Fin}/T_{Fin} \leq 4$ and $8\,\mu\text{m} \leq L_{Fin} \leq 12\,\mu\text{m}$
    - HfO_2 as gate oxide
    - $AlSi_{1\%}$ lines for connections
    - SU-8 protection layer from liquid
    - Estimated final misalignment between layers: $\leq 1.5\,\mu\text{m}$.
- **Main contributions to the field**:
  - Investigation of the Si-bulk oxidation through FEA simulations. A good match between fabricated and simulated devices was achieved. The possibility of relying on a software, especially for such critical step, allows to reduce the time and cost of the fabrication testing procedure;

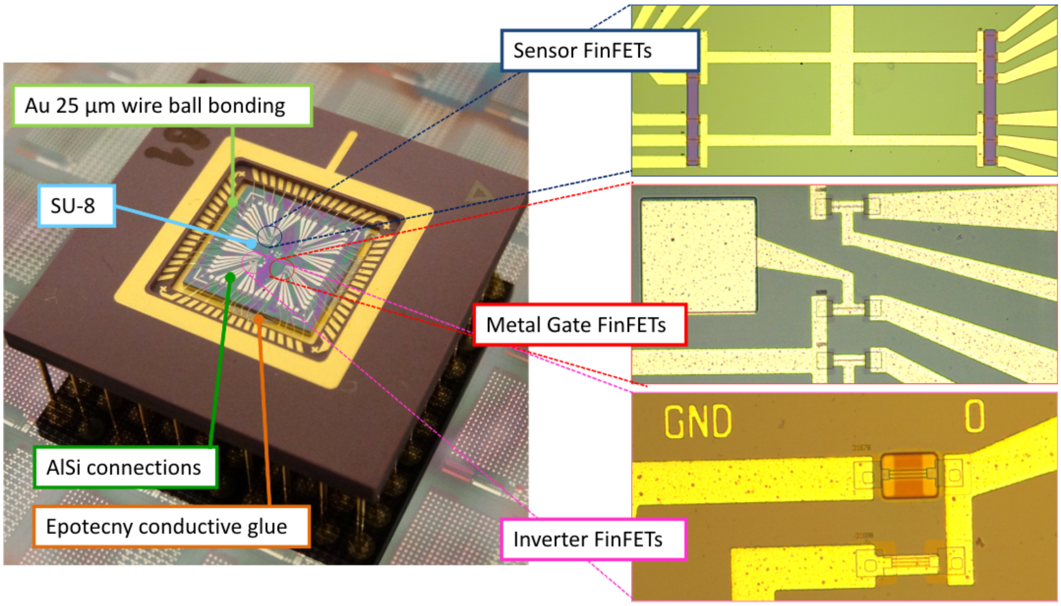


Figure 3.18: Final die connected to a multiple pin chip carrier with the three available devices: metal and liquid gate FinFETs and two-component common source amplifiers.

- Definition of two impacting factors for the correct FET electric behaviour on Si-bulk:
  - Substrate resistivity $\geq 0.1 - 0.5\,\Omega\,\mathrm{cm}$;
  - Extension of the implanted regions to avoid p-type paths into the Si-Bulk.
- Optimization of the existing etching recipes for enhanced selectivity;
- Definition of a lift-off process based on standard photoresist for high resolution and residues-free sensing channels;
- Optimization of the existing SU-8 protocol for stable and robust adhesion.

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4 Characterization of ALD HfO_2 thin layers

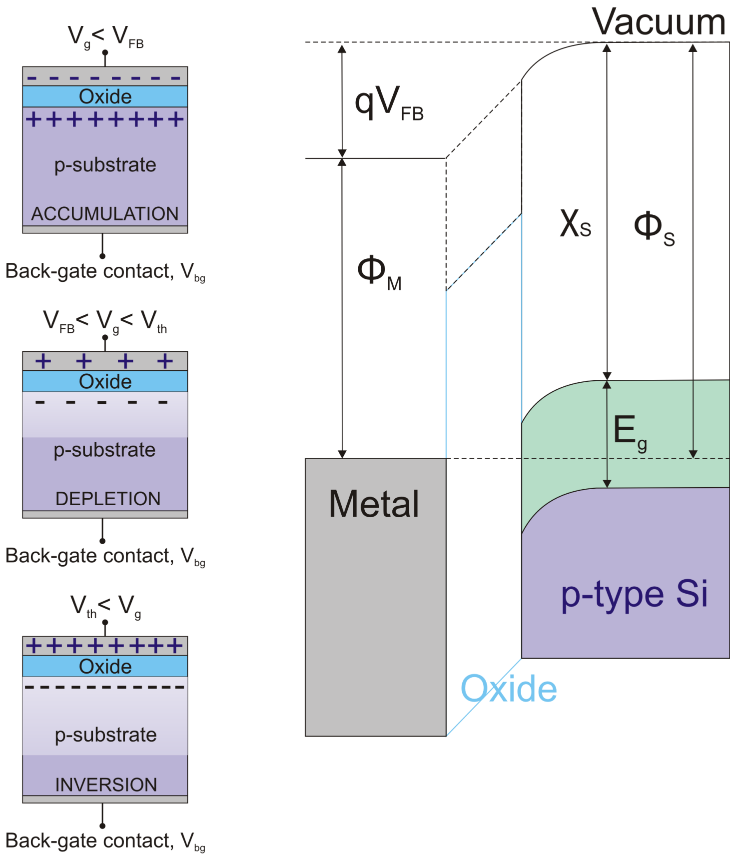
This chapter provides the main results of the electrical characterization of thin layers of HfO_2 deposited by Atomic Layer Deposition (ALD). As it has been introduced in Chap. 1, high-k dielectrics are not only a key-element in CMOS scaling, but they also play an important role in pH sensing applications. In order to implement HfO_2 as sensing gate oxide is necessary to verify its electrical properties, especially for a deposition process not known as thermal oxidation of SiO_2. The characterization has been performed by Metal-Oxide-Silicon Capacitors (MOSCAPs), fabricated, as well as the FinFETs, at CMi, EPFL.
The main objectives of the characterization are:

- Definition of (i) a compatible process flow and (ii) a layout with multifunction testing structures;
- Identification of different estimation methods of the dielectric constant and their outputs;
- Evaluation of the main HfO_2 parameters for the optimization of the oxide quality.

4.1 Description of the MOSCAP

The MOSCAP is a simple structure characterized by complex physical mechanisms happening at the interfaces. Looking at Fig. 4.1a, a MOSCAP is composed of a backside contact, a silicon doped substrate, an oxide layer and, at the top, another metal contact as gate electrode. With no source and drain regions, this structure behaves as a capacitor, preventing the current flow between the two terminals. Figure 4.1b illustrates the band diagram of the MOS structure. The flat band voltage, V_{FB}, corresponds to the gate voltage, V_g, at which the energy band diagram is flat, thus no space charge arises at the oxide-silicon interface. The threshold condition V_{th}, instead, identifies the V_g at which an inverted layer is created underneath the oxide. The voltage applied at the gate defines the three operating regions as shown in Fig. 4.1a:

- **Accumulation**: The device is operating below V_{FB}, thus at $V_g - V_{FB} < 0$. For a Poly-Si gate, a negligible band bending arises, due to the high doping, whereas in the Si substrate



(a) (b)

Figure 4.1: (a) MOSCAP structure for the three different operating regimes and (b) MOS band diagram under depletion bias condition.

the bending expands in a larger region with a smooth gradient. For the metal gate, no bending is assumed. The potential applied at the gate gives rise to a negative charge located at the metal-oxide interface. An equal charge of opposite sign appears at the surface of the silicon, at the silicon-oxide interface. This thin, hole-rich layer is called accumulation layer. The total gate oxide capacitance in accumulation is given by:

$$C_{ox} = C_{acc} = \frac{\varepsilon_{ox} A}{t_{ox}} \tag{4.1}$$

where ε_{ox} is the dielectric constant of the oxide, A the capacitance area and t_{ox} is its thickness. From such value the dielectric constant of HfO$_2$ can be estimated.

- **Depletion**: When a small positive bias is applied at the gate, $V_{FB} < V_g < V_{th}$, holes near the silicon surface are repelled. A negative charge appears underneath the gate oxide and a positive charge of equal magnitude can be found at the metal-oxide interface. While the gate charge is a surface charge, because of the large amount of free carriers, the charge in the silicon is a depletion charge given by ionization of the acceptor atoms. Its extension is called depleted region, which starts from near the interface and, as the voltage increases, broadens towards the bulk. The total capacitance in depletion, C_{dep}, is then equal to the series of C_{ox} and the semiconductor capacitance C_s:

$$C_{dep} = \frac{C_{ox}C_s}{C_{ox} + C_s} \tag{4.2}$$

with

$$C_s = \frac{\varepsilon_{Si}A}{x_{dep}} = \frac{\varepsilon_{Si}}{\sqrt{\frac{2\varepsilon_{Si}}{qN_A\phi_S}}} \tag{4.3}$$

where A is the capacitance area,x_{dep} the depletion width, q is the elementary charge, N_A is the substrate doping and ϕ_S the surface potential.

- **Inversion**: If a larger positive voltage is applied, $V_g - V_{th} > 0$, the surface potential will continue to increase and when the concentration of electrons at the interface become higher than the original doping concentration, the inversion regime begins. The electrons of the inversion layer are mainly supplied by mechanisms of generation-recombination in the depletion region, which are rather slow processes at room temperature. In this regime, the total capacitance of the device is again limited by the oxide capacitance. The capacitance of the inversion layer, is, in fact, very large compared to C_{ox} and, because they are in series, its contribution is negligible. The capacitance of the MOS structure in inversion is theoretically equal to the capacitance in accumulation, thus $C_{acc} = C_{inv}$.

More details on the distribution of charge as a function of the surface potential and silicon depth according to the Poisson's law can be found, for example, in [1]. In order to characterize the devices, the gate voltage is swept from negative to positive voltage, superimposing a small AC signal to the DC bias. According to frequency, different C-V curves can be obtained, as illustrated in Fig. 4.2. At high frequency, i.e. 1 MHz, electrons in the substrate are not generated fast enough to respond to the AC voltage. So, to balance the charge on the metal, the depletion layer width varies with the ac signal. At high frequencies, the minimum capacitance C_{min} in inversion is equal to the depletion capacitance at the maximum depletion depth x_{dmax}:

$$C_{min} = \frac{\varepsilon_{Si}A}{x_{dmax}} = \frac{\varepsilon_{Si}A}{\sqrt{\frac{2\varepsilon_{Si}}{qN_A 2\phi_f}}} \tag{4.4}$$

Therefore, the C-V curve in accumulation and inversion reaches the same C_{ox} value at low frequency, while at high frequency it does not.

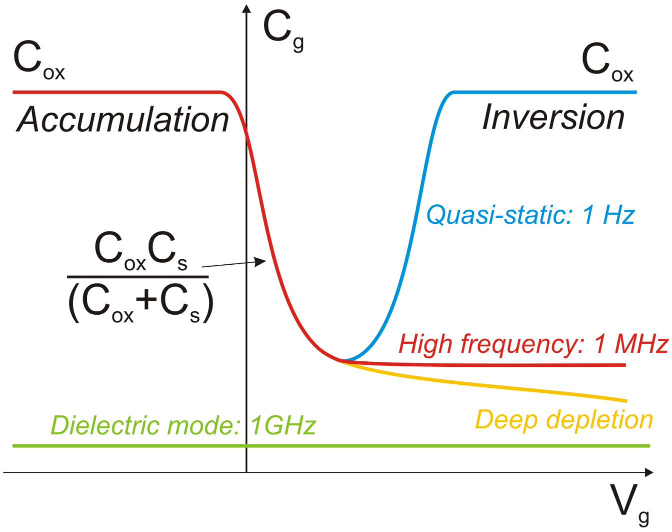


Figure 4.2: C-V curves of the MOSCAP as a function of frequency and regime

4.2 Fabrication process of MOSCAPs

This section describes the fabrication of MOSCAP structures. Two versions of the process are proposed: the former features several photolithography masks including the deposition of a Poly-Si gate. The latter is a one-step process at low temperature, simplified from the original one. Since most of the process steps have previously been described, only the Atomic Layer Deposition (ALD) of HfO_2 is further addressed in details. Specifications of the fabrication tools, chemicals and materials are reported in Chap. 3.

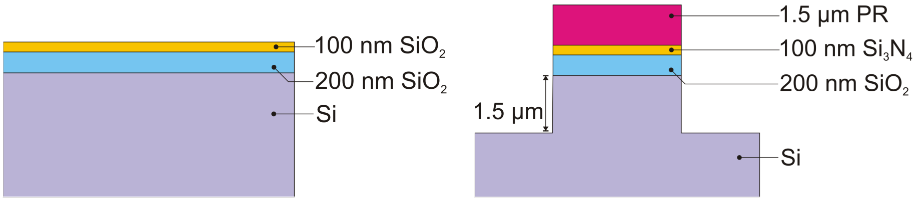
4.2.1 Insulated Si trenches and Poly-Si gate

The MOSCAP structures were fabricated at CMi, as well as the FinFETs. The fabrication process is characterized by:

- **Technology:** Silicon bulk
- **Total number of steps:** 41
- **Total number of masks:** 4 Chromium masks
- **Critical steps:**
  1. CMP for Si-trench insulation
  2. Poly-Si doping by $POCl_3$ diffusion
- **Main cleanroom techniques:**
  1. UV lithography
  2. LPCVD, wet and dry oxidation, ALD, sputtering
  3. DRIE, RIE, wet etching, CMP
  4. SEM, FIB, TEM, mechanical profilometers, spectroscopic ellipsometer and reflectometer

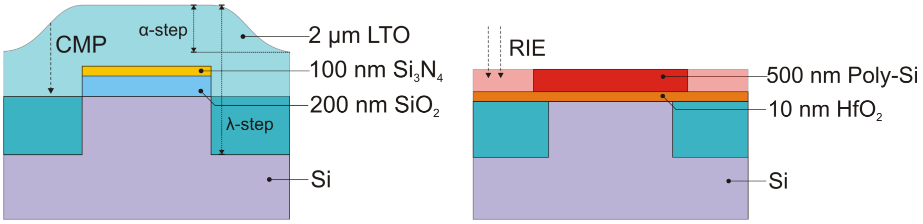
The whole fabrication process can be simplified as shown in Fig.4.3. The starting substrate was a p-type silicon wafer, single side polished, with a resistivity of 0.1-0.5 Ω cm, a diameter of 100 mm and thickness of 525 µm. Two initial layers of SiO_2 and Si_3N_4, respectively 200 and 100 nm thick, were deposited by dry oxidation and Low Pressure Chemical Vapour Deposition (LPCVD, Fig. 4.3a). By Ultraviolet (UV) photolithography and a photoresist layer of 1.5 µm the Si pads was patterned onto the initial stack of layers. Silicon trenches of about 1.5 µm height were transferred from the hard mask into the Si-bulk by Deep Reactive Ion Etching (DRIE, Fig. 4.3b). After the photoresist removal, a 2 µm thick layer of Low Thermal Oxide (LTO) was uniformly deposited (Fig. 4.3c). The combined use of a surface profiler and a spectroscopic reflectometer, simply indicated with α-step and λ-step, was needed to control the Chemical Mechanical Polishing (CMP). Exposed Si pads at the same level of the LTO were obtained (Fig. 4.3c). After RCA cleaning, the ALD of a thin oxide layer was performed according to different parameters under investigation. The gate contact was realized by a 500 nm thick layer of Poly-Si deposited by LPCVD, patterned by UV photolithography and etched by the same RIE recipe used previously for the Si trenches (Fig. 4.3d). The Poly-Si gate was doped by $POCl_3$ diffusion, a technique involving the growth by dry oxidation of an oxide enriched in phosphorous at the Poly-Si surface and consequent dopant diffusion. For the MOSCAPs, the gate is larger than the Si pad in order to be sure that the capacitance area corresponds exactly to the whole pad area previously defined (Fig. 4.3e). MOSFETs are also available in the layout. In this case the size of the Poly-Si gate is smaller than the Si pads and the $POCl_3$ diffusion creates self-aligned source and drain contacts while doping the gate (Fig. 4.3f). For this process there is no need for the precise ion implantation. The doping oxide was removed by a deglaze bath and a layer of LTO of 300 nm can be deposited as passivation layer. At the end, the vias were created by photolithography and by a combined step of RIE and wet etching. $AlSi_{1\%}$ was sputtered and patterned for the metal contacts connecting the Poly-Si gate.

The advantage of this process is the possibility of fabricating MOSFETs at the same time as MOSCAPs, which can add important information to the characterization. The creation of vertical Si trenches guarantees electrical insulation between adjacent devices, especially for the MOSFETs. However, after the first fabrication, the temperature of the Poly-Si deposition and diffusion (≈ 1000 °C) resulted to be incompatible with HfO_2, causing its degradation into completely leaky devices. Figure 4.4a represents the C-V curve of a MOSCAP featuring a 5 nm thick SiO_2 gate oxide grown by dry oxidation, fabricated with the process flow described above. As it will be discussed in Sec. 4.5.1, the result in terms of hysteresis of this layer is excellent. However, as shown in Fig. 4.4b it has not be possible to obtain any C-V characteristics for the MOSCAP featuring a HfO_2 gate oxide. Most probably, at such temperature, the crystallization and densification of the hafnia become so intense that leakage current paths are possible at the edges of the crystallographic grains [2]. Another difficulty observed with this fabrication process concerns the value of ε_{SiO_2} which resulted less than 2, while the expected value is 3.9. The control of the Poly-Si doping is quite difficult and most probably the observed value was lower because of the series capacitance coming from a remaining low doped portion of Poly-Si. It is possible to deposit Poly-Si at low temperature and perform the doping by ion



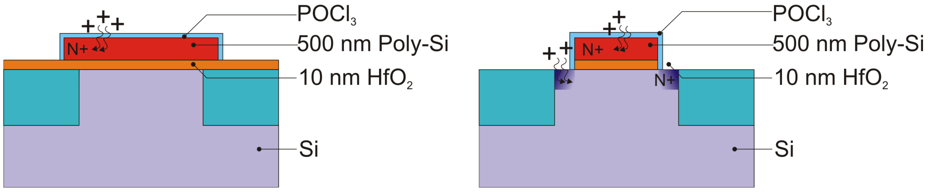
(a) Starting substrate

(b) Si trench



(c) LTO and CMP

(d) Poly-Si gate patterning



(e) Doping by diffusion, MOSCAP

(f) Doping by diffusion, MOSFET

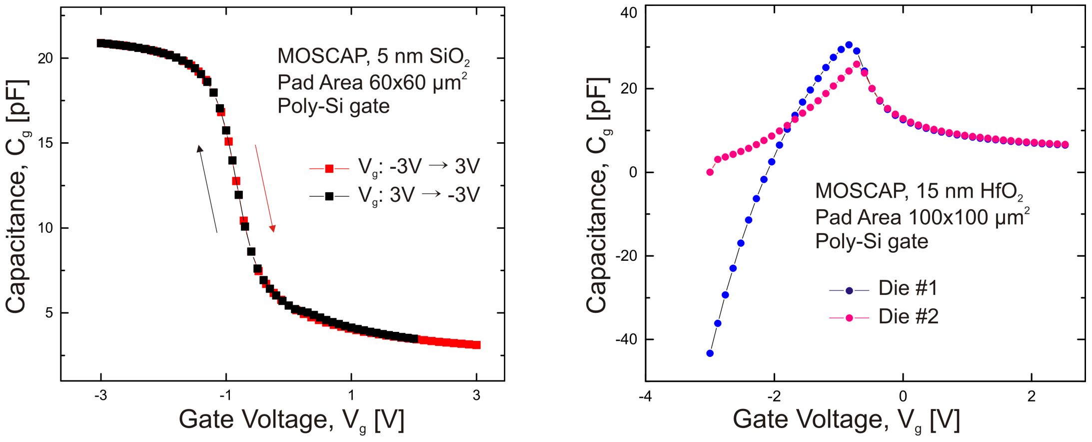
Figure 4.3: Simplified process flow of MOSCAPs and MOSFETs with Poly-Si gate: cross-section draws of MOS interfaces.

implantation, but the process, already quite complex, would have become too long. The characterization of HfO_2 was in fact performed in parallel with the FinFETs fabrication and many parameters should have to be tested before implementing the oxide as sensing gate. For such reasons the process was changed into a one-mask step.

4.2.2 A low temperature process with Al-gate

The simplified, low temperature fabrication process is characterized by:

- **Technology:** Silicon bulk
- **Total number of steps:** 14
- **Total number of masks:** 1 Chromium mask
- **Critical steps:** -
- **Main cleanroom techniques:**
  1. UV lithography
  2. Wet oxidation, ALD, sputtering
  3. DRIE, RIE, wet etching, CMP

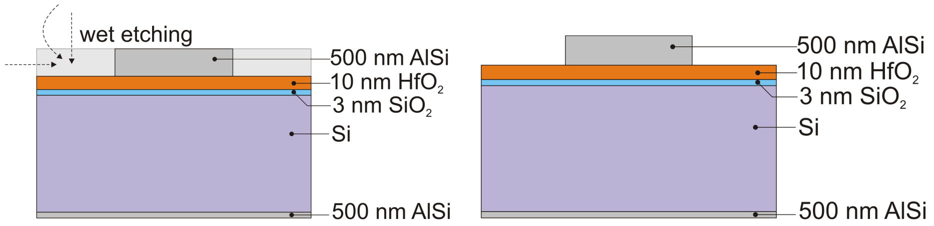


(a) SiO_2 (b) HfO_2

Figure 4.4: C-V measurements for a MOSCAP with (a) 5 nm SiO_2 thick gate oxide and (b) 15 nm HfO_2 thick gate oxide, both fabricated with a Poly-Si gate.

4. SEM, TEM, mechanical profilometers, spectroscopic ellipsometer and reflectometer

The starting substrate was a p-type silicon wafer, single side polished, with a resistivity of 0.1-0.5 Ω cm. ALD was directly performed as first step. According to the type of investigation, a different type of RCA cleaning can be performed before the deposition. Also, an intermediate layer can be deposited in a controlled way, especially SiO_2 by dry oxidation. An $AlSi_{1\%}$ (or Al) layer was then deposited by sputtering and patterned by standard photolithography. The metal gate was etched by a wet solution based on phosphoric acid which allows to process many wafers at the same time. A CMP, to polish the wafer back-side, and a metallization, to guarantee a good back-gate contact, were performed at the end of the process.



(a) Starting layer (b) Metal gate patterning

Figure 4.5: Simplified process flow for MOSCAPs with Al gate: cross-section draws of MOS interfaces.

This process is extremely simple and fast and it allows to differentiate many parameters and to study their impact on the ALD outcome. The absence of the insulated Si trenches does not have any impact on the MOSCAPs, but MOSFETs are no more available. The ε_{SiO_2} obtained after the implementation of this process is 3.7.

4.2.3 Atomic layer deposition of HfO_2

The main challenge of high quality high-k oxides is the deposition. Differently from SiO_2 they do not have the great advantage to be grown by thermal oxidation. As reported in [3], there are several deposition methods, as sputtering, Metal Organic Chemical Vapor Deposition (MOCVD) and ALD. Despite the high quality and absence of defects of MOCVD, only ALD can deposit down to 2 nm with good uniformity. ALD is a method of cyclic deposition and oxidation which can be described in four steps:

1. The surface is exposed to the first precursor which is absorbed as monolayer up to saturation; for the deposition of HfO_2 the first precursor is tetrakisethylmethylamino hafnium (TEMAH) at 80 °C;
2. The excess of TEMAH is removed by purging the reaction chamber with inert gas as N_2;
3. A second precursor, H_2O is pulsed in the reaction chamber reacting with TEMAH and forming a byproduct;
4. The reaction chamber is purged again and the excess of H_2O and the byproduct are removed.

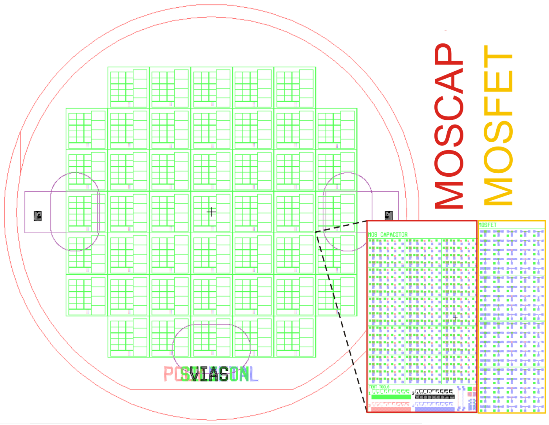
Table 4.1 summarizes the ALD parameters used for the deposition of HfO_2. According to the desidered thickness the four steps were repeated according to the deposition rate (1 Å per cycle for HfO_2). After the deposition, the layer thickness was always verified by a spectroscopic ellipsometer on multiple wafer locations (Sopra, GES-5E). Usually, $\Delta t_{HfO_2} \approx 1.2 - 1.5$ nm has been observed between the set thickness and the measured one.
As it will be shown in the next sections, even a small $\Delta t_{HfO_2} \approx 0.2$ nm can drastically influence the value of the estimated dielectric constant.

Table 4.1: ALD parameters for HfO_2

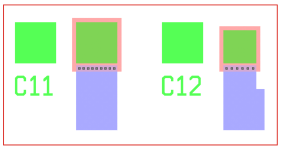
	Temp. [°C]
TEMAH	80 °C
H_2O	Room Temperature
Reaction chamber	200 °C

4.2.4 Layout and fabricated devices

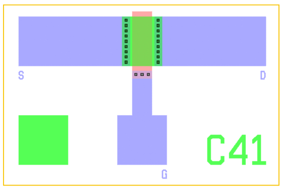
The wafer layout for MOSCAP structures is highly packed with a total of 45 dies, as shown in Fig.4.6a. On each die, MOSCAPs and MOSFETs are available. As previously described in the fabrication process, MOSFETs cannot be fabricated with the one-mask process. In Fig. 4.6b and 4.6c the four masks can be distinguished: *green* for the definition of the Si pads, *red* for the Poly-Si gate, *black* for the vias and *blue* for the metal contacts. For the simplified process either the mask for the definition of the Si pads or the Poly-Si gate can be used, taking into account a different capacitance area for the estimation of ε_{HfO_2}. MOS capacitors of different area are available to verify the capacitance vs area scalability. Some of the final fabricated structures are shown in Fig.4.7a and 4.7b. Figure 4.7a shows two MOSCAPs and a MOSFET



(a) Complete MOS wafer layout



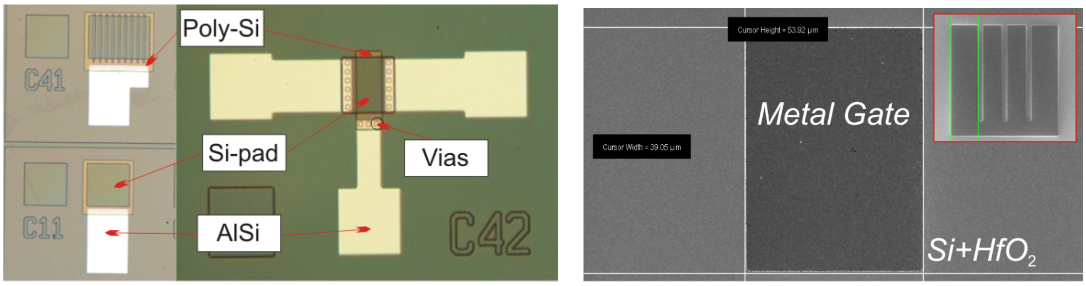
(b) MOSCAP



(c) MOSFET

Figure 4.6: Wafer layout: (a) wafer overview according to the different devices available; (b) two MOSCAPs and (c) a MOSFET.

realized with the more complex process. Fig. 4.7b is a SEM picture of a simple metal gate patterned on a Si substrate after ALD of HfO_2. In the inset of Fig. 4.7b, fingered capacitors are available to test the limit of photolithography and fringing effects.



(a) Poly-Si gate

(b) Metal gate

Figure 4.7: Fabricated MOS devices: (a) MOSCAPs and MOSFET fabricated with a Poly-Si gate and (b) SEM top view of a MOSCAP with Al gate and (inset) a fingered capacitor.

4.3 Measurement set-up and parameters

The measurements performed in this section have been realized at NanoLab, EPFL, with the following instrumentation:

1. Precision semiconductor analyzer (Agilent, 4156A)
2. Low-leakage switching matrix (Agilent, B2200A)
3. C-V meter (Hewlett Packard, 4248A)
4. Light-proof, electrically shielded cascade probe station (Cascade Microtech Inc., Summit 12000)

The HP4248A C-V meter was used to perform C-V measurements. I-V measurements were performed using the B2200A Femto Leakage Switch Mainframe combined with the 4156A Precision Semiconductor Parameter Analyzer. The instruments were controlled by a GPIB connection with a remote computer using the IC-CAP software (Agilent). In order to study the hysteresis effect due to non ideal oxide, the C-V measurements were performed by two continuous voltage sweeps, from accumulation to inversion and vice versa. In Tab. 4.2 the main parameters used for the measurements are reported. The hold time is the waiting time before the starting of the first measure. The integration time is the time of the A/D conversion. The higher the integration time, the higher the resolution. Averaging indicates the number of repeated measurements over which the average is calculated. If it is set to one, the meter will perform single measures. The delay time indicates the time between the triggering and the start of the measurement. The overall measurement time is given by the sum of the integration time, averaging and delay time, all multiplied by the number of measures, plus the hold time.

Table 4.2: C-V meter set-up parameters

Parameter	Value	Unit
Hold Time	5	[s]
Integration Time	20	[ms]
Averaging	8	[N°]
Delay Time	0.5	[s]
AC amplitude	25	[mV]
AC frequency	1	[MHz]

The electrical characterization of HfO_2 thin layers has addressed the following parameters:

- **Dielectric constant**, ε_{HfO_2}: As described by Eq. 4.2, it is estimated from the maximum of the gate oxide capacitance, corresponding to the capacitance in accumulation, C_{acc}. According to the interfacial layer and oxide thickness measurement, as described in Sec. 4.4.1, its estimation can be more or less accurate.
- **Hysteresis**, ΔV_H: The hysteresis is evaluated from C-V measurements performed from accumulation to inversion (down sweep) and inversion to accumulation (up sweep). The gate voltage at which $C_{ox} = C_{acc}/2$ is extracted for both up and down sweep and the difference provides ΔV_H. An alternative common method is to use $(C_{max} + C_{min})/2$ but, being the contribution of deep depletion difficult to be extracted, $C_{ox} = C_{acc}/2$ is adopted for all capacitors.
- **Breakdown voltage**, V_{BD}: The gate voltage V_g was swept from 0 to 15 V in order to evaluate the breakdown voltage. In this case, the leakage current through the device was monitored. The instrument compliance current was usually fixed at $I_g = I_c = 1\,\text{mA}$. The V_g value at which the oxide undergoes the breakdown is clearly visible by the abrupt transition of $I_g(V_g)$ to $I_c(V_{BD})$.
- **Equivalent oxide thickness**, EOT: Given an oxide different from SiO_2, EOT represents what would be the thickness of an equivalent layer of silicon dioxide. In our case, it is defined as:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} t_{HfO_2} \tag{4.5}$$

Moreover, the EOT is a parameter that is directly extracted from the measurement of the oxide capacitance under analysis as $EOT = \varepsilon_{SiO_2}/C_{ox}A$, without involving t_{HfO_2}.

- **Flat band voltage**, V_{FB}: It is extracted from the C-V measurements using the method proposed in [4], i.e. the flat band voltage is the voltage gate where the second derivative of the squared capacitance is zero. A similar method was proposed by [5]. This second method evaluates the second derivative of the inverse of the squared capacitance and it defined the flat band voltage at the maximum value. However, the second derivative in this last method introduces a lot of noise and in some cases the flat band voltage is no longer well defined.

4.4 Characterization of MOSCAPs based on HfO_2

Before entering into the results of the electrical characterization of HfO_2, different estimation methods of the dielectric constant are described. The dielectric constant ε is, in fact, an important parameter reflecting the quality of the oxide. The accurate determination of its value is important for circuit design, where a mismatch between simulated and fabricated oxides may change the circuit output. It is very easy, though, to obtain values which have been under or over estimated, according to the evaluation method and the metrology tools. The thinner the layer, the higher the variance between the methods. Transmission Electron Microscopy (TEM) images can directly provide the real thickness, but it not conceivable to implement such technology for each deposition. The ellipsometer used in the characterization, on the contrary, is not able to provide sub-1.5 nm accuracy especially interfacial layers with uncertain chemical composition. It is then important to know the limit and the complexity of each estimation methods in order to choose the suitable one for the purpose of the characterization and to understand the precision and accuracy of the results.

4.4.1 Comparison of HfO_2 estimation methods

The difficulty in the estimation of the dielectric constant relies in a double challenge of determining the thickness of the deposited layer and the interfacial layer. In a realistic situation, in fact, HfO_2 is not directly deposited onto a silicon substrate but an interfacial layer (IL) is present in between. A large number of publications have reported its presence between the high-k oxide and the silicon substrate [6, 7]. The chemical composition of the IL is complex and mainly depends on the deposition conditions and the presence of a native SiO_2 prior to the deposition [8]. Many works refers to this IL as a silicide, namely $Hf_xSi_{1-x}O_y$ [9, 10]. In the fabrication process described before, this layer is practically unavoidable. Depending on the substrate surface cleaning process, its nature and thickness can vary and, according to post-processing treatments, can be further modified. Figure 4.8 shows the TEM images of the gate oxide stack obtained with different cleaning procedures performed at CMI, EPFL. These images confirm the presence of the interface layer between the hafnium oxide and the silicon surface, whose thickness varies from $0.5\,\text{nm} \leq t_{SiO_x} \leq 1.5\,\text{nm}$. Such layer will be referred to either as IL or t_{SiO_X}.

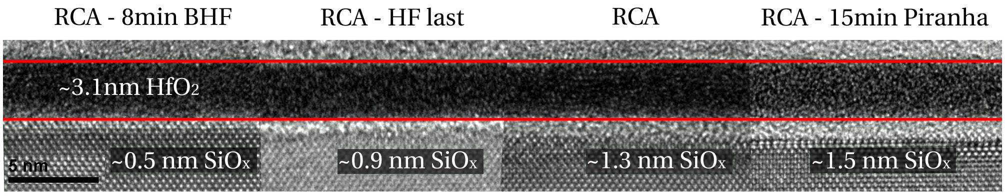


Figure 4.8: TEM image of the gate oxide stack obtained with different cleaning processes (courtesy of M. Zervas, LSM, EPFL).

In order to evaluate the different estimation methods, a HfO$_2$ MOSCAP with the following known parameters is considered:

- Area, A_{pad}: $134 \times 120\,\mu\text{m}^2$
- HfO$_2$ thickness evaluated by the ellipsometer: 8.6 nm
- Capacitance: $C_{ox} = 192.04\,\text{pF}$.

No annealing and a standard full RCA procedure were performed. Moreover, $\varepsilon_{SiO_2} = 3.9$ will be considered.

Method N.1

One simple approach for the estimation of $\varepsilon_{\text{HfO}_2}$ is to consider the HfO$_2$ thickness measured by the ellipsometer after ALD:

$$\varepsilon_{HfO_2} = C_{ox}\frac{t_{HfO_2}}{\varepsilon_0 A_{pad}} \tag{4.6}$$

where C_{ox} is the oxide capacitance in accumulation obtained from the C-V measurements, A_{pad} is the MOSCAP area and ε_0 the vacuum permittivity. Equivalently, the EOT will be:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} t_{HfO_2} = \frac{\varepsilon_{SiO_2}}{C_{ox}A_{pad}} \tag{4.7}$$

After the introduction of the problem related to the interfacial layer it is clear that this approach based only on t_{HfO_2} will provide an underestimated ε_{HfO_2} and an overestimated EOT. However, this method is a quick and costless approach. Assuming that the thickness evaluated by the ellipsometer corresponds entirely to t_{HfO_2}, the resulting ε_{HfO_2}, for method N.1, is **11.6**.

Method N.2

Equation 4.6 can be modified to take into account the IL:

$$\frac{1}{C_{ox}} = \frac{t_{HfO_2}}{A_{pad}\varepsilon_0\varepsilon_{HfO_2}} + \frac{t_{SiO_x}}{A_{pad}\varepsilon_0\varepsilon_{SiO_x}} \tag{4.8}$$

that becomes:

$$\varepsilon_{HfO_2} = \frac{C_{ox}\varepsilon_{SiO_x}t_{HfO_2}}{A_{pad}\varepsilon_0\varepsilon_{SiO_x} - t_{SiO_x}C_{ox}} \tag{4.9}$$

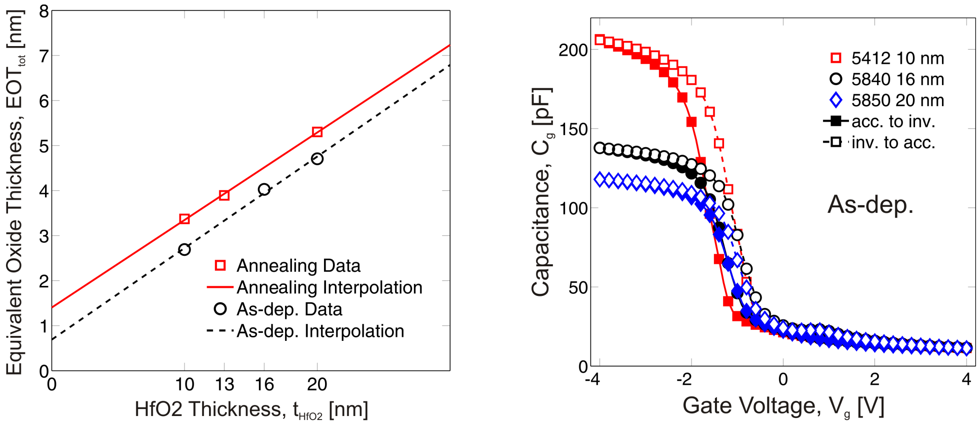
Considering the information on the IL of the TEM image provided in Fig. 4.8, the resulting ε_{HfO_2}, for method N.2, is **17.8**. To understand how much the result depends on small thickness, it is useful to think that by using the IL thickness of full RCA followed by an HF step (0.9 nm instead of 1.3 nm for a simple RCA, as observed in 4.8), ε_{HfO_2} will drop to 14.3. This method is more accurate than the previous one but an extremely precise thickness of both the HfO_2 and the SiO_x layer is needed. Since IL thickness changes during annealing, this method will be applied only for wafers where no annealing was performed and the thickness of IL is known from the TEM images of Fig. 4.8. It is also important to notice that ε_{SiO_x} is unknown. Dedicated studies to its determination [11] have reported low-k values similar to ε_{SiO_2}, thus it will be considered $\varepsilon_{SiO_2} = 3.9$.

Method N.3

A last method of the estimation of ε is provided. From Eq. 4.8 the *EOT* can be written as follow:

$$EOT_{tot} = EOT_{SiO_x} + EOT_{HfO_2} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{SiO_x}}t_{SiO_x} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}}t_{HfO_2} \tag{4.10}$$

If the interface layer is considered to be similar enough to SiO_2, EOT_{SiO_x} can be substituted with its thickness. Otherwise the precise ε_{SiO_x} is needed. From Eq. 4.10 both the interface layer thickness and the high-k dielectric constant can be extracted. Figure 4.9a shows the plot of the total EOT as a function of the HfO_2 thickness. The values were obtained from the C-V characteristics of MOS capacitors with different oxide thickness reported in Fig. 4.9b. From the interpolated curves of Fig. 4.9a corresponding to Eq. 4.10 two important parameters can be extracted: the EOT_{SiO_x}, given by the intercept on the y-axis, and the high-k dielectric constant ε_{HfO_2} extracted from the slope. The EOT_{tot} (y-axis) was calculated from the measured oxide capacitance in accumulation as $EOT_{tot} = \varepsilon_{SiO_2}/C_{ox}$. For the method N.3, the dielectric constant value is found to be **19.2**. Such value is in good agreement with expected values [12, 13] and publications that have used the same model [7, 14]. Moreover, it is possible to observe an increase of the interface layer (EOT_{SiO_x}) after the annealing. For such reason the IL thicknesses of Fig. 4.8 obtained according to different RCA are valid only for not annealed



(a) (b)

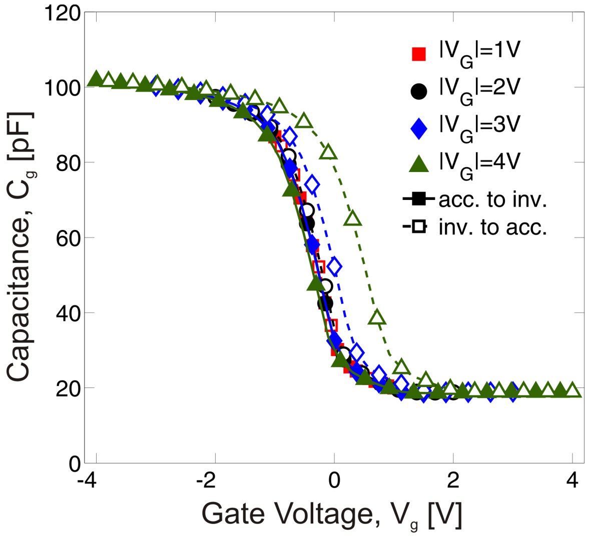
Figure 4.9: Estimation of the dielectric constant using method N.3: (a) EOT$_{tot}$ as a function of t_{HfO_2} for wafer treated with annealing (squares) and without (circles); (b) C-V measurements of HfO$_2$ MOSCAPs with different thicknesses and no annealing (as-deposited).

wafers. Method N.3 and the model expressed by Eq. 4.10 are reliable tools and, if the oxide deposition can be considered linear, it is also possible to plot EOT$_{tot}$ as a function of the ALD cycles. TEM images would provide the highest accuracy, however, the assumption of the linear deposition can be considered a good compromise between the data obtained by TEM and the ellipsometer. The disadvantage of this method is that at least three devices of different thickness are needed.

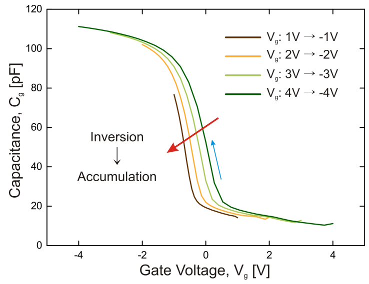
In conclusion, three different methods of estimation of ε_{HfO_2} have been identified. Each of them provide a different accuracy but also a different fabrication complexity. In the following sections, the results of the electrical characterization of HfO$_2$ thin layers will be provided: method N.1, indicated with $\varepsilon^1_{HfO_2}$, will be mainly used to compare the impact of the different factors but, as described, the value of ε_{HfO_2} will result underestimated; method N.2, indicated with $\varepsilon^2_{HfO_2}$, will be used for not annealed wafers and will provide a more accurate ε_{HfO_2}; the use of method N.3 has been limited at the description provided above.

4.4.2 Charge nature of the HfO$_2$ hysteresis

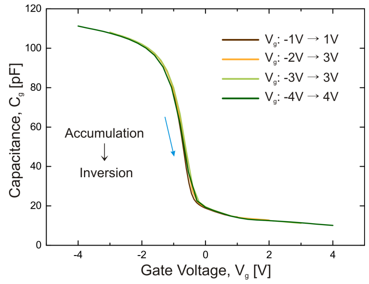
An unfortunate feature of all the Si-HfO$_2$-Al stack is the presence of hysteresis, independently from the type of oxide treatment. A specific hysteretic behaviour was identified. Fig. 4.10 shows repeated C-V measurements of a generic HfO$_2$ MOSCAP. The amplitude of the gate sweep has been varied from $|V_g| = 1$ V to $|V_g| = 4$ V. As expected, the amplitude of the hysteresis increases for higher voltage range, since more charges can be trapped and de-trapped. The total gate sweep was also performed in two separated steps: from inversion to accumulation (Fig. 4.10b) and accumulation to inversion (Fig. 4.10c). In this case it is clear that only the C-V branch from inversion to accumulation is shifted, meaning that the phenomenon mainly consists in a negative charge trapping/de-trapping mechanism at the oxide-substrate interface. Two effects can be seen: (i) the negative charge, that produces the shift of the curve, depends on the voltage amplitude; (ii) this negative charge seems to be completely released when the device is polarized in accumulation, meaning that it does not effect the sweep from accumulation to inversion. This type of behaviour has been reported specifically for HfO_2 [15, 16]. Fig. 4.11 simply describes the charge configuration at the interface in accumulation and inversion. For the reasons just presented, energy states more advantageous for electrons, situated near the oxide conduction band, are depicted at the interface (ellipses with positive signs). This could have a double effect. First, it leads to a higher probability for the electrons of being trapped into the oxide when they are attracted at the interface during inversion, and they are easily de-trapped when the device is swept back to accumulation (Fig. 4.10a). Second, oxygen charged ions can be easily generated [17]. In turns, they will affects the kinetics of oxide annealing and growth of silicon dioxide at the interface, involving a large number of parameters, such as the flat band voltage and the dielectric breakdown. This behaviour, that is probably the main cause of the hysteresis, is similar for the all the analysed wafers, excluding those with thermal SiO_2 that will presented in Sec. 4.5.



(a) Continuous gate sweep



(b) Inversion to accumulation

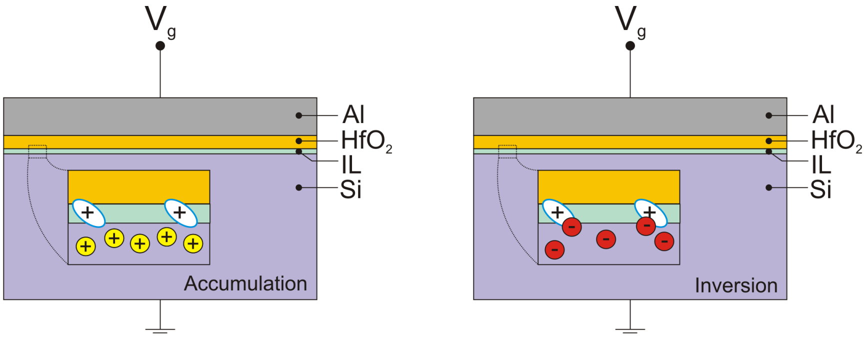


(c) Accumulation to inversion

Figure 4.10: C-V repeated measurements for different sweep range: (a) continuous measurement; (b) C-V branch from inversion to accumulation and (c) from accumulation to inversion.

4.4.3 Impact of annealing treatments

This section analyses wafers with or without annealing performed before or after metallization. For all wafers, a full standard RCA cleaning was performed before the ALD. The comparison is made among wafer 5302, no annealing treatment (as-deposited), wafer 5653, treated with



(a) Accumulation

(b) Inversion

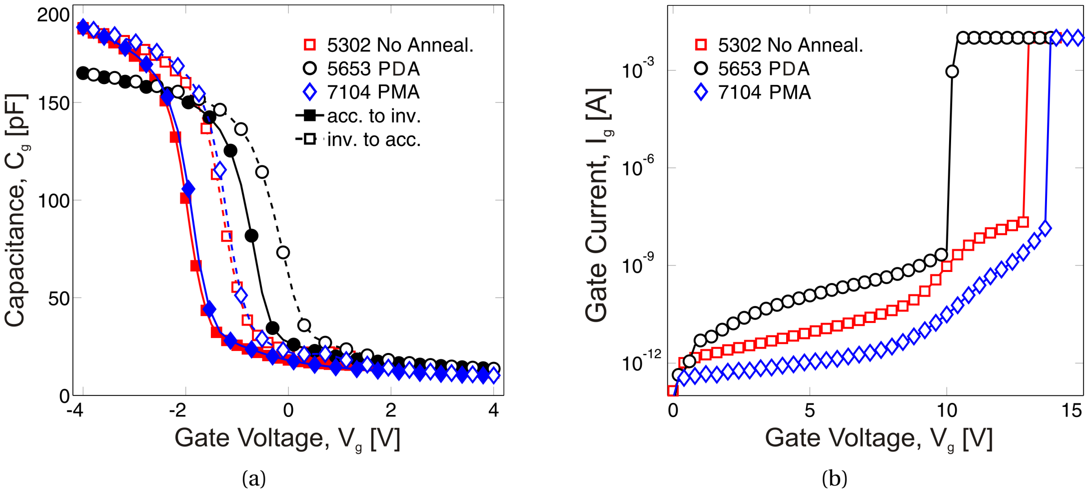
Figure 4.11: MOS charge trapping mechanism: cross-section draws showing the charge configuration in (a) accumulation and (b) inversion.

annealing before the metal gate deposition (PDA, post-deposition annealing) and wafer 7104, treated with the same annealing but performed after the metal gate deposition (PMA, post-metallization annealing). The annealing was performed at 500 °C for 1 hour in N_2 gas environment. For all the wafers the targeted thickness was $t_{HfO_2} = 10\,\text{nm}$. Measurements by the ellipsometer reported a $t_{HfO_2} = 8.6\,\text{nm}$. The results in terms of oxide capacitance, C_{ox}, dielectric constant, $\varepsilon^1_{HfO_2}$ (estimation method N.1) and $\varepsilon^2_{HfO_2}$ (estimation method N.2), EOT, amplitude of hysteresis, ΔV_H, and breakdown voltage, V_{BD}, are reported in Tab.4.3.

According to the EOT values and dielectric constants, the PMA seems not to affect the structure of the gate oxide. The capacitance in accumulation, in fact, reaches the same maximum value with respect to the not annealed samples. The PDA, instead, shows a reduced dielectric constant and an increased EOT, suggesting an increase of the IL underneath the hafnium oxide, in agreement with the observations of Sec. 4.4.1. The increase of the IL has been in fact reported also for such relative low temperatures (such as 500 °C) [10, 11]. Another possible explanation of the lower ε_{HfO_2} is the modification of the HfO_2 crystalline structure after PDA. Moreover, the PDA has a slight positive effect on the amplitude of the hysteresis reducing the trap density in the oxide. Figure 4.12 shows the C-V and the I-V curves of the three reference wafers. In Fig. 4.12a, the annealing performed after the metallization has a negligible effect on the C-V curves. In Fig. 4.12b, the leakage current for the PMA capacitor is one decade lower with respect to the as-deposited wafer and two decades below the PDA wafer. Kim H. *et al.* [18] reported that by depositing thin films of Ti onto a stable metal oxide film which has a high permeability for oxygen (such as ZrO_2 or HfO_2), the interface quality can be

Table 4.3: Effect of annealing on the electrical properties of HfO_2 MOSCAPs

Wafer	Anneal	C_{ox} [pF]	$\varepsilon^1_{HfO_2}$	$\varepsilon^2_{HfO_2}$	EOT [nm]	ΔV_H [V]	$V_{BD}[V]$
5302	No	192.04	11.6	17.8	2.891	0.72	12.4
5653	PDA	166.55	10.1	-	3.334	0.41	10.5
7104	PMA	194.92	11.8	-	2.849	0.69	13.7



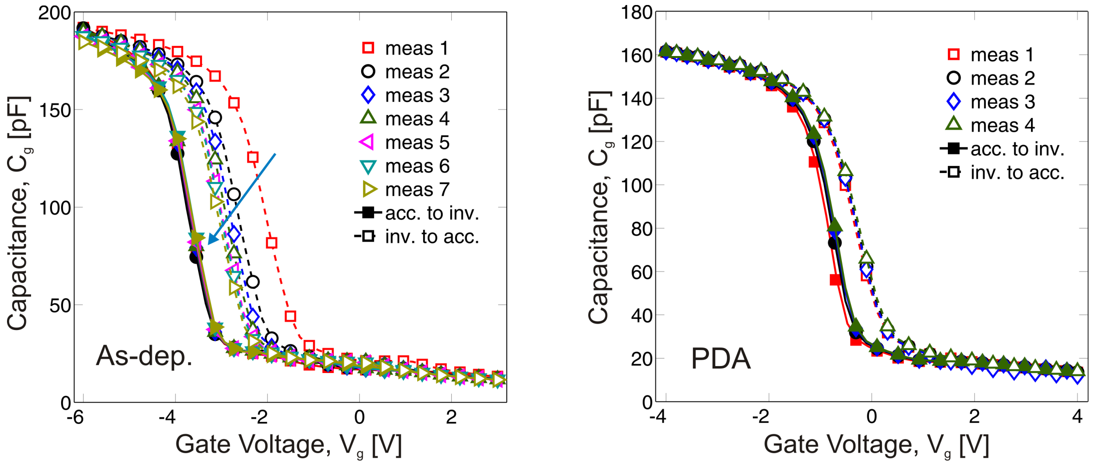
(a) (b)

Figure 4.12: Impact of annealing on the electrical properties of MOSCAPs: (a) C-V and (b) I-V characteristics of wafer 5302 (no annealing), wafer 5653 (annealing before metal gate deposition) and wafer 7104 (annealing after metal gate deposition).

improved. The phenomenon is due to diffusion of oxygen ions from the interface layer across the continuous oxide and dissolution into the Ti overlayer. Moreover, a recent publication [19] have analysed the effect of PDA and PMA and it confirms that the annealing has beneficial effects only if it is carried out after the metal gate deposition, but no comment on the hysteresis have been reported. The decrease of the oxide capacitance for a PDA wafer can be caused by an increase of the IL underneath the hafnium oxide due to oxygen diffusion in absence of a metal cap during the annealing, or an important modification of the crystalline structure. Furthermore, from the C-V curves, it is possible to observe that the annealing modifies the charge inside the oxide, shifting the characteristics towards right. All the three wafers show a counter-clockwise hysteresis, meaning a large trapping/de-trapping mechanism of electrons from/to the substrate [7]. As previously described, electrons are trapped inside the oxide when the device is biased in inversion and then they are released when an opposite bias is applied to the device.

For what concerns the hysteresis, the wafer treated with PDA not only shows a lower value but it is electrically more stable. Fig. 4.13a shows C-V repeated measurements performed on the same MOSCAP. The as-deposited wafer (Fig. 4.13a) shows an hysteretic behaviour which is monotonically reduced by increasing the number of the measurements. The shift of this curve during repeated measurements seems to stop after 6-8 measures. The same behaviour was observed in the wafer treated with PMA. Wafer treated with PDA (Fig. 4.13a) shows more stable curves and no dependence on repeated measurements, confirming the positive effect of PDA in reducing the density of interfacial defects and the instability over repeated measurements [20].

Final outcome: The PDA seems to be beneficial in reducing the density of trapped charges



(a) As-deposited

(b) Post-deposition annealing

Figure 4.13: Repeated C-V measurements: (a) 5302 (as-deposited) and (b) 5653 with annealing prior to metallization (PDA).

and defects at the Si-IL interface. With respect to the other wafers (as-deposited or PMA), the hysteresis is lower and the C-V measurements does not present instability according to the number of performed measurements. On the other hand, the total C_{ox} capacitance is lower, meaning either an increase of the IL thickness or a degradation of the dielectric constant due to a major crystallization.

4.4.4 Impact of RCA cleaning procedures

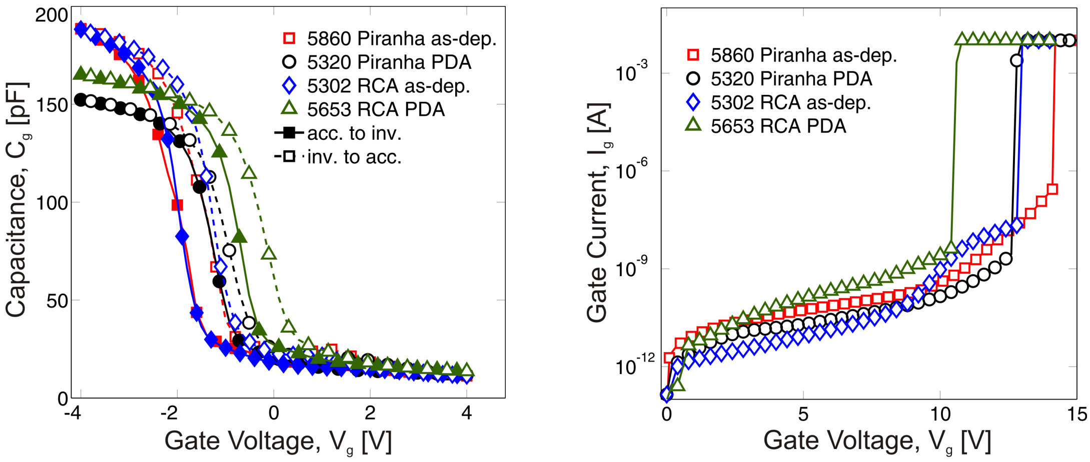
In this section, the impact of the cleaning process on the HfO$_2$ electrical characteristics is analysed. RCA is the standard cleaning procedure used in MOSFET processing. A Full RCA is composed of two steps: RCA1 is a $H_2O : NH_4OH : H_2O_2$ solution that chemically attacks organic impurities while RCA2 is a $H_2O : HCl : H_2O_2$ solution that readily dissolves metal impurities, in particular Fe and Na. Three different treatments have been considered: full RCA, full RCA with additional HF-last and full RCA followed by a Piranha cleaning, which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). Five different types of wafers have been characterized, as reported in Tab. 4.4. The comparison is made among wafer 5302, standard RCA, wafer 5653, standard RCA and PDA, wafer 7130, full RCA and HF-last step and PDA, wafer 5860, full RCA and Piranha with no annealing and wafer 5320 with PDA.

Looking at the results reported in Tab. 4.4, the effect of annealing prevails on the impact of the cleaning procedures. The TEM image of the HF-treated wafer (Fig. 4.8) showed a very low IL that should result in an higher oxide capacitance. But this is not observed. Most probably, the HF surface is not appropriate for the HfO$_2$ deposition, mainly in combination with a post-deposition annealing.

From Fig. 4.14 the effect of the Piranha cleaning after a standard full RCA in presence and not of a PDA can be evaluated. Figure 4.14a shows the results in terms of C-V measurements and

Wafer	RCA	Anneal.	C_{ox}[pF]	$\varepsilon^1_{HfO_2}$	$\varepsilon^2_{HfO_2}$	EOT [nm]	$\Delta V_H[V]$	$V_{BD}[V]$
5302	Full	No	192.04	11.6	17.8	2.891	0.72	12.4
5653	Full	PDA	161.41	9.7	-	3.38	0.44	10.5
7130	Full+HF	PDA	152.19	9.2	-	3.648	0.8	9.1
5860	Full+Pir.	No	192.48	11.6	18.8	2.885	0.6	14.0
5320	Full+Pir.	PDA	155.40	9.4	-	3.573	0.27	12.7

Table 4.4: Electrical characteristics of HfO_2 MOSCAPs treated for different RCA procedures.



(a)

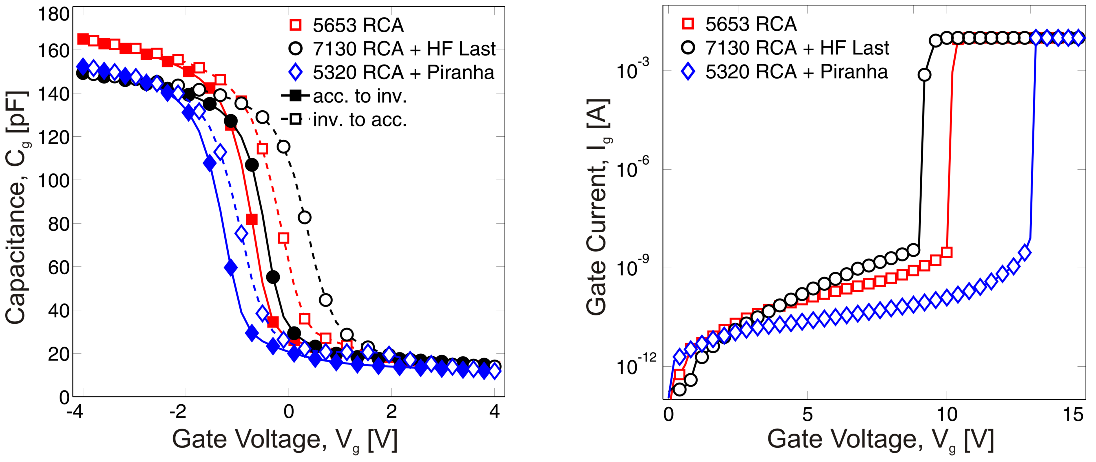
(b)

Figure 4.14: Effect of Piranha cleaning: (a) C-V and (b) I-V characteristics of 5302 (RCA, as-deposited), 5653 (RCA and PDA), 5320 (RCA + Piranha, as-deposited) and 5860 (RCA + Piranha and PDA).

Fig. 4.14b in terms of I-V curves. From the C-V curves there is no a clear independent impact of Piranha over the annealing. As observed before, it is confirmed that the PDA affects some of the oxide features: C_{ox} decreases and V_{BD} is lower. For what concerns Piranha, the most relevant effect is the increase of the breakdown voltage when no PDA was performed.

Figure 4.15 shows the C-V and I-V curves of wafers treated with the three different cleaning processes and PDA. Each IL resulting from the RCA has a different amount of interface charge that produces the shift of the characteristics. The smaller hysteresis and the highest breakdown voltage are obtained for the Piranha cleaning, but in terms of oxide capacitance the best value is obtained for the standard full RCA.

Figure 4.16 shows repeated C-V measurements performed on the three wafers treated with different RCA cleaning processes all with PDA. The measurements were repeated four times on the same MOS capacitor. In accordance with section 4.4.3, the PDA leads to stable repeated curves. In terms of hysteresis, a better result is obtained for the wafer 5320 treated with the Piranha cleaning, as shown in Fig. 4.16c, confirming the result obtained in Fig. 4.15a. The biggest hysteresis and the lowest oxide capacitance were found on wafer 7130 (Fig. 4.16b), suggesting that the HF cleaning induces more fixed charges and bulk oxide traps, that de-



(a)

(b)

Figure 4.15: Effect of Piranha and HF-last cleaning: C-V (a) and I-V (b) characteristics of wafer 5653 (RCA Full), wafer 7130 (RCA Full + HF Last) and wafer 5320 (RCA Full + Piranha).

grade the MOS capacitor. Fig. 4.16d shows the shift of the flat band voltage during repeated measurements on the same MOSCAP. The flat band voltages were extracted as defined in Sec. 4.3. The theoretical value of the flat band is ~ -0.9 V, given by the work function difference between the Al metal and the semiconductor affinity. The flat band voltage is shifted on the left (positive fixed charge) for the wafer cleaned with Piranha (5320), while it is shifted on the right (negative fixed charge) for the other two wafers (5653 and 7130).

Final outcome: Different RCA procedures not only result in a different thickness of the IL, but its chemical nature is different [21], meaning that each IL has different electrical properties as demonstrated by the presented results. By adopting HF cleaning no good results were achieved, thus it is not recommended. Between RCA and RCA+Piranha two differences have been remarked. First, Piranha treatment shows the thinnest hysteresis with respect to the standard RCA, both in case of PDA and not. Second, a higher dielectric constant is observed for the Piranha cleaning for wafer with no annealing[1]. In agreement with the presented results, Green *et al.* [22] have reported that the use of a chemical oxide (the oxide produced by a Piranha cleaning) as IL results in almost no barrier to film nucleation, enabling linear and predictable growth at constant film density, and the most two-dimensionally continuous HfO_2 film.

4.4.5 Impact of the metal gate photolithography

This section describes three different annealing conditions and their impact on the HfO_2 layer. Figure 4.17 shows three different scenarios illustrating when the annealing could be performed during the process: (a) before metal deposition, (b) after metal deposition and

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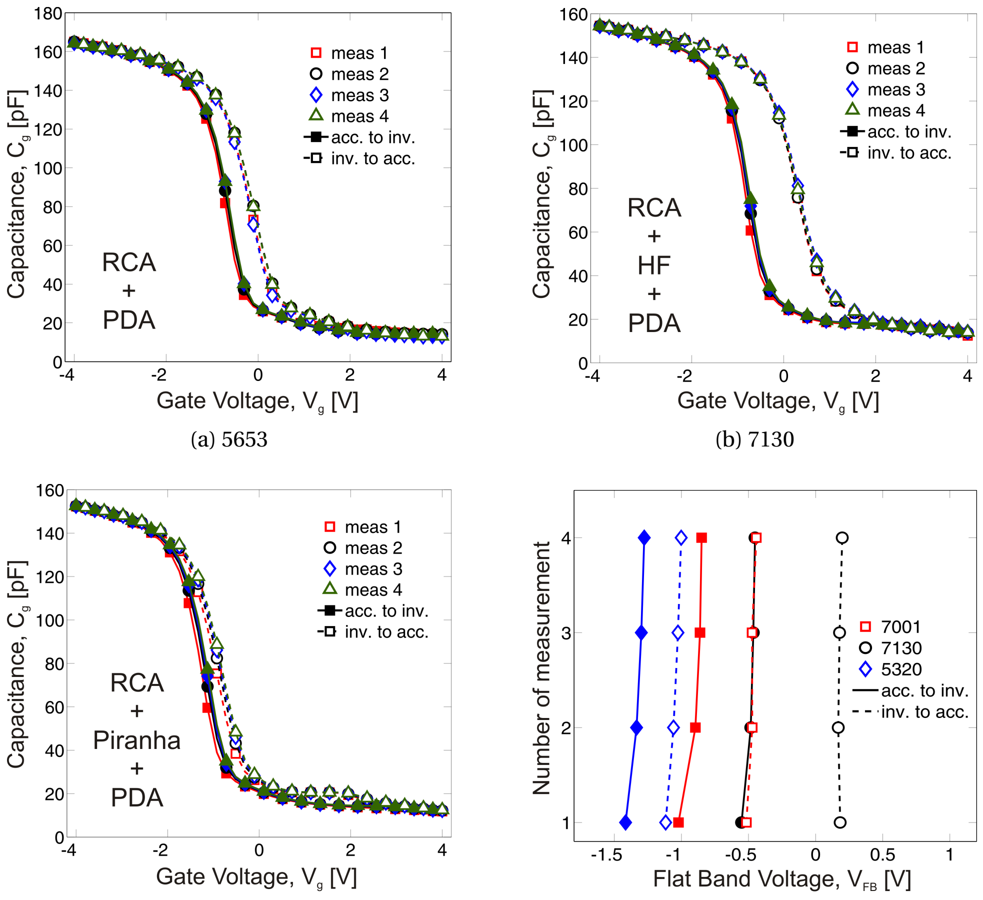
[1] no information on final thickness available in case of PDA

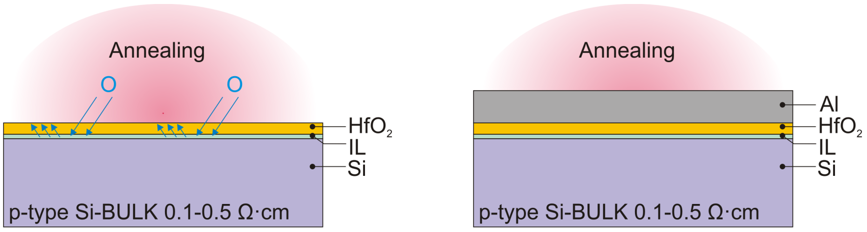


(a) 5653 (b) 7130

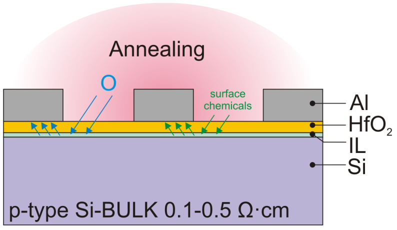
(c) 5320 (d)

Figure 4.16: Repeated measurements for different RCA cleaning procedures: C-V curves of 4 repeated measurements on the same MOS capacitor for (a) 5653 (RCA and PDA, top left), (b) 7130 (RCA + HF-last and PDA) and (c) 5320 (RCA Full + Piranha and PDA); (d) flat band values.

(c) after metal patterning. During the annealing with no metal, the oxygen can diffuse from the atmosphere (especially in absence of a very low vacuum level) through the hafnium, oxidizing the silicon interface. Moreover, if there is an excess of oxygen in the deposited hafnium, this oxygen can act as an oxidation agent of the silicon substrate during the annealing treatment. The mechanism of the IL increase during the annealing is reported for annealing temperature around 500 °C [10, 11] and higher temperature [8, 9]. As a consequence, the gate oxide capacitance decreases. The annealing treatment performed after the metal gate deposition has almost no effect on the capacitor characteristics. To explain the very different behaviours between PMA and PDA, the metal gate, deposited all over the oxide, is supposed to act as a barrier against the diffusion of oxygen from the annealing tube. On the other hand, an improvement of the PDA has been observed on the stability measurements, together with a reduced value of hysteresis. This suggests the PDA can solve interface defects and traps only in absence of the metal layer.



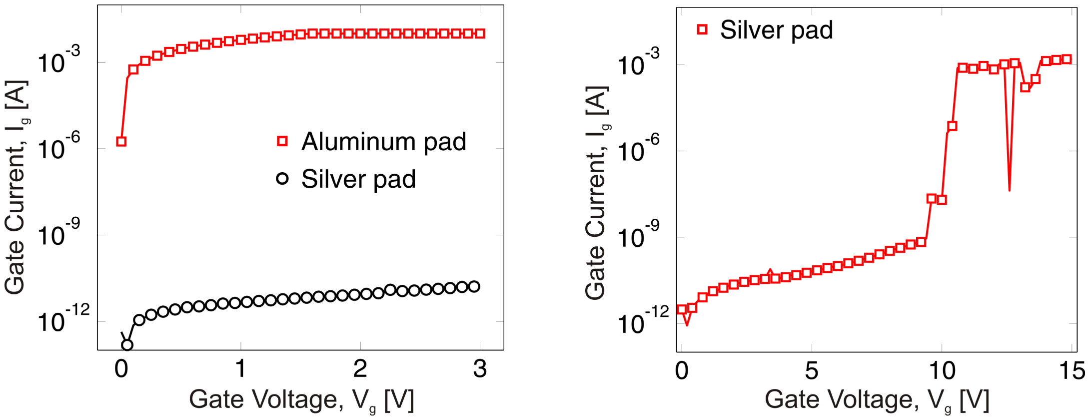
(a) PDA (b) PMA



(c) After Al wet etching

Figure 4.17: Different annealing scenarios: (a) after ALD deposition, (b) after metal deposition, (c) after metal gate etching.

A third particular situation exists, depicted in Fig. 4.17c, where the annealing is performed after the lithography and aluminum wet etching by ANP (Acetic-Nitric-Phosphoric acid). After this annealing, none of the devices were working properly anymore. The measured leakage current through the oxide was very high for very low bias. To verify if the oxide was leaky all over the wafer (were the metal was removed), few metal contacts were created by manually depositing some silver paste. The measured leakage current on these contacts was 9 orders of magnitude lower. The comparison is presented in Fig. 4.18a. In Fig. 4.18b the detailed I-V curve, obtained on the silver pads, looks like all previous I-V curves. An unpredicted reaction may have occured between the chemical reagents remained after the wet etching and the aluminum, producing leakage paths through the oxide. Nevertheless, this unpredicted reaction has happened only in presence of metal contacts, because the oxide was not leaky when measuring the current through the silver contacts deposited after the annealing. This behaviour was also observed for the wafers which were analysed before, treated with PMA and PDA and which were working properly up to this final annealing. A deep chemical investigation of the surface would be necessary to fully understand this phenomenon. Anyway, the assumption of a diffusion and reaction of the chemical agents used in the wet etching for Al (HNO_3, CH_3COOH and H_3PO_4) and Al itself is validated by *not* observing this behaviour: (i) in presence of the manually deposited silver pads and (ii) when the metal was patterned by lift-off instead of the wet etching. All the results that will be presented in Chap. 5 concerning the FinFETs have been obtained adopting the lift-off process and no leakage problem has resulted.



(a)

(b)

Figure 4.18: Effect of annealing after Al wet etching: (a) I-V curves for the standard Al pads and manually deposited silver pads up to $V_g = 3\,\text{V}$; (b) I-V curve for a MOSCAP created with silver paste up to $V_g = 15\,\text{V}$.

4.5 MOSCAPs based on SiO_2/HfO_2 stack

The previous sections have described the characterization of HfO_2 layers directly deposited on Si substrates. An IL layer seems to be inevitably located at the Si interface. Annealing performed at different process step and cleaning procedures have resulted in small changes in the oxide electrical properties. Satisfying results have been reported in terms of dielectric constant, low level of leakage current and high breakdown voltages. Anyway, hysteresis values are still quite pronounced with the lowest value of $\Delta V_H = 0.27\,\text{V}$ obtained for a RCA+Piranha cleaning and PDA. Considering pH sensing the main application of the FinFETs, ΔV_H is still five times higher than $\Delta V_{th} = 56\,\text{mV/pH}$, which is the maximum threshold voltage shift expected for $\Delta\text{pH} = 1$. Here, the integration of a thermally grown thin layers of SiO_2 is described in order to avoid the hysteresis.

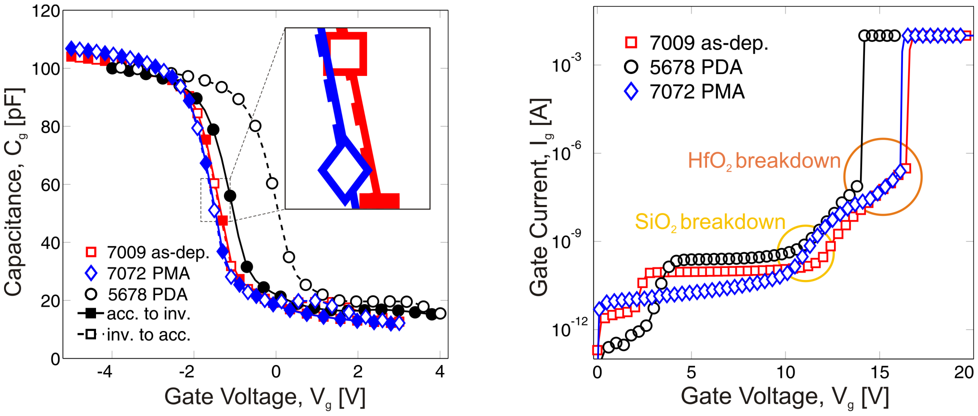
4.5.1 Hysteresis-free MOSCAPs

The interface with the Si substrate must be of the highest quality in terms of roughness and absence of interface defects, especially for oxides that tent to crystallize as high-k dielectrics [3]. Amorphous oxides, as SiO_2, are able to configure their interface bonding to minimise the number of defects and have no grain boundaries. In Sec. 4.4.4 the chemical oxide left by a Piranha cleaning was shown to have a positive effect on the hysteresis. However, the growth control of such oxide can be critical and it has been preferred to grow a precise amount of thermal SiO_2 by dry oxidation, with the scope of achieving low values of hysteresis. About 3 nm of thermal SiO_2 were deposited before the ALD of HfO_2. A standard full RCA cleaning was performed. Two out of four wafers were treated with PDA (5678 and 5319), one wafer was treated with PMA (7072) and the last one was left as-deposited (7009). The main parameters extracted from the C-V measurements are reported in Tab. 4.5. As it is possible to see from the values of ΔV_H, the hysteresis has been reduced to a negligible value, for both wafers without annealing and with PMA.

Figures 4.19a and 4.19b show the results in terms of C-V and I-V measurements: an excellent result is achieved in the reduction of the hysteresis. The thermal SiO_2 reduces the hysteresis because the thermal oxide provides a better surface to deposit the hafnium oxide and the interface traps and surface defects are clearly reduced. Moreover, the silicon dioxide is thicker than the SiO_x-based oxide; this reduces the probability of electrons trapping at the SiO_2/HfO_2 interface and reduces also the effect of the trapped charges on the flat band shift (because they are located farther from the silicon substrate). A $\Delta V_H \approx 10\,\mathrm{mV}$ has been estimated. The annealing performed after the metal gate deposition produces a slight increase of the oxide capacitance and it does not effect at all the hysteresis (Fig. 4.19b). Contrarily, the annealing performed without metal gate restores the hysteresis, as confirmed by both wafers 5678, with $\Delta V_H \approx 0.7\,\mathrm{V}$, and wafer 5319, with $\Delta V_H \approx 0.94\,\mathrm{V}$ (Tab. 4.5). Most probably, the diffusion of oxygen in absence of the metal cap, recreates an uncontrolled IL, most probably at the SiO_2/HfO_2 interface.

Table 4.5: Electrical characteristics of SiO_2/HfO_2 MOSCAPs

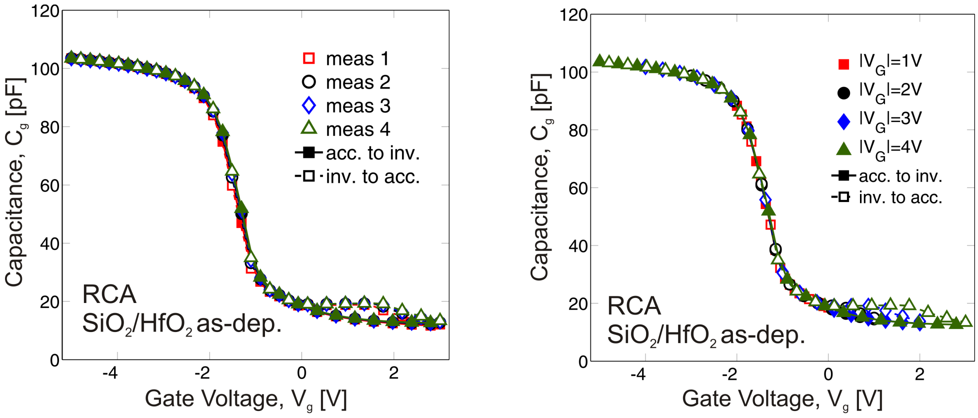
Wafer	Anneal	$C_{ox}[pF]$	ε_{HfO_2}	EOT [nm]	$\Delta V_H[V]$	$V_{BD}[V]$
7009	No	105.18	26.0	5.279	0.009	16.5
7072	PMA	107.20	30.1	5.180	0.012	16.1
5678	PDA	100.22	17.2	5.541	0.686	14.4
5319	PDA	101.37	16.0	5.477	0.943	14.0



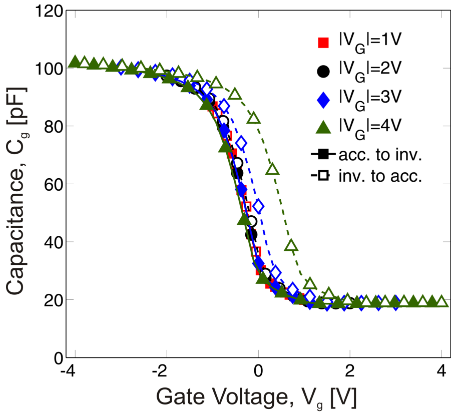
(a) (b)

Figure 4.19: (a) C-V and (b) I-V (right) characteristics of wafer 7009 (as-deposited), wafer 5678 (PDA) and wafer 7072 (PMA).

Looking at the I-V curves of Fig. 4.19b, good values for the leakage current are achieved, always below of the nA range up to $V_g = 10\,\mathrm{V}$. In Fig. 4.19b, it is also possible to distinguish between electrons tunnelling the oxides, directly or by trap assisted tunneling [23, 24], and the



(a) As-deposited (b) As-deposited



(c) PDA

Figure 4.20: C-V repeated measurements for SiO$_2$/HfO$_2$ stack: (a) repeated measurements and (b) sweep range variation for 7009 (as-deposited) and (c) 5678 (PDA).

breakdown voltages of SiO$_2$, around $V_g \approx 11\,\mathrm{V}$, and HfO$_2$, around $V_g \approx 15\,\mathrm{V}$. Figure 4.20a shows C-V repeated measurements on the same SiO$_2$/HfO$_2$ MOSCAP. The wafer without annealing shows a very stable behaviour both for repeated consecutive measurements (Fig. 4.20a) and for different amplitudes of the voltage sweep range (Fig. 4.20b). The same behaviour was observed for the PMA wafer. Instead, the PDA wafer with hysteretic behaviour is dependent on the sweep range (Fig. 4.20c), as remarked also from the previous measurements.

For what concerns the dielectric constants reported in Tab. 4.5, the accuracy of the thickness measurement obtained by the ellipsometer has a great impact on the extracted dielectric constant. Most probably, the SiO$_2$ thickness is overestimated resulting in an overestimated ε_{HfO_2} and EOT as well.

Final outcome: The stack of SiO$_2$ and HfO$_2$ is a very good solution to avoid hysteresis generated by depositing the hafnium directly on silicon. The thickness of the SiO$_2$ layer has to be calculated as a trade-off between the maximum tolerated hysteresis and the minimum dielectric constant needed. Hysteresis-free and electrically stable MOSCAP have been obtained for as-deposited and PMA wafers, but the PDA resulted to re-introduce the restore the hysteretic effect.

4.6 Summary

This last section summarizes the results achieved by the *characterization* of HfO_2 MOSCAPs for its integration as sensing gate oxide for FinFETs[2].

- **Technical outcomes**:
  - *Annealing treatments:*
    - **As-deposited:** Taking into account the IL thickness, $\varepsilon_{HfO_2} = 17.8$ is achieved;
    - **Post Metallization Annealing:** It has a beneficial effect with respect to the as-deposited wafers in terms of leakage current and breakdown voltage, $I_g < 1\,\text{pA}$ and $V_{BD} = 13.7\,\text{V}$;
    - **Post Deposition Annealing:** It has three main effects: (i) smallest hysteresis, $\Delta V_H \approx 0.4V$, (ii) excellent stability in terms of repeated measurements, (iii) increase of the interface layer (of about $\sim 0.5\,\text{nm}$ of EOT) and consequent lower C_{ox}.
  - *Cleaning treatments:*
    - **Piranha:** It has a beneficial effect with respect to the full standard RCA, both in terms of dielectric constant and breakdown voltage, $\varepsilon_{HfO_2} = 18.8$ and $V_{BD} = 14\,\text{V}$;
    - **Piranha with Post Deposition Annealing:** It achieves the minimum hysteresis, $\Delta V_H = 0.27\,\text{V}$;
    - **HF w/o Post Deposition Annealing:** It is not recommended, it results in low C_{ox} and very high hysteresis, $\Delta V_H = 0.8\,\text{V}$.
  - *Thermal SiO_2 as IL :*
    - **As-deposited:** It completely avoids hysteresis, $\Delta V_H = 12\,\text{mV}$, excellent stability for repeated measurements and variations of the sweep range are also obtained;
    - **Post Metallization Annealing:** It does not affect the hysteresis, $\Delta V_H = 9\,\text{mV}$, an excellent stability for repeated measurements and variations of the sweep range are also preserved;
    - **Post Deposition Annealing:** It is not recommended, it restores hysteresis, $\Delta V_H = 0.7\,\text{V}$, but it preserves the stability for repeated measurements.
- **Main contributions to the field**:
  - Design and fabrication of a layout with multiple function devices for the investigation of thin oxides, according to the complexity of the investigation the layout can be partially or fully exploited;
  - Definition of some impacting factors on the oxide, in terms of annealing, cleaning procedures and metal gate patterning;

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[2] results provided as average values

  - Suppression of the hysteresis by deposition of a few nanometers of thermal oxide underneath the HfO_2.

For the implementation of HfO_2 as gate oxide of the FinFETs, a Piranha cleaning after the standard RCA and a post deposition annealing have been performed. The patterning of the metal gate has been realized by lift-off, but the post-metallization has been limited to 15 minutes, only to be beneficial for the conformity of the metal lines. Unfortunately, the implementation of the thermal SiO_2 was not possible, since this result was achieved only after the FinFET fabrication was completed. Nevertheless, it represents the most important achievement of this chapter and should be implemented for the next generation of FinFETs. Also, additional tests should consider the possible of other type of IL, with higher dielectric constant [25].

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5 Experimental Results: Metal and Liquid Gate FinFETs

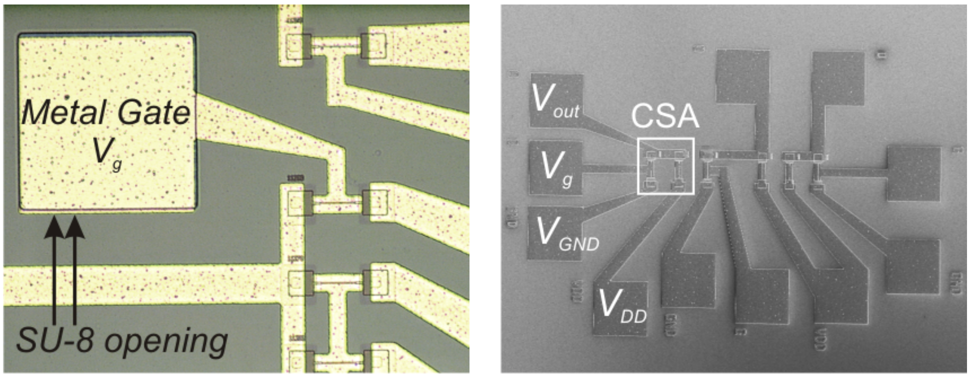
This chapter collects all the measurements performed with the FinFETs fabricated as described in Chap. 3. HfO_2 was implemented as gate oxide, after its characterization presented in Chap. 4. The first section provides the electrical characterization of metal gate FinFETs, whilst the second section presents the main results of the experiments carried out in a liquid environment. The same architecture has been implemented as both sensor and driver transistor. The two FinFET functionalities are combined in a unique physical scenario, through a clear definition of the outputs and the analysis of the results. A conclusive comparison with respect to other works based on SiNWs for sensing applications is proposed.

5.1 Electrical characterization of metal gate FinFETs

The measurements performed in this section have been realized at NanoLab, EPFL, with the following instrumentation:

1. Precision semiconductor analyzer (Agilent, 4156A)
2. Low-leakage switching matrix (Agilent, B2200A)
3. Light-proof, electrically shielded cascade probe station (Cascade Microtech Inc., Summit 12000)

The electrical characterization of metal gate FinFETs aimed at verifying that the devices work correctly and it also provided a valuable comparison with respect to the liquid gate FinFETs. According to the selected fabrication technology, the length of the microfluidic channels was limited to $8\,\mu m \leq L_{Fin} \leq 12\,\mu m$. For comparison purpose, only metal gate FinFETs with the same length were characterized. The characterization was performed after the back-gate contact metallization. Figure 5.1 shows that the metal contacts close to the channel device are still available after the SU-8 coverage. This holds true for single devices, as shown in Fig. 5.1a, and inverters, as shown in Fig. 5.1b. If no potential is applied at these terminals, no chemical reaction is observed when the exposed metal contacts are immersed in the electrolyte solution. The other contacts are located close to the sides of the die for the bonding to the chip carrier pads. For the metal inverters, instead, the contacts are all located close to the device, as it can be seen from the SEM picture in Fig. 5.1b. This is due to the fact that the number of external pads is limited by the chip carrier and all the contacts were needed for the sensing inverter that cannot be measured in the probe station. The potential applied at the terminals are indicated with V_g for the gate, V_{ds} for the source-drain and V_b for the back-gate.

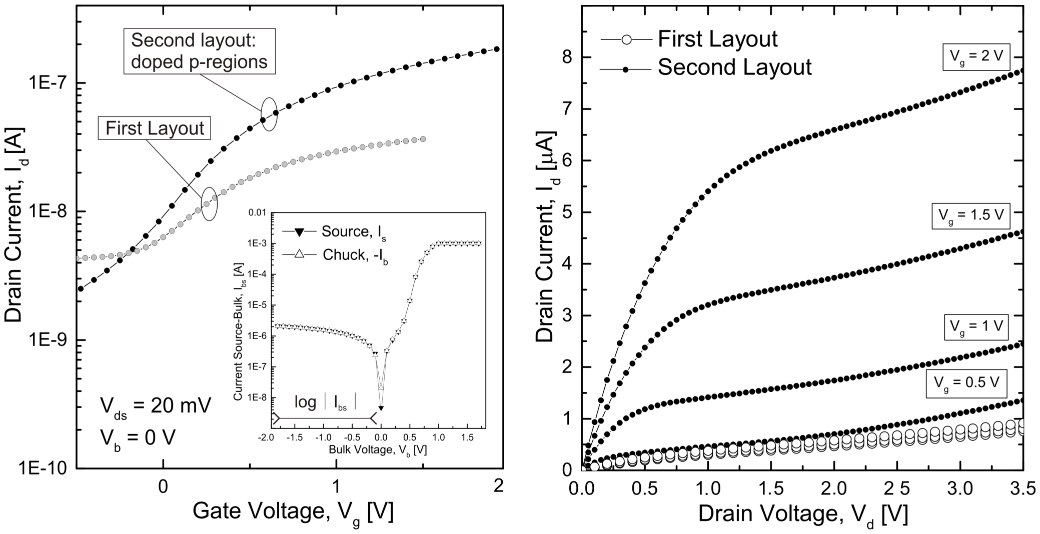


(a) (b)

Figure 5.1: Metal gate FinFETs: (a) optical image of single FinFETs with opening in the SU-8 layer for the gate contact; (b) SEM top view of a common source amplifier (CSA) before SU-8 coverage with terminals in evidence.

5.1.1 Single metal gate FinFETs

As mentioned in Sec. 3.5, the extension of the doped regions as well as the doping of the substrate play an important role in the correct behaviour of the transistors. The graphs in Fig. 5.2a and Fig. 5.2b show the transfer and output characteristics of the first fabricated FinFETs. The first configuration (low substrate doping and small doped regions) resulted in very leaky devices with an I_{off} drain current not lower than 3 nA and, as a consequence, an I_{on}/I_{off} ratio that does not reach one order of magnitude. The $I_d(V_d)$ characteristics of Fig. 5.2b do not show any significant dependence to V_g, meaning that the current flows under the wires through the Si-bulk due to punchthrough. Moreover, the inset of Fig. 5.2a shows that no low current can be achieved when the p-n+ junctions are in a reverse bias with $3\,\text{nA} < |I_{bs}| < 1\,\mu\text{A}$ (inset of Fig. 5.2a), pointing out again a problem of electrostatic control at the bulk level. When the implanted area were extended to the oxidized regions without leaving any residual p-type regions, as it was previously showed in Fig. 3.11a, the FinFET electrical behaviour slightly improved. The $I_d(V_g)$ characteristic reached an $I_{on}/I_{off} \approx 10^2$ and the $I_d(V_d)$ behaved with a certain dependence from V_g. However, the increasing I_d at higher V_d and an excessive value of I_{off} at low V_g are still consequences of a not complete control of the parasitic current through the bulk. To solve this issue, it was necessary to increase the substrate doping from $N_A \approx 5 \times 10^{15}\,\text{cm}^{-3}$ to $N_A \approx 1 \times 10^{17}\,\text{cm}^{-3}$ to prevent the source and drain depletion regions to merge together. The final $I_d(V_g)$ characteristics of the optimized devices are shown in Figs. 5.3a and 5.3b. The following results are largely improved with respect to the previous

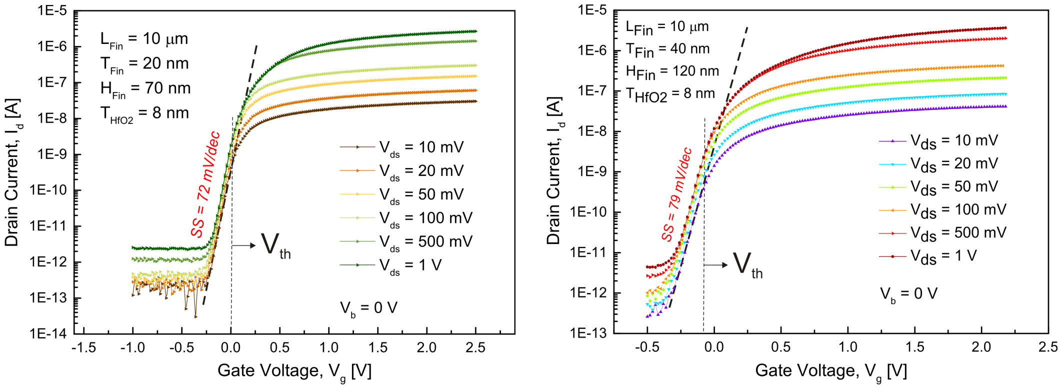


(a) $I_d(V_g)$

(b) $I_d(V_d)$

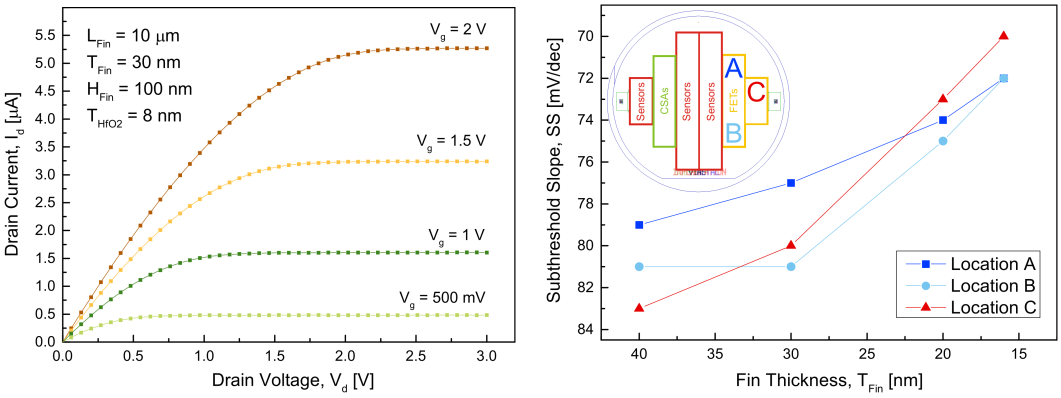
Figure 5.2: (a) $I_d(V_g)$ transfer characteristics for the first and second layout at $V_{ds} = 20\,\mathrm{mV}$ and $V_b = 0\,\mathrm{mV}$; the inset shows the current I_{bs} trough the p-n+ junctions; (b) $I_d(V_d)$ output characteristics for $0.5\,\mathrm{V} < V_g < 2\,\mathrm{V}$ for the two layouts.

ones and define the proper layout and substrate doping for the realization of the sensors. Despite the unusual length for transistors, the metal FinFETs showed excellent $I_d(V_g)$ transfer characteristics for the whole range $10\,\mathrm{mV} < V_d < 1\,\mathrm{V}$. For most values of V_d, an I_{off} close to 1 pA is achieved, which is the current limit of the instrument itself, as it is clearly shown in Fig. 5.3a for $V_g < -0.25\,\mathrm{V}$. As a result, high $I_{on}/I_{off} = 2{\cdot}10^6$ values are achieved at $V_{ds} = 500\,\mathrm{mV}$ and $V_{ds} = 1\,\mathrm{V}$, with $20\,\mu\mathrm{A}$ driving current and $10\,\mathrm{pA}$ I_{off} current. Such a result implies that there are no more parasitic contributions from the Si-bulk and there is only one current path through the FinFET channels. Figure 5.3d shows the subthreshold slope values obtained for different T_{Fin} and according to different locations as illustrated in the inset. The values are in the range $70\,\mathrm{mV/dec} < SS < 83\,\mathrm{mV/dec}$ with the steepest value achieved for the smallest $T_{Fin} = 16\,\mathrm{nm}$. Towards smaller thicknesses the subthreshold slope spread is slightly reduced. Generally, the wet oxidation inevitably introduces small geometrical variations leading to small differences in the electrical properties. Figure 5.3e shows the device transconductance normalized with respect to the fin perimeter. The various characteristics match quite well, meaning that the defined geometrical dimensions are quite accurate. The maximum value is $g_m = 11\,\mu\mathrm{S}\,\mu\mathrm{m}^{-1}$ which is a quite small value limited by the long channel length. Figure 5.3f shows the output conductance g_{ds} which, for $V_g = 500\,\mathrm{mV}$ is in the range $1 \cdot 10^{-8}\mathrm{A\,V^{-1}} < g_{ds} < 2 \cdot 10^{-6}\mathrm{A\,V^{-1}}$.



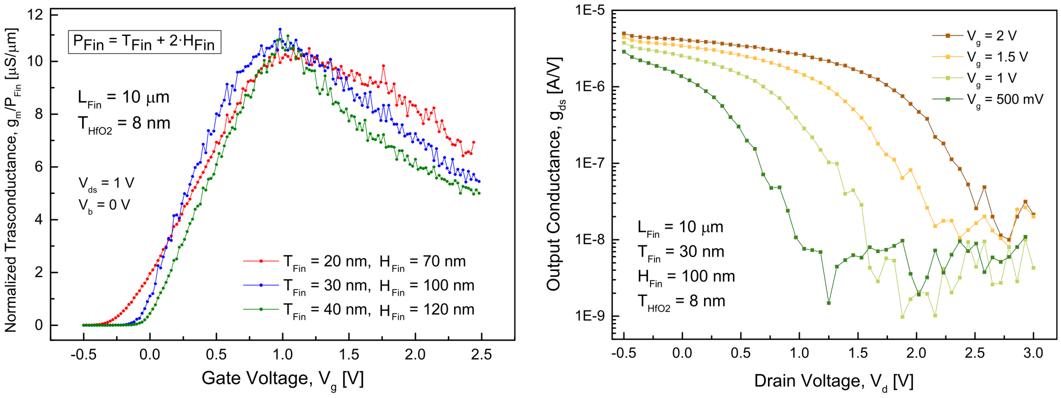
(a) $I_d(V_g)$ for $T_{Fin} = 20\,\text{nm}$

(b) $I_d(V_g)$ for $T_{Fin} = 30\,\text{nm}$



(c) $I_d(V_d)$ for $T_{Fin} = 30\,\text{nm}$

(d) Subthreshold Slope



(e) $g_m(V_g)/P_{Fin}$

(f) $g_{ds}(V_d)$ for $T_{Fin} = 30\,\text{nm}$

Figure 5.3: Electrical characterization of metal gate FinFETs: $I_d(V_g)$ for FinFET with $t_{HfO2} = 8\,\text{nm}$, $L_{Fin} = 10\,\mu\text{m}$, (a) $T_{Fin} = 20\,\text{nm}$ and (b) $T_{Fin} = 30\,\text{nm}$; (c) $I_d(V_d)$ for $T_{Fin} = 30\,\text{nm}$ at different V_g; (d) subthreshold slope $SS(T_{Fin})$ at different wafer locations; (e) normalized $g_m(V_g)/P_{Fin}$ and $V_{ds} = 1\,\text{V}$; (f) $g_{ds}(V_d)$ at different V_g.

Table 5.1 summarizes the final fin dimensions together with their main electrical properties. The fin dimensions are indicated by $\mathrm{T_{Fin_0}}$[nm]/$\mathrm{H_{Fin_0}}$[nm], as defined at the e-beam lithography step before the oxidation, and by $\mathrm{T_{Fin}}$[nm]/$\mathrm{H_{Fin}}$[nm] after. The dimensions have been obtained trough several FIB cuts and $\Delta T_{Fin} = 5\,\mathrm{nm}$ and $\Delta H_{Fin} = 15\,\mathrm{nm}$ have been estimated. The threshold voltage V_{th} has been calculated at the V_g at which the slope tangent dissociates from the $I_d(V_g)$ curve (as shown in Figure 5.3a). This approach gives a good approximation on when the device is leaving weak inversion. For a more circuit-oriented approach the definition used in [1] could be used. As reported in Tab. 5.1 the devices feature V_{th} values close to 0V, according to their dimensions. The definition of depletion and enhancement-mode devices [2] is on the edge of its applicability. In the complex, these devices can be defined as "normally on", i.e. depletion-mode devices, especially because a current level of a few nA at $V_g = 0\mathrm{V}$, is an optimal operating condition for sensing applications.

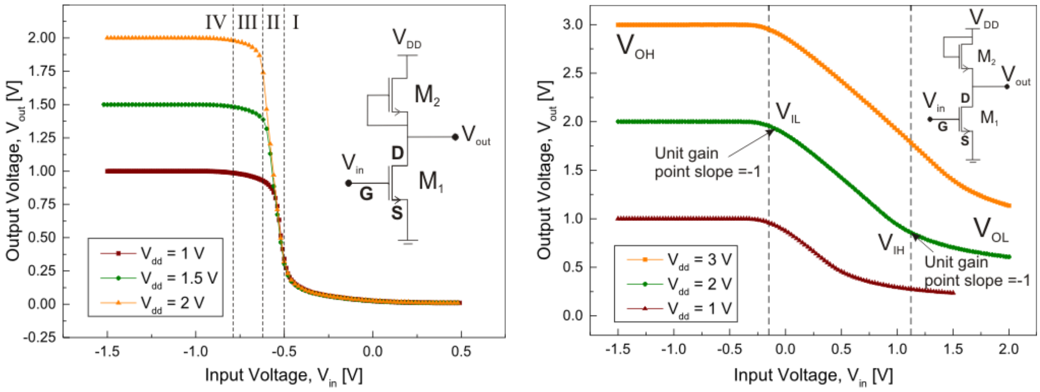
Table 5.1: Electrical parameters of metal gate FinFETs

$\mathrm{T_{Fin_0}}$/$\mathrm{H_{Fin_0}}$[nm/nm]	$\mathrm{T_{Fin}}$/$\mathrm{H_{Fin}}$[nm/nm]	$\mathrm{SS_{best}}$[mV/dec]	$\mathrm{I_{on}/I_{off}}$	$\mathrm{V_{th}}$[mV]
50/220	16/50	70	$1\cdot10^5$	50
60/220	20/70	74	$1.4\cdot10^6$	0
70/220	30/100	77	$1.5\cdot10^6$	-50
80/220	40/120	79	$2\cdot10^6$	-100

The local oxidation technique allowed to achieve an excellent bulk insulation and results comparable to other similar works related to FinFETs on Si-bulk [3, 4] and to some extent improved, i.e. SS values. The extremely reduced fin width also leads to such improvements with respect to other reported FinFETs on SOI [5]. To further enhance the performance of the devices, FinFET length scaling, gate oxide thickness reduction and higher doped p-regions at the junction level have to be considered.

5.1.2 Two-component common source amplifiers

As previously described in Chap. 2, two FinFETs were connected to implement a logic inverter: one FinFET has been used as driving transistor, whereas the second one has been used as load. Fig. 5.4a and Fig. 5.4b show the $V_{out}(V_{in})$ characteristics with both FinFETs fabricated with a metal gate. The difference between the two graphs is the type of connection of the FinFET load: in the schematic of Fig. 5.4a inset, the gate of the load transistor is shorted to the source terminal, while in Fig. 5.4b to the drain terminal. These two connections will be called depletion and enhancement-load, respectively, even tough those definitions technically refer to the type of device and not the connection. As for the single FinFETs, the aim of the characterization is later to substitute one component with a sensor embedded into a microfluidic channel. The two transistors have the same length, $L_{Fin} = 10\,\mu\mathrm{m}$ and $t_{HfO2} = 8\,\mathrm{nm}$, while T_{Fin} differs of about 10nm. In first approximation, the maximum gain of



(a) Depletion-load connection (b) Enhancement-load connection

Figure 5.4: $V_{out}(V_{in})$ characteristics of metal gate amplifiers obtained by connection of two FinFETs with $L_{Fin} = 10\,\mu\text{m}$, $T_{M1} = 30\,\text{nm}$ and $T_{M2} = 40\,\text{nm}$ at different V_{DD}: (a) the gate of the load transistor is shorted to the source terminal, while in (b) to the drain terminal as shown in the insets.

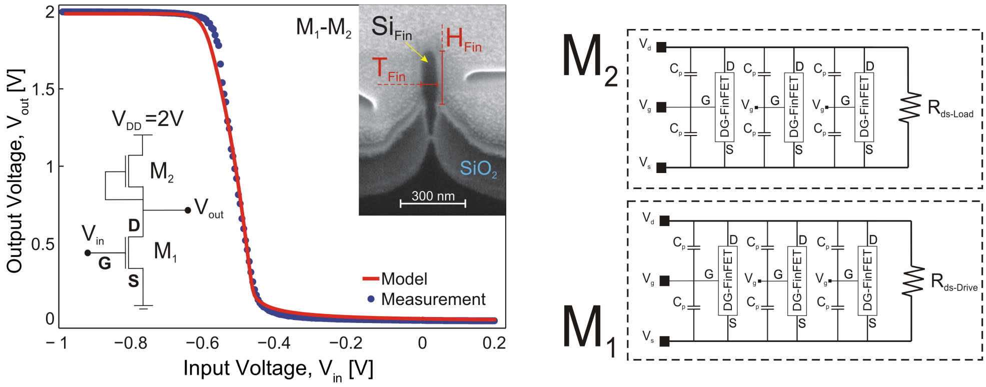
the common source amplifier (CSA) is only proportional to the ratio of H_{Fin}:

$$A = \left|\frac{\Delta V_{out}}{\Delta V_{in}}\right| \propto \frac{L_{M1}}{L_{M2}} \cdot \frac{H_{M2}}{H_{M1}} \propto \frac{H_{M2}}{H_{M1}} \tag{5.1}$$

with $H_{M1} = 100\,\text{nm}$ and $H_{M2} = 120\,\text{nm}$. Figure 5.4a shows that the amplifier realized by the connection of the two FinFETs M1 and M2 can achieve full V_{out} swing between 0 and V_{DD}. According to the basic inverter theory, one can define the maximum input low voltage V_{IL} and the minimum input high voltage V_{IH} at the V_{in} for which the gain slope $\delta V_{in}/\delta V_{out}$ is equal to -1. The more V_{IH} approaches V_{IL}, the more abrupt the transition will be, implying high gain. The value $|V_{IH} - V_{IL}| = 0.15\,\text{V}$ was calculated for the depletion-load connection and it is valid for all V_{DD} values. As expected, for the enhancement-load connection, the value is much higher, being $|V_{IH} - V_{IL}| = 1.2\,\text{V}$, as shown in Fig. 5.4b. Since the transistor M_2 is characterized by a $V_{th} \approx 0\,\text{V}$, such configuration also provides a full V_{out} swing. In the four defined region of Figure 5.4a the two transistors M1 and M2 operate as follows:

- (I) M_1 is in cut-off and M_2 in triode region
- (II) M_1 is in saturation and M_2 in triode region
- (III) M_1 is in saturation and M_2 in saturation
- (IV) M_1 is in triode region and M_2 in saturation

Figure 5.5a shows the match between the circuit simulation described in Chap. 2 and the experimental data. In order to obtain a good match, mainly in the transition region, it has been introduced, at the output of each group of three FinFETs a resistance, $R_{ds-Load} = 27\,\text{M}\Omega/\text{device}$ for the FinFET load and $R_{ds-Drive} = 1\,\text{M}\Omega/\text{device}$ for the FinFET driver, which was not taken into account in the model used in [6]. Gate to source and drain parasitic capacitances, $C_p = 10\,\text{fF}$, have also been added. The implemented R_{ds} values are in agreement with the values shown in Fig. 5.3f and the operating regimes mentioned above. According to the results of the electrical characterization, only the depletion-load connection has been implemented for sensing applications, since no advantages are expected for the other type at this preliminary experimental stage. As demonstrated in Chap. 2, only a high geometrical differentiation between driver and load would produce a significant difference between the depletion and enhancement amplifier.



(a)

(b)

Figure 5.5: (a) Output characteristic of the fabricated and simulated amplifying stage based on metal-gate FinFETs. The Verilog-A model implemented in SPICE simulations is in good agreement with the experimental data; the insets show the schematic of the circuit and a cross section of one fabricated FinFET; (b) schematic of the amplifier as implemented in the simulations.

Thanks to the model implemented for circuit simulations it was also possible to compute the average power dissipated by the two configurations. As expected, for the depletion load circuit it is much lower than the enhancement configuration, with $P_{dep} = 344\,\text{nW}$ and $P_{enh} = 10.6\,\mu\text{W}$, for $V_{DD} = 2\,\text{V}$. Such result highlights another advantage of the depletion mode connection with respect to the enhancement mode.

5.2 Measurements in a liquid environment

In this section, the measurements obtained from the devices operating in a liquid environment are presented. Most of the experiments aimed at pH sensing, with evaluation of some of the important parameters for a sensor, e.g. sensitivity, reliability, stability, accuracy and repeatability. The detection of FimH protein was also demonstrated with preliminary results. The measurements presented here have been performed in collaboration with the Nanoelectronics group of the University of Basel. The following instrumentation has been used:

1. A tubing pump (MCP, Ismatec) for the solution flow;
2. A valve selector system (CHEMINERT VICI, Valco Instruments Co. Inc.) for the exchange of solutions at different pH values;

3. An Ag/AgCl flow through reference electrode (MI-16-702, Microelectrodes Inc.), included in the tubing;
4. A switching box (Keithley, 3706) and a LabView program for automatically measuring up to 48 FinFETs;
5. A source meter (Keithley, 2636) to set the potential at the source, drain and back-gate contacts.

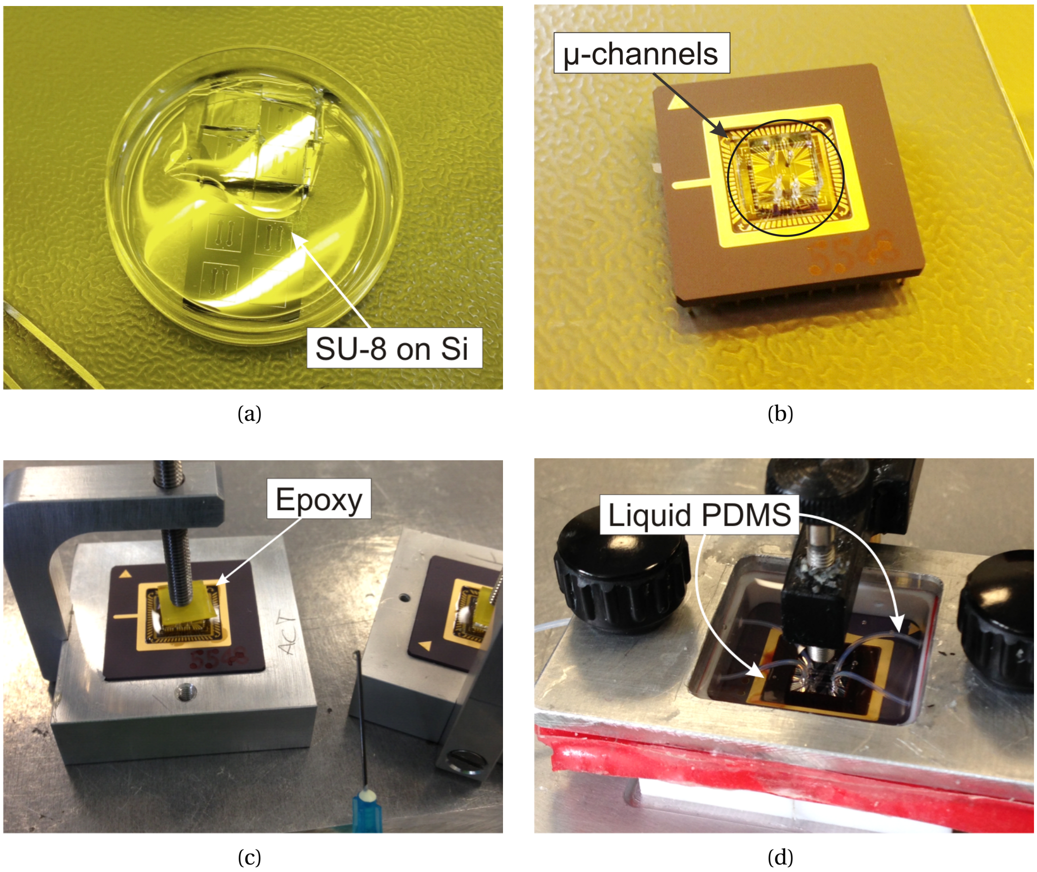
5.2.1 Assembly of the microfluidic platform

Microfluidic channels were produced by pouring polydimethylsiloxane (PDMS) onto SU-8 molds, patterned on Si wafers, degassing and heating at 60 °C for 2 hours. The die-chip carrier complex was cleaned by O_2-plasma (30 W, 33 Pa, 45 s) before the microchannel alignment. The PDMS cubes were extracted (Figure 5.6a) and carefully aligned with respect to the device channels (Figure 5.6b). The microfluidic channels are in fact located at the bottom of the PDMS cube, allowing the electrolyte solution to come in contact with the sensors. The PDMS cube was then fixed by pouring liquid Epoxy, also needed to protect the wires bonded to the chip carrier. In a previous experimental phase, the PDMS cube had only the function of defining the Epoxy contour (as shown in Figure 5.7a) and after removing the cube, the die surface was completely covered by a liquid chamber. The use of the microchannels defined in the PDMS, and the consequent confinement of the liquid, improve the measurement isolation and stability. Once the Epoxy was hardened by annealing at 120 °C for 1 hour, the channels were already correctly aligned. Polytetrafluoroethylene (PTFE) tubes were inserted into vertical holes previously created by a needle, and they were fixed together with the platform into a plastic-metallic support (Figure 5.6b). Liquid PDMS was poured into the support covering the PDMS cube and the PTFE tubes to create a complete embedded system after curing the PDMS at 120 °C for 2-3 hours. Such a system, shown in Fig. 5.7b, is extremely resistent, preserving the electronic components from any liquid leakage and limiting the formation of air bubbles. To perform the measurements the PFTE tubes were finally connected to the flow-through Ag/AgCl reference electrode, the tubing pump and the electrolyte solutions.

5.2.2 Definition of the experimental outputs

As mentioned in the introduction chapter, the sensitivity can be defined in different ways. To adopt a clear and coherent convention throughout all this chapter, the following definitions will apply:

- Threshold voltage, V_{th}: differently from the common definition in electronics, such threshold is here defined according to a specific value of I_d current at which the FinFET slope is constant, thus making the evaluation of ΔV_{th} more reliable.
- Intrinsic Sensitivity, *S*: expressed in mV/pH corresponds to the threshold voltage variation ΔV_{th}, induced by ion surface protonation and deprotonation by changing the pH solutions;



(a) (b) (c) (d)

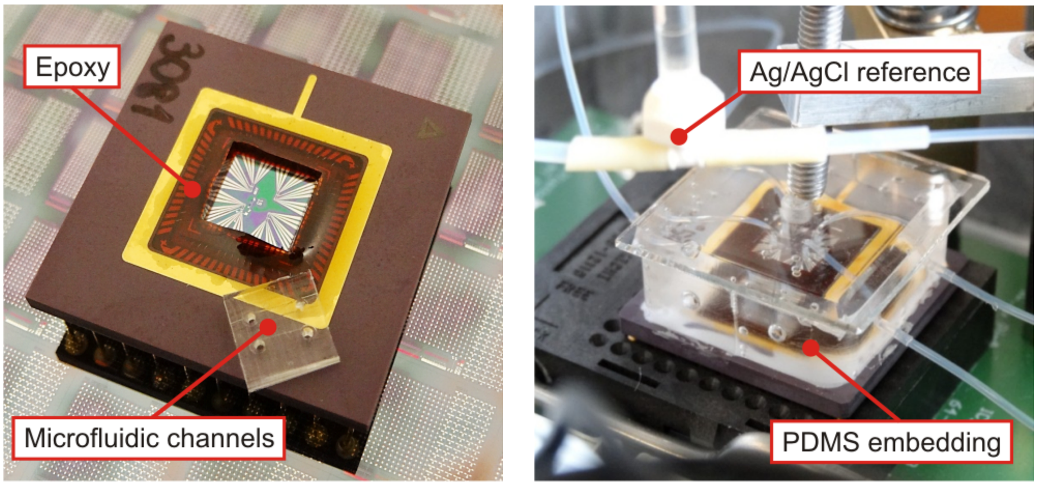
Figure 5.6: Assembly of the microfluidic platform: (a) PDMS microchannels obtained by SU-8 mold patterned onto a Si substrate; (b) device alignment of the pulled out PDMS cube; (c) poured Epoxy with a plastic support to keep the PDMS cube under pressure while hardening; (d) PTFE tubes inserted into the PDMS cube and liquid PDMS deposited all over.

- Relative sensitivity, ΔI_d: expressed in A/pH, is the I_d current variation at a specific biasing point of the reference electrode, V_{ref}, per pH unit change;
- Readout Sensitivity, S_{out}: expressed in percentage, is the relative current variation given by $\Delta I_d / I_{d_0}$, where I_{d_0} is the current before the pH change;
- Standard deviation, σ_{I_d}: expressed in Ampere, is the standard deviation of a population of I_d data $x_1, x_2, ..., x_N$ acquired during a period of time when both V_{ref} and pH are fixed:

$$\sigma_{I_d} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2} \tag{5.2}$$

where

$$\mu = \frac{1}{N}\sum_{i=1}^{N}(x_i) \tag{5.3}$$



(a) (b)

Figure 5.7: (a) Die-chip carrier assembly with the microchannels located at the bottom of the PDMS cube and Epoxy surrounding the Au wires bonded to the chip carrier; in the real platform the PDMS cube is not removed and the whole system is additionally embedded in other PDMS as shown in (b), where the PTFE tubes are connected to the PDMS cube, the reference electrode and the pumping system, while the chip carrier is connected to a PCB for the data acquisition.

Each population of data has been acquired during a time period $\Delta t = 100\,\mathrm{s}$ and sampling rate of 3 Hz. Pumping effects are removed but drift in time contributes to σ_{I_d};

- Signal-to-Noise Ratio, SNR: equal to $\Delta I_d/\sigma_{I_d}$, is an indicator of the accuracy of the measurement;
- Standard Error, $SE_{V_{th}}$: expressed in mV, refers to the standard error of the slope intercept of the population of V_{th} data acquired during the long-term stability measurement. It is an indicator of the V_{th} fluctuation around the slope intercept calculated by linear fit. Differently from σ_{I_d} it is independent from drift in time, which is analysed separately.

The intrinsic sensitivity S is measured in steady-state with the reference electrode potential V_{ref} sweeping from weak to strong inversion region of the transistor. The ΔV_{th} is computed at a fixed $I_{th} = 2\,\mathrm{nA}$. On the other hand, S_{out} was determined for a fixed potential at V_{ref} during time-dependent measurements. Time-dependent measurements are very important for kinetic studies where fast reactions could not be monitored in steady-state. They are also advantageous in the presence of hysteretic effects, which could interfere with small ΔV_{th}, mainly for biological sensing applications. Additionally, according to the read-out, the circuit input could be either a current or a voltage. Therefore, it is important to confront both approaches for a complete investigation. As a general condition for all the measurements, the voltage at the back-gate is set at $V_b = 0\,\mathrm{V}$ to guarantee the p-n+ junctions to not contribute in terms of current.

5.3 pH sensing measurements

Similarly to the characterization of metal gate FinFETs, the liquid gate FinFETs are addressed first as single devices and then as connection of two n-MOS components implementing a logic inverter, where the driver FET is the liquid gate sensor. Biasing the reference electrode at different potentials allows to exploit the different operation regions of the transistor. The results are discussed in terms of the experimental outputs previously defined.

5.3.1 Single liquid gate FinFETs

The first experiments aimed at testing the electrical control of the reference electrode on the FinFET channels. The devices feature the same geometrical dimensions of the metal gate FinFET characterized before, i.e. $T_{Fin} = 30\,\text{nm}$, $H_{Fin} = 100\,\text{nm}$ and $L_{Fin} = 10\,\mu\text{m}$ with an 8 nm thick HfO_2 layer. The transfer characteristic $I_d(V_{ref})$ was measured for $0\,\text{V} < V_{ref} < 1.75\,\text{V}$ at constant pH = 6, as reported in Fig. 5.8a. The liquid gate FinFETs exhibit the same good electrical behaviour as for the metal gate ones, confirming the quality of the bulk oxidation and the p-n+ junctions.

In the majority of the experiments, the liquid gate FinFET characteristic is shifted with respect to the metal gate by a quantity $\Delta V_{sol} \approx 0.75\,\text{V}$. This difference comes at least from two contributions:

$$\Delta V_{sol} = \Delta\Phi_{Al-Ag} + \Delta\chi_{sol} \tag{5.4}$$

where $\Delta\Phi_{Al-Ag}$ is the work-function difference between the Al metal gate and the Ag reference electrode and $\Delta\chi_{sol}$ is the surface dipole potential introduced by the solution [7]. The estimation of those is critical and may be, here, quite rough, especially because the Al used for the metallization contain a percentage of silicon and the reference electrode is covered by AgCl. A reasonable approximation would be considering $\Delta\Phi_{Al-Ag} = 0.5\,\text{V}$ since the values reported in [8] and [9] lead to $0.4 < \Delta\Phi_{Al-Ag} < 0.6$. A shift of $\Delta V_{sol} \approx 0.75\,\text{V}$ was observed at the current $I_d = 1\,\mu\text{A}$, so $\Delta\chi_{sol} \approx 0.25\,\text{V}$ can be estimated. The right Y-axis of Fig. 5.8a reports the $I_d(V_g)$ corresponding to the same FinFET entity, fabricated with a metal gate where $V_{ref} = V_g + \Delta V_{sol}$ applies. This holds true for all the graphs where liquid and metal gate FinFETs are reported together.

Moreover, the liquid gate FinFETs always perform a less steep subthreshold slope, $SS = 180\,\text{mV/dec}$ with respect to $SS \approx 80\,\text{mV/dec}$ of the metal gate FinFETs. With respect to a Metal-Oxide-Semiconductor (MOS) stack, the Electrolyte-Oxide-Semiconductor (EOS) presents additional capacitances at the interface, such as the depletion C_{DL} or adsorption capacitance C_a [10, 11]. The additional capacitances would theoretically affect the subthreshold, being for a MOSFET:

$$SS_{MOS} = \frac{kT}{q} ln(10) \left(1 + \frac{C_{dep} + C_{it}}{C_{ox}}\right) \tag{5.5}$$

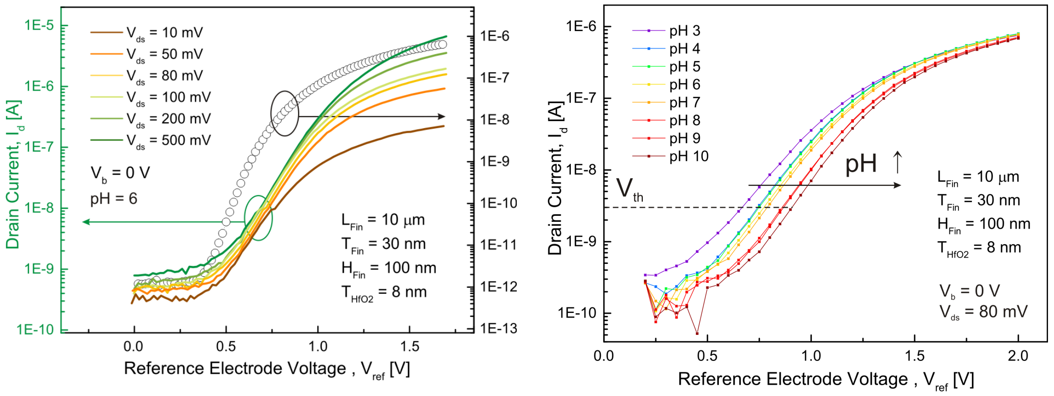
and for a EOS system:

$$SS_{EOS} = \frac{kT}{q} ln(10) \left(1 + \frac{C_{dep} + C_{it}}{C^*_{ox}}\right) \tag{5.6}$$

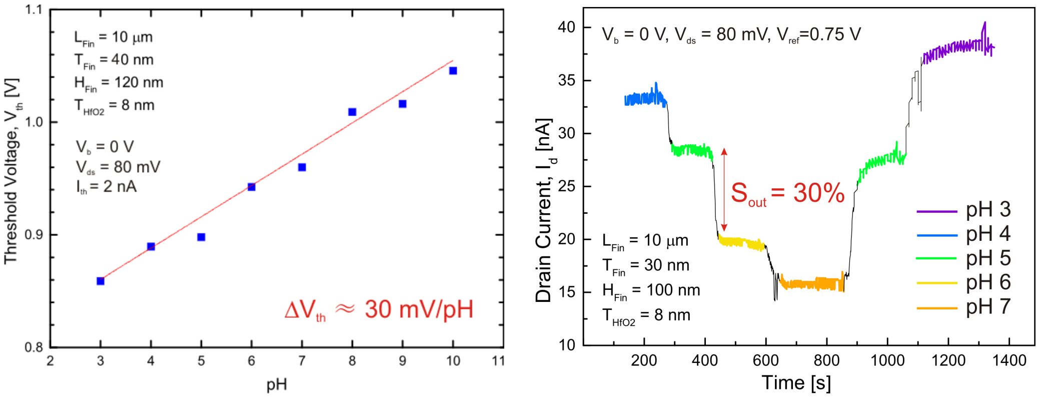
with

$$\frac{1}{C^*_{ox}} \approx \frac{1}{C_{ox}} + \frac{1}{C_{DL}} \tag{5.7}$$

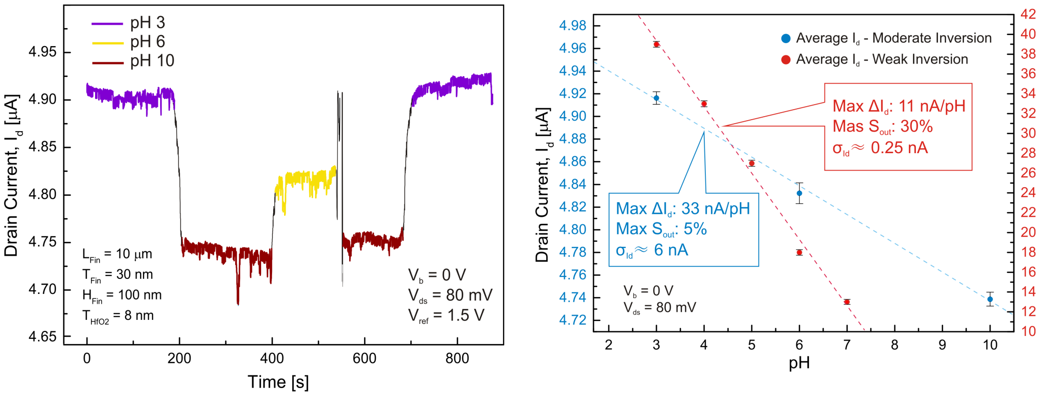
where k is the Boltzmann constant, T the temperature in K, q the electronic charge, C_D the Silicon depletion capacitance, C_{it} the capacitance associated with interface states, C_{ox} the oxide capacitance and C_{DL} the double-layer capacitance [11]. According to the values of $C_{ox} \approx 1.5\,\mu F\,cm^{-2}$ and $C_{DL} = 16\,\mu F\,cm^{-2}$ [12], the only significant contribution to the subthreshold slope remains the gate oxide capacitance. As a consequence, it cannot be targeted as the cause of the slope degradation. To our knowledge, there are no other direct physical causes to induce such degradation. As it is possible to observe from the Y-axis comparison, the I_d currents at $V_g = 0\,V$ differs by almost three orders of magnitude. Considering that the steepest subthreshold slope contribution for the metal gate FinFETs comes from the smallest I_d values, its deterioration may be a result of the different I_{off} values. For a more reliable comparison, the same measurement set-up conditions should be fixed.



(a) $I_d(V_{ref})$ at fixed pH = 6
(b) $I_d(V_{ref})$ for $3 \le pH \le 10$



(c) V_{th} for $3 \le pH \le 10$
(d) I_d vs. t for $3 \le pH \le 7$



(e) I_d vs. t for $3 \le pH \le 10$
(f) I_d vs. t for $3 \le pH \le 10$

Figure 5.8: Electrical characterization of liquid gate FinFETs: (a) $I_d(V_{ref})$ for $T_{Fin} = 30$ nm, $L_{Fin} = 10$µm at fixed pH = 6 for different V_{ds} on the left Y-axis and $I_d(V_g)$ for the equivalent metal gate FinFET at $V_{ds} = 100$ mV on the right Y-axis; (b) $I_d(V_{ref})$ for 3 ≤ pH ≤ 10 at $V_{ds} =$ 80 mV; (c) $V_{th}(pH)$ for $T_{Fin} = 40$ nm, $L_{Fin} = 10$µm extracted at $I_d = I_{th} = 2$ nA; (d) I_d vs. time, for a FinFET sensor for five different pH values at $V_{ds} = 80$ mV and $V_{ref} = 0.75$ mV; (e) I_d vs. time for a FinFET sensor for three different pH values at $V_{ds} = 80$ mV and $V_{ref} = 1.5$ mV; (f) measured average I_d for different pH values, for a FinFET sensor operating in weak inversion (right Y-axis, red dots) and moderate inversion (left Y -axis), blue dots.

Steady-state measurements

Figure 5.8b illustrates the $I_d(V_{ref})$ characteristics for different pH values at $V_{ds} = 80\,\mathrm{mV}$. The curve shifts monotonically according to the pH in the whole range $3 \le pH \le 10$. By increasing the pH, the V_{th} moves toward more positive values. However, the threshold voltage shift is not constant, as also shown in Fig. 5.8c. The sensitivity calculated by linear fit is $S = 30\,\mathrm{mV/pH}$, less than the expected value for HfO_2. The FinFET sensor is functional, but its response is not completely exploited. Since the oxide cannot provide a "full-response" with respect to the H^+ concentration, it becomes more sensitive to the different salt concentration of each pH chemical composition [13]. As a consequence, ΔV_{th} is neither constant nor linear. This result arises from a deterioration of the oxide at the surface. The value $\Delta V_{th} = 30\,\mathrm{mV}$ is lower than the expected value of SiO_2 [14], indicating that the HfO_2 layer could have been either removed or modified by excessive cleaning procedures.

Time-dependent measurements

Time-pH dependence measurements were carried out by fixing the potential V_{ref}, as shown in Fig. 5.8d, where the initial current was $I_d = 33\,\mathrm{nA}$, and Fig. 5.8e, with $I_d = 4.9\,\mu\mathrm{A}$. As reported in Fig. 5.8d, abrupt current transitions with a maximum $S_{out} = 30\%$ for the transition pH $5 \rightarrow 6$ and an average $\Delta I_d = 6\,\mathrm{nA/pH}$ were measured. The standard deviation corresponding to each population of I_d values is $0.2\,\mathrm{nA} < \sigma_{I_d} < 0.3\,\mathrm{nA}$, resulting in a good $SNR \approx 30$. The signal drift over time is also notably low, being $|\delta I_d/\delta t| \approx 1 \times 10^{-12}\,\mathrm{A\,s^{-1}}$. The same experiment was carried out at higher current values, in moderate inversion regime, as reported in Fig. 5.8e. The sensor exhibits a higher relative current variation, with maximum $\Delta I_d = 33\,\mathrm{nA/pH}$ for pH < 6, minimum $\Delta I_d = 18\,\mathrm{nA/pH}$ for pH > 6 and $\Delta I_d = 24\,\mathrm{nA/pH}$, calculated as mean value. The maximum S_{out} did not exceed 5%. Elevated noise is also observed, corresponding to about $\sigma = 6\,\mathrm{nA}$, leading to a poor $SNR \approx 6$, five times smaller than the previous operating region. The signal is also less stable in time with a $|\delta I_d/\delta t| \approx 80 \times 10^{-12}\,\mathrm{A\,s^{-1}}$. Figure 5.8f summarizes the comparison.

In the initial measurements described above the sensors were not yet optimized in terms of sensitivity and readout sensitivity. However, they pointed out important aspects on the general behaviour of the liquid gate FinFETs that will be further addressed in the following sections.

5.3.2 Fully pH-responsive FinFETs

The cause of the oxide degradation previously presented has not been identified. However, in order to prevent a deterioration of the surface oxide, more gentle fabrication cleaning procedures have been adopted after the HfO_2 Atomic Layer Deposition. In particular, avoiding HF solutions and high power O_2 plasma led to the fabrication of fully pH responsive devices.

Steady-state measurements

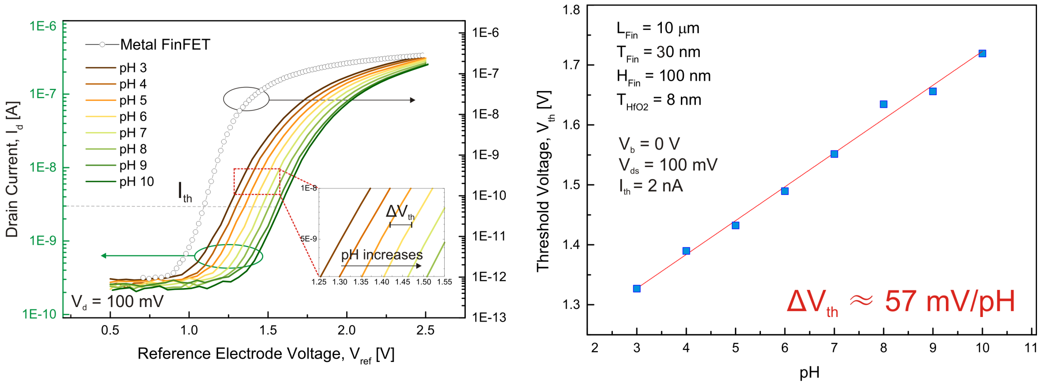
Figure 5.9a shows the optimized $I_d(V_{ref})$ transfer characteristics for different pH values. From an electrical point of view the results are equivalent to the ones presented in Fig. 5.8b with $I_{on}/I_{off} \approx 10^4$ and an $SS \approx 180\,\mathrm{mV/dec}$. On the other hand, it is possible to observe in the inset of Fig. 5.9a that the V_{th} shift is drastically improved, in terms of absolute value and linearity. From Fig. 5.9b it is possible to observe that a $\Delta V_{th} \approx 57\,\mathrm{mV/pH}$ is obtained. Such a value is the double of the value previously presented in Fig. 5.8b and it is close to the Nernst limit. The fabricated FinFETs finally achieved a full pH response and, as a consequence, the sensitivity with respect to other chemicals seems suppressed. The local SOI insulation through Si_3N_4 has been demonstrated to be fully reliable also for the fabrication of the liquid gate FinFETs. The maximum intrinsic sensitivity has been reached by the implementation of an HfO_2 layer as gate oxide.

Time-dependent measurements

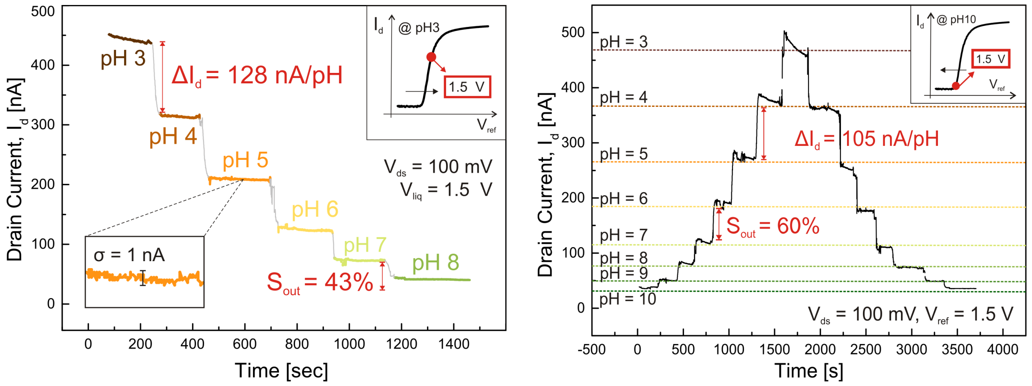
Time-dependent measurements have then been performed at different V_{ref} potentials. Figure 5.9c shows the I_d variations when V_{ref} was set to 1.5 V. As presented before, for increasing pH values the $I_d(V_{ref})$ curve shifts towards more positive values, meaning that, for the same V_{ref}, I_d will be smaller. In other terms, the FinFET operating region moves from moderate to weak inversion region. The higher ΔI_d, i.e. $\Delta I_d = 128\,\mathrm{nA/pH}$, was obtained for the pH transition $3 \rightarrow 4$. The higher S_{out} values were instead achieved where the subthreshold slope is steeper. The maximum $S_{out} = 43\%$ was obtained for the pH transition $7 \rightarrow 8$. In Fig. 5.9c, it is possible to appreciate the low noise with $\sigma \approx 1\,\mathrm{nA}$ and resulting averaged $SNR \approx 80$. Figure 5.9d shows another time-dependent measurement. In this case the FinFET was biased starting from its minimum I_d value. In this case the curve can only shift towards left, otherwise the current will not vary, meaning that the pH value should decrease. The pH has been changed from 10 to 3 and backwards. As expected in this case, the higher S_{out} values, i.e. $55\% < S_{out} < 60\%$, are obtained for the first measurements, where the slope is steep and constant, while the higher current variation, $\Delta I_d = 105\,\mathrm{nA/pH}$ is obtained at the transition pH $5 \rightarrow 4$. The graph of Fig. 5.9d also demonstrates the repeatability of the measurements when the pH values are exchanged in the opposite direction.

5.3.3 pH measurements at different biasing point

Figure 5.10 summarizes the time-dependent measurements corresponding to different operating regions of the transistor. All data are reported in Tabs. 5.2, 5.3 and 5.4. Figures 5.10a and 5.10b refer to the time-dependent measurements previously described: in both cases, V_{ref} is set to 1.5 V but for opposite pH values, i.e. 3 and 10. In other words, since the FinFET characteristic shifts in the opposite direction, these two experiments cover the same subthreshold region. As a consequence, the current variation can be exponentially fitted. Figure 5.10c, instead, shows the I_d variations when the FinFET is biased close to the strong inversion, at



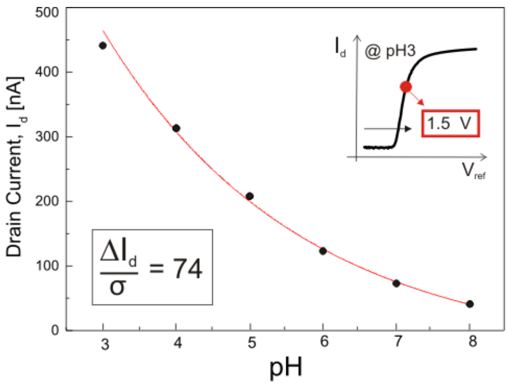
(a) $I_d(V_{ref})$ for 3 ≤ pH ≤ 10 (b) V_{th} for 3 ≤ pH ≤ 10



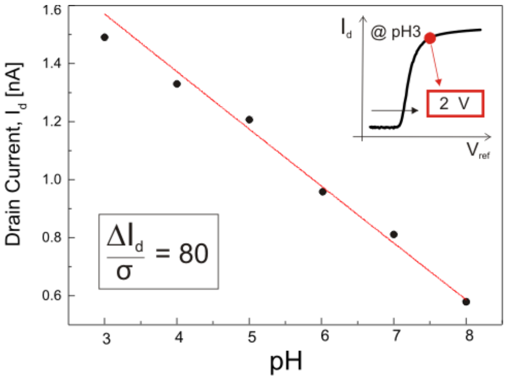
(c) I_d vs. t for $3 \leq pH \leq 8$ at $V_{ref} = 1.5$V (d) I_d vs. t for pH 3 ≤ pH ≤ 10

Figure 5.9: Electrical characterization of liquid gate FinFETs: (a) $I_d(V_{ref})$ transfer characteristic for a metal (right Y-axis) and liquid gate (left Y-axis) FinFET with $T_{Fin} = 30$nm for 3 ≤ pH ≤ 10 with the inset showing the curve shift ΔV_{th}; (b) $V_{th}(pH)$ for a single FinFET with $T_{Fin} = 40$nm, extracted at $I_d = I_{th} = 2$nA; (c) I_d, for a FinFET sensor during a time period of 25 minutes for $3 \leq pH \leq 8$ at $V_{ref} = 1.5$V; (d) I_d, during a time period of 1 hour from pH 10 to 3 and backwards at $V_{ref} = 1.5$V.

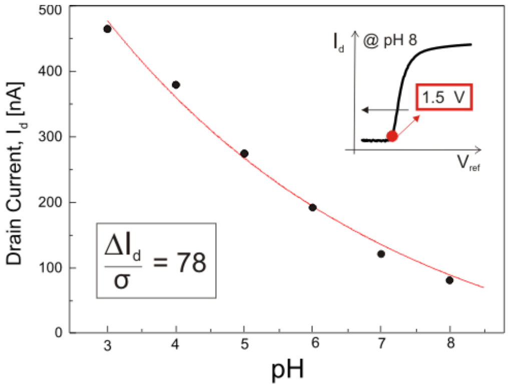
$V_{ref} = 2$V. As expected, such configuration leads to the highest averaged $\Delta I_d \approx 176$nA/pH but to low S_{out} which never exceeds 25%. In this case the experimental data are linearly fitted. The comparison of the three graphs with their mathematical fits reflects the intrinsic logarithmic nature of the FET transfer characteristic.



(a) $V_{ref} = 1.5\,\text{V}$ at pH=3



(b) $V_{ref} = 2\,\text{V}$ at pH=3



(c) $V_{ref} = 1.5\,\text{V}$ at pH=8

Figure 5.10: FinFET response according to different V_{ref} bias as reported in Table 5.2: (a) $V_{ref} = 1.5\,\text{V}$ at pH=3; (b) $V_{ref} = 2\,\text{V}$ at pH=3; (c) $V_{ref} = 1.5\,\text{V}$ at pH=8; the insets report the SNR as reported in Table 5.4.

Table 5.2 summarizes the S_{out} obtained from the reported measurements. The maximum $S_{out} = 60\%$ value has been achieved when the device is biased in the subthreshold region, where the subthreshold slope is higher and constant. Since the maximum intrinsic sensitivity S has been achieved with the use of HfO_2 the only means to increase such value is to increase the *SS* of the liquid gate FinFET, as previously introduced in Sec. 1.3 according to the relation:

$$S_{out} = \frac{\Delta I_d}{I_d} = \frac{\Delta V_{th}}{SS} \tag{5.8}$$

Table 5.3 collects the ΔI_d between each pH transitions. The maximum value, $\Delta I_d = 271\,\text{nA}$ is obtained for the transition 5 → 6 when the FinFET is biased at the onset of the strong inversion, at $V_{ref} = 2\,\text{V}$. With such biasing the overall $\Delta I_d \approx 176\,\text{nA/pH}$ is achieved.

Table 5.4 shows the ratio $SNR = \Delta I_d / \sigma_{I_d}$ for all pH values. For all V_{ref} values the signal accuracy is quite robust, with $74 \le SNR \le 80$. The smaller *SNR* values do not correspond to a specific level of current, i.e. operating regimes.

Table 5.2: FinFET pH sensor: readout sensitivity, S_{out}

	FinFET S_{out} [%]					
pH	3→4	4→5	5→6	6→7	7→8	3-8
V_{ref1} = 1.5 $V_{@ph3}$	29	33	40	40	43	**37**
V_{ref2} = 2 $V_{@ph3}$	9	7.5	22	15	28	**17**
V_{ref3} = 1.5 $V_{@ph8}$	18	40	42	60	56	**43**

Table 5.3: FinFET pH sensor: current variation according to pH, ΔI_d

	FinFET, ΔI_d [nA]					
pH	3→4	4→5	5→6	6→7	7→8	3-8
V_{ref1} = 1.5 $V_{@ph3}$	128	105	85	50	32	≈**80 nA/pH**
V_{ref2} = 2 $V_{@ph3}$	130	100	271	148	232	≈**176 nA/pH**
V_{ref3} = 1.5 $V_{@ph8}$	85	105	82	71	45	≈**77 nA/pH**

Table 5.4: FinFET pH sensor: signal to noise ratio, *SNR*

	FinFET, SNR = $\Delta I_d / \sigma_{Id}$					
pH	3→4	4→5	5→6	6→7	7→8	3-8
V_{ref1} = 1.5 $V_{@ph3}$	44	87.5	85	71	80	≈ **74**
V_{ref2} = 2 $V_{@ph3}$	32	42	117	123	210	≈ **80**
V_{ref3} = 1.5 $V_{@ph8}$	42	87	82	88	90	≈ **78**

Some important conclusions on the biasing of the reference electrode for non steady-state measurements can be drawn:

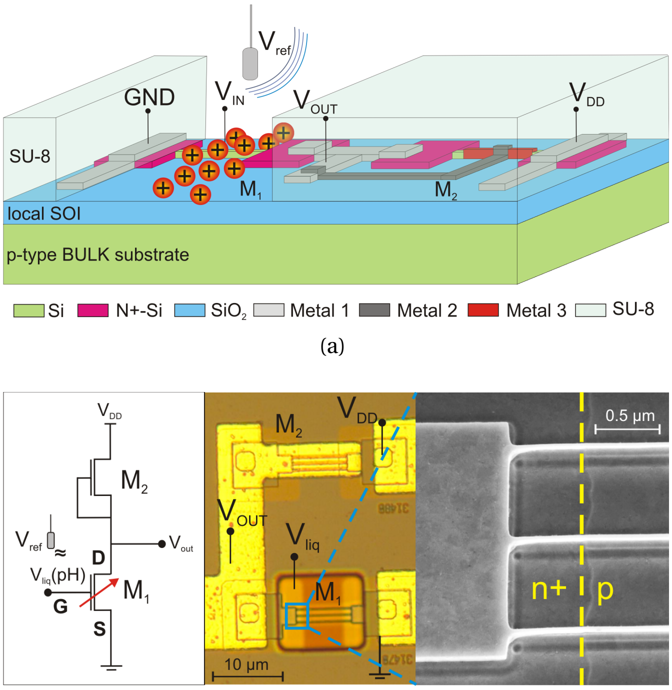
- **Linearity**: Due to the intrinsic logarithmic nature of the transfer characteristic of FET device, the linearity of the sensor will be dependent on the biasing point set by the reference electrode. Biasing the sensors at $V_{ref} = 2\,\text{V}$ from low to high pH values, the current variation can be linearly fitted. However, being the $I_d(V_{ref})$ known, the linearity represents a minor constraint with respect to other types of sensors where linearity is highly demanded.

- $\mathbf{S_{out}}$ and $\mathbf{\Delta I_d}$: They are naturally complementary. After calibration of the sensor, their maximum values are easily accessible by setting V_{ref}. S_{out} is constant as constant is the FET subthreshold slope, while ΔI_d is linear above the subthreshold region and exponential below. It is worth to mention that, according to a specific circuit readout, the sensor current output can be designed to match specific requirements in terms of output conductance and noise. The choice of the operating point with high S_{out} or ΔI_d is strictly connected to the type of measurements, e.g. ionic or biological, and circuit design.
- **Current fluctuation**, $\sigma_{\mathbf{I_d}}$: All the optimized FinFET have shown quite low σ_{I_d} values and high SNR value. In first approximation, no dependence from the operating regime of the FinFET has been identified. In conclusion, the high values of σ_{I_d} obtained in the Sec. 5.3.1 were exclusively connected to a heavy deterioration of the surface, whose impact was much higher at higher currents.

The considerations on the FinFET sensitivity and the biasing point represent an important insight on the general subject of "sensitivity". Despite such considerations are based on simple mathematical outcomes, most of the cited works related to SiNW for sensing do not clearly define the conditions for which the "sensitivity" is calculated. Once the intrinsic pH sensitivity is defined by the surface oxide the readout sensitivity will be defined and limited by the well-known electronic properties of the FET device, independently of the liquid environment.

5.3.4 Sensing common source amplifier

It has been shown that the sensor linearity naturally depends on the reference electrode biasing point. Herein, a pH sensing unit composed of two n-channel FinFETs is presented. The two FinFETs are connected together in order to achieve (i) high linearity window and (ii) amplification of the ΔV_{th}. Figure 5.11a shows the proposed circuit: a common-source amplifier, where the active transistor is replaced by a FinFET-based sensor and the load is implemented with a gate-source shorted FinFET with a metal gate.



(a)

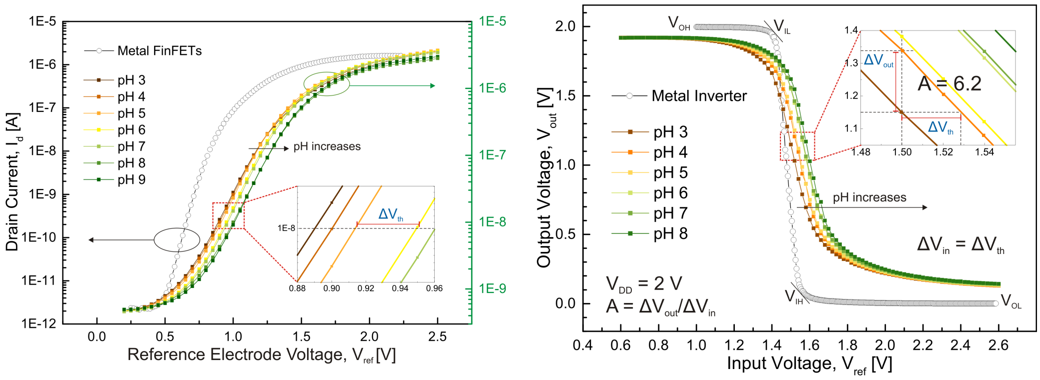
(b)

Figure 5.11: (a) Schematic representation of the proposed pH sensor with a sensing FinFET exposed to the H$^+$ solution and reference electrode (left) connected to a metal gate FinFET protected by an SU-8 layer (right); (b) schematic of the FinFET-based amplifier with metal gate FinFET M2 connected as depletion-mode load and sensing FinFET M1 as driver (left); top view of the fabricated amplifier with SU-8 opening over the channel of M1 (middle); SEM SiNW detail showing the separation between n+ and p regions (right).

As previously mentioned, only sensing measurements when the FinFET metal gate terminal is connected to its source have been investigated. Such connection provides several advantages: (i) the output voltage can be as high as the power supply, V_{DD}, (ii) the slope of the $V_{out}(V_{in})$ characteristic is very steep in the transition region and (iii) lower power consumption. When the potential at the surface is modified, the input variation, $\Delta V_{in} = \Delta V_{th}$, caused by a surface reaction is amplified as an output variation ΔV_{out}. In first approximation the gain can be expressed as:

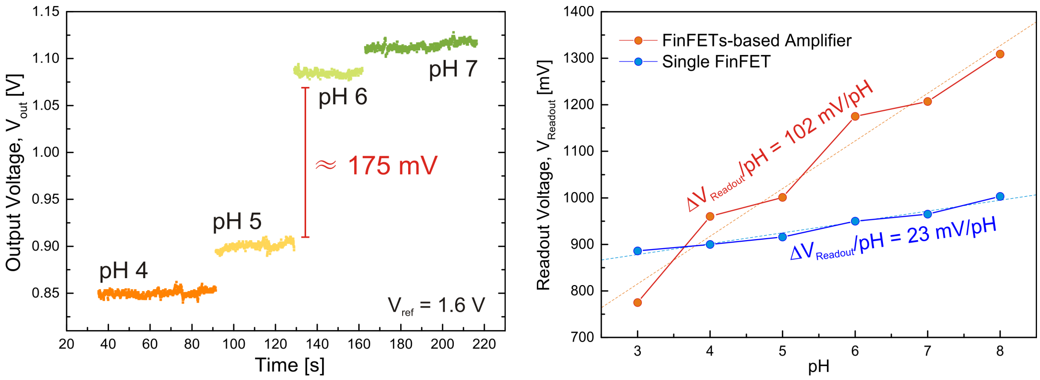
$$A_v = \left|\frac{\Delta V_{out}}{\Delta V_{th}(pH)}\right| = g_{m_{sens}} \cdot R_{out} = \frac{g_{m_{sens}}}{g_{ds_{sens}} + g_{ds_{load}}} \tag{5.9}$$

where ΔV_{th} is function of the pH solution and R_{out} is the output resistance of the amplifier, given by the inverse of the conductance g_{ds} of the FinFET. In contrast to the exponential FET operation, the voltage variation readout is expected to be linear as well as more favorable in terms of signal processing and noise tolerance of small signals. This holds true especially for biosensors where current variations are usually very small [15]. With the measurement set-up used for the single FinFETs, the driver sensing transistor was first characterized independently from its load. The single sensor exhibits a monotonic pH response with a $\Delta V_{th} \approx 23\,\text{mV/pH}$, which was calculated as the average value of all the pH transitions. The $I_d(V_{ref})$ transfer characteristic is proposed in Fig. 5.12a where the $I_d(V_{ref})$ of the equivalent metal gate FinFET is also shown. Being the ΔV_{th} less than the expected one for HfO_2, it is clear that these sensors are part of those which inherited a surface deterioration from the fabrication process, as previously explained for the single sensor. However, this limitation does not compromise the aim of this work, which is to evaluate the advantages of the proposed configuration. The amplifying stage has then been tested in a liquid environment for different pH values. The result is shown in Fig. 5.12b. All the data extracted from the $V_{out}(V_{in})$ characteristic are reported in Tab. 5.5.



(a) $I_d(V_{ref})$ for $3 \leq pH \leq 9$

(b) $V_{out}(V_{ref})$ for $3 \leq pH \leq 8$



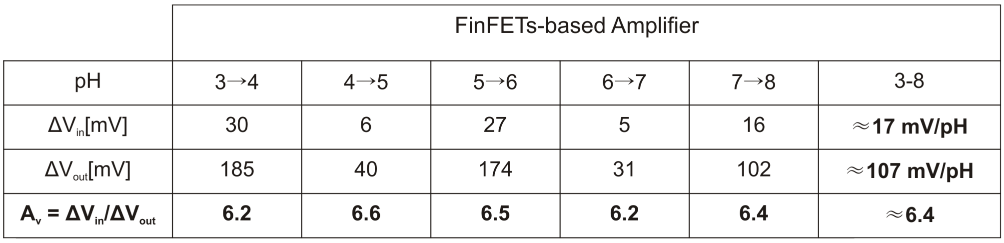
(c) V_{out} vs. t for $4 \leq pH \leq 7$ at $V_{ref} = 1.6\,\mathrm{V}$

(d) $V_{Readout}(pH)$

Figure 5.12: Electrical characterization of sensing common source amplifier: (a) $I_d(V_{ref})$ for a metal gate FinFET (left Y-axis) with $V_g = \Delta V_{sol} - V_{ref}$ and liquid gate FinFET (right Y-axis) with $T_{Fin} = 30\,\mathrm{nm}$; $I_d(V_{ref})$ was obtained for 3 ≤ pH ≤ 9 with the inset showing the curve shift ΔV_{th}; (b) $V_{out}(V_{ref})$ of a metal gate (black curve) and sensing (colored curves) FinFET amplifier, at $V_{DD} = 2\,\mathrm{V}$, with $T_{FinM1} = 30\,\mathrm{nm}$ and $T_{FinM2} = 40\,\mathrm{nm}$; $V_{out}(V_{ref})$ was measured for 3 ≤ pH ≤ 8; the inset shows the curve shift ΔV_{th} along with the corresponding ΔV_{out}; (c) output voltage V_{out} of the FinFET-based amplifier vs. time for different pH values, at $V_{ref} = 1.6\,\mathrm{V}$; (d) comparison of performances of a single FinFET sensor and FinFET inverter, for 3 ≤ pH ≤ 8, where $V_{Readout}$ corresponds to ΔV_{th} for the single FinFET and ΔV_{out} for the inverter.

As shown in Fig. 5.12c, each $V_{out}(V_{ref})$ curve exhibits a gain $A_v > 6$, with an average gain $A_v \approx 6.4$. The maximum $\Delta V_{out} = 185\,\mathrm{mV/pH}$ is achieved between pH 3 → 4, and an overall $\Delta V_{out} = 107\,\mathrm{mV/pH}$ is averaged over pH 3 to 8. The ΔV_{out}/pH has been calculated at $V_{ref} = 1.6\,\mathrm{V}$, where the inverter slope is constant over the whole pH range. Thanks to the voltage-to-voltage transduction, the gain can be kept constant and independent from the different ΔV_{in}/pH. As previously described for the single FinFET, also the sensing inverter shows a slight performance degradation as compared to the inverter with only metal gate FinFETs. The output swing $|V_{OH} - V_{OL}|$ is reduced from 2 V to 1.8 V affecting also $|V_{IH} - V_{IL}|$ which increases to 0.3 V. As discussed in Chap. 2, this last value provides an operating window where the linearity is guaranteed by the $V_{in}(V_{out})$ relation. For quantitative and repeated measurements it is an ideal condition. For a steeper ON-OFF transition, the inverter slope could be optimized by sizing the FinFET length.

Table 5.5: FinFET pH sensing CSA: gain between pH 3 and 8



	FinFETs-based Amplifier					
pH	3→4	4→5	5→6	6→7	7→8	3-8
ΔV_{in}[mV]	30	6	27	5	16	≈**17 mV/pH**
ΔV_{out}[mV]	185	40	174	31	102	≈**107 mV/pH**
$A_v = \Delta V_{in}/\Delta V_{out}$	**6.2**	**6.6**	**6.5**	**6.2**	**6.4**	≈**6.4**

To further verify the pH sensing amplification obtained with the voltage readout, a time-dependence experiment has been performed. The reference electrode potential has been fixed at $V_{ref} = 1.6$V and the device has been exposed to solutions of different pH over time, as shown in Fig. 5.12c. The output voltage variations extracted from the time-dependent measurements are in agreement with the previous data reported in Table 5.5. For each set of pH values it is also possible to calculate the standard deviation corresponding to the mean value of V_{out}, $\sigma_{V_{out}} \approx 2.3$mV, resulting in a $\Delta V_{out}/\sigma_{V_{out}} \approx 76$ for the pH transition $5 \rightarrow 6$ and an average $\Delta V_{out}/\sigma_{out} \approx 45$. Both V_{out} and ΔV_{out} to noise ratios are then quite robust.

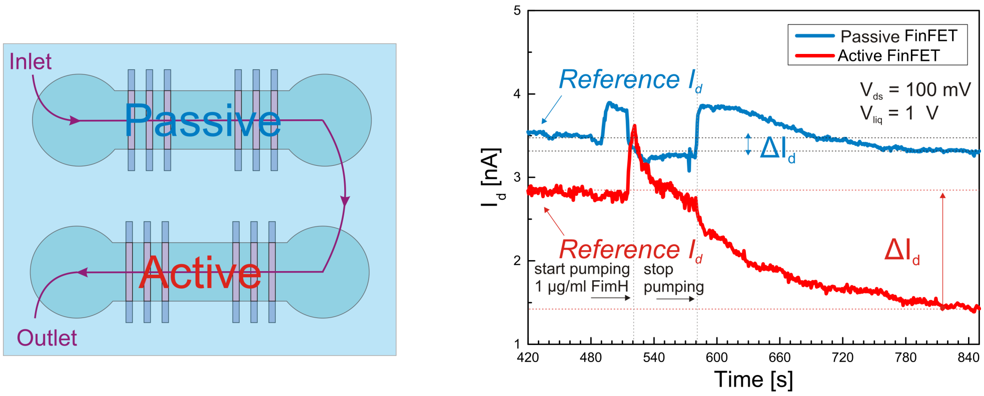
Figure 5.12d describes in a glance the performance of such an architecture. Its overall response has been demonstrated to be 4.4 times higher than that of a single FinFET sensor. Using a linear fit, a readout sensitivity $\Delta V_{Readout} = 102$mV/pH for the FinFET amplifier and $\Delta V_{Readout} = 23$mV/pH for the single FinFET has been calculated. The physical Nernst limit is thereby exceeded as amplification at the sensor readout level. Also for these experiments, the local bulk insulation achieved excellent electrical performance with full inverter output swings. Additionally, the demonstrated amplification has been achieved with applied voltages smaller than 2 V, with a very low consumed DC power of the order of few microWatts.

Unfortunately, no FinFETs achieving full pH response have been implemented in such configuration. However, having demonstrated single FinFETs with $\Delta V_{th} = 56$mV and a constant gain of $A_v \approx 6.4$, a $\Delta V_{out} = 0.36$V is expected.

5.4 Preliminary biosensing application: FimH detection

Preliminary results on the detection of FimH protein with functionalized FinFETs are presented here. The experiments were carried out with the same measurement set-up used for pH sensing at the laboratory of the Nanoelectronics group of Basel, while the preparation of the protein and the functionalization have been performed by the Institute of Molecular Pharmacy, always at University of Basel.

The FinFET surface was modified in order to recognize FimH protein. In medical treatment, the expression of this adhesin at different phases during an infection plays the most important role in the adhesion of bacterial pathogens. It is considered as a promising target for anti-adhesive therapy [16]. Monitoring this protein is crucial for the early detection and treatment of urinary tract infection by uropathogenic Escherichia coli, one of the most common infections affecting millions of people every year [17]. For the FinFET functionalization, UV-ozone treatment was used to maximize the number of free silanol groups on the surface, which was then covered with APDMES for 30 minutes. After washing with i-PrOH, the FinFETs were cured at 80 °C for 1 hour. In order to obtain active and passive FinFETs, the amine-functionalized FinFETs reacted overnight in phosphate buffer at pH = 7.5, half with NHS ester of the recognizing molecule and half with a negative control. After washing with double distilled water, the FinFETs were equilibrated with 1 mmol HEPES buffer at pH = 8. Having active and passive devices is extremely important, mostly looking towards integrated systems. Performing differential measurements and subtract the two signals to get rid of noise and drift is very important. Moreover, the eventuality of addressing more than one type of sensing with multiple wires on the same chip, should be verified by the effectiveness of the surface functionalization specific to a certain protein. As depicted in Figure 5.13a, active and passive FinFETs were located on the same die but on the two different available channels. During the functionalization, the microfludic channels were in fact addressed separately. During the measurement they were connected together to the pumping system.



(a)

(b)

Figure 5.13: FimH protein detection: (a) drawing illustrating the solution path from inlet to outlet; (b) current I_d vs. time of a passive FinFET and an active FinFET: at time t = 515 s, $1\,\mu\mathrm{g\,mL}^{-1}$ of FimH contained in the solution was injected.

For this type of measurement, $V_{ref} = 1\,\mathrm{V}$ and $V_{ds} = 100\,\mathrm{mV}$ were set, targeting high $\Delta I_d / I_d$ and $\Delta I_d / \sigma_{I_d}$ at small currents. After the injection of $1\,\mu\mathrm{g}\,\mu\mathrm{L}^{-1}$ of FimH equilibrated in 1mM HEPES buffer at pH = 8 the liquid gate FinFET clearly shows its sensitivity to the protein, in contrast with its passivated twin. The active sensor exhibits a sensing variation of $\Delta I_d / I_d \approx 50\%$ with respect to the initial reference current, while the passive control shows a weak influence of

$\Delta I_d/I_d \approx 6\%$, as presented in the I_d vs Time graph of Fig. 5.13b. FimH protein sensing has then been successfully achieved on functionalized devices.

5.5 FinFET long-term stability

Long-term stability measurements have been performed over 4.5 days[1]. The liquid environment has been kept at constant pH = 6. Every 30 minutes the pumping system was automatically activated to renew the liquid on top of the sensors. After a stabilization time of about two minutes the $I_d(V_{ref})$ was traced by sweeping the reference electrode. The V_{th} is then extracted at the same $I_{th} = 2\,\mathrm{nA}$ as plotted in Fig. 5.14a. The FinFETs behaved in an extremely stable way with drift $\delta V_{th}/\delta t \approx 0.14\,\mathrm{mV\,h^{-1}}$ for multiple wire FinFETs, as shown in Fig. 5.14a, and $\delta V_{th}/\delta t \approx 0.13\,\mathrm{mV\,h^{-1}}$ for the single wire FinFETs, as shown in Fig. 5.14b. These measurements, repeated more than 200 times, demonstrate the measurement repeatability. The standard deviation of the V_{th} mean value is $\sigma_{Vth} \approx 0.8\,\mathrm{mV}$. Two equivalent instances of the FinFET, D3 and D4, located at two different die corners, have also been compared. An excellent superposition of the V_{th} values of the two devices is obtained, as shown in Fig. 5.14b. By subtracting the two V_{th} set of data (Fig. 5.14c), the residual $\Delta V_{th} \approx 0.6\,\mathrm{mV}$ with $\sigma_{Vth} \approx 1\,\mathrm{mV}$ demonstrates the reliability of the fabrication process at the die level. A small drift in time, $\delta\Delta V_{th}/\delta t \approx 0.08\,\mathrm{mV\,h^{-1}}$ was observed for the relative ΔV_{th}. The same substraction, presented in Fig. 5.14d, has been done for the devices D1 and D2 resulting in a more negligible drift in time, $\delta\Delta V_{th}/\delta t \approx 0.08\,\mathrm{mV\,h^{-1}}$ but higher $\sigma_{Vth} \approx 4\,\mathrm{mV}$. These data prove two important sensor properties: stability and reliability of the single sensor at the wafer and die level.

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[1] The first 30 hours have been removed due to a sudden drift at h = 28, probably related to the measurement set-up

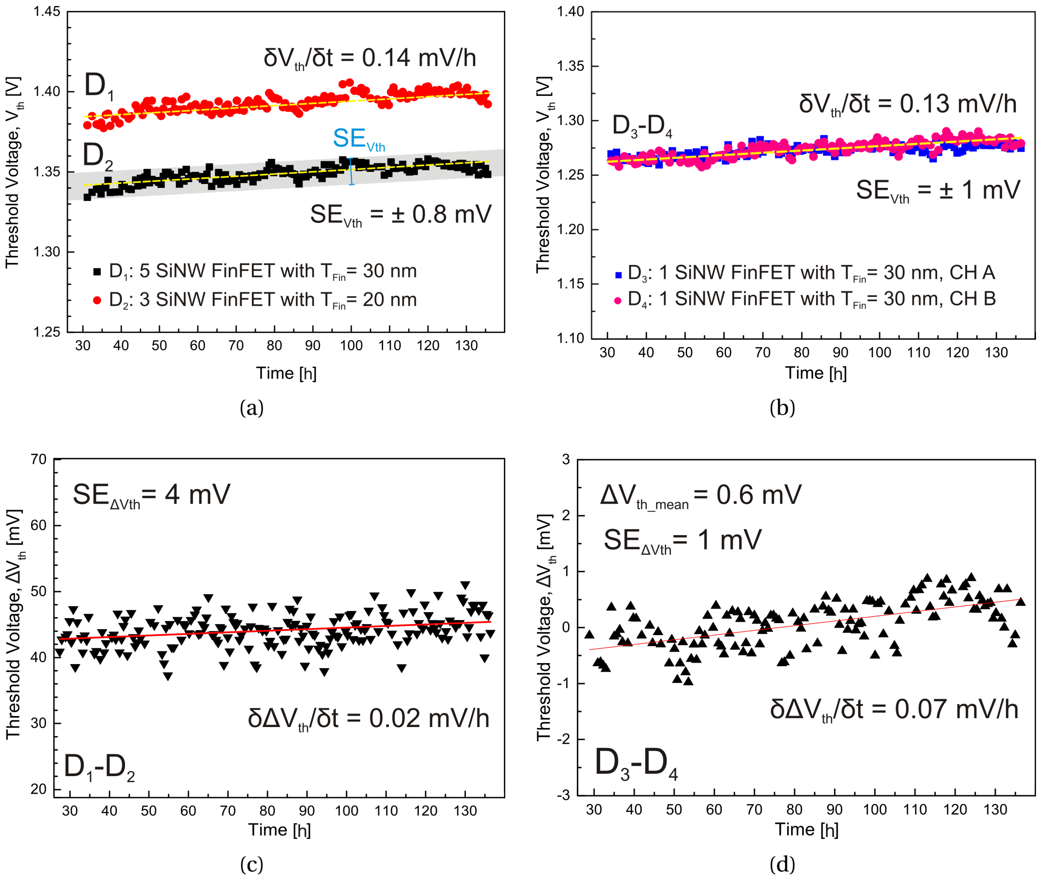

Figure 5.14: FinFET long-term stability measurement over 4.5 days: (a) V_{th} for different multi-wire FinFET sensors at constant pH = 6; (b) V_{th} for equal single-wire FinFET sensors at different die locations and constant pH = 6; (c) result of the subtraction of the data set of V_{th} for the devices $D_1 - D_2$ and (d) $D_3 - D_4$;

5.6 Comparison with other works

Herein, the experimental results are presented in comparison with other works, previously introduced in Chap. 4.9. The comparison is organized in three fields:

1. **Sensitivity, Stability and Accuracy:** It describes the sensor output in terms of ΔV_{th}, $S_{out} = \Delta I_d / I_d$, stability over time $\delta V_{th}/\delta t$, and accuracy, calculated as the inverse of the SNR. The comparison is reported only for pH sensors. Here, ΔV_{th} is taken into account only as direct surface potential change.
2. **Voltage supply**: It collects the voltage supply used for the detection, independently from the type of sensing, ionic or biological.
3. **Signal amplification**: It reports the SiNW-related work where ΔV_{th} has been amplified by a front and back-gate coupling or a common-source connection.

All data are reported as maximum achieved values. Table 5.6 collects data concerning the first field.

Table 5.6: Comparison of FinFET sensitivity, stability and accuracy with other works

Reference	ΔV_{th}[mV/pH]	S_{out}[%]	$\delta V_{th}/\delta t$[mV/h]	SNR^{-1}
This work	HfO_2: 57	60	0.13	0.012 pH[2]
Microsens SA [18]	Al_2O_3 : 53.7	-	0.2	0.01 pH
Abe et al. [19]	Al_2O_3 : 52 to 58	-	0.3	-
Lee et al. [20]	FS [3]: 58.3	42	-	-
Park et al. [21]	-	3 [4]	3.6[5]	0.2 pH
Yoo et al. [22]	SiO_2: 24.5[6]	19	-	-
Kim et al. [23]	SiO_2: 40	(-)[7]	-	0.016 pH
Ahn et el. [24]	SiO_2: 22[8]	-	27	-
Vu et al. [25]	SiO_2: 41	50[9]	-	-
Stern et al. [26]	-	85[10]	-	-
Cui et al. [27]	-	18[11]	-	-
Tarasov et al. [13,28]	Al_2O_3: 58-59	-	-	0.005 pH [12]
Chen et al. [29]	SiO_2, 60[13]	7	-	-
Bedner et al. [30,31]	Al_2O_3, HfO_2: 58-59	-	-	0.00017 pH[14]

As previously discussed, the intrinsic sensitivity depends on the oxide outer layer and its quality [7,11,32]. In the first experiments, in fact, despite HfO_2 was implemented as gate oxide the full pH response was not achieved for unknown reasons related to the fabrication process. The optimized FinFETs together with the work of Tarasov *et al.* [13], Bedner *et al.* [31] and Abe *et al.* [19] have reported a $\Delta V_{th} \approx 58\,mV/pH$. The commercial device MSFET 3320 with datasheet available at [18] implements AlO_2 with $\Delta V_{th} \approx 53.7\,mV/pH$ as sensing gate oxide. Additionally, in Chen *et al.* [29] it is reported a change of ΔV_{th} up to 60 mV/pH for a SiO_2 layer thanks to a local gate. It is not clear, though, how the surface potential has been calculated. It may refer to a subthreshold slope modulation by the local gate which turns in higher current variations, but not an actual ΔV_{th}.

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[2] at sampling rate of 3 Hz during a time period of $\Delta t = 100\,s$

[3] Functionalized Surface

[4] given as change in resistance

[5] estimated from the relative change in resistance over 8 hours a pH = 7 provided in the work

[6] extracted dividing the total ΔV_{th} by the coupling factor provided in the work

[7] considering S_{out} in terms of decades, $N_{dec} = \Delta V_{th}/SS$, and being $SS = 100 mV/dec$ reported in the work, it is expected that $S_{out} = 0.4$ dec/pH vs. $S_{out} = 0.3$ dec/pH obtained in this work

[8] when no amplification through double-gates applies

[9] graphically estimated; indeed, if the number of decades are estimated by $N_{dec} = \Delta V_{th}/SS$, and being 85 mV/dec reported in the work, it is expected that $S_{out} = 0.5$ dec/pH vs. $S_{out} = 0.3$ dec/pH obtained in this work

[10] extracted graphically

[11] extracted graphically

[12] an accurate definition of SNR is provided, at sampling rate of 10 Hz and 1 Hz bandwidth

[13] it maybe referred to a different potential change

[14] an accurate definition of SNR is provided, at sampling rate of 10 Hz and 1 Hz bandwidth

For a fixed ΔV_{th}, S_{out} will be limited by the FET slope. According to the comparison presented in Tab. 5.6, the fabricated FinFETs provide higher readout response with respect to most of the cited works. However, its subthreshold slope can be improved. Indeed, the works of Kim *et al.* [23] and Vu *et al.* [25] should achieve higher S_{out}, since higher swings are reported in their works. A higher S_{out} is also estimated for the work of Stern *et al.* [26], but no electrical characterization is provided for this work.

Concerning the stability over time, there are not a lot of works providing such characterization. The stability achieved by the FinFET is higher than the one reported by the commercial device of Microsens SA [18]. The testing procedures of the commercial device are surely more accurate and demanding than the presented experiments, but the stability can be reported as an excellent result.

Similarly to $\delta V_{th}/\delta t$, the SNR is rarely reported and the definition itself may differ from work to work. Moreover, a deep investigation on noise should be addressed in a wide range of frequency, as has been done by Kim *et al.* [23], Tarasov *et al.* [13] and Bedner *et al.* [30]. In first approximation, the accuracy of the FinFET results to be quite robust, as it has also been demonstrated by the repeated measurements presented in Sec. 5.5.
Table 5.7 addresses the problem of power consumption. The dissipated power P_{Fin} varies from tens to hundreds of nW, i.e. $8\,\text{nW} \leq P_{Fin} \leq 150\,\text{nW}$ for $V_{ds} = 100\,\text{mV}$, according to the operating regime. For the biological application that has been briefly described the calculated

Table 5.7: Comparison of FinFET voltage supplies with other works

Reference	V_{ds}[V]	V_{ref}[V]	V_b[V]
This work	0.1	0.5 to 2.5	0
Microsens SA [18]	1	(-)[15]	-
Lee et al. [20]	1	-3 to 2.5	-
Park et al. [21]	-5 to 5	-	-
Yoo et al. [22]	1	-	0 to 3
Kim et al. [23]	0.1	0 to 2	-
Ahn et el. [24]	0.05	-2.5 to 0	-
Vu et al. [25]	-2 to -0.5	-1.2 to -0.5	-20 to 20
Stern et al. [26]	-20 to 20	-40 to 40	-
Cui et al. [27]	-	-10 to 10	-
Tarasov et al. [13]	0.1	-0.5 t 1.5	-1 to 6
Chen et al. [29]	-	-	-
Knopfmacher et al. [33]	-	-1 to -0.5	-3 to -7
Elfstrom et al. [34]	0 to 2	-30 to 10	-
Crone et al. [35]	0 to 80[16]	-	-
Li et al. [36]	0 to 1	-30 to 20[17]	-

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[15] with $I_d = 50\,\mu\text{A}$ reported in the datasheet, $P = 50\,\mu\text{W}$ can be estimated

[16] meant as V_{DD} of a ring oscillator

[17] range of characterization, V_g for the experiments is not reported

power is even lower, with $P_{Fin} \approx 0.4\,\text{nW}$. The other applied voltages are $0.5\,\text{V} \leq V_{ref} \leq 2.5\,\text{V}$ and $V_b = 0\,\text{V}$. The applied voltage at the backgate is, indeed, very important to guarantee the compatibility of the sensor with CMOS ICs. Only Kim *et al.* [23] clearly report the power consumption level with $3\,\text{nW} \leq P \leq 15\,\text{nW}$ for $I_d < 10^{-7}\,\text{A}$ and no use of backgate is described. Such result is in agreement with ours, since the device and operation mode proposed in [23] are quite similar. Some operating voltage conditions of the main cited works are reported in Tab. 5.7. The works of Kim *et al.* [23], Lee *et al.* [20] and Ahn *et al.* [24] feature applied supply voltages that are considered compatible with future electronic integration. Not by chance, these works are quite recent in time and oriented to a deeper electronic characterization of their devices. On the other hand, works more oriented towards some original proof of concept, as Stern *et al.* [26], Elfstrom *et al.* [34] and Cui *et al.* [27] were more relaxed of the power constrain, especially at the back-gate contact.

Table 5.8 groups together some works where an amplification of ΔV_{th} is achieved either through a capacitance coupling or by the connection of two components. Knopfmacher *et al.* [33] reported how the Nernst limit can be overcome at the readout level by exploiting the coupling of the back-gate and liquid gate capacitances. Similar works, i.e. Yoo *et al.* [22] or Ahn *et al.* [24] followed, using either the back-gate or side gates . Despite the interesting proof of concept of the initial approach, this methodology is limited by the use of the back-gate and the high applied voltage needed to achieve an enhanced coupling effect. Moreover, the use of side gate [24] drastically reduces the sensor surface area. On the other hand, the amplification presented in Sec. 5.3.4 is based on the simple connection of two, or more, devices. The readout sensitivity is boosted by a specific circuit design and parameter optimization with no need for a back-gate and low voltage applied. Lee *et al.* [20, 37] presented two different works with a similar approach. The first work features a couple of complementary SiNWs with a maximum $\Delta V_{out} = 162\,\text{mV}$, and gain of $A_v = 2.7$. In the second more recent work two n-type SiNWs are connected but, being the sensing device implemented as load, the output is limited to $\Delta V_{out} = 38\,\text{mV}$, less than the response expected from a single FET.

Table 5.8: Comparison of FinFET readout amplification with other works

Reference	ΔV_{out} [mV]	$\Delta V_{out}/\Delta V_{in}$
This work	185	6.6
Lee et al. [20]	162	2.7
Lee et al. [37]	38	-
Knopfmacher et al. [33]	220[18]	3.6
Yoo et al. [22]	720	-

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[18] assuming as reference 59.5 mV/pH, as reported in the work

5.7 Summary

This last section summarizes the results achieved by the *electrical characterization* of metal and liquid gate FinFETs.

- **Technical outcomes**[19]:
  - *Metal gate FinFETs:*
    - Subthreshold Slope, SS = 74 mV/dec;
    - Ratio between I_{on} and I_{off}, $I_{on}/I_{off} = 10^6$;
    - Full-swing inverters with $|V_{IH} - V_{IH}| = 150\,mV$;
  - *Liquid gate FinFETs:*
    - Subthreshold Slope, SS ≈ 200 mV/dec;
    - Ratio between I_{on} and I_{off}, $I_{on}/I_{off} = 10^4$;
    - Full pH response with $\Delta V_{th} = 57\,mV/pH$;
    - Readout sensitivity, $S_{out} = 43\%$
    - Stability over time, $\delta V_{th}/\delta t = 0.14$ mV/h;
    - Accuracy, 0.013 pH with SNR = 80;
    - Low power consumption with $P_{Fin} = 10\,nW$;
    - Sensing common source amplifier with gain $A_v = 6.4$.
- **Main contributions to the field**:
  - Demonstration of a well-known electronic unit, the FinFET, as pH and biological sensing unit. The Double-Gate fully depleted architecture is fully exploited for sensing, with the maximization of the FinFET surface exposed to the liquid environment;
  - Excellent outcome of the long-term stability measurements. Together with the low power consumption, it paves the way for a realistic integration of FinFETs into reliable diagnostics and monitoring tools;
  - Demonstration of an "in-situ" amplification based on the connection of two n-MOS components. Based on simple circuit design, the readout sensitivity and linearity can be enhanced for the detection of low charged biological entities.

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[19] results provided as average

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6 Conclusions and Outlook

In this last chapter, the main achievements of this thesis are summarized. From these results, the advantages of FinFETS as sensing devices are outlined and compared to other electronic devices. Finally, prospects for the fabrication process and potential clinical diagnostics applications are discussed.

6.1 Main achievements

The main achievements of each chapters can be summarized as follows[1]:

1. **TCAD Simulations for the Design and Integration of FinFETs**
   The FinFET initial parameters were determined by FEA simulations. With $T_{Fin} = 50\,\mathrm{nm}$, aspect ratio $H_{Fin}/T_{Fin} \geq 3$ and a channel doping concentration $N_A \leq 10^{16}\,\mathrm{cm}^{-3}$, the ideal subthreshold slope of 59 mV/dec can theoretically be achieved. Circuit simulations in SPICE, based on Verilog-A models, were carried out and investigated to design advantageous different types of readout circuits. The following sensing architectures were demonstrated: (i) a common-source amplifier for enhanced sensing readout up to 1 V/pH, i.e. 25 dB gain, (ii) a NOR sensing logic switch with $\Delta V_{on-off} = 2\mathrm{V}$, (iii) a pseudo differential amplifier with tunable gain and a (iv) sensing ring oscillator with $\Delta f = 13\,\mathrm{MHz/pH}$.
2. **Technological Development of FinFETs for Sensing Applications**
   The realization of FinFETs succeeded out of many technological challenges and it can be considered one of the main achievement of the overall work. The outcome of the fabrication are sub-20 nm vertical fins with $H_{Fin}/T_{Fin} \geq 3$ on Si-bulk, realized with more than 80 steps and 7 overlapping mask layouts. To complete the process at least 3 outsourced services were needed, making the fabrication process also challenging in terms of compatibility and coordination with the external partners. The control of the critical local bulk oxidation for the fin insulation was calibrated and optimized by FEA

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[1] results provided as best values

simulations.

3. **Characterization of ALD HfO_2 thin layers**
   This characterization aimed at the determination of the main electrical properties of HfO_2 deposited by ALD. Different estimation methods of the dielectric constant has been discussed. After optimization of some fabrication factors, such as the annealing and the cleaning procedure, $\varepsilon_{HfO_2} = 19.2$ and $V_{BD} = 14\,\mathrm{V}$ with $I_g < 1\,\mathrm{pA}$ were achieved. For what concerns the hysteretic behaviour of HfO_2, it was possible to obtain negligible values, i.e. $\Delta V_H = 9\,\mathrm{mV}$, only by the deposition of a few nm of thermal SiO_2 at the Si interface.
4. **Experimental Results: Metal and Liquid Gate FinFETs**
   The metal gate FinFETs showed an excellent electronic output: $SS = 70\,\mathrm{mV/dec}$ and $\mathrm{I_{on}/I_{off}} = 10^6$. A full pH response with $\Delta \mathrm{V_{th}} = 57\,\mathrm{mV/pH}$ was achieved thanks to the implemented HfO_2 as sensing gate oxide. Many time-dependent measurements were carried out to analyze the FET behaviour when subjected to pH variations and different biasing points. The current variations, $\Delta I_d/\mathrm{pH}$ were in agreement with the expected FET linear-exponential behaviour. A readout sensitivity $S_{out} = 60\%$ and a $SNR = 80$ were achieved. In comparison to other works, the outstanding FinFET features are its stability and accuracy. The stability has been verified with repeated measurements over 4.5 days with a final drift in time of $\delta V_{th}/\delta t \approx 0.13\,\mathrm{mV\,h^{-1}}$. The accuracy has been estimated from the SNR to be 0.01 pH. A sensing common source amplifier has also been demonstrated for the amplification of $\Delta \mathrm{V_{th}}$ with a $\Delta V_{out}/\Delta V_{th} = 6.6$. This result has been obtained by the connection of two FinFETs and could further be optimized by proper transistor sizing. FimH protein has been detected with a response of $\Delta I_d/I_d \approx 50\%$ for functionalized FinFETs with respect to $\Delta I_d/I_d \approx 6\%$ for passive FinFETs.

6.2 Critical discussion of the main advantages of the FinFET on Si-bulk as sensing element

The main advantages of a **FinFET** as sensing element have been identified to be *stability*, *reliability* and *low power consumption.* In terms of sensitivity, excellent results have been obtained. It has been pointed out that, for a given FET device with a specific intrinsic sensitivity ΔV_{th} and subthreshold slope, the same results can be achieved. On the other hand, the demonstrated high stability, is strictly connected to the high channel control, a property already well-known for the FinFET as electronic unit. In this context, it is worth to mention that 22 nm FinFETs are already implemented today in the last Intel's microprocessor on Si-bulk.

If the FinFET is compared to its planar counterpart, the original **ISFET**, their properties should be distinguished in two fields according to their applications: chemical-ionic and biological. Better performances are, in fact, not expected in terms of sensitivity for the ISFET as *chemical* sensor, since the whole surface is involved in the chemical modification. However, for small *biological* entities which are not uniformly distributed in the solution, the dimension and geometry of a functionalized FinFET probe or array would make the difference. Generally, a nanoscale **SiNW** as well as the FinFET, would provide a higher response than other devices, in case of a very localized change of surface potential. If the conductive channel has a comparable dimension with respect to the molecule to be detected, a complete switch ON-OFF of the conduction channel is also possible. Anyway, such an observation does not have a physical origin, because every surface potential change is theoretically detectable. In reality, two signals with similar amplitude, one coming from the SiNW and one from the species to be detected, are more easily comparable, especially in the absence of a good readout circuit. SiNWs, down to 5 nm, will be considered optimal ultra-sensitive biodetectors, as long as sensing ICs will not provide advanced readout functions. For what concern the type of substrate, the use of **Si-bulk** with respect to **SOI** does not have any influence on the sensing properties. It is worth mentioning that the common use of the back-gate for sensing SiNWs on SOI is not compatible with a monolithic CMOS integration approach. Moreover, the development of a sensor should always be compliant with low power constraints of IC integration.

6.3 Outlook

In order to fully exploit the potential of FinFETs as sensors for diagnostic purposes and homecare applications, there are some technological improvements and investigations that could be performed at short and long term.

6.3.1 Technology

For the next batch of devices the following improvements could be taken into account:

- **Gate oxide:** In Sec. 4.5.1, the use of a thermal SiO_2 as interface between the Silicon substrate and the HfO_2 layer resulted in negligible hysteresis; the thermal SiO_2 should be included in the future fabrication and, at longer term, an alternative interfacial layer with higher dielectric constant should be investigated;
- **Substrate:** Towards a faster fabrication, the process could be reiterated with much less steps on SOI wafers, in order to save time and resources for the experiments. The FinFETs will benefit of a better control of the geometrical dimensions;
- **FinFET length:** To improve the robustness of the fins and the electrical performances, their length should be reduced at least from 10 µm to 1 µm. An additional step of e-beam lithography should then be implemented also for the SU-8 layer;
- **Common source amplifier:** The FinFETs can be sized more properly in order to better exploit the gain of the amplifying stage, as previously discussed in Sec. 5.3.4;
- **Integration of the reference electrode:** For the integration in portable or wearable devices, this is a critical point. A first implementation of a pseudo reference electrode should take into account the work of Kim et *al.* [1] from the technology point of view and the work of Tarasov et *al.* [2] for the realization of a true reference SiNW electrode.
- **Noise analysis:** A deep investigation of noise in the frequency domain should be per-

formed as, for example, it has been done by Bedner *et al.* [3]. Especially for fully depleted devices such an investigation could lead to interesting results.

If the possibility of an outsourced fabrication process is taken into account, the FinFETs should be designed and monolithically integrated directly in the CMOS chip used for the readout, as the one described in [4]. While the design of the chip layout could be performed at the academic level, the final tapeout should then be processed in a manufacturing cleanroom. In this way, the research could really focus on the potentiality of such SiNWs as sensors, taking advantage of all IC benefits from the electronic point of view.

6.3.2 Potential diagnostics applications

In Chap. 1, a large number of sensing applications have been mentioned. However, together with the large number of new possibilities that such a technology is capable to introduce, many open questions come along. One of the most promising application of FET sensors is the detection of cancer markers, which are usually proteins [5]. One of the most common markers is the prostate-specific antigen (PSA), which is concentrated in prostatic tissue. Elevated serum PSA level, between 4 and 10 $\mathrm{ng\,mL^{-1}}$, has become an important marker of prostate cancers, at a stage when intervention should reduce morbidity and mortality. However, the merits and methods of screening continue to be debated [6]. For example, PSA levels may be less than 4 $\mathrm{ng\,mL^{-1}}$ in 15 to 38% of men with cancer, indicating a high false-negative rate. From this perspective, the correlation of more screening tools become essential and the role of PSA detection less reliable. The cancer pretreatment and the related harms [7] represent other problems which started to arise from the detection of such markers. It becomes, in fact, very difficult for medical doctors to take action when a patient is diagnosed with high levels of PSA but the cancer has not developed yet. Watchful waiting (active surveillance) is a viable option for certain patients, but patient-reported quality of life and psychological well-being are similar between a definitive diagnose and watchful waiting.

Other possible novel applications where less clinical issues arise and the outcome is less subjected to incertitude can be mentioned:

- **Intra-body monitoring:** A CMOS readout chip integrating the FinFET sensors could be applied for monitoring of the pH or other chemical species within blood. Continuous intra-arterial blood pH monitoring is, in fact, highly desirable in clinical practice [8], either during anesthesia in major surgery (at least 10 hours) or for post-operative monitoring (several days) [9]. However, devices with appreciable accuracy are still not commercially available to date and arterial blood samples are usually drawn intermittently and analyzed by a conventional blood gas analyzer (BGA). Several limitations are associated with intermittent blood sampling [10]. The accuracy should be maintained within ±0.02 pH, without the need for recalibration. For example, the change in hydrogen ions is directly connected to the onset of angina and electrocardiographic abnormalities in ischaemic patients [11].

Monitoring of the intragastric pH also represents an interesting application field. Acid-related diseases are often chronic, under investigated and over treated [12]. The gastric acid output (GAO) can be monitored continuously to address such diseases, but the absence of a non-invasive, accurate and reproducible tool has slowed down its clinical use. Recently, a first attempt for continuous and real-time monitoring has been attempted by catheter-free pills integrating a pH sensor, which wirelessly transmits the data to a small recorder [13, 14]. Differences between the old 24-hour catheter pH systems and these new methods have been reported [15, 16] making this field still open for investigation and improvement.

- **New patterns for health control:** A recent field of research is focusing on the chemical information contained in the human sweat or saliva, which are more accessible than blood. For example, the sodium concentration contained in the sweat and sweat rate could be used to indicate the proper time to hydrate during physical exercise and avoid the risk of muscle cramps. In [17] a rapid colorimetric detection of pH in sweat and saliva is proposed. FET devices could be used for more precise and direct analysis in order to validate the correlation between pH and critical health status such as dehydratation, through sweat analysis, or enamel decalcification, an acidic breakdown of calcium in the teeth, through saliva analysis. Wearable devices for athletes could integrate such monitoring functions.
- **Single-cell analysis:** Blood analysis are normally performed by centrifugation of millions of red blood cells, causing the loss of information by sub-population which may become sick. The single-cell approach, instead, analyzes a large number of individual cells and it determines the distributions of cellular properties [18, 19]. The identification of abnormalities in sub-groups turn out to be a hallmark of physiology and pathology [20]. For example, sickle cell anemia is a blood disorder characterized by an abnormal, rigid, sickle shape of the red blood cells. The abnormal cells can obstruct capillaries and restrict blood flow to an organ, resulting in ischemia, pain, necrosis and often organ damage. If promptly addressed, the effects of the disease may be limited and life expectancy increased. It is also known that the cytosol composition of such cells is different from that of the healthy ones, especially the concentration of sodium and calcium [21]. Lee *et al.* [22] have proposed a lysis method for opening the cells based on a PDMS array with μ-holes able to contain only one cell. Upon an electromagnetic field applied through electrodes locally patterned (electrophoresis), cells release the cytosol components which are then analysed by fluorescence. Such label-die method can be substituted by the direct analysis of the cytosol components by the FinFET fabricated on a Si substrate and aligned with the PDMS trapping array, as shown in Fig. 6.1. The FET devices would have the double use of electrophoresis tools and sensors.

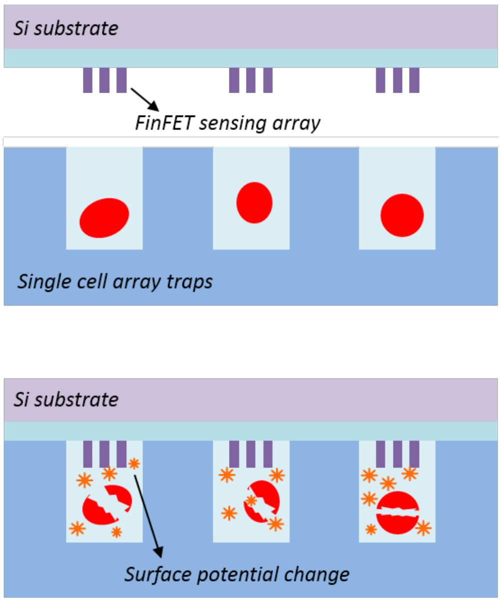

Figure 6.1: Single-cell trapping array with FinFET sensors integrated in the top cover.

6.4 Concluding remarks

With the results presented in Sec. 6.1, the advantages of implementing FinFETs as sensing units have been demonstrated. The same FinFET architecture has been implemented as both sensing and circuit device with excellent outputs. The FinFET structure has been optimized to achieve good electronic proprieties, i.e. high subthreshold slope and I_{on}/I_{off}. A high quality HfO_2 gate oxide has been implemented for full pH response. Boosting both electronic and sensing properties have resulted in pH sensors with state-of-the-art features: (i) full and constant pH response, (ii) high readout sensitivity and high current variation, (iii) robust signal to noise ratio, (iv) low power consumption and voltage supply, (v) enhanced long-term stability and repeatability. The simple connection of two devices has resulted in the amplification of the sensing event without the use of a back-gate. More complex circuits based on frequency readout and logic switch have also been demonstrated by SPICE simulations.
From the technology point of view, the FinFETs have been realized by a top down approach on Si-bulk by a reliable and validated process flow, providing a valuable alternative to SOI substrates, commonly used for SiNWs.

In conclusion, the presented sensing platform based on highly-stable, low-power FinFETs on Si-bulk can be implemented for efficient label-free sensing for non-invasive simultaneous monitoring of human physiological signals, in terms of pH and other chemical and biological entities. The FinFET is demonstrated to be a high-profile candidate for such an enhanced system. The use of scalable high-k dielectric FinFETs for both sensing and circuit applications is, in fact, in accordance with the material and physics constraints which come along Moore's law of scaling, and it is fully compatible with CMOS integration, paving the way towards

Sensing Integrated Circuits.

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A The center of microNanoTechnology (CMi)

The Center of MicroNanoTechnology (CMi) is a complex of cleanrooms situated at the BM building at EPFL. The manin facility on the level -1 offers ten ISO 5/Class 100 working areas separated according to their functionality. Five additional ISO 6/Class 1.000 and ISO 7/Class 10.000 working areas have recently been opened on the superior level and linked together via an elevator. Figure A.1 shows all the available working areas with their specific type of process.

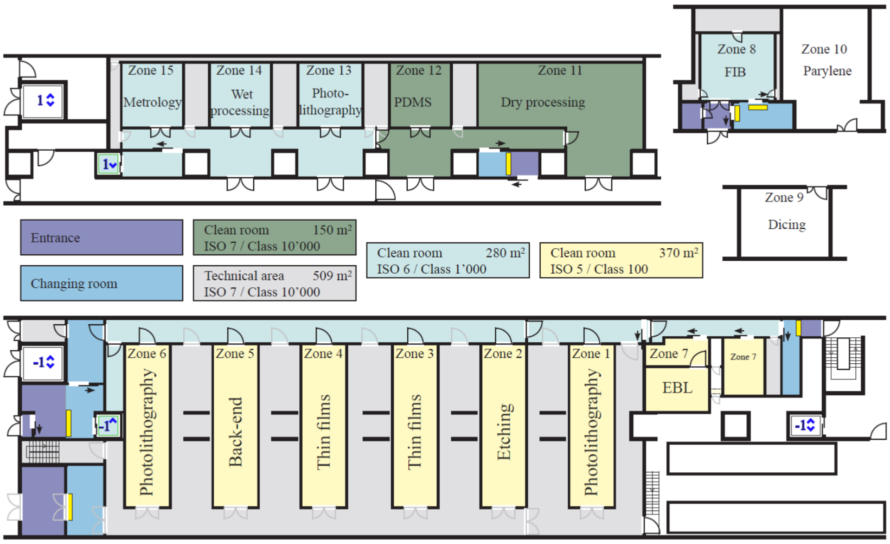

Figure A.1: The CMi cleanroom complex of all working areas with corresponding classment and type of proces (http://www.cmi.epfl.ch).

For a microelectronic compatible process the use of the equipment available on level -1 is highly recommended. All the zones located at level -1 have been involved in the fabrication of the FinFETs herein presented. The use of zone 8, where a Focused Ion Beam (FIB) and Scanning Electron Microscope (SEM) are located, has been indispensable throughout the whole process. Some of the areas on level 1 have been used mostly for the final device packaging prior to the microfluidic assembly.

B Process simulation code for local SOI oxidation

```

#--- 2D Grid definition -------------------------------------------
line x location=0.0      spacing=  10<nm> tag=SiTop
line x location=0.6<um>  spacing=10<nm> tag=SiBottom
line y location=0.0      spacing= 10<nm> tag=SiLeft
line y location=1.5<um>      spacing= 10<nm> tag=SiRight

#--- Initial simulation domain -------------------------------------
region Silicon xlo=SiTop xhi=SiBottom ylo=SiLeft yhi=SiRight
init concentration=1.0e+16<cm-3> field=Boron wafer.orient=100

#--- MGOALS settings for automatic meshing in newly generated layers -
mgoals min.normal.size=1<nm> max.lateral.size=0.1<um> \
           normal.growth.ratio=1.4

\#---Mask Definition ad Silicon Etching-------------------------------------
mask name=etching_mask segments = { 345<nm> 405<nm> 1035<nm> 1095<nm> }
etch silicon type=anisotropic thickness=0.22<um> mask=etching_mask

#---Growing Gate Oxide---------------------------------------
mgoals min.normal.size=1<nm> max.lateral.size=2.0<um> \
  normal.growth.ratio=1.4 accuracy=2e-5
deposit Oxide thickness=5<nm> isotropic

#---Nitride Spacer---------------------------------------
mask name=etching2_mask segments = { 290<nm> 460<nm> 980<nm> 1150<nm> }
deposit nitride type=isotropic thickness=50<nm>
etch nitride type=anisotropic thickness=50<nm> mask=etching2_mask

#---Oxide Etching---------------------------------------
etch oxide  type=anisotropic thickness=0.005<um> mask=etching2_mask

#---Silicon Etching---------------------------------------
etch silicon type=isotropic time=1.0 rate= {0.1015}
struct tdr=etching

#---Bulk Oxidation---------------------------------------
#####---Ramp up

temp_ramp name=RampUp temperature=800<C> time=17.5<min> ramprate=10<C/min>
temp_ramp name=RampUp temperature=975<C> time=5<min> ramprate=5<C/min>
temp_ramp name=RampUp temperature=1025<C> time=12.5<min> ramprate=2<C/min>
```

```
gas_flow name=Ramp_up flowN2=10 flowO2=0.5
diffuse temp_ramp=RampUp gas_flow=Ramp_up

#####---Oxidation
gas_flow name=Oxidation flowN2=10 flowO2=10
diffuse temperature=1050<C> time=85<min> gas_flow=Oxidation


#####---Ramp down
gas_flow name=Ramp_down flowN2=10 flowO2=0
temp_ramp name=RampDown temperature=1050<C> time=80<min> ramprate=-3<C/min>
diffuse temp_ramp=RampDown gas_flow=Ramp_down
struct tdr=oxidation
```

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- Solid analytical skills for device design and problem management and solving
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- Proficiency in English and French, Italian mother tongue, basic German

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02 - 09/2007	**Internship at INRIM, Turin, Italy** *Characterization of magnetic nanoparticles for cancer treatment based on hyperthermia*

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- Design and fabrication of micro and nano devices for diagnostics and medical applications
- MEMS and NEMS (Micro- and Nano-Electromechanical Systems)
- State-of-the-art nanoscale electronic and solid-state physics devices
- Foundation (seminars, courses, personal interest) in Risk Management and Quality System Regulations

Technical Skills

Technology	➢ Cleanroom techniques: photo/e-beam lithography, dry/wet etching, thin film deposition, electron microscopy (SEM, FIB, TEM), microelectronic and microfluidic packaging. ➢ Electrical characterization of MOSFETs, ISFETs and MOSCAPs in dry/liquid environment. ➢ Experienced with high vacuum, cryogenic, electromagnetic and photonic apparatus; ➢ Experienced in cell handling, pH environment testing and surface functionalization;
Information Technology	➢ Finite Element Analysis: Sentaurus, ANSYS, ATLAS ➢ Electronic Design Automation: Cadence PSpice ➢ Programming: Labview, Verilog-A, C++, VHDL, FORTRAN99, Matlab, Office

List of Publications

Journal Papers

S. Rigante, P. Scarbolo, D. Bouvet, M. Wipf, K. Bedner, and A. M. Ionescu, "Technological Development of High-k Dielectric FinFETs for Liquid Environment", *Solid-State Electronics*, Accepted, In Press, 2014

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