Parallel vs. Serial Inter-plane communication using TSVs

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***Abstract*— 3-D integration is a promising prospect for implementing high performance multifunctional systems-on-chip. Through Silicon Vias (TSVs) are the enablers for achieving high bandwidth paths in inter-plane communications. TSVs also provide higher vertical link density and facilitate the heat flow in the 3-D circuits as compared to other potential schemes such as inductive links. However, reliability issues and crosstalk problems among adjacent TSVs decrease the yield and performance of TSV based circuits. Reducing the number of TSVs employed for inter-plane signal transferring can alleviate these problems. This paper proposes to exploit serialization to reduce the number of TSVs in a 3D circuit and presents a comparison between different aspects of TSV-based 3-D circuits such as area, power, crosstalk and yield in parallel and serial vertical links.**

Keywords—TSV, Crosstalk, Serialization

I. INTRODUCTION

3-Dimensional (3-D) integration is a design paradigm that can mitigate many of the increasing challenges for designing modern *System on Chips* (SoCs). 3-D circuits provide a potent approach to enhance the performance and integrate diverse functions within a multiple-plane stack. Performance improvement in 3-D circuits originates from the drastic decrease in the on-chip interconnect length, since in recent circuits the interconnect latency is the bottleneck limiting the performance of the circuits. Thus storage access on a plane above/below the processing plane is crucial to enhancing performance. Employing an efficient medium for data communication among different planes is a key factor in achieving a high performance 3-D system. *Through Silicon Vias* (TSVs) produce the highest interconnect bandwidth for 3-D systems as compared to other vertical links such as wire bonding, peripheral vertical interconnects, and solder-ball arrays. Moreover, they support better heat transport within plane and mitigate the thermal problems, which are much more critical in 3-D circuits as compared to 2-D ones.

On the other hand, manufacturing issues are one of the primary challenges for TSV-based 3-D circuits. Vertical interconnects require additional manufacturing process steps rather than standard process. These additional steps increase the manufacturing cost and lead to lower fabrication yield for the entire system. As shown in [9], increasing the number of TSVs adversely affects the yield of a 3-D circuit. Moreover the area footprint of TSVs and related keep-out areas is significant.

Crosstalk among TSVs is another important concern that can affect the signal integrity and timing of the transferred data. In standard 2-D circuits the crosstalk is usually caused by the two neighboring wires on the same layer. 3-D circuits are more vulnerable to crosstalk since TSVs are bundled and thus most TSVs are surrounded by other TSVs. Consequently, a TSV can be affected by several adjacent TSVs from all directions

Serialization can be considered as a solution to alleviate the challenges related to TSV bunches for transferring data among the planes. Converting parallel data into higher-rate serial data can reduce the number of TSVs and consequently area and cross-talk effects. Conversely, using serializer/deserializers circuits can add complexity to system design, specifically when bandwidth is limited and with respect to power consumption.

This paper proposes a case study of serial vs. parallel data communication for TSV-based 3-D circuits. For parallel data communication, crosstalk and resulting jitter is investigated. The power consumption, area and fabrication yield for serial and parallel approaches are compared.

In the following section the cross talk among a bunch of TSVs is considered for several cases. In Section III a review of serialization method is presented and the simulation results are discussed in Section IV. Some conclusions are offered in Section V.

II. CROSS TALK

One of the challenges in TSV-based 3-D circuits is the cross talk between adjacent TSVs. To analyze the effect of neighboring TSVs on each other an accurate model for TSVs is required. Different models for TSVs have been proposed in [4][6]. The *RLC* model used in our study is shown in Fig. 1 where the resistance of this model is described as [7]:

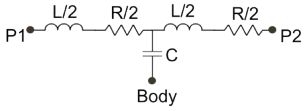


Fig. 1. *RLC* model for TSV

$$R = R_{dc} + R_{ac} \quad (1)$$

This work is funded in part by the Swiss National Science Foundation (No. 260021_126517), European Research Council Grant (No. 246810 NANOSYS).

where R_{dc} and R_{ac} are defined as:

$$R_{dc} = \frac{\rho l_{tsv}}{\pi r^2} \tag{2}$$

$$R_{ac} = l_{tsv} \frac{\sqrt{\pi \mu f \sigma}}{r\sigma} \tag{3}$$

and l_{tsv}, r, denote the length and radius of the TSV. The frequency is denoted by f, the magnetic permeability by μ , and the electric conductivity of the TSV metal by σ.

The capacitance and inductance of the TSV is:

$$C_{si} = \frac{2\pi\varepsilon_{si} l_{tsv}}{\ln\left(\frac{r + tox}{r}\right)} \tag{4}$$

$$L_{tsv} = l_{tsv} f(b) \tag{5}$$

$$f(b) = \frac{\mu}{2\pi}\left[\ln\left(2b^{-1} + \sqrt{(0.5b)^{-2} + 1} + 2b^{-1} - \sqrt{(0.5b)^2 + 1}\right)\right] \tag{6}$$

where t_{ox} is the dielectric thickness and ε_{si} is the dielectric constant of silicon and $b=2r/l_{tsv}$.

Each TSV can affect the adjacent TSVs in two ways. The first way is injecting the noise in silicon bulk via TSV body capacitor (C_{TSV}), which can be transferred to the victim TSV along the capacitive, resistive silicon path (Csi and R_{si}). The second way is inductive coupling between the inductors of adjacent TSVs.

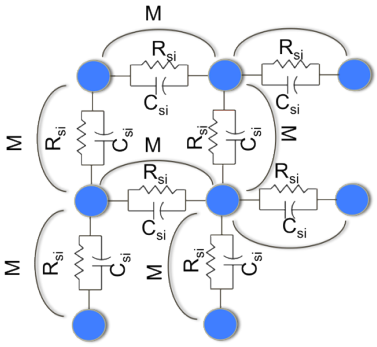


Fig. 2. TSV to TSV coupling where M shows the mutual inductance

The model for analyzing the crosstalk in TSV bunches is shown in Fig. 2. For simplicity, each TSV is assumed to be affected only by the four closest neighboring TSVs. The resistance and capacitance of the bulk and as in [8]:

$$R_{si} = \frac{\rho d}{2rl_{tsv}} \tag{7}$$

$$C_{si} = \frac{\pi\varepsilon_{si}}{\cosh^{-1}\left(\frac{d}{2r}\right)} \tag{8}$$

Where d is the pitch of the two TSVs.

The mutual inductance of two adjacent TSVs is described by (6) where b is defined as $2d/l_{tsv}$[7].

Fig. 3 illustrates different topologies for TSV bunches considered to study crosstalk. In Fig. 3(a) the body of each TSV is connected to ground through a guard ring, p+ well over the resistive, capacitive bulk which prevents neighboring TSVs to induce noise to it. Fig. 3(b) shows a shielded topology where ground TSV are employed to mitigate the interference between adjacent TSVs and in Fig. 3(c) a bunch of signaling TSVs are located without using shielding methods.

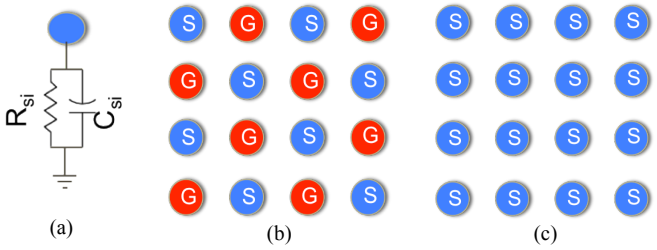


Fig. 3. Different topologies for studying crosstalk where (a) shows the grounded TSV, (b) is the shielded topology and (c) is the bunch of TSV without shielding.

Fig. 4 shows the eye diagram for the output signal of a TSV whit a diameter of 5 µm located in a bunch of 16 TSVs with the pitch of 10 µm. As expected, the signal integrity for the TSVs with connection to ground is better than the other topologies since the signal is not affected by the neighboring TSVs. Exploiting ground TSVs can alleviate the crosstalk issues, but it drastically increases the number of TSVs and hence the reliability and yield challenges in the circuit.

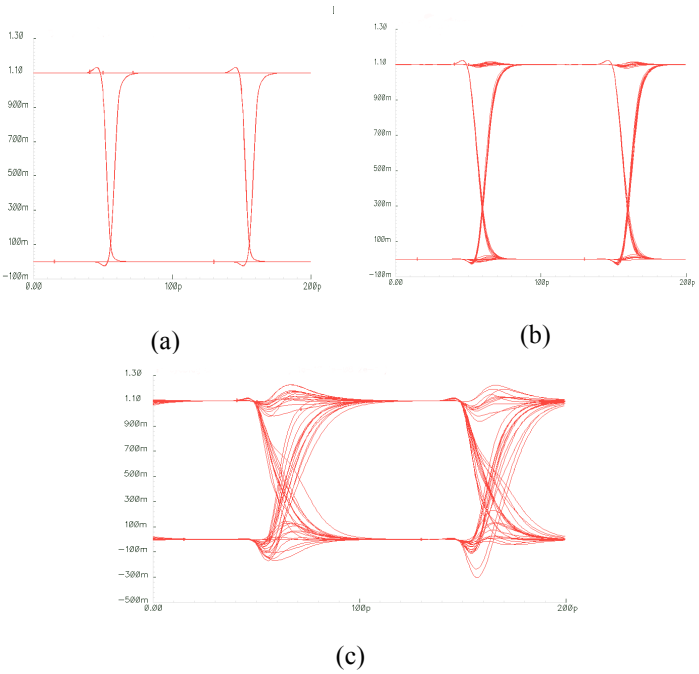


Fig. 4. Eye diagram for different schemes for 16 bit where (a) is for grounded TSVs, (b) is for shielded TSVs and (c) is for coupled TSVs

III. SERIALIZATION

Although data parallel TSV connection provide the highest bandwidth for inter-layer data communication, reliability, yield and area issues suggest the use of serial communication,

Moreover exploiting TSV bunches can affect the signal integrity due to crosstalk between the TSVs as discussed in the previous section. These problems encourage us to explore the data serial/parallel trade-off for decreasing the number of TSVs while preserving the performance of the system.

Serialization is one of the solutions for overcoming the aforementioned issues. Since TSVs can transfer data up to 40 Gb/s [10][11], serializing the data and reducing the number of TSVs can help to improve the yield and fabrication cost of the system and reduce the area occupied by the TSVs. Fig. 5 shows the two approaches for inter-plane communication where the serial structure shown in (b) replaces n parallel circuit shown in (a) using *n:1*/*1:n* serializer/deserializer. The area and power consumed by serializer/deserializer must be considered as the overhead of serialization. Typically, the area of the serializer and deserializer is very small compared to the TSV footprint and reducing the number of TSVs considerably saves area which makes the power consumption the only real drawback of this approach.

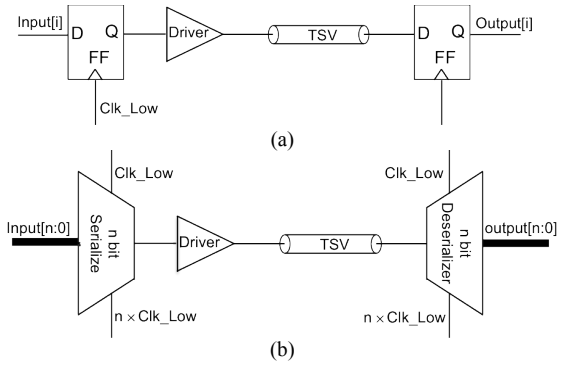
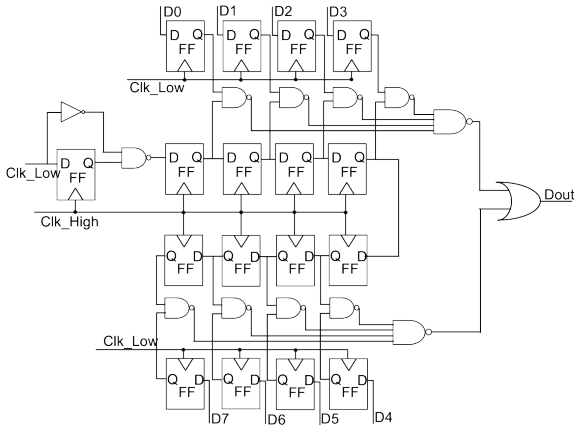
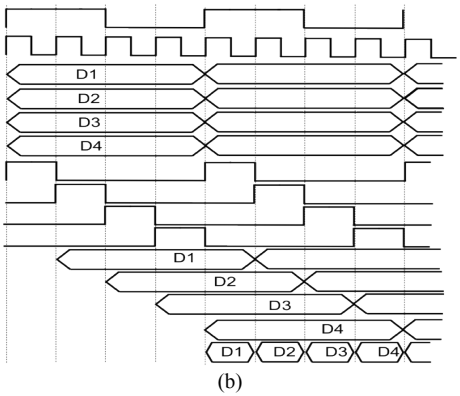


Fig. 5. Parallel and serial method for inter-plane data communication where (a) shows the parallel approach and (b) is the serial one.

A tree-type serilazer/deserializer [4] is designed in 65 nm CMOS technology that can operate at up to 10 GHz serial clock frequency. The structure of the serializer is shown in Fig. 6(a) where the serialization rate is 8. Different phase selection signals are generated and used to sample the inputs and serialize as shown in Fig. 6(b).



(a)



(b)

Fig. 6. Serializer circuit and signaling

Using encoding schemes to reduce the power consumption of the serialization circuit is one potential solution to reduce the switching activity and hence the power consumption of the circuit. Some encoding methods such as ETI [2] and TCI [3] have been designed and simulated. Simulation results show that the power consumed by the encoder/decoder circuits is much more than the power reduced by decreasing the switching activity. Accordingly, exploiting encoding methods is not a proper solution to reduce the power consumption of serialization method.

IV. SIMULATION RESULTS

This section presents the simulation results for different aspects of inter-plane communication such as jitter, area, and fabrication yield.

The fabrication yield of the 3-D circuit is described as [9]:

$$Y = \left(Y_{die}\right)^{N_{tier}} . \left(Y_{stacking}\right)^{N_{tier}-1} \tag{9}$$

$$Y_{stacking} = Y_{bonding}\left(1 - f_{tsv}\right)^{N_{tsv}} \tag{10}$$

where N_{tier} is the number of layers stacked and Y_{die} is the yield of a single die, $Y_{bonding}$ is the yield of 3-D process, f_{tsv} is the TSV failure rate and N_{tsv} the total number of TSVs. To estimate the effect of TSV number on the yield of a two-plane 3-D circuit, we assume that Y_{die}, $Y_{bonding}$, and f_{tsv} are 0.95, 0.98 and 1e-6 where N_{tier} is two.

TSVs are modeled using the *RLC* model shown in Fig. 1. The *RLC* model shown in Fig. 1 is used to estimate the resistance, inductance, and capacitance of the TSVs. Three different TSV diameters are considered where the parameters of the interconnects are listed in Table 1.

TABLE I. TSV PARAMETER

TSV diameter [μm]	R [mΩ]	C [fF]	L [pH]
5	297	18	46
10	103	41	36
50	17	218	17

The crosstalk for 16 bundled TSVs is simulated. Three different topologies shown in Fig. 3 are considered. The bandwidth of the input data is 5 Gb/s. To measure the TSV

signal quality, an eye diagram plot is used and the jitter of the signal is calculated and listed in Table. II.

TABLE II. JITTER FOR A BUNCH OF 16 TSVS

Pitch [μm]	With Shielding	Without shielding
	Jitter [ps]	Jitter [ps]
D= 5μm		
10	1.12	8.59
15	0.74	7.36
20	0.53	4.95
D=10		
20	0.4	2.34
30	0.34	1.4
40	0.21	1.34
D=50		
100	0.27	0.75
150	0.18	0.
200	0.11	0.32

As shown in this table, the jitter is felt more in smaller TSVs since the inductance of the TSVs decreases by increasing the size of TSVs. Moreover by increasing the size of TSVs the pitch of adjacent TSV also increases which reduces the inductive and capacitive coupling between the TSVs. Ground shielding can reduce the jitter of the bunch of 16 signaling TSVs up to 86% while it increases the number of TSVs to 44.

To alleviate crosstalk problem without drastically increasing the TSV area, serialization method is considered. Simulation results for different number of bits is listed in Table III where TSVs with 10 um diameter are used. Since the area of the serializer and deserializer is less than the footprint of the TSV, the area reported in the table is the area of TSVs.

TABLE III. OPERATING FREQUENCY, POWER, AND AREA FOR DIFFERENT SERIALIZATION RATE

	Parallel Clok Freq.	Serial Clock Freq.	Power	Area
8bit				
Parallel	1000		237	628
W/O encoding	1000	8	984.6	78.5
TCI encoding	1000	9	1202	78.5
16 bit				
Parallel	529		385	1256
W/O encoding	529	7.5	1326	78.5
TCI encoding	529	8	1530	78.5
32 bit				
Parallel	273		251	2512
W/O encoding	273	7.75	2193	78.5
TCI encoding	273	8	2345	78.5

As shown in Fig. 7, reducing the number of TSVs from 32 to 1 can improve the fabrication yield of the whole circuit by 0.0022% which is negligible.

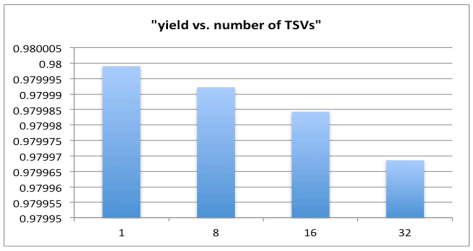


Fig. 7. Yield vs. Number of TSV

Since the designed serializer/deserializer circuit can operate at maximum frequency of 10 GHz, the frequency of the input signal limited to 10/n GHz where *n* is the serialization rate. For signals below this frequency the performance of the system does not degrade due to serialization where for faster signals errors caused by serialization circuit decreases the performance of the system.

V. CONCLUSIONS

The crosstalk effect on bundled TSVs is considered where for a buch of 16 TSVs, up to 8.95 ps jitter is added to a 5 GHz bandwidth data due to TSV to TSV coupling. Exploiting grounded TSVs to shield the signaling TSVs can reduce the jitter by 86% but alternatively increases the total number of TSVs to 44.

Serialization is proposed to improve the signal integrity and reducing the number of TSVs. Using serialization drastically reduces the TSV area and improves the fabrication yield of the circuit by 0.0022%. On the other hand the power consumed by the serializer/deserializer is not negligible and should be carefully considered and compared to the power of the whole 3-D circuit to find out if this approach is a proper solution for a certain application or not.

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