A Low-Overhead Method for Pre-bond Test of Resonant 3-D Clock Distribution Networks

Somayyeh Rahimian, Vasilis F. Pavlidis, and Giovanni De Micheli
Integrated Systems Laboratory, EPFL, Lausanne, Switzerland
{somayyeh.rahimianomam, vasileios.pavlidis, giovanni.demicheli}@epfl.ch

***Abstract*—Designing a low power clock network in synchronous circuits is an important task. This requirement is stricter for 3-D circuits due to the increased power densities. Resonant clock networks are considered efficient low power alternatives to conventional clock distribution schemes. These networks utilize additional inductive circuits to reduce power while delivering a full swing clock signal to the sink nodes. Test is another complex task for 3-D ICs, where pre-bond test is a prerequisite. Contactless test has been considered as an alternative for conventional test methods. This paper, consequently, introduces a design methodology for resonant 3-D clock networks that supports wireless pre-bond testing through the use of inductive links. By employing the inductors comprising the *LC* tanks of the resonant clock networks as the receiver circuit for the links, the need for additional circuits and/or interconnect resources during pre-bond test is essentially eliminated. The proposed technique produces low power and pre-bond testable 3-D clock distribution networks. Simulation results indicate 98.5% and 99% decrease in the area overhead and power consumed by the contactless testing method as compared to existing methods.**

Keywords – 3-D integration, resonant clocking, contactless testing, inductive link

I. INTRODUCTION

3-D integration is a promising candidate for implementing high performance multifunctional systems. One of the main challenges for the high volume production of 3-D circuits is manufacturing and the related yield implications. Fabrication processes for 3-D circuits include some additional steps as compared to standard CMOS processes, such as wafer thinning and TSV fabrication. This manufacturing complexity makes 3-D circuits more susceptible to manufacturing defects, which can lower the overall yield of the bonded 3-D system. Testing vertical interconnects prior to bonding the next layer is an efficient method to improve the yield of the 3-D circuit [1]. Another useful method to improve yield is wafer level pre-bond test, which includes testing each layer prior to bonding [2], [3].

A common method for wafer level test is to employ a probe card and mechanically connect the test needles to the *device under test* (DUT) [4]-[5]. The area overhead of the test pads, the risk of damage in low-k dielectrics and deforming the pads are the important issues in conventional wafer level test. Wafer level test of the unbonded wafers for 3-D systems is subjected to new issues that should be addressed. For example, broken scan chains that should be considered to support pre-bond scan test [4]-[5]. Another issue resembling the broken chains is the, typically, fragmented clock networks within each layer of the stack. Due to this situation, new methods are needed to provide synchronization to each layer during pre-bond test.

Low power is also a significant design objective for clock distribution networks [6]. The decrease in the interconnect length for 3-D circuits can result in a reduced number of clock buffers and provide more power-efficient clock networks [7]. Conversely, volumetric integration can exacerbate power densities accentuating thermal issues for these circuits. Consequently, designing low power clock networks for 3-D circuits becomes a predominant issue.

By employing resonant clocking the clock buffers are removed considerably reducing power [8]-[10]. In this approach, on-chip inductance is added to the clock network forming a resonant circuit with the interconnect capacitance. Consequently, the power consumed by the network decreases, since the energy alternates between electric and magnetic fields instead of being dissipated as heat. This on-chip inductance can also be utilized as the receiver of an inductive link providing the clock signal within a layer during pre-bond test.

By wireless transmission, the clock signal can, consequently, be propagated with low overhead. Moreover, wireless test can eliminate the need for test probe pads used only for pre-bond test. Wireless test has been explored and reported to improve the cost and reliability of the test process in VLSI circuits by reducing the manufacturing defects caused by adding test pads [11]-[13]. Possible technologies for wireless test are RF, near field (including capacitive and inductive coupling), and optical communication. Due to the short distance between the layers in 3-D integrated circuits and the on-chip inductors for the resonant clock networks, near field communication is the proper candidate for wireless test in these circuits [11].

The contribution of this paper is, consequently, a design methodology of resonant clock networks for 3-D circuits that support wireless pre-bond test through the use of inductive links. Resonant operation is ensured for each layer either in test or functional mode and the clock signal characteristics are maintained within each layer and for either operating mode. To support wireless communication between the *automatic test equipment* (ATE) and the DUT, the off-chip part of the inductive link is designed to deliver a full swing sinusoidal clock signal for the test and normal operation frequencies.

Recent techniques for providing pre-bond testable clock networks are discussed in Section II. The concept of resonant clock networks is introduced in Section III. A new method for the pre-bond wireless test of resonant clock networks is proposed in Section IV. The design of 3-D resonant clock networks and the transceiver circuits producing the clock signal for scan and at-speed testing is described in this section. Simulation results are presented in Section V for a case study where the correct operation of the proposed technique is demonstrated. A comparison with other pre-bond test techniques is of-

fered, where the advantages and limitations of the new technique are also discussed. Some conclusions are drawn in the last section.

II. Existing Synchronization Methods for Pre-Bond Test of 3-D ICs

At-speed scan test ensures good test coverage for integrated circuits [14]-[17]. Scan-based test requires that test patterns are scanned at a low clock frequency before the fast capturing clock is applied. To provide at-speed scan test, the scan chain is loaded at the test clock frequency; afterwards, two clock pulses at operating frequency are applied to the chain [14]. Therefore, to produce the proper timing for capturing the data, the clock signal should efficiently switch between the two frequencies. In other words, any technique that provides the clock signal for test should satisfy this requirement. In this section, different methods of supporting synchronization during pre-bond scan test for 3-D circuits are discussed.

To better explain these methods consider the two-layer 3-D circuit shown in Fig. 1(a). The second layer includes four disconnected networks. These networks connect with *through-silicon vias* (TSVs) to the first layer where the main tree supplies the clock signal to the entire clock distribution network. To test prior to bonding the second layer, the clock signal must be provided to these disjoint networks. The most common method to perform this task is by using redundant wiring and an additional clock driver following, for example, the principles of the technique in [3] (see Fig. 1(b)). Another way to deliver the clock signal is to use a *delayed locked loop* (DLL) for each local network [18] (see Fig. 1(c)).

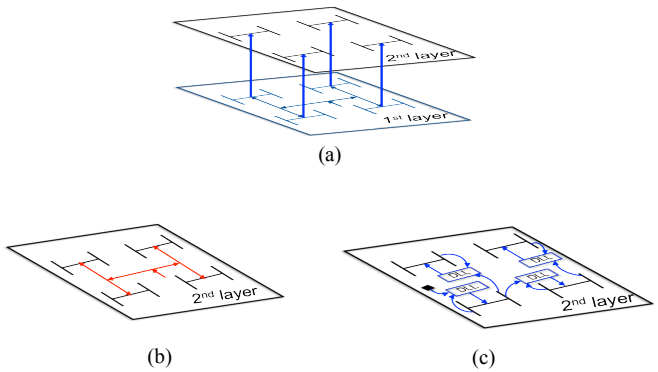

Figure 1. Different methods to pre-bond test a 3-D circuit with two layers (a), the clock signal for pre-bond test of the second layer is provided by (b) the use of redundant wiring, and (c) the use of a DLL for each local network.

Both of these methods can also be applied (with significant overhead) to resonant clock networks, the fundamental concepts of which are presented in the following section.

III. Principles of Resonant Clock Network Design

A design of a global clock distribution network is presented in [9], in which four resonant circuits are connected to a conventional H-tree structure. Each quadrant consists of an on-chip spiral inductor that resonates with the wiring capacitance of the clock network and a decoupling capacitor connected to the other end of the spiral inductor. A simple lumped circuit model is utilized in [9] to determine the resonant inductance. The resonant frequency of the network is (in first-order) estimated by $f_{res} = \frac{1}{2\pi\sqrt{LC}}$ where C and L, respectively, denote the equivalent capacitance of the interconnect network and the inductance of the spiral inductors. The decoupling capacitor is employed to provide a positive voltage offset on the grounded end of the resonant inductor and adapt the voltage level to the CMOS logic level [20]. This capacitor should be sufficiently large to guarantee that the resonant frequency of the decoupling capacitor $f_{res\_dec} = \frac{1}{2\pi\sqrt{LC_{decap}}}$ is much lower than the desired resonant frequency of the clock network.

To deliver a full swing signal at the sink nodes, the magnitude of the transfer function of the network H_{out}, should be close to one. This parameter is often set to 0.9 [9], [20] (for the remainder of the paper a "full swing signal" implies any signal swing that satisfies this specification). When $|H_{out}|$ is fixed at 0.9, the driver resistance can be determined by

$$R_{driver} = \sqrt{\frac{\left|H(j\omega)\right|^2 \cdot \left|Z_{in\_\omega}\right|^2}{0.9^2} - Im\left(Z_{in\_\omega}\right)^2} - Re\left(Z_{in\_\omega}\right). \qquad (1)$$

Several resonant circuits can be utilized to improve the characteristics of the clock signal. If the resonant circuits are placed closer to the driver, fewer resonant circuits are needed. Alternatively, when these circuits are placed close to the sink nodes, more LC tanks are required. Since the equivalent inductance is the parallel combination of all the inductors, increasing the number of resonant circuits leads to a larger required inductance for each circuit. Using a higher number of larger inductors results in greater area occupied by the resonant inductors.

The number of resonant circuits also affects the output signal swing. As discussed in [20], by increasing the number of resonant circuits and placing these circuits closer to the sink nodes, each inductor resonates with a smaller part of the circuit resulting in lower attenuation of the output signal swing. Alternatively, increasing the number of resonant circuits and using larger inductors in each LC tank reduces the quality factor of the LC tanks, since in spiral inductors the *effective series resistance* (ESR) increases more aggressively than the inductance [9]. A lower quality factor for resonant circuits produces a higher signal loss and decreases the output signal swing.

IV. Design of Wirelessly Pre-Bond Testable 3-D Resonant Clock Networks

Combining the inductive coupling and the resonance operation is an efficient way to remove area and power overheads that the existing pre-bond test techniques entail. The design of 3-D resonant clock networks supporting inductive pre-bond test is discussed in this section. For the resonant clock network the available on-chip inductors can form part of the inductive links that transfer the clock signal during pre-bond test. Since every local network includes at least one LC tank to support resonance, the resonant inductor can also be utilized as the receiver of the link (see Fig. 2). Consequently, each network resonates separately, providing the clock signal to the registers (FFs) in the proximity. No other means (*e.g.,* DLLs or redundant wires) are, therefore, needed to connect these networks.

There are two important aspects to design a wirelessly testable resonant 3-D clock network; 1) designing the on-chip resonant 3-D clock network and 2) providing the transceiver cir-

cuit required for wireless communication during the pre-bond test. To support the pre-bond test for a resonant clock network, resonant operation should be achieved for each unbonded layer during test irrespective of the employed pre-bond test approach. The resonant 3-D clock network should be designed so that resonant operation at a specific frequency is individually achieved for each layer during test as well as for the entire 3-D system during normal operation. A design methodology for 3-D resonant clock networks is presented in subsection IV-A. In subsection IV-B, a transceiver circuit that can deliver the clock signal to the on-chip clock network in both operating and test frequencies is proposed. Since the ATE layer can be used to test several DUTs, the design of the transceiver aims at simplifying the receiver circuit and shifting any design complexity to the transmitter side.

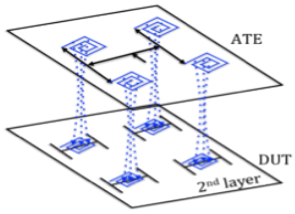

Figure 2. Inductive transfer of the clock signal for pre-bond test.

A. *Resonant clocking for 3-D ICs*

Based on the previously mentioned design considerations for resonant networks, different clock network topologies are considered to adapt the planar resonant clock networks to 3-D circuits [19]. The related tradeoffs among the location and number of *LC* circuits to support resonance for those topologies should also be carefully considered in the design process. A candidate topology is denoted as "symmetric topology" where each layer contains resonant circuits. In another structure, denoted as "asymmetric topology", the resonant circuit is placed in only one layer and should resonate with the total capacitance of the 3-D stack at the desired frequency. During pre-bond test, however, each layer should separately resonate. Note that this requirement is an additional constraint specific to resonant networks and is not related to the techniques that can be employed to connect the incomplete networks [3], [18] in either a standard or resonant clock distribution approach. Consequently asymmetric structures, which can be considered as an extension of 2-D clock networks, do not support pre-bond test in a straightforward manner, since the resonant circuit is contained within only one layer.

The other important parameter in designing a resonant 3-D clock network is the number of TSVs used to connect the physical layers. From this perspective, different topologies can be explored. For example, a single TSV (or a small group of TSVs connected in parallel) is placed at the center of each layer or multiple TSVs are placed in more than one location. In the multiple TSV structure, one of the layers contains a complete clock tree, where for the other layers the clock network consists of several disconnected networks each connected to the first layer by TSVs. Increasing the number of TSVs results in more partial networks increasing the area occupied by the TSVs.

To specify the parameters of resonance for a 3-D system, a distributed *RLC* model of the clock distribution network is employed. For an H-tree resonant network, the number of sinks is determined based on the circuit area and the load capacitance that each sink drives. Assuming a 3-D clock network with N layers and n branch levels in each layer, the number of sink nodes is $N \cdot 2^n$. TSVs can be placed at any of these n levels. Connecting the networks within each layer at the i^{th} level of the primary clock network results in $2^{(i-1)}$ TSVs. For these TSVs, the number of *LC* tanks in each layer should be more than the TSVs such that at least one *LC* tank is connected to each local network to ensure the resonance behavior during pre-bond test. The location of *LC* tanks is swept from the TSVs to the sinks and the resonant parameters, power consumption, and driver resistance for each topology are determined. Based on this comparison, the topology with the desired characteristics can be selected.

To determine the resonant parameters for a specific topology, the driver resistance is adapted to produce a transfer function amplitude of 0.9 for a wide range of inductor sizes using (2). The driver resistance and corresponding power consumption are swept versus the inductance. The inductance for which the driver resistance is maximum or the power consumption is minimum (which do not necessarily occur for the same frequency) is determined. In a 3-D system, the transfer function for different layers can be different due to the effect of the TSV. Not surprisingly, the layer(s) with the greatest distance from the clock driver exhibit(s) the lowest signal swing. The driver size should be determined such that the signal swing for every layer meets the specifications. Consequently, the transfer function magnitude of the last layer should be used in (2). Following this process, the number of the *LC* tanks and the parameters of the resonant circuits are determined for normal operation.

B. *Transceiver circuit for the inductive link*

In standard clock networks, the clock signal is pulse shaped and if inductive links transfer the clock signal, the coupled current and voltage should be recovered at the receiver. Alternatively, in resonant clock networks, the global clock signal is sinusoidal and the buffers at sink nodes can convert the clock signal to a square waveform. Alternatively, proper flip-flops for resonant clock networks can be utilized [21]. Due to the sinusoidal shape of the coupled clock signal in resonant clock networks, the receiver circuit in these networks is less complex as compared to inductive links in conventional clock networks. Since the receiver voltage is also sinusoidal, no additional receiver circuitry is required to recover the transferred voltage.

The circuit of the inductive link is illustrated in Fig. 3. The inductance of the receiver L_R is determined as described in the previous section. The coupled voltage is determined by

$$V_R = L_R \frac{dI_R}{dt} + M \frac{dI_T}{dt}, \tag{2}$$

$$|V_R| = \left(L_R \cdot I_{R\max} + M \cdot I_{T\max}\right) \cdot \omega, \tag{3}$$

where ω denotes the frequency of the coupled signal.

The clock signal at the sink nodes is described by

$$V_{sink} = H_d(j\omega) \cdot V_R, \tag{4}$$

where $H_d(j\omega)$ is the transfer function for the local clock tree and V_{sink} is the amplitude of the clock signal at the sink nodes. The transmitter inductance L_T and, hence, the transmitter current I_T should be determined such that the clock signal at sink nodes described by (4) is a full swing signal in both frequencies. From (2) and (4), I_T is written as

$$I_T = \frac{V_{sink}}{Z_d(\omega)} \cdot \frac{Z_d(\omega) - L_R \cdot j\omega}{M \cdot j\omega}, \quad (5)$$

where Z_d denotes the impedance of the clock network.

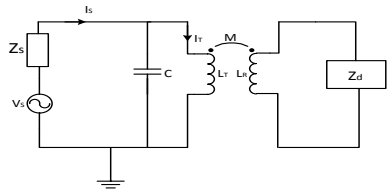

Figure 3. Adapted tranceiver circuit for an inductive link, where the receiver is included in the resonant clock network.

The capacitance C is added to the transmitter circuit to reduce the source current and power consumption of the tester since the source current can be described by

$$I_S = I_T \cdot \left(1 - L_T C \omega^2\right). \quad (6)$$

The inductance and capacitance of the transmitter are determined such that I_s is minimized. To provide a full swing clock signal in both scan and at-speed test modes, the coupled voltages in these two modes should be determined such that

$$V_{sink}(\omega_S) = V_{sink}(\omega_a), \quad (7)$$

where ω_s and ω_a denote, respectively, the scan and at-speed test frequencies. Since the magnitude of the received voltage is proportional to the signal frequency, to deliver a full swing clock for pre-bond test in different frequencies, the LC parameter of the transmitter must be adapted. The scan test clock frequency is lower than the clock frequency in normal operation. Consequently, a larger inductance is needed during scan test to deliver a full swing clock signal. To satisfy this constraint, an additional LC circuit is used to amplify the low frequency current coupled to the chip. This auxiliary circuit should be switched off during high frequency at-speed test mode. The schematic of the transmitter circuit is depicted in Fig. 4. By applying ω_a and ω_s in (4) to (6) and some algebraic manipulations, L_{T1}, C_1, L_{T2}, and C_2 are determined respectively, where $L_{T1} + L_{T2}$ and $C_1 + C_2$ denote the total inductance and capacitance of the transmitter during scan test. The scan-enable signal controls a transmission gate, which connects/disconnects the auxiliary LC circuit during scan/at-speed test modes.

The receiver circuit consists of the resonant inductor and a small voltage divider to produce the voltage offset. During the test mode, the inductive link can only transfer AC signals and the coupled voltage has no DC offset. To adapt the voltage level of the received signal to the CMOS logic level, a voltage divider is used to produce a 0.9 V DC voltage from a 1.8 V voltage source. This circuit is connected to the local clock network by a transmission gate, which is on during pre-bond test and is off in normal operation. During the normal operation, the clock signal delivered by the TSVs has an offset of $V_{dd}/2$. Consequently, in normal operation this divider can be disconnected. Note that this voltage divider is practically the sole overhead of the proposed method. The resistance of the voltage divider should be determined such that the leakage current of the divider is negligible as compared to the current drawn by the clock network. Increasing the resistance of the divider circuit decreases the power consumed by the voltage divider and alternatively, increases the area occupied by the circuit. The transmission gate employed to switch the voltage divider off during normal operation curtails the leakage current of the divider while negligibly increasing the area overhead of the test circuitry.

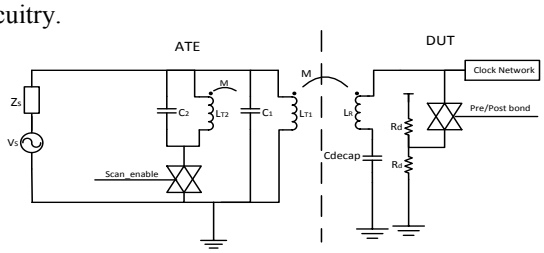

Figure 4. Schematic of the tranceiver circuit used for wireless pre-bond test.

Note that the different test techniques mentioned in this work are proposed to support synchronization during pre-bond test. Power/ground and the signals for testing are assumed to be provided by traditional means, such as I/O and power/ground pads at the periphery of each layer. In Figs. 1(b) and 1(c) the clock signal can be provided by a pin and be distributed through the redundant resources. In all existing approaches test pads can be added next to each clock network to individually provide the clock signal to each network. This approach requires several extra test pads (depending on the number of incomplete clock networks), used only for pre-bond test and have no use in post-bond operation consuming valuable routing resources. Alternatively, the proposed wireless approach can provide a fast test process with a negligible area overhead for resonant clock networks.

As compared to the methods described in [4] and [18] to ensure pre-bond test the usage of inductive links for pre-bond test includes the least area overhead. The power consumed in test mode is lower, since the power consumed by DLLs or the redundant wires is virtually eliminated for the wireless approach. These benefits are exemplified in the following section.

V. SIMULATION RESULTS

In this section, a resonant clock network for a two layer 3-D circuit is designed and simulated using Cadence Spectre. The transceiver circuit for the wireless test technique is designed and the power and area overheads of this new method are compared with the methods shown in Figs. 1(b) and 1(c).

A case study of a 3-D H-tree resonant clock network with 256 leaves is considered. The 3-D circuit is assumed to consist of two layers each containing 128 sink nodes. The load capacitance at each node is assumed to be 20 fF and the operating and test frequencies are 1 GHz and 400 MHz, respectively. The total area of the network is 3.4 mm × 3.4 mm.

The PTM interconnect model for a 0.18 μm CMOS technology is used to estimate the resistance, inductance, and capacitance of the horizontal interconnects. The amount of the resonant inductance is determined as described in Section IV-A. The decoupling capacitor that should be sufficiently large to not affect the frequency of resonance is set to C_{decap} = 60 pF. The number of LC tanks, the inductor size for each resonant circuit, and the clock driver resistance are listed in Table 1.

A path of the preferred network among the different variants is shown in Fig. 5(a) where the TSVs are placed on the fourth level of the network. In this structure, eight TSVs are used to connect the two layers and each layer contains eight LC tanks with a resonant inductance of 16 nH for each tank. The inductor size is 250 μm × 250 μm, which is a typical size for inductors employed for distributing the clock signal [22]. Re-

garding the area of the clock network and the number of *LC* tanks, the distance between resonant inductors is 900 μm which is sufficiently large to obviate interference between adjacent *LC* tanks. The power consumption of the clock network is reduced by 35% in comparison to a standard clock network, exhibiting the low power behavior of resonant clock networks.

Table 1. Design parameters and power consumption for different resonant 3-D clock network topologies.

	# *LC* tanks	*L* [nH]	R_{driver} [Ω]	Power [mW]	
				Standard	Resonant
1 TSV	8	8	6.2	137.5	110
2 TSVs	8	7.5	5.9	139	107
4 TSVs	16	17.5	6.1	147	103
8 TSVs	16	16	6.5	130	**85**
16 TSVs	32	31	5.8	136	98
32 TSVs	64	50	3.5	132	96

For the design of the off-chip transmitter in the wireless approach depicted in Fig. 5(c), a sinusoidal voltage source with an output impedance of 25 Ω is considered. For a distance of 20 μm between the adjacent layers a coupling coefficient of 0.25 can be achieved [22]. The transmitter inductance for the operating frequency L_{T1} and the corresponding capacitance C_1 are 17 nH and 6 pF, respectively. The auxiliary inductance L_{T2} and capacitance C_2 employed for the scan test frequency are 22.5 nH and 7 pF respectively. For the on-chip voltage divider, a resistor R_d of 100 KΩ is utilized to provide the offset voltage with an insignificant increase in power and area.

To evaluate the benefits of the wireless pre-bond test technique, a comparison is performed with the redundant wiring approach, shown in Fig. 5(b) and the DLL-based technique in [18]. The power and area overheads for the compared methods are listed in Table 3. For DLLs, the power and transistor count reported in [18] are considered where the circuit has also been designed in a 0.18 μm technology process. Eight DLLs are used to supply eight disconnected clock trees. For the redundant wiring method, the area and power of the additional wires method are considered, while for the wireless technique the area and power of the voltage divider and the transmission gates are considered.

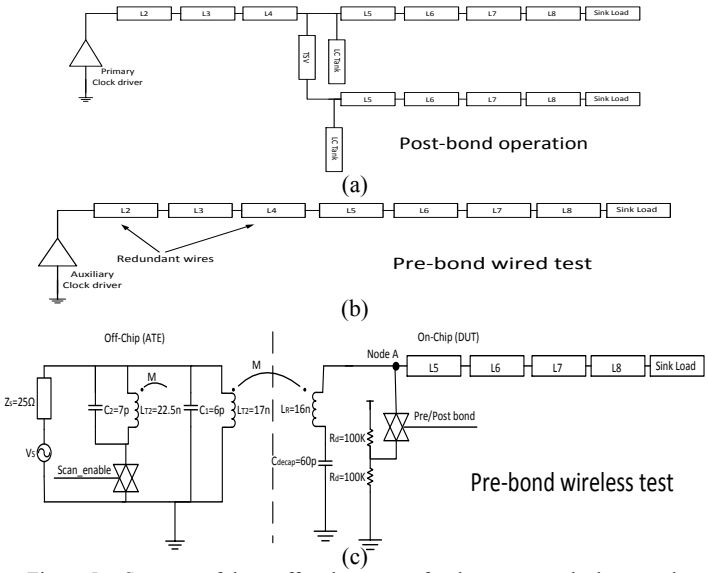

Figure 5. Segment of the preffered structure for the resonant clock network where (a) is the post-bonded network, (b) is the network in pre-bond test mode using redundant wiring, and (c) is the network using wireless pre-bond test.

The width of redundant wires and test clock drivers are determined as described in [19]. The redundant wire width is determined to be half the wire width in the first layer and the driver size is also reduced to 47% of the main clock driver. Since the voltage divider is much smaller than the DLLs and additional wires, a considerable reduction in the power and area overheads is achieved by the wireless approach.

As reported in Table 2, the proposed approach reduces the power consumption by 99% and 99.6% as compared to using redundant wiring and DLLs, respectively. The interconnect area is reduced by 98.5% in comparison to redundant wiring and the transistor count is reduced by 99.5% as compared to employing DLLs.

Table 2. Power and area overheads for different methods of pre-bond test.

	DLL [18]	Redundant wiring	Proposed method
Power (mW)	6.5	2.8	0.026
Interconnects area (μm^2)	~0	110200	1600
Transistor count	3664	20	16

As shown in Fig. 6, this circuit switches between the test and operating frequencies when the scan enable signal toggles without missing any clock cycle. Since in this system the scan-enable signal is used to switch the test frequency mode, the timing of the clock and scan-enable is proper for the *Launch-off-Capture* (LOC) test method where both launch and capturing are performed when scan-enable is zero.

The improvements offered by this method are scalability, ease of test, reducing the test power, reducing the silicon area, and improving reliability. The reliability is enhanced by preventing potential damages, which can occur during probing pads in wired test approaches. Alternatively, during normal operation, the use of resonant clocking offers significant power savings, demonstrating the advantages of this unified scheme. This approach is a proper way to support pre-bond synchronization for resonant clock networks. Applying this technique, however, for standard clock networks requires additional inductors that considerably increase the area overhead. This overhead may be reduced by advanced on-chip inductors, the area of which is comparable to the area of standard probes. Furthermore, for hierarchical clock networks with large number of sinks, using *LC* tanks for all levels of the networks is not a prudent practice. Clustering adjacent disconnected clock networks using (short) redundant wires and exploiting an *LC* tank for each cluster can be a compromise to reduce the area overhead, while maintaining the power benefits of the wireless approach during pre-bond test.

I. CONCUSIONS

A wireless synchronization method for the pre-bond test of resonant clock networks in 3-D circuits is proposed. This method intertwines the resonant networks and contactless inductive communication to produce low power and pre-bond testable clock distribution networks. The low power property originates from the phenomenon of energy resonance, while the minimal overhead pre-bond testability is assured by employing inductive links, where the receiver circuit is the induc tor of the on-chip *LC* tank. The number of *LC* tanks, the reso nant circuit parameters, and the driver size for normal operation relating to the clock network are determined such that a full swing signal is provided at the sink nodes and the power consumption of the circuit is lowered.

The transceiver circuit is designed to produce a full swing clock signal in both the test and operating frequencies. The proposed technique exhibits a negligible on-chip area overhead. A 256-sink H-tree clock network with operating and test frequencies of 1 GHz and 400 MHz, respectively, is considered as the case study. The area occupied by the additional circuits used for testing is reduced by 98.5% in comparison to the redundant wiring method, where in the same time the power consumed for pre-bond test is reduced by 99%. The power consumed by the proposed clock network during normal operation is reduced by 35% as compared to a standard clock distribution network indicating that interweaving resonant clock networks and wireless test can be highly beneficial for 3-D circuits.

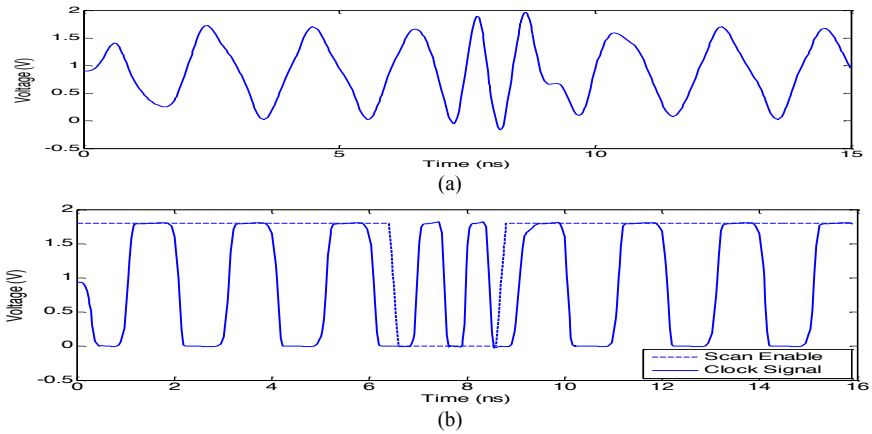

Figure 6. Clock signal at the receiver side of the inductive link where (a) is the clock signal received by the inductor at node A (see Fig. 5(c)) and (b) is the clock signal after the clock buffers at the sink nodes.

REFERENCES

[1] B. Noia and K. Chakrabarty, "Pre-bond Probing of TSVs in 3D Stacked ICs," *Proceedings of the IEEE International Test Conference,* pp.1-10, September 2011.

[2] J. Li and D. Xiang, "DfT Optimization for Pre-bond Testing of 3D-SICs Containing TSVs," *Proceedings of the IEEE International Conference on Computer Design*, pp. 474-479, October 2010.

[3] X. Zhao, D. L. Lewis, H. H. S. Lee, and S. K. Lim, "Low-Power Clock Tree Design for Pre-bond Testing of 3-D Stacked ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 30, No. 5, pp. 732-745, May 2011.

[4] X. Wu, P. Falkenstern, and Y. Xie, "Scan Chain Design for Three-dimentional Integrated Circuits (3D ICs)," *Proceedings of the International Conference on Computer Design*, pp. 208-214, October 2007.

[5] T. Y. Kim and T. Kim, "Clock Tree Synthesis with Pre-bond Testability for 3D Stacked IC Design," *Proceedings of the IEEE Design Automation Conference*, pp.723-728, June 2010.

[6] T. Xanthopoulos *et al.*, "The Design and Analysis of the Clock Distribution Network for a 1.2 GHz Alpha Microprocessor," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 402-403, February 2001.

[7] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Network for 3-D Integrated Circuits," *Proceedings of the IEEE International Custom Integrated Circuits Conference*, pp. 651-654, September 2008.

[8] S. C. Chan, K. L. Shepard, and P. J. Restle, "Design of Resonant Global Clock Distributions," *Proceedings of the IEEE International Conference on Computer Design*, pp. 248-253, October 2003.

[9] J. Rosenfeld and E. G. Friedman, "Design Methodology for Global Resonant H-tree Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 15, No. 2, pp. 135-148, February 2007.

[10] V. S. Sathe, J. C. Kao, and M. C. Papaefthymiou, "A 1 GHz FIR Filter with Distributed Resonant Clock Generator," *Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 44-45, June 2007.

[11] E. J. Marinissen *et al.*, "Contactless Testing: Possibility or Pipe-Dream?," *Proceedings of the Conference on Design, Automation, and Test in Europe,* pp. 676-681, April 2009.

[12] C. V. Sellathamby *et al*., "Non-contact Wafer Probe Using Wireless Probe Cards," *Proceedings of the IEEE International Test Conference*, pp. 1-6, November 2005.

[13] A. Radecki *et al.*, "6W/25mm^2 Inductive Power Transfer for Non-Contact Wafer-Level Testing," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 230-232, February 2011.

[14] N. Ahmed, M. Tehranipoor, C. P. Ravikumar, and K. Butler, "Local At-Speed Scan Enable Generation for Transition Fault Testing Using Low-Cost Testers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* Vol. 26, No. 5, pp. 896-906, May 2007.

[15] V. Vorisek, T. Koch, and H. Fischer, "At-Speed Testing of SOC ICs," *Proceedings of the Conference on Design, Automation, and Test in Europe*, Vol. 3, pp. 120-125, February 2004.

[16] B. Keller, A. Uzzaman, L. Bibo, and T. Snethen, "Using Programmable On-Product Clock Generation (OPCG) for Delay Test," *Proceedings of the Asian Test Symposium*, pp. 69-72, October 2007.

[17] X. Lin *et al.,* "High-Frequency, At-Speed Scan Testing," *IEEE Design & Test of Computers*, Vol. 20, No. 5, pp. 17- 25, September 2003.

[18] M. Buttrick and S. Kundu, "On Testing Pre-bond Dies with Incomplete Clock Networks in a 3D IC Using DLLs," *Proceedings of the Conference on Design, Automation, and Test in Europe*, pp. 14-18, March 2011.

[19] S. Rahimian, V. F. Pavlidis, and G. De Micheli, "Design of Resonant Clock Distribution Networks for 3-D Integrated Circuits," *Proceedings of the International Workshop on Power and Timing Modeling, Optimization, and Simulation*, pp. 267-277, September 2011.

[20] M. R. Guthaus, "Distributed *LC* Resonant Clock Tree Synthesis," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1215-1218, May 2011.

[21] S. E. Esmaeili, A. J. Al-Khalili, and G. E. R. Cowan, "Low-Swing Differential Conditional Capturing Flip-Flop for *LC* Resonant Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, in press, pp. 1-5, June 2011.

[22] J. Xu et al., "AC Coupled Interconnect for Dense 3-D ICs," IEEE Transactions on Nuclear Science, Vol. 51, No. 5, pp. 2156-2160, October 2004.