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Low-Power Clock Distribution Networks for 3-D ICs

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***Abstract*— Designing a low power clock network in synchronous circuits is an important task. This requirement is stricter for 3-D circuits due to the increased power densities. Resonant clock networks are considered efficient low-power alternatives to conventional clock distribution schemes. These networks utilize additional inductive circuits to reduce the power consumption while delivering a full swing clock signal to the sink nodes. Test is another complex task for 3-D ICs, where pre-bond test is a prerequisite. This paper, consequently, introduces a design methodology for resonant 3-D clock networks that lowers the power of the clock networks while supporting pre-bond test. Several 3-D clock network topologies are explored in a 0.18 µm CMOS technology. Simulation results indicate 43% reduction in the power consumed by the resonant 3-D clock network as compared to a conventional buffered clock network. By properly distributing the inductance within the layers of the 3-D stack, resonance is ensured both in pre-bond test and normal operation. The important aspects of this approach are introduced in this paper.**

Keywords- 3-D integration, clock distribution network, resonant clocking, wireless testing, inductive link

I. INTRODUCTION

A primary challenge in designing synchronous circuits is how to distribute the clock signal to the sequential parts of the circuit [1]. This issue can be more challenging for 3-D circuits since a clock path can spread across several planes with different physical and electrical characteristics [2].

As the area of the integrated circuits increases, larger networks are required to distribute the clock signal, which results in higher capacitive loads and resistive losses of the interconnects degrading the signal integrity along these interconnects. A common solution to alleviate this problem is to insert clock buffers in the intermediate nodes of the clock network. Although buffer insertion improves clock signal integrity, clock buffers significantly increase the power consumed by the network. 3-D integration drastically decreases the interconnect length of the global wires, which can reduce the number of clock buffers and result in more power-efficient clock networks. Alternatively, thermal issues are more pronounced in 3-D integrated circuits. Clock networks consume a great portion of the power dissipated in a circuit [3]. Consequently, designing low power clock networks for 3-D circuits is a primary challenge.

An efficient approach to eliminate the repeaters and reduce power is to use resonant clocking [4]-[6]. In this approach, on-chip inductance is added to the clock network and forms a resonant circuit with the interconnect capacitance, decreasing, in this way, the power consumed by the network, since the energy alternates between electric and magnetic fields instead of dissipating as heat.

Test is another important issue in 3-D circuits. Pre-bond test, includes testing each plane before bonding to other planes and can improve the yield of 3-D systems [7]. 3-D clock networks often include several disconnected networks in some of the planes, which connect with through-silicon-vias (TSVs) to the plane where the main tree feeds the clock signal to the entire clock distribution network. To provide pre-bond test, a complete clock tree is required within each plane. A technique to provide such a tree by employing additional wiring has recently been presented [8], where power is also a primary objective of this technique. In another approach each disconnected clock tree is driven by a DLL, enabling pre-bond test for each plane of the 3-D system [9].

The design of 3-D resonant clock networks and the related constraints have not been explored as compared to traditional planar clock networks [7]-[10]. To support the pre-bond test for a resonant clock network, resonant operation should be achieved for each unbonded layer during test irrespective of the employed pre-bond test approach. The resonant 3-D clock network should be designed so that resonant operation at a specific frequency is individually achieved for each layer during test as well as for the entire 3-D system during normal operation while maintaining the low power characteristics of the resonant networks.

This paper, consequently, proposed a design methodology of resonant clock networks for 3-D circuits that support pre-bond testing. The proposed 3-D resonant clock networks considerably lower the power of the clock distribution system, while pre-bond test is supported by the proper design and allocation of the *LC* tanks within each plane. Provisions are also taken so that the added interconnects resources to support pre-bond test only marginally increase the power and area budgets of the clock distribution network.

In this way, resonant operation is ensured for each plane either in test or functional mode and the clock signal characteristics are maintained within each plane and for either operating mode. Different designs of a resonant clock network for up to eight-plane 3-D circuits are investigated. Simulation results indicate that using a resonant clock network can significantly decrease the power consumption of the clock tree in 3-D circuits. Furthermore, the results confirm that the power consumed in a 3-D clock network is lower than a 2-D clock network due to the shorter interconnect length.

In the following section, the design of resonant clock networks for 2-D circuits is reviewed. A design methodology for 3-D resonant clock networks supporting pre-bond test is

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proposed in Section III. Simulation results are presented in Section IV. Some conclusions are drawn in the last section.

II. Resonant clocking

A seminal work, introducing the concept and design of resonant transmission lines has been published in [10]. A design of a global clock distribution network is presented in [4] in which four resonant circuits are connected to a conventional H-tree structure as illustrated in Fig. 1. Each quadrant consists of an on-chip spiral inductor that resonates with the wiring capacitance of the clock network and the decoupling capacitor is connected to the other end of the spiral inductor. A simple lumped circuit model is utilized to determine the resonant inductance. The resonant frequency of the network is (in first-order) estimated by $f = \frac{1}{2 \cdot \pi \cdot \sqrt{LC}}$ where C and L, respectively, denote the equivalent capacitance of the network wiring and inductance of the spiral inductors. The decoupling capacitor is employed to provide a positive voltage offset on the grounded end of the resonant inductor and adapt the voltage level to the CMOS logic level [11]. This capacitor should be sufficiently large to guarantee that the resonant frequency of the decoupling capacitor $f_{decap} = \frac{1}{2 \cdot \pi \cdot \sqrt{LC_{decap}}}$ is much lower than the desired resonant frequency of the clock network.

Based on this structure, a design methodology for resonant H-tree clock distribution networks is proposed in [5]. In this work, the clock tree is modeled with a distributed *RLC* interconnect as illustrated in Fig. 2. This electrical model is utilized to determine the parameters of the resonant circuit and the output impedance of the clock driver such that the power consumed by the network and the clock driver are minimum, while a full swing signal is delivered at the output nodes.

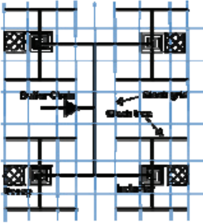


Fig. 1. Resonant clock network with four resonant circuits [8].

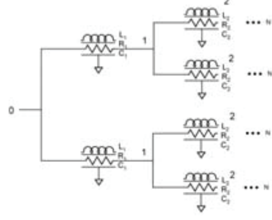


Fig. 2. Distributed *RLC* model of a 16-sink clock network

To deliver a full swing signal at the sink nodes, the magnitude of the transfer function of the network, H_{out}, should be close to one. This parameter is often fixed to 0.9 [5], [11] (for the remainder of the paper a "full swing signal" implies any signal swing that satisfies this specification). As shown in [5], when $|H_{out}|$ is fixed at 0.9, the driver resistance can be determined by

$$R_{driver} = \sqrt{\frac{|H_{\omega}(j\omega)|^2 \cdot |Z_{in_\omega}|^2}{0.9^2} - Img(Z_{in_\omega})^2} - Real(Z_{in_\omega}) \ , \qquad (1)$$

where H_{ω} and Z_{in_ω} notate the transfer function and input impedance of the network.

Several resonant circuits can be utilized to improve the characteristics of the clock signal. The number of *LC* tanks (resonant circuits) also depends on the location of these circuits. If the resonant circuits are placed closer to the driver, fewer circuits are needed and, alternatively, where these circuits are placed close to the sink nodes, more *LC* tanks are required. Since the equivalent inductance is the parallel combination of all the inductors as shown in Fig. 2, increasing the number of resonant circuits leads to a larger required inductance for each circuit. Using a higher number of larger inductors results in larger area occupied by the resonant inductors.

The number of resonant circuits affects the output signal swing and power consumed by the clock network. As discussed in [11], by increasing the number of resonant circuits and placing these circuits closer to the sink nodes, each inductor resonates with a smaller part of the circuit resulting in lower attenuation of the output signal swing and lower power consumption. Alternatively, increasing the number of resonant circuits and using larger inductors in each *LC* tank reduces the quality factor of the *LC* tanks, since in spiral inductors the effective series resistance (ESR) increases more aggressively than the inductance [5]. A lower quality factor for resonant circuits produces a higher signal loss and degrades the output signal swing. Increasing the equivalent resistance of the clock network due to increased resistance of resonant inductors also increases the power consumed by the network. The signal swing and power consumption for a clock network with 256 sinks using an ideal driver for different number of *LC* tanks is illustrated in Fig. 3. Since the change in signal swing and power consumption versus number of *LC* tanks is in different directions, there is an optimum number of *LC* tanks that can simultaneously increase the signal swing and reduce the power. Note that this increased signal swing results due to a decrease in the capacitance of the network, which in turn reduces power.

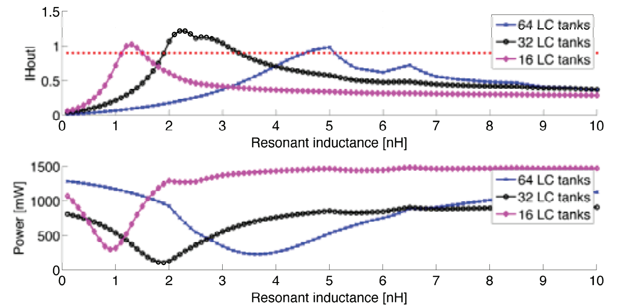


Fig. 3. $|H_{out}|$ and Power consumption for different number of *LC* tanks.

To determine the number of resonant circuits that maximize the output signal swing, one approach is to only consider the capacitance of the clock network and employ the first-order estimation to determine the total resonant inductance [11]. By doubling the number of *LC* tanks, the inductance of each tank is also doubled. In this approach, the inductive component of the network wires is not considered. In large clock networks with long interconnects, the inductance of the wires cannot be neglected [5]. Furthermore, this method assumes that placing the resonant circuit in different locations does not change the equivalent capacitance of the network (*i.e.,* the capacitance seen by the primary clock driver). These simplifications can

result in inaccurate estimation of the resonant inductance, adversely affecting the signal swing.

The signal swing for a clock network with 256 sinks using an ideal driver for different number of *LC* tanks is illustrated in Fig. 4. Employing any inductance within the crosshatched region, this clock network meets the signal swing specifications. The resonant inductance determined by the simplified approach is illustrated by the dotted lines, where due to imprecise estimation of the inductance, the clock network cannot deliver a full swing signal to the sinks (as required by the dashed horizontal line). As depicted in Fig. 4, using the simplified model from [11] can reduce $|H_{out}|$ from 0.9 to 0.65.

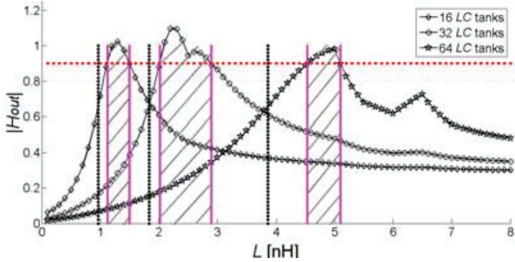


Fig. 4. $|H_{out}|$ for different number of *LC* tanks and resonant inductance using the model in [11] (dotted vertical lines) and the proposed approach (solid vertical lines).

In our approach, a distributed *RLC* model for the network wires is used to determine the required parameters for resonance. Different locations for the resonant circuits from the root to the sinks are investigated. For each location, the driver resistance is adapted to produce a transfer function magnitude of 0.9 for a wide range of inductor sizes using (1). The signal swing and corresponding power consumption are swept versus the inductance. The inductance for which power consumption is minimum is determined. This method is employed in the following section to design different case studies of 3-D resonant clock networks.

III. Resonant clocking for 3-D ICs

Different clock network topologies can be considered to adapt the conventional (planar) resonant clock networks to 3-D circuits [2]. In the first topology denoted as "symmetric topology", each plane contains resonant circuits and can be separately investigated. In another structure, denoted as "asymmetric topology", the resonant circuit is placed in only one plane and should resonate with the total capacitance of the 3-D stack at the desired frequency. During pre-bond test, each plane should separately resonate. Note that this requirement is an additional constraint specific to resonant networks and is completely different to the techniques that can be employed to connect the local networks [8], [9] in either a standard or resonant clock distribution approach. Consequently asymmetric structures, which can be considered as an extension of 2-D clock networks, do not support pre-bond test in a straightforward manner, since the resonant circuit is contained within only one plane.

The other important parameter in designing a resonant 3-D clock network is the number of TSVs used to connect the physical planes. From this perspective, different topologies can be explored, for example, using a single TSV in the center of each plane or by using multiple TSVs. In the multiple TSV structure, one of the planes contains a complete clock tree, where for the other planes the clock network consists of several disconnected local networks each connected to the first plane by TSVs. Increasing the number of TSVs provides more local networks increasing the area occupied by the TSVs. Four topologies for a two-plane 3-D circuit with 32 sinks are shown in Fig. 5.

RLC models to analyze the different 3-D structures are depicted in Fig. 6. In single-TSV topologies the equivalent resistance of the circuit is determined as the resistance of each plane divided by the number of planes (the wire resistances are essentially connected in parallel due to the symmetry of the topology, see Fig. 5a). By increasing the number of TSVs and omitting some wires in the upper planes, the symmetry is no longer preserved and the equivalent resistance cannot be considered as connected in parallel which results in higher equivalent resistance for the 3-D circuit. Alternatively, increasing the number of TSVs results in decreased capacitance for horizontal interconnects in 3-D circuit. Note that the capacitance per length of TSVs is higher than the horizontal interconnects and increasing the number of TSVs adds some capacitance to the clock network. The short length of the TSVs, however, makes the capacitance of the horizontal wires to dominate the network capacitance. Thus, increasing the number of TSVs, typically, decreases the total capacitance of the investigated topologies.

Increasing the number of TSVs can result in lower power due to the decreased capacitive load of the clock network. Alternatively, increasing the resistance of the circuit increases the power consumed by the clock network. Predicting which behavior is dominant is not straightforward and strongly depends on the interconnect characteristics of the clock network. Utilizing wide wires results in a stronger capacitive behavior, while using long wires increases the resistive component. For this case study, as shown in Table 1, there is not a uniform trend for the design parameters as a function of the number of TSVs.

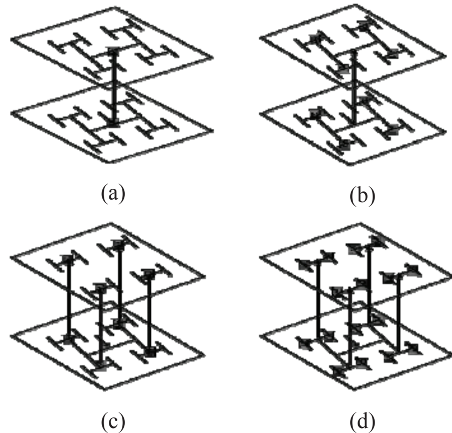
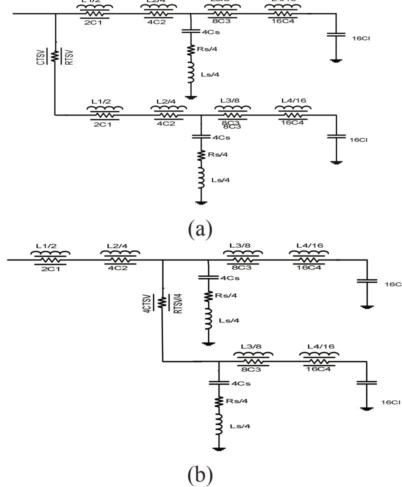


Fig. 5. Different topologies for a two-plane 3-D resonant clock network where (a) is a single TSV structure with one *LC* tank per plane, (b) is a single TSV structure with four *LC* tanks per plane, (c)

is a four TSV structure with four *LC* tanks per plane, and (d) is a four TSV structure with eight *LC* tanks per plane.



(a)

(b)

Fig. 6. *RLC* model for a two-plane 3-D circuit with four *LC* tanks where (a) is the model for the single-TSV and (b) is the model for four-TSV structures.

To specify the parameters of resonance for a 3-D system with a specific number of TSVs, a distributed *RLC* model of the clock distribution network is employed. The number of *LC* tanks in each plane is assumed to be more than the TSVs such that at least one *LC* tank is connected to each local network. The location of *LC* tanks is swept from the TSVs to the sinks. The driver resistance described by (1) is plotted over the inductance to determine the resonant parameters, similar to the 2-D case. In a 3-D system the transfer function for different planes can be different due to the effect of the TSV. Not surprisingly, the last plane (the plane with the greatest distance from the clock driver) has the lowest signal swing. The driver size should be determined such that the signal swing for every plane meets the specifications. Consequently, the transfer function magnitude of the last plane should be used in (1). Following this process, the number of the *LC* tanks and the parameters of the resonant circuits are determined for normal operation.

IV. SIMULATION RESULTS

Assuming an H-tree network as the preferred network in [5], the number of sinks is determined based on the circuit area A and the load capacitance that each sink drives, C_L. A case study of an H-tree resonant clock network with 256 leaves is considered. The load capacitance at each node is assumed to be 20 fF and the operating frequency is 5 GHz.

The PTM model for a 0.18 µm CMOS technology is used to determine the resistance, inductance, and capacitance of the horizontal interconnects. The total area of the network is 3.4 mm × 3.4 mm. For a conventional (non-resonant) clock network, inverters are properly inserted and sized at the intermediate nodes to deliver a full swing clock to the output, while in the resonant clock network, resonant circuits are added to the clock tree to provide a proper clock signal at the output. The amount of the resonant inductance is determined as described in the previous section. The decoupling capacitor that should be sufficiently large not to affect the frequency of resonance is set to 60 pF. The effective series resistance (ESR) for the inductors is determined from [5].

Different topologies of 3-D circuits are explored. To form a 3-D system, the 2-D circuit is folded into several planes. The number of *LC* tanks and the inductor size for each resonant circuit are listed in Table 1.

The power consumed by different topologies for standard and resonant clock networks is listed in columns 5 and 6 of Table 1. As reported in this table, the power consumed by the resonant clock network is considerably lower than the standard network in 3-D circuits. This improvement is accompanied by an increase in the area occupied by the resonant circuits. The area of a resonant clock network increases due to these additional circuits, but alternatively, omitting the clock buffers can decrease the area of the resonant networks.

Increasing the number of planes decreases the length of the wires in the network for a specific number of sinks. Omitting long interconnects as required for some of the topologies shown in Fig. 4 reduces the resistive voltage drop and the capacitance of the network and decreases the power consumed by the network. For a 3-D circuit with two planes, the power consumption reduces up to 64%, where this reduction reaches to 70% and 72% for circuits with four and eight planes, respectively. Decreasing the equivalent capacitance of the network also results in larger resonant inductance and increases the area of the resonant clock network.

Table 1. Design parameters and power consumption for different topologies for equal total number of sinks.

		# *LC* tanks	*L* [nH]	Power [mW]	
				Standard	Resonant
2-D	-	32	2.2	543	310
3-D 2 planes	1 TSV	16	1.5	385	241
	2TSV	16	1.4	374	230
	4 TSV	16	1.5	353	244
	8 TSV	16	1.3	312	**196**
	16 TSV	32	3	347	218
	32 TSV	64	5	304	203
3-D 4 planes	1 TSV	16	1.8	308	190
	2 TSV	16	1.6	297	174
	4 TSV	16	1.7	289	**162**
	8 TSV	32	3.2	295	176
	16 TSV	64	6.5	308	184
3-D 8 planes	1 TSV	8	1	299	173
	2 TSV	16	2	283	**152**
	4 TSV	32	3	311	188
	8 TSV	64	5	307	181

The preferred 3-D structure that decreases the power consumption of the clock network by 72%, consists of eight planes which is the maximum number of planes investigated in this case study. Each plane connects to the others using two TSVs. 16 *LC* tanks are used in this structure (two *LC* tanks per plane) and the inductance for each *LC* tank is 2 nH. The number of planes and the number of *LC* tanks is determined such that the highest voltage swing is achieved (which implies that the Q-factor of the spiral inductors is also the highest).

Another case study with 64 sinks in each plane is considered. The total area of each plane is 1.7 mm × 1.7 mm. Simulation results for different topologies are listed in Table. 2.

In this case study, the size of the clock network and, hence, the network capacitance increases as the number of planes increases. Since the resonant frequency is fixed at 5 GHz, increasing the overall network capacitance reduces the requirement for the resonant inductance. Again several topologies for any number of planes that utilize a different number of TSVs can be selected.

Each of these topologies require a specific number of TSVs and, typically, the larger the number of TSVs, the lower the overall wire capacitance within each plane. Consequently, using more TSVs improves power as reported in Table 2. Note, however, that the equivalent resistance of the network for the 3-D stack increases as the TSV number increases. Thus, for specific topologies and number or layers, further increasing the TSVs leads to an increase in power. This behavior is due to the increase in the equivalent resistance of the network that counteracts the beneficial decrease in the wire capacitance. For example, for the case of 4 planes, a topology with more than 8 TSVs results in higher power.

Table 2. Design parameters and power consumption for different topologies for equal number of sinks in each plane.

		# *LC* tanks	*L* [nH]	Power [mW]	
				Standard	Resonant
2-D	-	8	2	95	43
3-D 2 planes	1 TSV	8	1.3	201	102
	4 TSV	8	1.2	195	98
	8 TSV	8	1.3	192	93
	16 TSV	16	2.7	187	**89**
3-D 3 planes	1 TSV	12	0.9	243	128
	4 TSV	12	0.8	238	121
	8 TSV	12	1.7	227	113
	16 TSV	16	1.9	219	**107**
3-D 4 planes	1 TSV	16	1.8	308	190
	4 TSV	16	1.6	297	174
	8 TSV	16	1.7	289	**162**
	16 TSV	32	3.2	295	176
3-D 5 planes	1 TSV	20	1.2	352	187
	4 TSV	20	1.4	345	172
	8 TSV	20	1.2	334	**166**
	16 TSV	40	2.6	339	174

V. Conclusions

A design methodology for resonant clock networks in 3-D circuits is proposed in this paper. The number of *LC* tanks and the resonant circuit parameters are determined such that a full swing signal is provided at the sink nodes and the power consumption of the circuit is minimized. The effect of different parameters including the number of planes and number of TSVs among the planes for designing 3-D resonant clock networks is investigated. A 256-sink H-tree clock network operating at 5 GHz is considered as the case study where a power reduction of 72% is achieved for an eight-plane resonant clock network in comparison to a 2-D standard network.

Acknowledgments

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