Invited Paper

A CMOS-compatible silicon photonic platform for high-speed integrated opto-electronics

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ABSTRACT

We have developed a CMOS-compatible Silicon-on-Insulator photonic platform featuring active components such as p-i-n and photoconductive (MIM) Ge-on-Si detectors, p-i-n ring and Mach-Zehnder modulators, and traveling-wave modulators based on a p-n junction driven by an RF transmission line. We have characterized the yield and uniformity of the performance through automated cross-wafer testing, demonstrating that our process is reliable and scalable. The entire platform is capable of more than 40 GB/s data rate. Fabricated at the IME/A-STAR foundry in Singapore, it is available to the worldwide community through *OpSIS*, a successful multi-project wafer service based at the University of Delaware.

After exposing the design, fabrication and performance of the most advanced platform components, we present our newest results obtained after the first public run. These include low loss passives (Y-junctions: 0.28 dB; waveguide crossings: 0.18 dB and cross-talk -41±2 dB; non-uniform grating couplers: 3.2±0.2 dB). All these components were tested across full 8" wafers and exhibited remarkable uniformity. The active devices were improved from the previous design kit to exhibit 3dB bandwidths ranging from 30 GHz (modulators) to 58 GHz (detectors). We also present new packaging services available to *OpSIS* users: vertical fiber coupling and edge coupling.

Keywords: Silicon integrated photonics, modulator, photodetector, ring resonator, travelling-wave, Mach-Zehnder, Process Development Kit (PDK)

1. INTRODUCTION

The semiconductor industry has recently reached a level at which fundamental limits in the scaling down of transistors become a significant roadblock. One major issue is power dissipation in electrical connection driven at very high frequencies. The continuing of exponential scaling of computing capabilities will require the development of massively parallel architectures, for which optical interconnects are widely recognized as an enabling technology. At a higher level, the demand for increased communication bandwidth in large data centers has grown through the past decades, driven by the rise of the Internet and the entry in the age of "big data". Unfortunately, the high cost of discrete optical components used in standard communication links, and their assembly into functioning systems, are important challenges to continued bandwidth scaling. Moreover, for on-chip interconnects, seamless integration next to the central processing units is a prerequisite to high-speed operation.

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One proposed solution for the two above challenges that has attracted remarkable attention in recent years, from both industry and academia, is to build integrated photonic circuits on a silicon platform. Leveraging the investments made in complementary metal-oxide-semiconductor (CMOS) fabrication, it is possible to build low-cost, high-complexity systems in silicon that achieve close integration between electronics and photonics. Recent efforts have shown that such platforms can achieve impressive performance with the promise of very low costs and high yield. *Luxtera* has developed a 25 Gb/s platform, the first one that is fully integrated with CMOS electronics.[1] Kim et al. have demonstrated both modulators and detectors working at speeds of 30 Gb/s.[2] Just recently, IMEC announced the upcoming launch of a fully integrated 25 Gb/s platform via the ePIXfab MPW.[3]

In this paper, we present the performance of the OpSIS-IME silicon photonics platform. This platform features a host of optimized passive elements such as low-loss grating couplers and waveguides, as well as high-speed active elements including 58 GHz gain-peaked Ge photodetectors, 45 GHz, high-tunability silicon ring modulators and 30 GHz traveling wave Mach-Zehnder modulators. The high bandwidth of the modulators and photodetectors enable the platform to support a data rate of 50 Gb/s per channel and potentially higher. The platform is available to the research community and to private developers as part of the *OpSIS*-IME multi-project-wafer (MPW) foundry service, in which a reticle is split between users as shown schematically in Fig. 1.

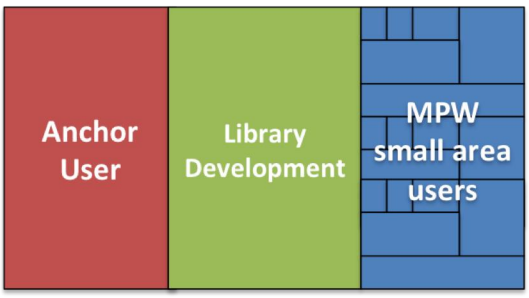


Fig. 1: Concept of Multi-Project-Wafer (MPW) service. Anchor users are typically companies buying large areas over several runs for long-term projects

2. FABRICATION

The silicon photonic circuits were fabricated at the Institute of Microelectronics (IME), a research institute of the Agency for Science, Technology and Research (A*STAR).[4] Silicon-on-Insulator (SOI) wafers from Soitec, 8 inches in diameter, with a 220 nm device layer and a 2um buried oxide (BOX) layer were used as a substrate. Three anisotropic etch steps were employed to define silicon heights of 0, 90 nm, 160 nm and 220 nm, which were used to build the grating couplers, rib waveguides and ridge waveguides. Six separate ion implantation steps (p++, p+, p, n++, n+, n) allowed for the design of the modulators and an additional p-type implant in germanium was used to define the anode of the Ge photodetectors. The implants were followed by a rapid thermal anneal (RTA) of 1030 °C for 5 seconds to activate the dopants. Epitaxial germanium-on-silicon was then selectively grown in regions defined by an SiO_2 mask layer up to a height of 500 nm, with a thin buffer layer to avoid excessive dislocations. Ion implantation in the Germanium was followed by annealing at 500 °C for 5 minutes. Finally, contact vias and two levels of Aluminum interconnects were fabricated. A schematic platform cross-section is show in Fig. 2.

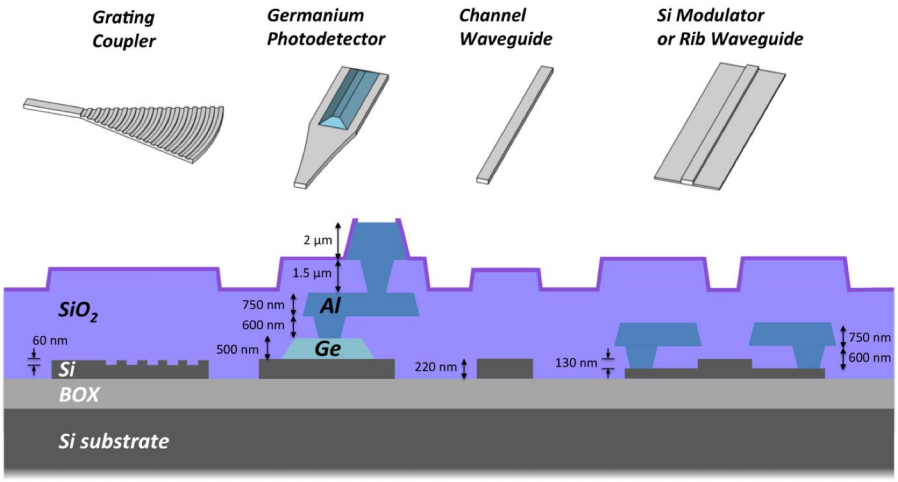
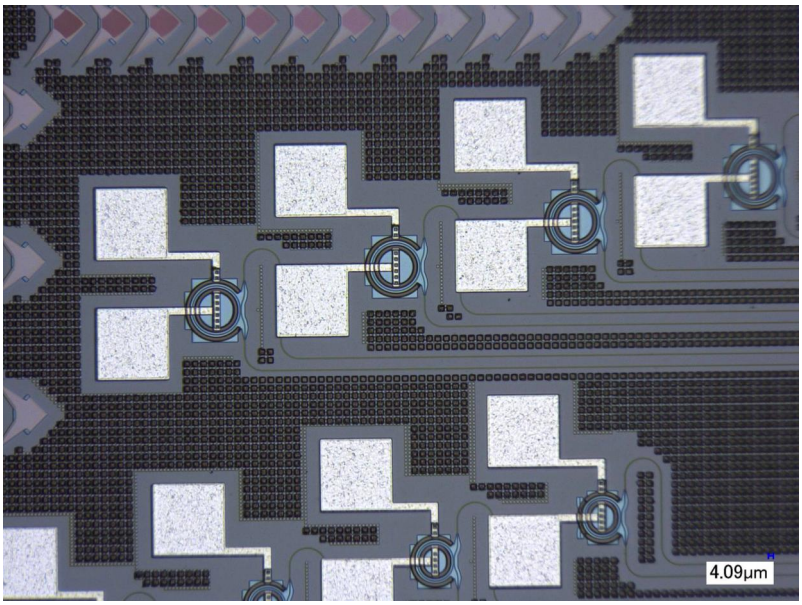


Fig. 2: Schematics of the layers cross-section and the key components of the platform.

3. PHOTONIC DEVICE LIBRARY

The *OpSIS*-IME device library features a large variety of passive and active devices, of which we select a few to present here. All these devices are building blocks available to *OpSIS* users for their own system design. Extensive wafer-scale testing has been conducted to characterize their performances (see Video 1). Due to the requirements of testing at high speeds, some measurements were done on a smaller set of devices. The average and standard deviation measurements that follow are from cross-wafer testing.



Video 1: Overview of one of many test dies used to characterize active and passive library elements using a wafer-scale setup: http://dx.doi.org/doi.10.1117/12.2017053.1

3.1 Passive Devices

High performance passive components are essential for building large-scale photonic systems. Grating couplers are used extensively on our platform to couple light on and off chip, in particular because they enable efficient wafer-scale testing. The library grating coupler uses a single, shallow silicon etch of 60 nm (leaving a 160 nm thick silicon layer). We fabricated and tested non-uniform gratings to better match the diffracted profile with single mode optical fibers. We achieve a cross-wafer average insertion loss of 3.1 dB at 1550 nm with a 1.5 dB bandwidth of 50 nm.
Low-loss waveguides were also demonstrated on our platform. The standard routing waveguide consisting of a 1.2 μm wide rectangular channel was measured to have an average propagation loss of 0.27±0.06 dB/cm. Rib waveguides with 0.5 μm width and 90 nm slab thickness had an average loss of 1.5±0.6 dB/cm.

3.2 Photodetector

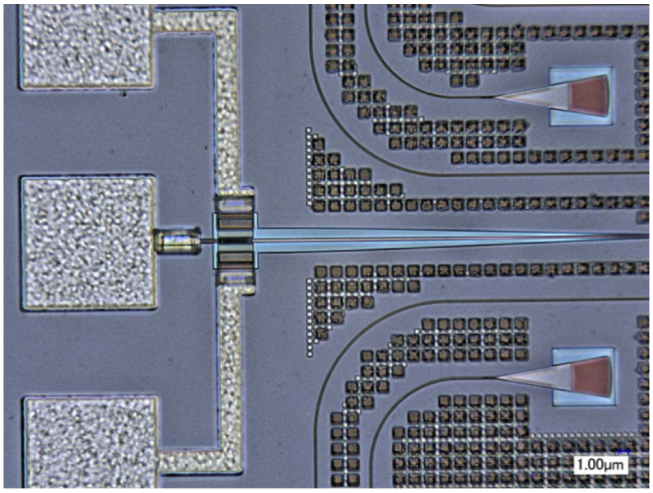


Fig. 3: Micrograph of a basic Germanium photodetector without inductor for gain-peaking (500x, real colors)

The platform photodetectors were built using evanescently coupled, Germanium, p-i-n diodes with a 11 μm long section of germanium grown on top of a silicon waveguide (black rectangle in Fig. 3). Cross-wafer testing yielded an average responsivity of 0.74±0.13 A/W and a dark current of 4.0±0.9 μA at 2 V reverse bias. Inductive gain peaking based on a spiral metal inductor placed in series with the diode (see Fig. 4a) was successfully implemented to enhance the detector bandwidth.[5] The RF performance of the detector was characterized using a Vector Network Analyzer (VNA) driving a high-speed Lithium Niobate modulator and detecting the electrical response from the photodetector. The frequency response of the modulator was calibrated using an ultrafast (70 GHz) commercial photodetector (u2t) and was normalized out of the platform photodetector measurement. The resultant 3dB bandwidth was measured to be 58 GHz, as shown in Fig. 4b.

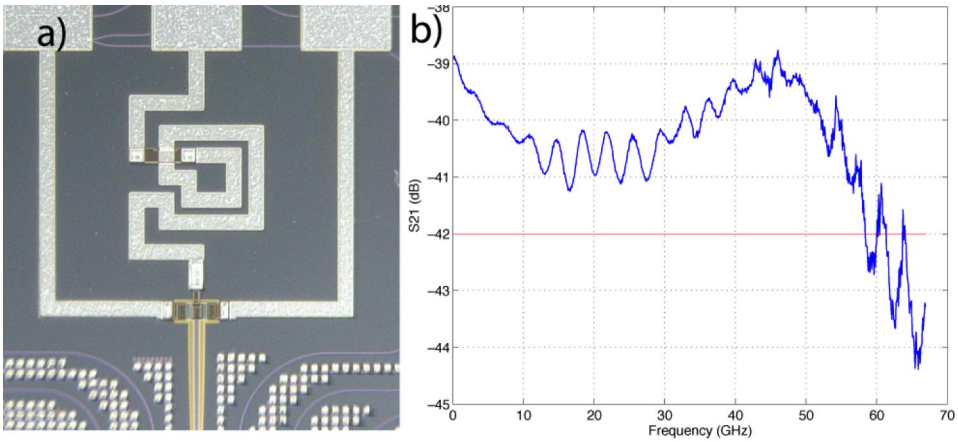


Fig. 4: a) Image of gain-peaked photodetector. b) EO response of photodetector showing 58 GHz bandwidth.

3.3 Traveling Wave Modulator

Traveling wave Mach-Zehnder modulators were built with 3 mm active length, lateral PN junction phase shifters and metal GS transmission line electrodes of 33Ω impedance.[6] Use of intermediate p+ and n+ doping reduced the parasitic resistance of the slab. The net insertion loss of the device, excluding routing and coupling, was measured to be 7 dB. The arms of the modulator are intentionally unbalanced by 100 μm to provide a convenient method of setting the bias point. By applying a DC bias voltage and measuring the spectrum shift, the small signal Vπ was found to be 7V around 0V bias. The bandwidth of each arm was measured individually by driving the arm with the VNA and terminating with a 25Ω resistor (Fig 5c). The 3dB bandwidths of both arms were measured to be over 30 GHz with less than 1V bias. The eye diagram at 40GB/s with 0.25V bias and 2.5 Vpp driving voltage is shown in Fig. 5b. Under these conditions 5.1dB extinction ratio was achieved with excess loss (due to modulator biasing) of 1.7dB. Note that the drive voltage listed above is measured at the output of a 50Ω instrument; actual voltages on the device are slightly lower (voltage intake is 67% for a 25Ω termination at low frequencies).

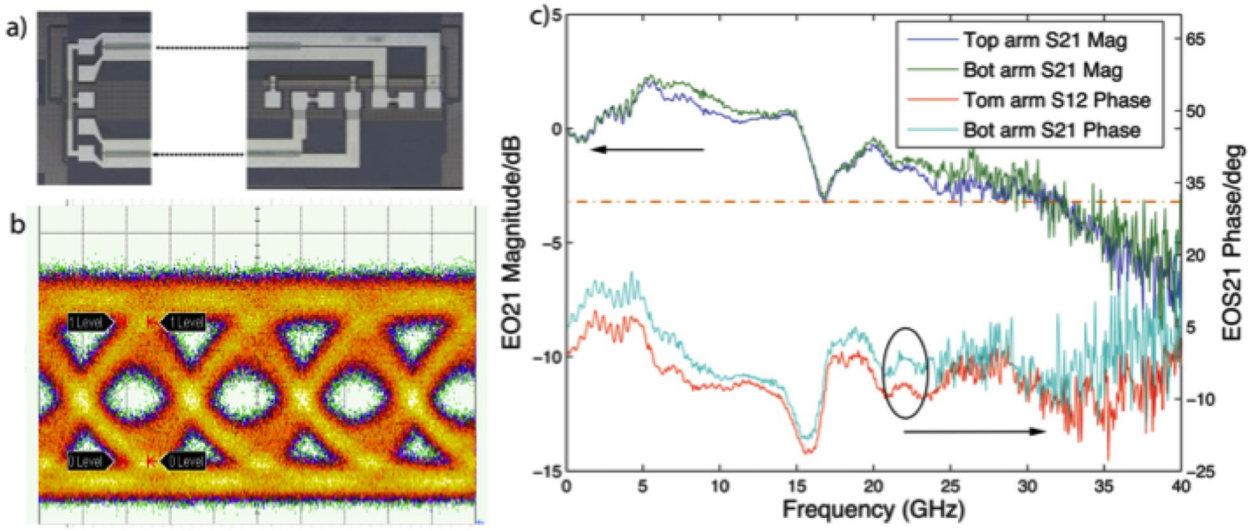


Fig. 5: a) Image of 3mm traveling wave modulator. b) Eye-diagrams at 40Gb/s under differential-drive with 0.25V bias and 2.5Vpp drive voltage. c) RF performance at 1V bias. The amplitude shows a 3 dB bandwidth of 30 GHz.

3.4 Ring Modulator

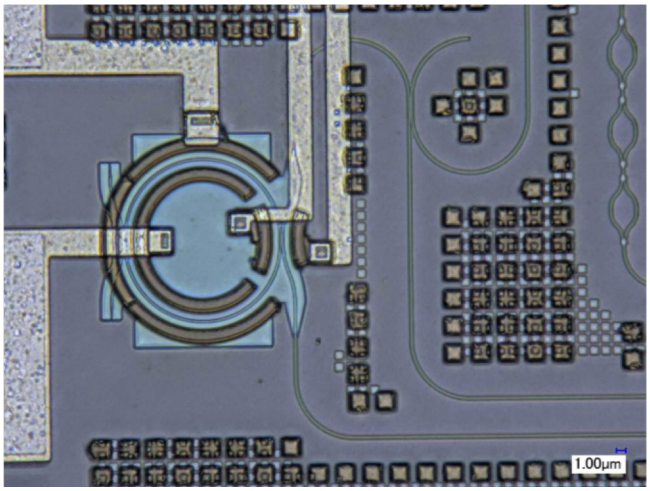


Fig. 6: Micrograph of a ring modulator (500x, real colors)

Ring modulators with a 12 µm radius were built using 0.5 µm wide rib waveguides and a 90 nm slab thickness (see Fig. 6). A heavily doped p-n junction was used to increase the tuning efficiency. Typical loaded quality factor of 2,800 and free spectral range of 7.65 nm were observed. The small signal tunability was measured to be 28 pm/V by analyzing the spectrum shift as a function of bias voltage (Fig. 7a). The 3 dB bandwidth was measured by a VNA to be 45 GHz at 0V bias (Fig. 7b), enabling a 50 Gb/s data rate. It is estimated that these rings will achieve 5dB extinction ratio when driven by a 2.4Vpp signal and when the '1' bit is biased to have 7dB modulation loss.

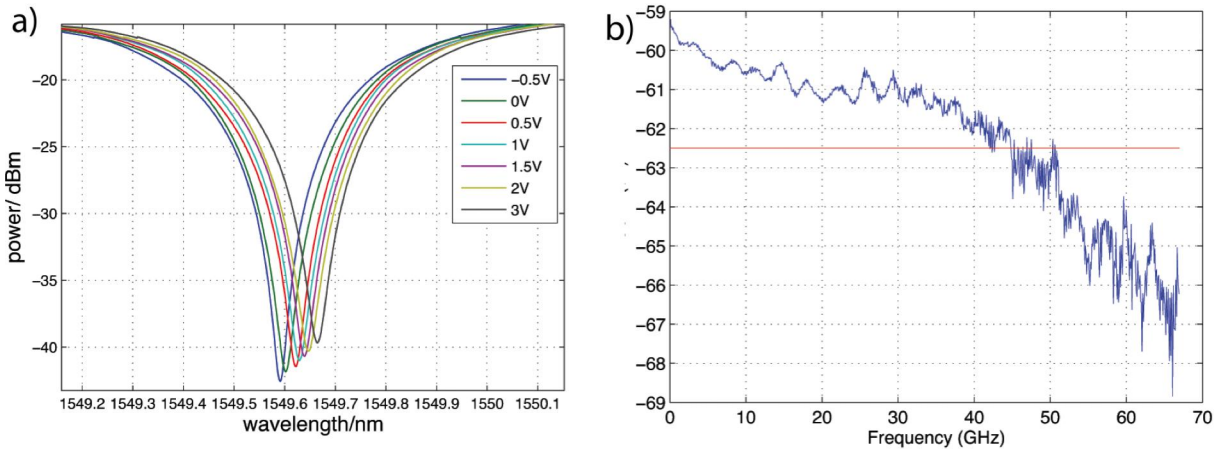


Fig. 7: a) Ring resonance shift at different bias voltages. b) EO response at 0 V bias showing a 3 dB bandwidth of 45 GHz.

CONCLUSIONS

We show in table 1 a summary of the improved performances in active devices and passive components from version 1 to version 2 of the PDK.

Table 1: Summary of the improvements in performances of key passive and active devices following the release of version 2 of the PDK in January 2013. IL: insertion loss; PD: photodetector; MZ: Mach-Zehnder; WG: waveguide.

	OpSIS-IME PDK V2	Opsis-IME PDK V1
Modulators And Detectors		
Inductive Peaking Ge PD	**0.7 A/W, 58 GHz**	0.54A/W, 20GHz
Ring Modulator	**28 pm/V, 45 GHz**	11pm/V, 19GHz
Traveling Wave MZ	**7V Vπ, 30 GHz**	7V Vπ, 15.8GHz
Passive Components		
New Y-junction	**0.3 dB IL**	1.3 dB IL
WG Crossing	**0.18 dB IL**	
Nonuniform Grating Coupler	**3.1 dB IL**	3.7dB IL
1.2um Wide Channel WG	**0.4 dB/cm**	
500nm Rib WG	**2.0 dB/cm**	2.4dB/cm

To conclude, we present another significant development in the scope of services offered by *OpSIS* to its users in the form of optical packaging of silicon chips coupled to polarization-maintaining (PM) optical fibers. Working with two different partner companies, we offer two types of coupling: vertical incidence through grating couplers (with PLC Connections, MA), or edge-coupling into waveguide tapers (with Chiral Photonics). Figure 8 shows a picture of the packaged chip using PM fiber with tapered spot-size-converters on each side to achieve a $1/e^2$ mode field diameter of about 2 μm, with insertion loss of 2dB per facet and polarization extinction ratio > 20 dB. The package has been tested at cryogenic temperature with unchanged performance, as well as after dropping it on the floor, demonstrating good robustness for a wide range of applications and environments.

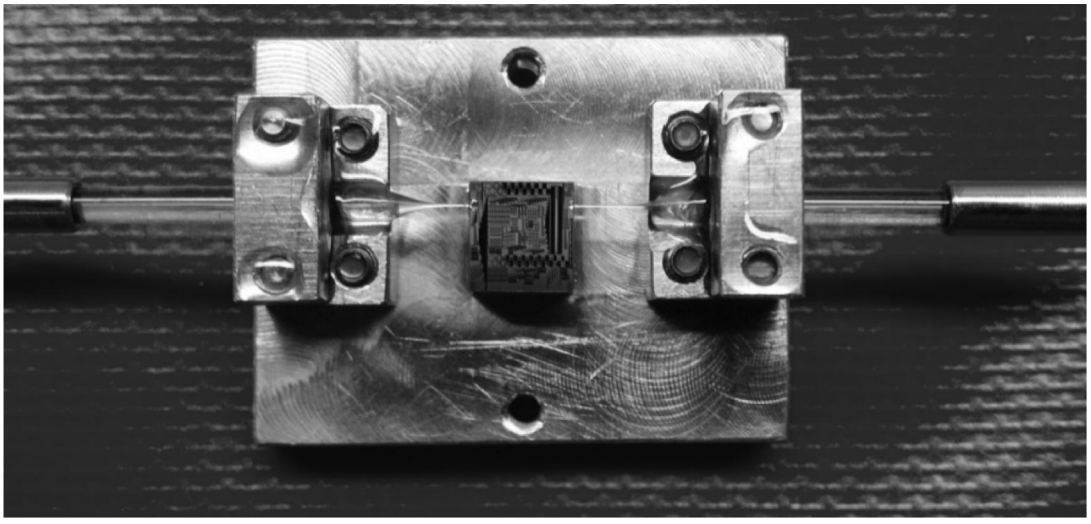


Fig. 8: Photograph of a silicon chip in its optical package to polarization-maintaining fibers. Edge coupling to tapered silicon waveguide is achieved with a spot-size-converters in the fibers.

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