Integration of Intra Chip Stack Fluidic Cooling using Thin-Layer Solder Bonding

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***Abstract*— Three-dimensional (3D) stacking of integrated-circuit (IC) dies by vertical integration increases system density and package functionality. The vertical integration of IC dies by area-array Through-Silicon-Vias (TSVs) reduces the length of global interconnects and accordingly the signal delay time. On the other hand, the ongoing miniaturization trend of ICs results in constantly increasing chip-level power densities. Thus, the development of new chip cooling concepts is of utmost importance. Therefore, scalable cooling solutions for chip stacks, such as interlayer cooling, need to be investigated. This paper presents a new concept for the integration of intra chip stack fluidic cooling, namely die-embedded microchannels for single- and two-phase thermal management, using a patterned thin-layer eutectic solder bonding technique for the stack assembly. Results showed the successful fabrication of 5-layer chip stacks with embedded microchannels and high aspect ratio TSVs. Optical inspections demonstrated the proper bond line formation and direct current (DC) daisy-chain electrical tests indicated the successful combination of TSVs with thin-layer solder interconnects. Mechanical shear tests on die-on-die bonded samples showed the strength of the patterned thin-layer solder bond (16MPa). An added solder ring-pad component to seal the electrically active pad from any conductive liquid coolant was also investigated and reflow tests on such geometries showed the appearance of a balling effect along the solder ring line. This balling was found to be mitigated when the ring aspect ratio (deposited solder height to ring width ratio) was kept below the experimentally observed critical value of 0.65.**

Keywords—3D stacking, thin-layer solder bonding, TSV, interlayer chip cooling, solder sealing ring.

I. INTRODUCTION

In the semiconductor industry, integrated-circuit (IC) feature sizes have been gradually reduced to integrate more transistors per area. This trend, as predicted by Moore's Law [1], is a result of shrinking transistor dimensions, with the benefit of reducing switching time and decreasing operating voltages. However, the signal propagation on electrical wires suffers from dimensional scaling and starts dominating the IC performance.

Three-dimensional (3D) stacking of integrated-circuit dies presents itself as an interesting alternative. It increases system density and package functionality by vertically integrating two or more chips. The vertical integration of IC chips using Through-Silicon-Vias (TSVs) reduces the length of global interconnects and accordingly the signal delay time, while also improving bandwidth between dies. Furthermore, the proximity of dies improves their communication energy efficiency and hence reduces overall power dissipation.

Efficient heat dissipation in IC packages is crucial to support the packing density and performance scaling of future systems [2, 3]. The ongoing miniaturization trend of ICs results in constantly increasing chip-level power densities. The demand for higher computational performance results in microchips with an increasing amount of cores and cache memory. These cores communicate via long wires which consume a lot of energy and generate a considerable amount of heat. The International Technology Roadmap for Semiconductors (ITRS) projects that the power density of a single chip package will increase to 108 W/cm^2 for cost performance applications in 2018 [4], from the current power density of 60–80 W/cm^2. Thus, heat removal has become an ever increasing challenge, and the development of new chip cooling concepts is of utmost importance. Indeed, the reliability, performance, and power dissipation of interconnects and transistors are heavily dependent on their operating temperature. Therefore, backside microchannel fluidic cooling concepts, be it single-phase water or two-phase dielectric evaporative cooling using environmentally-friendly refrigerants, were introduced into high-end server products [5-8].

Single cavity backside heat removal of micro-electronics and power electronics devices using dielectric evaporative fluids (refrigerants) was demonstrated to be an effective and controllable process. However, applying these concepts to the backside of 3D stacks instead of single chips will only be of temporary efficiency, as a major limitation of vertically integrated packages is that heat fluxes and thermal interface resistances accumulate with each layer. Therefore, scalable cooling solutions, such as interlayer cooling, need to be investigated. Several studies have already focused on the fabrication and assembly of such new systems. Dang et al. [9] showed the feasibility of a silicon chip with an embedded microchannel heat sink and novel thermofluidic chip input/output (I/O) interconnects, fabricated using wafer-level and CMOS compatible batch processing, with its extension to a 3D chip stack using Through-Silicon-Vias (TSVs) for electrical vertical integration. King et al. [10] reported for the first time the confi-

guration, fabrication, and experimental testing of a 3D integrated system that can support the power delivery, signaling, and heat removal requirements for high performance chips. However focus was directed on fabrication as well as assembly and no thermal measurements were performed nor presented.

The present paper chooses to focus on a new concept for the integration of intra chip stack fluidic cooling, namely die-embedded microchannels for two-phase evaporative thermal management, with high aspect ratio TSVs placed inside the silicon fins for maximum throughput. This concept relies on a patterned thin-layer eutectic solder bonding technique for the stack assembly, in contrast to the currently used solder balls, which mainly results from the need to avoid the addition of a fabrication step to close the die-embedded microchannels while minimizing the gap between two given dies within the stack, in order to limit cross-talk between the microchannels of an individual die. The compatibility and performance of this bonding technique are assessed here by the fabrication and electro-mechanical testing of 5-layer chip stacks that include the aforementioned cooling concept. Finally a new ring-pad design is fabricated and demonstrated, compatible with the thin-layer solder technique, to seal the inner pad from the liquid with the ring structure, should the cooling medium be water.

II. Intra-chip Stack Thermal Management: Concept, Design and Fabrication

Fig. 1a and 1b show a concept for an intra-chip stack thermal management system, developed for the CMOS Advanced Interlayer Cooling consortium (CMOSAIC), whose principal aim is to build a first-of-its-kind package and investigate heat transfer effects in such systems using water as well as refrigerant cooling. The purpose of this particular test vehicle is to demonstrate the feasability of intra chip stack fluidic cooling via two-phase evaporative heat transfer in the multiple evaporators (*E1* to *E4* on Fig. 1). Fluid delivery into the stack is done through a cover manifold (not shown on Fig. 1) for which details are given in [11]. The package consists of a chip stack attached to a larger silicon interposer. Five 380µm-thick 10x10mm^2 silicon chips (LV1 to 5, see Fig. 1a and 1b) are flip-chip bonded using thin-layer eutectic solder bonding as interconnects to form the chip stack, as shown on Fig. 1a. Individual dies were processed on both sides, at wafer-level, with embedded microchannels on their backside for integrated cooling. The fabrication process is described in the following sub-sections, according to Fig. 2.

Step A: TSVs and Metallization

Step A shows the TSV implementation as well as the front side metallization, which can either be the daisy-chain wires (for electrical measurements through the stack) or wires acting as resistive heaters mimicking the power map of a microprocessor in future heat transfer tests.

380µm tall TSVs were integrated into a double-side polished silicon wafer with equal thickness, to allow the implementation of microchannels with a fin height of 100µm. A rather aggressive aspect ratio (diameter to height) of 1:7 was targeted for the TSVs, setting the TSV diameter to 60µm. The complete fabrication process of the copper TSVs is discussed in [12] and is shown on Fig. 3a: (1) lithography, (2) silicon etching, (3) wafer cleaning, (4) dielectric coating, (5) seed layer deposition, (6) two-step TSV electroplating, and (7) Chemical Mechanical Planarization (CMP). As discussed in [12], the silicon etching was performed using the Deep Reactive Ion Etching (DRIE) technique to ensure a high etching rate. The notching artifacts at the bottom of the TSVs result from surface charging of the dielectric etch stop and need to be considered in the mask design. Therefore, the TSV diameter on the mask required an offset of 15µm to ensure the desired diameter of 60µm. Finally, the dielectric layer in the TSV was obtained by wet oxidation of the silicon.

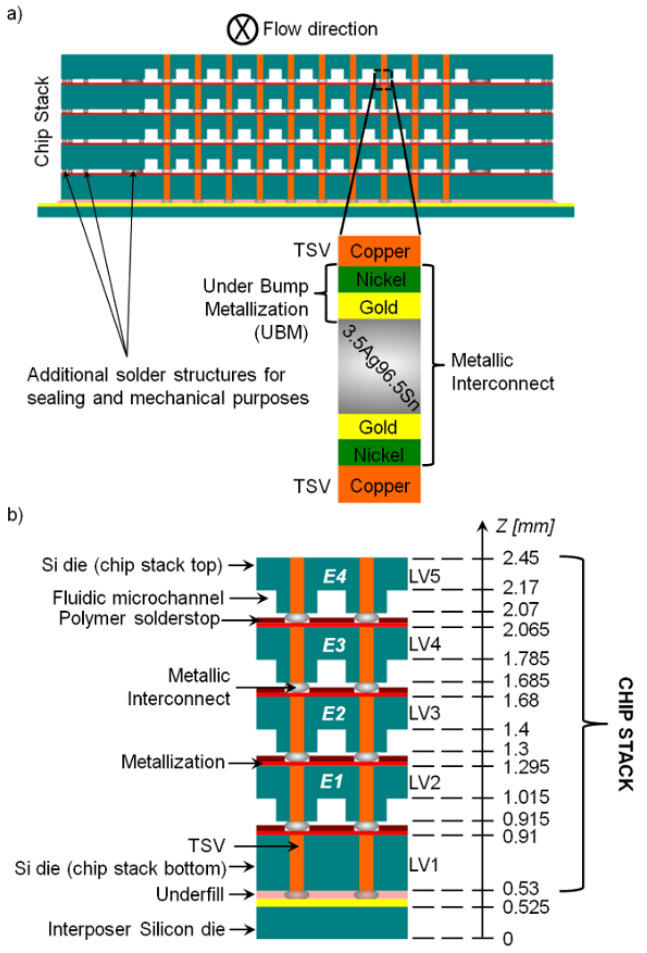

Fig. 1. Test vehicle description–chip stack package with silicon embedded heat transfer structures. a) Ensemble view of package with all components. b) Vertical cross-section describing the multiple layers and their respective thicknesses.

The electroplating step was also fine-tuned for this specific design. Before electroplating, the following preparation steps were performed: (1) low power oxygen (O_2) plasma for 1 minute, (2) deionized (DI) water rinse for 30 seconds, (3) 4% sulfuric acid (H_2SO_4) dip for 40 seconds, (4) bath conditioning for 90 seconds, and (5) copper electroplating at 10mA/cm^2 for 30 seconds. The above sequence was used for both electroplating steps (see Fig. 3b) and their roles were to increase the wettability of the surface, clean the copper oxide

from the seed layer and reduce the amount of contaminants, give sufficient time for the bath species to diffuse through the whole TSV length and finally increase the thickness of the seed layer, thus reducing its resistivity and closing any residual small voids.

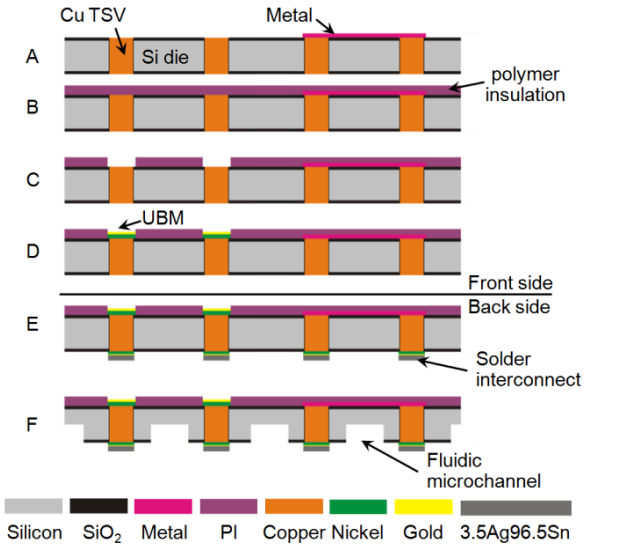

Fig. 2. Process integration flow for the fabrication of a middle die within the chip stack (LV2 to LV4, see Fig. 1b), after TSV implementation.

The electroplating setup was also refined from its original state by adding a diffuser and optimizing the position of the showerhead, thus allowing increased uniformity and coplanarity acroos the electroplated wafer. With the above measures taken the occurrence of bump void defects (BVD) was limited to areas with lithographic/etching defects, due to the higher mass transfer on these locations.

Furthermore, the CMP process was revamped using an in-house slurry that offered increased removal rate. During CMP the temperature was kept below 25°C and the backside pressure was regulated for both faces of the wafer, to ensure homogenous removal on the latter's surface. The backside pressure was regulated at different values, due to the large wafer bowl increase induced by the high stress of the thick copper overburden. Moreover, an additional annealing plus CMP steps might be necessary to induce and mitigate copper pumping.

To validate that the TSVs are fully filled and electrically conductive, daisy chain measurements were performed and optical cross sections were examined. Based on the daisy chain measurements the resistance per TSV could be extrapolated, as shown on Fig. 4. Most of the TSVs were found to have a lower than 2[Ω] resistance, with an averaged value of 0.7[Ω] for all measured samples. The cross section of the fabricated TSV is presented on the left side of Fig. 3b and shows no major defects.

Finally, the front-side metal layer was sputter-deposited (750nm for copper daisy-chain lines, 250nm aluminum for heaters) directly on top and around the open vias (for LV1 to 4), some of these connecting the pads for the daisy-chain lines or the heaters at each level.

Steps B, C, D

Steps B and C show the spin coating, curing and patterning via a Reactive Ion Etching (RIE) process of a 2µm-thick polymer solderstop layer made of polyimide, preventing electrical shorting after solder reflow on the previously deposited metal lines. Peak temperature reached during curing was 300°C.

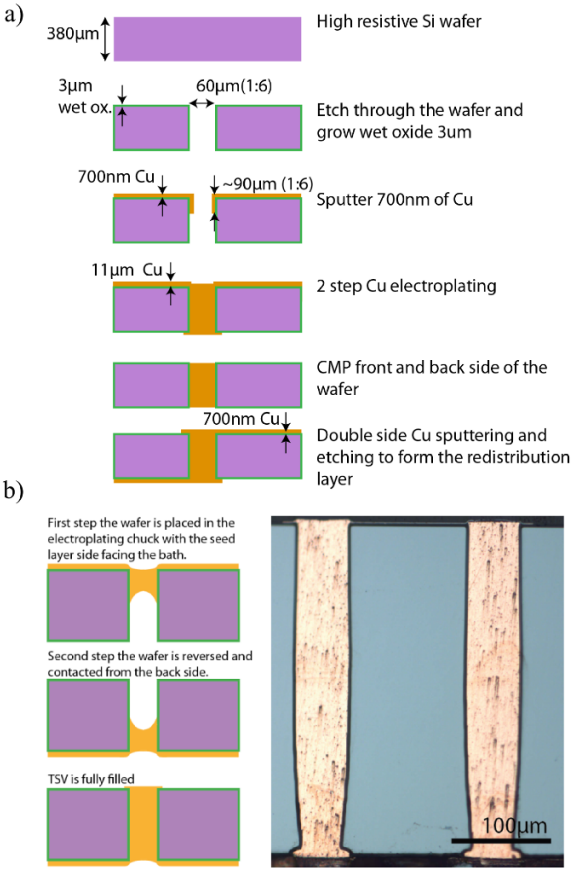

Fig. 3. a) Illustration of the TSV process flow. b) Illustration of the two-step TSV electroplating process with a cross-section of the reults.

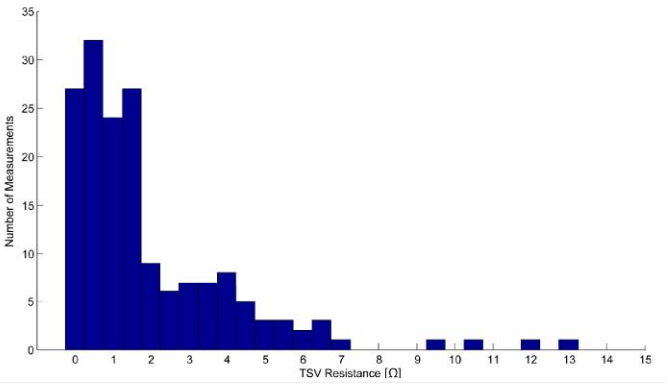

Fig. 4. Histogram of the calculated TSV resistance. Most of the TSVs have a value below 2Ω.

In step D the Under Bump Metallization (UBM, 1µm nickel plus 500nm gold) was sequentially deposited on the

same wafer side via sputtering on top of the still open vias (for LV1 to 4), thus forming carrier pads and allowing the flip-chip bonding of the superior chips. The UBM shape is equivalent to the one on the solder side (see Step E).

Step E: Thin-Layer Solder Interconnects

On the back side of the wafer, solder interconnects with their respective UBM pads were electroplated (58µm in diameter, 2µm-thick nickel, 1µm gold, 12µm eutectic silver tin) for the bonding to the inferior chip (for LV1 to 5). Eutectic 3.5Ag96.5Sn was chosen as lead-free solder. The choice of the eutectic phase was driven by its low-melting temperature (221°C) as well as its thermodynamic and mechanical stability. Initially, a 150 nm-thick copper seed layer was sputter-deposited on top of the silicon dioxide. The electro-deposition of the nickel gold UBM and the eutectic AgSn (bath SOLDERON BP TS 4000) was performed sequentially through a positive photoresist (AZ4662, AZ Electronic Materials) with a 15 µm thickness. Finally, the photoresist was stripped and the seed layer removed by wet chemical etching. Additional thin solder structures for fluidic sealing and mechanical purposes [11] were deposited during the same step.

Step F: Microchannels

Step F shows the formation of the multiple evaporator layers where flow boiling heat transfer will occur within the chip stack (*E1* to *4* on Figure 1b). Fifty 100x100µm microchannels were patterned etched on the backside of each chip (for LV2 to 5) via a two-step DRIE process, with the patterning done trough lithography on a thick postive photoresist (AZ Electronic Materials).

III. ASSEMBLY

A. Solder Reflow

Prior to flip-chip bonding, the fabricated dies (LV1 to LV5, Fig. 1b) were reflowed on a hot plate at a temperature of 265°C, using hot water-soluble flux. Subsequently, the samples were cleaned in water, to remove any flux residue and enhance scanning electron microscope (SEM) inspection quality (see Fig. 5a) before flip-chip bonding. Fig. 5b shows a Focused Ion Beam (FIB) cut through a reflowed solder pad, where no major defects could be detected inside the solder bulk.

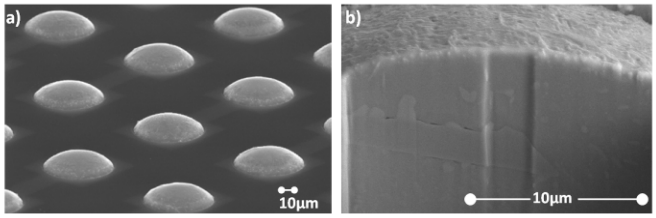

Fig. 5. a) Flux-reflowed solder pads, 58µm in diameter and 12µm thick. b) FIB cross-section of a reflowed solder bump.

B. Flip-Chip Bonding

The chip stack was formed via sequential flip-chip bonding of its multiple dies (LV1 to LV5, Fig. 1b). The bonding of a chip's solder backside to its corresponding inferior carrier front side was performed by a force-controlled reflow process utilizing a flip-chip bonder (SET FC150).

Initially, the solder on the chip backside was wetted with flux by a stamping process. The chip was then aligned with respect to the pads of the carrier on the inferior chip's front side (planar plus parallelism alignment). After touchdown between chip solder and carrier, the joining by force-controlled reflow is performed according to the force and temperature profiles presented in Fig. 6. The force profile is imposed through the upper arm of the flip-chip bonder. The temperature profile is applied to both arm and bottom chuck, meaning to the chip and carrier. The process starts by ramp heating between ambient conditions and 150°C in 2 minutes (1.15°C/ sec), at which temperature the flux is activated. After a 15 seconds step, linear heating is resumed until 265°C in 100 seconds. The 12.6 [N] (0.6g/ pad) force was applied while the sample was at 150°C, still below the liquidus point of the solder. Once at 265°C, a 30 seconds dwell time was applied. The process resumes by cooling down both chip and carrier to room temperature.

Finally, this same bonding method was also used to manufacture die-on-die samples for electrical and mechanical tests (see below).

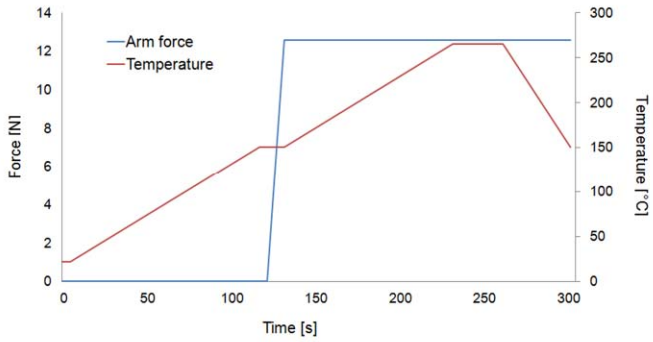

Fig. 6. Flip chip bonding (force-controlled reflow) process used for die-to-die bonding and chip stacking. In blue: force control. In red: temperature control for both chip and carrier side.

SEM photographs on Fig. 7 and Fig. 8 show the successfully assembled chip stack, with the die-embedded microchannels and the formed thin solder bond line between the TSVs. The concave shape of the solder joint seen on Fig. 7d insures that the solder was not squished during bonding, which can be a concern at such thin solder depositions. Cross-sectional SEM pictures (Fig. 8) depict constant thicknesses of the formed solder joints and the proper alignement of TSVs within the chip stack.

C. Electrical Measurements

Madhour et al. [11] calculated the resistance of the same thin-layer AgSn solder bond to be between 1 and 5 [mΩ] via direct current (DC) daisy-chain measurements that spun from 6 to 94 active pads between two solder bonded silicon dies (without TSVs). The same daisy-chain structure was used here to measure the combination of TSVs and thin solder pads, by preparing die-on-die solder bonded samples assembled via the

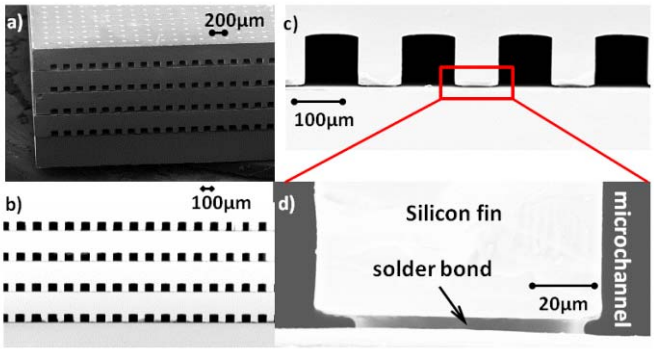

Fig. 7. a) Isometric view of a 5-layer chip stack (4 fluid cavities, 4 active layers with TSVs). b) Front view of 100X100µm fluidic microchannels. c) Zoom-in on cavities, fin thickness is 100µm. d) View of the die-to-die thin-layer eutectic solder bond (5µm), the silicon fin as well as the fluidic microchannel.

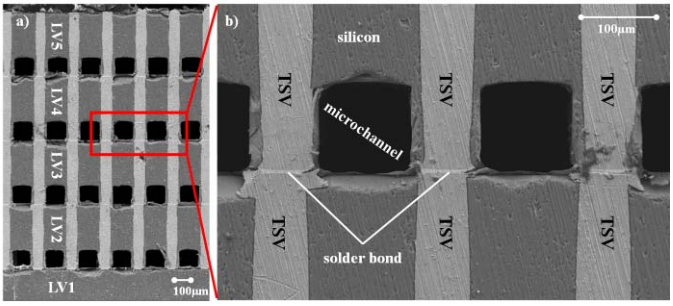

Fig. 8. a) Cross-section of the assembled chip stack. The LV1 to LV5 chips, the microchannels, the TSVs as well as the thin-layer solder bonds are all visible. b) Zoom-in on microchannels, TSVs and solder pads.

process previously described (bottom die = carrier = 10x10mm^2, top die = chip = 9.5x10mm^2). The top die was an LV2 chip (Fig. 1b) and the bottom die was a simple silicon 525µm-thick carrier. 4-point Kelvin resistive measurements on a manual probe station showed that an electrical connection was made after bonding and that the linear increase in the number of active pads from line to line was matched by the linear increase in line resistance.

Fig. 9a shows the schematic of the 4-point measurement used to determine the resistance of a single TSV plus solder pad combination. Fig. 9b shows the results of said measurement, showing that the resistance varies between 0.6 and 1.8 [Ω], which is within the uncertainty of the TSV resistance values (Fig. 4).

D. Mechanical Shear Tests

To evaluate the mechanical integrity of the stack, the previously described electrically measured die-on-die samples underwent mechanical testing. The bonding method of thin film solder joints limits the choice of structural testing to post-bond testing. Thus, die shear testing was carried out with a dedicated test setup. Because the applied critical load scales with the number of bonds per die, the shear setup ideally measures the load reaction in-line with the loading movement. For this purpose we used a SELmaxi load frame (Thelkin AG, dual column tension and compression tester) [13] and mounted the samples vertically in-line with the load axis, as Fig. 10 demonstrates.

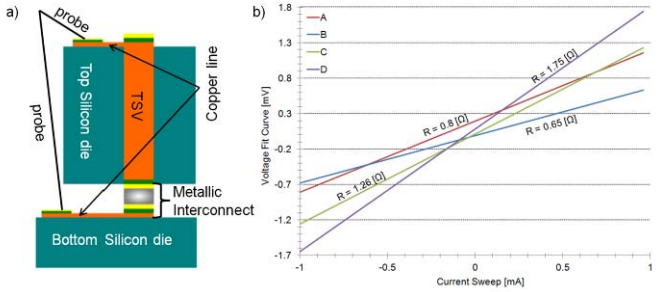

Fig. 9. a) Schematic of the 4-point DC Kelvin measurement for a single TSV plus thin-layer solder pad combination. b) DC current sweep (-1 [A] to 1 [A]) with corresponding voltage response to determine the resistance of a single TSV plus thin-layer solder pad combination. A and B as well as C and D designate simlar daisy-chain locations measured on different samples and are representative values.

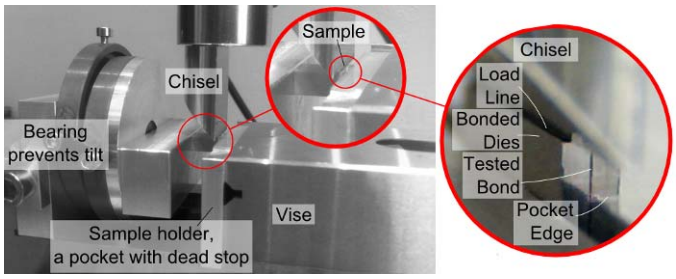

Fig. 10. Setup to shear test the thin-layer solder bonds.

One of the two dies rests in a pocket that forms a dead stop against the load axis. The other die is only constrained in the out of plane translation and rotation (x and rotation around y) using a dedicated bearing and sample holder fixed in a vise. Fig. 11 shows the load chisel that applies the shear load on the entire width of the die by displacing the same die vertically relative to the bonded die in the pocket. The chisel clamping allows a rotational alignment around the z-axis for an optimal load line.

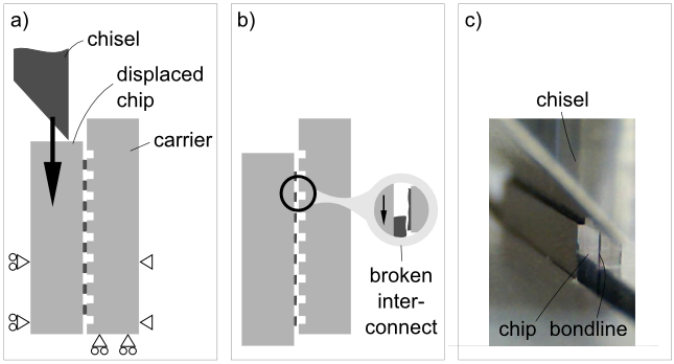

Fig. 11. a) Shear principle. b) Sheared state. c) Corresponding photo.

To monitor the sample reaction a displacement controlled shear speed of 10µm/second was chosen, which is a factor of 10 below standard JEDEC [14] low speed ball shear testing of 100 to 800µm/sec. Each shear test stopped prior to half bond pitch displacement. This avoided collisions of neighboring

bonds for clear post-shear imaging. Two different aspects of this mechanical loading were of interest: the load reaction giving the bond's shear strength, and the way the bond separates, the failure mode. Fig. 12 shows the load reactions, and the resulting shear strength values. Table I summarizes the results.

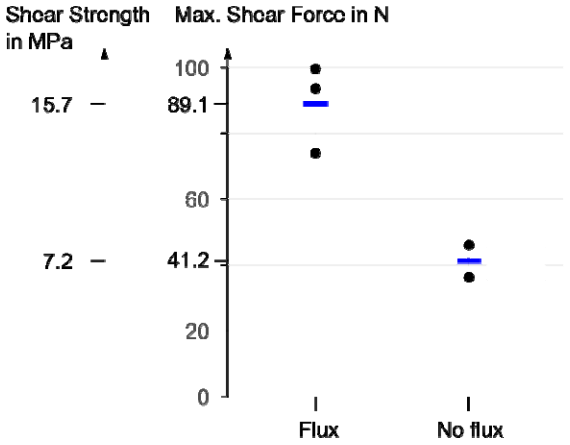

Fig. 12. Shear test results.

TABLE I. SHEAR TEST RESULTS

Bond type	Die-on-die solder bond shear tests – averaged values		
	Critical Force [N]	*Area [mm²]*	*Total Stress [MPa]*
Flux	89.1	5.7	15.7
No Flux	41.2	5.7	7.2

Although other experiments have shown that the onset of shear failure can occur before the maximum load reaction [15], usually the maximum force reading serves the shear strength calculation. The crucial detail is to which sheared area the force relates to. The calculation was based on the full pad diameter of 58µm of all 2156 sheared bonds per die and used the average obtained maximum force value. The strength of the flux-assisted bonds is more than twofold higher (16MPa) than the bonds formed without flux (7MPa). While assuming that all bonds break at the very same displacement generally overpredicts the shear strength, the assumption of the full pad area to be sheared at once underpredicts the shear strength value. Fig. 13 shows the typical failure modes observed.

All bonds separated either within the solder bulk material, or partly at the pad-to-solder interface (Fig. 14). None of the bonds showed any lifted pads, or cracks kinking into the substrate. Also channels and TSVs remained intact.

IV. FLUIDIC SEALING

A. Design and Fabrication

The use of water as a coolant requires additional sealing methods, to protect the electrical interconnects from shorting through the water. A ring-pad design (Fig. 15a) is proposed,

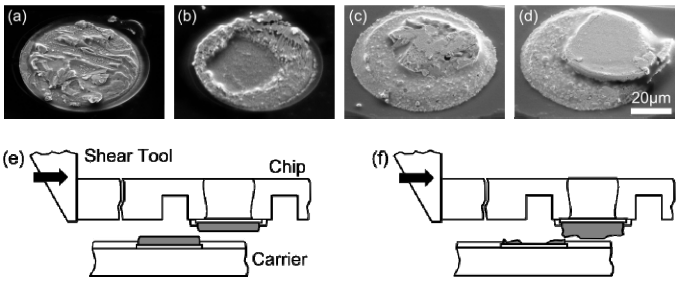

Fig. 13. Failure modes observed across the sheared carrier and chip (left to right). a) Ductile through solder (carrier side). b) Partial solder lift (carrier side). c) Ductile through solder (chip side). d) Partial solder lift (chip side). All pad diameters are equal to 58µm. The schematics (e) and (f) describe the failure mode principle for each, ductile and partial solder lift.

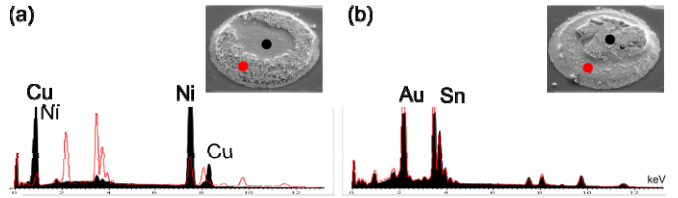

Fig. 14. EDX results of the different regions left behind after shearing: the partial solder lift (a) shows a clean separation between the solder components and the pad UBM metallization.

compatible with the presented thin-layer solder technique, to seal the inner solder pad (covering the TSV) from the liquid coolant with an additional solder ring structure. Fig. 15b shows the range of values experimented with for the two main ring geometry parameters, namely the gap between the central active pad and the ring as well as the ring width.

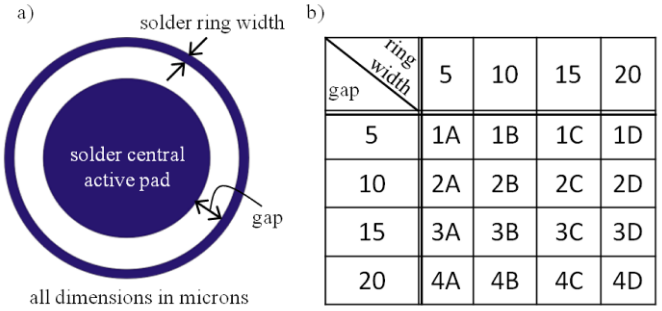

Fig. 15. Solder fluidic sealing concept. a) Design and geometry. b) Range of studied combinations of parameters and their different designations.

Since the ring-pads are novel structures, before the actual fluidic sealing tests their fabrication and reflowability must be assessed. The fabrication process for the sealing rings is the same as the one presented in §2, step E. Because of the difference in dimensions between the rings themselves and their corresponding central pads, different solder heights were deposited since local current densities differed during electroplating, which in turn resulted in discrepancies in solder quality (same for the Ni plus Au UBM). It was generally observed that less solder was deposited on the rings than on the central pads.

B. *Reflow Tests*

After fabrication (Fig. 16a), 10x10mm^2 chips containing homogeneous arrays of different ring-pad structures (from 1A to 4D, Fig. 15b) were reflowed on a hot plate at a temperature of 265°C, using hot water-soluble flux, and then cleaned to improve SEM inspection quality. Fig. 16b shows the SEM pictures for geometries 3A to 3D after reflow. These representative SEM photographs show that after the reflow, dome-shaped rings and rings with local solder accumulation, called balling, were observed for wide (3B to 3D) and narrow (3A) widths respectively.

Due to their very small gap between the ring and the central pad, structures 1A to 1D all shorted after reflow. The compiled reflow results are presented on Fig. 17 for geometries 2A to 2D and 3A to 3D since their dimensions correspond best to the silicon fins embedded in the chip stack. The aspect ratio of the initial plated ring solder height H_0 to the ring width W_r is plotted against the initial solder height H_0. Squares and circles indicate respectively dome-shaped rings and rings with balling. From these results, a close to constant critical aspect ratio of approximately 0.65 can be extracted, similar to the one established for thicker solder structures in [16], thus adding to the range of experimented deposited solder heights. Structures 4A to 4D behaved similarly. Brunschwiler et al. [16] showed that for long solder rails an invariant critical aspect ratio for different rail widths could be explained theoretically without the influence of gravitational forces (Bond numbers below one). In that case the minimal energy state was equivalent to the geometry with the minimal

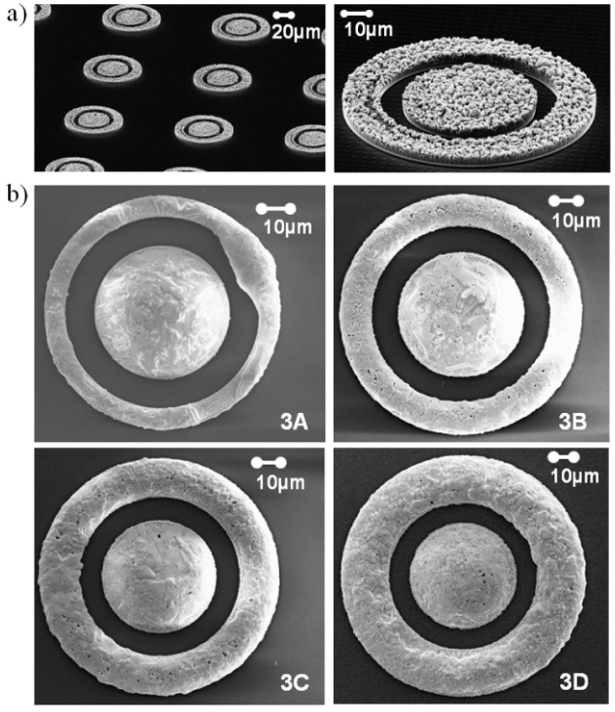

Fig. 16. a) Solder ring pads after electroplating. b) Ring pad structures 3A to 3D after reflow on hot plate and cleaning.

surface area and hence that geometry was independent of size, and only depended on the aspect ratio of the solder rail cross-section. Since it can be extrapolated that the ring-pad structures are basically curved rails, the same reasoning can be applied here.

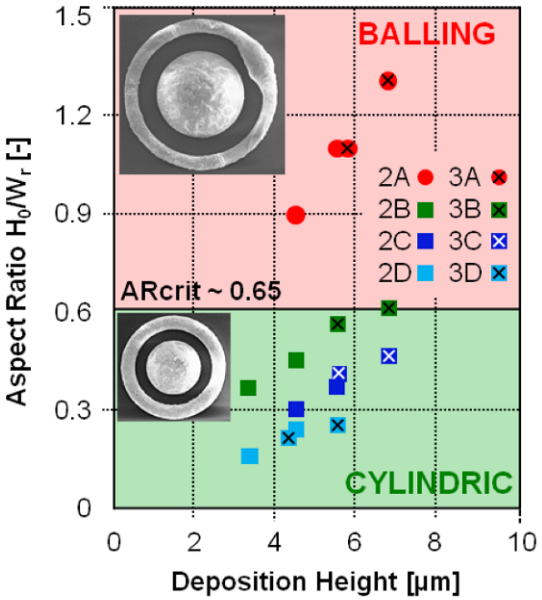

Fig. 17. Experimental categorization of ring pad solder shapes after reflow for varying deposition heights H_0 and ring aspect ratios (deposition height H_0 to ring width W_r). Dome- (squares) and ball- (circles) like shapes were identified below and above the critical aspect ratio of 0.65. Inserts depict SEM photographs.

V. CONCLUSIONS

A new concept for a high performance chip stack with integrated cooling, high TSV aspect ratio and thin-layer patterned solder bonding was introduced. The design, fabrication and integration of the different elements were discussed, and the assembly via sequential solder flip-chip bonding of the multiple dies was presented.

SEM photographs of a 5-layer chip stack and its corresponding cross-sections after assembly via flip-chip bonding showed the proper formation of the thin solder bond line (shape) between the multiple dies and its repeatable thickness (5µm ±1µm). Daisy-chain measurements on die-on-die samples showed successful electrical conductivity after solder bonding and allowed the resistance determination of a single TSV combined with a thin-layer solder pad. Results varied between 0.6 and 1.8 [Ω], which is within the uncertainty of the individual TSV resistance values (between 0.7 and 2[Ω]).

Shear tests were performed on die-on-die bonded samples to determine the stack's mechanical integrity. It was observed that the strength of the flux-assisted solder bonds was more than twofold higher (16MPa) than the bonds formed without flux (7MPa). Additionally, failure modes were identified. All bonds separated either within the solder bulk material, or partly at the pad-to-solder interface. None of the bonds showed any lifted pads, or cracks within the substrate. Also, channels and TSVs remained intact after the destructive tests.

Finally a new ring-pad design was presented, compatible with the patterned thin-layer solder technique, to seal the electrically active pad covering the TSV from the liquid coolant with a solder ring structure, should the cooling medium be water. A parametric reflow study on such solder geometries showed the appearance of a balling effect along the ring line and it seemed that the narrow solder ring pads demonstrated that effect the most, compared to the wider ones which yield in uniform dome-shapes. This balling can be mitigated when the ring aspect ratio (deposited solder height to ring width ratio) is kept below the experimentally observed critical value of 0.65.

VI. OUTLOOK

To advance the full integration of electrical, structural and liquid functions in 3D stacks all functions need to be demonstrated. Leak tests could determine the proper functionality of the proposed sealing method, for instance by direct-current (DC) electrical measurements between the central active pad and the sealing ring in presence of water.

Since the fluid entering the stack exerts a certain pressure, fluidic tests should evaluate whether the demand on the die-to-die solder joints increases. A 2-layer single bond line device could show the maximum sustainable fluid pressure supported by the thin solder joint and compare it to the bond's tensile yield strength.

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