A 3D architecture platform dedicated to high-speed computation for power system

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***Abstract*—This paper presents an innovative 3D hardware architecture for power system dynamic and transient stability. Based on an intrinsic parallel architecture by means of mixed-signal circuits (analog and digital) it overcomes the speed of numerical simulators for given models. This approach does not competing the accuracy and model complexity of the high performance numerical simulators. It intends to complement them with the advantage of speed, low-cost, portability and autonomous functions. The presented architecture provides an ultra-high speed platform by means of emulation principle. The proof of concept is an array of 4x24 nodes reconfigurable platform. Hardware details and comparisons with a reference digital simulator are given.**

***Index Terms*— Emulation, mixed analog digital integrated circuits, application specific integrated circuit (ASIC), power system simulation, power system stability, power system dynamics.**

I. INTRODUCTION

Power systems face many new challenges that it was not designed for. For example, it will support a bidirectional power flow at low and medium voltage levels of the power grid. The renewable electricity generation is also less predictable than that of the conventional method; it pushes therefore to a more complex system to be managed by the operators. The substitution of the large generation centers (decommissioning of large nuclear power plants) by multiple and distributed production centers will probably decrease the stability of the grid and mitigate its ability to absorb the additional kinetic energy after a perturbation.

Real-time optimization becomes therefore an important issue for power systems. The central objectives target the security of power supply but also the reduction of energy cost. High-speed computation is required in order to meet real-time optimization. Indeed, multiple scenario simulations are needed to provide power system stability assessment (PSSA). Then, new states of the analyzed power system can be obtained by means of different optimization methods.

Existing simulations methods are currently based on numerical algorithms solved by computers. Different hardware architectures have already been presented based on FPGAs, GPU and multi-core processors. Despite the use of parallel computation, simulation speed is related to the size of the simulated power system. The presented architecture overcomes this issue thanks to the intrinsic parallelisation of analog emulation. Rather than solving the Kirchhoff network equations by means of heavy matrix algorithm, it uses instantaneous analog computation [1] [2]. Then, models of generators and loads are computed on low-cost FPGAs that contains a dedicated pipelined architecture [4]. Analog-to-digital (ADC) and Digital-to-analog (DAC) high-speed converters provide the interface between the two computation methods.

This paper is organized as follow. We start by describing the system architecture called field programmable power network system (FPPNS) [2] [5]. We continue presenting the phasor emulation (PE) approach used to model analogically the power network. Then the platform is described in detail and the 3D connection structure that permits to enhance the number of nodes is shown. A speed and accuracy comparison between a reference simulator and the hardware platform is provided by means of an IEEE benchmark topology that contains 14-nodes and 30-nodes.

II. A POWER SYSTEM EMULATOR BASED ON A RECONFIGURABLE ARRAY OF NODES

The hardware platform is based on a modular array of power system nodes called FPPNS. Each reconfigurable node can be configured either as a generator, as a load or both.

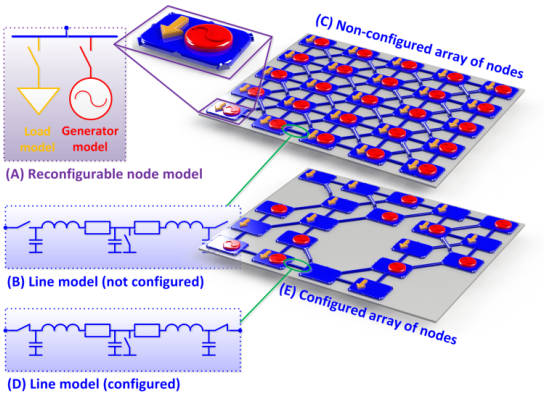

Fig. 1.The FPPNS emulation principle

This work is funded by ABB Switzerland Ltd Corporate research. All authors work with the Electronics Laboratory (ELAB) or the Power Systems Group (PWRS) of the Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: laurent.fabre@epfl.ch).

Each node can be analogically connected to other nodes by means of analog components representing the transmission line model. The grid topology is configured before each set of scenarios through programmable analog switches. It enables each line to be connected, disconnected or short-circuited. Fig. 1 shows a single node (A), a reconfigurable line model (B) (D) and the array of nodes (C) (E) to illustrate the FPPNS principle. The next chapter presents the model used for emulating the lines through analog computation.

III. THE PHASOR EMULATION (PE) APPROACH

The PE approach uses the complex representation of electrical variables (voltages and currents). It converts each RLC π-lines components in pure resistive components separated in two equivalent resistive networks [1] [3]. Fig.2 illustrates the PE phasor conversion where the serial resistive part R_s has been neglected when considering a high-voltage transmission line [3]. It remains the serial inductive impedance X_s .The parallel capacitive shunt X_p of the line is considered as a load and is included in the node model.

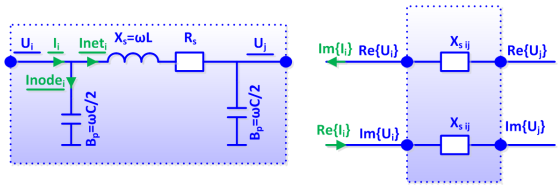

Fig. 2. On the left, the three phases RLC π-line modeling. On the right, the same RLC π-line represented with the PE approach.

Consequently the use of purely resistive components becomes possible for emulating the RLC π-lines building the grid thanks to the PE approach. The implementation is based on switches and programmable potentiometers for configuring the topology.

$$\underline{I_i} = \Re e\left\{\underline{I_i}\right\} + j\cdot\Im m\left\{\underline{I_i}\right\}$$
$$= \underbrace{\sum_{j=1}^{n}\left(\frac{1}{R_{S_{ij}} + j\cdot X_{S_{ij}}}\cdot\left(\underline{U_i} - \underline{U_j}\right)\right)}_{Inet_i} + \underbrace{\left(\underline{U_i}\cdot\left(j\cdot B_{P_{ij}}\right)\right)}_{Inode_i} \quad (1)$$

$$\Re e\left\{\underline{I_i}\right\} = \underbrace{\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2 + X_{S_{ij}}^2}\cdot\left(\Im m\left\{\underline{U_i}\right\} - \Im m\left\{\underline{U_j}\right\}\right)\right)}_{I_{net}\ A_i} - \underbrace{\left(B_{P_{ij}}\cdot\Im m\left\{\underline{U_i}\right\}\right)}_{I_{node}\ B_i} \quad (2)$$

$$-j\cdot\Im m\left\{\underline{I_i}\right\} = \underbrace{j\cdot\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2 + X_{S_{ij}}^2}\cdot\left(\Re e\left\{\underline{U_i}\right\} - \Re e\left\{\underline{U_j}\right\}\right)\right)}_{I_{net}\ C_i} - \underbrace{j\cdot\left(B_{P_{ij}}\cdot\Re e\left\{\underline{U_i}\right\}\right)}_{I_{node}\ D_i} \quad (3)$$

Fig. 3. (1) π-lines complex current equation. (2) Real part of the π-lines current in the PE approach. (3) Imaginary part of the the π-lines current in the PE approach.

IV. NODAL INTERFACE IMPLEMENTATION OF THE MIXED-SIGNAL PHASOR EMULATION (PE) APPROACH

The array of nodes is a lattice of analog components that computes the grid model through the PE approach. Each node is connected to interfaces that links digital and analog computation world. The interface provides local information to the grid through the DAC by means of current injection. It measures the global response of the grid through the ADC interface by means of voltage measurement. Each node interface (Fig.4) contains therefore two digital-to-analog converters, the reconfigurable analog components modeling the proximate grid, two analog-to-digital voltage converters and a feedback algorithm modeling the load or generator models.

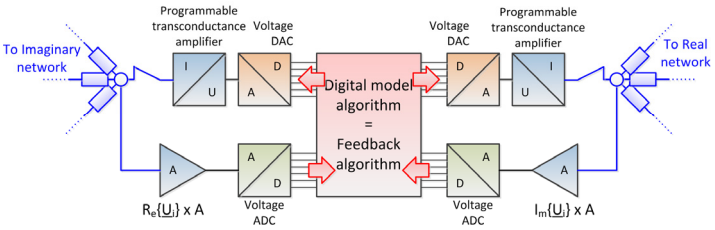

Fig. 4. Interface implementation of the PE mixed-signal approach

The nodal interface is separated in two parts: the first one is connected to the real part of the grid and the second one is connected to the imaginary part of the grid. Each part (Fig.5) contains a setting block (containing DAC), a part of the analog-grid computation and a sensing block (containing ADC). The DAC is followed by a configurable voltage-to-current interface. It allows injecting a nodal current or setting a node voltage. The grid configuration is reached by setting analog switches (topology) and configuring multiple programmable potentiometers (lines impedances). The node voltage sensing is obtains through a high speed ADC connected to a single-to-differential analog front end which increase the signal-to-noise ratio. The whole node implementation is realized through SPI interface. It uses a clock frequency of 10Mhz permitting to configure the full nodal interface in 15us.

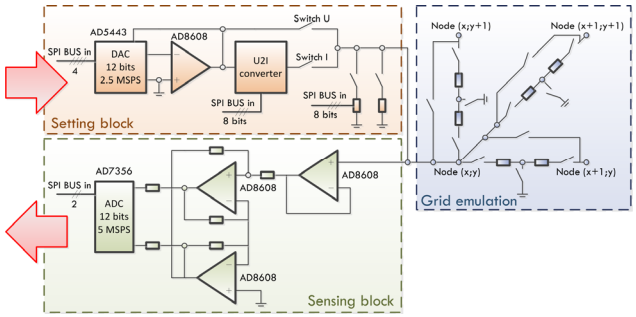

Fig. 5. Half part of node mixed-signal interface

Multiple load and generator models can be implemented using this interface. The following non-exhaustive list presents some models: constant impedance load, constant power load, constant current load, classical generator or generator model 1.1 using Park equations. The equations related to the described model are detailed in [2] [6].

V. SCALING FACTORS

Scaling factors links the grid electronic parameters (voltage, impedance and current) between simulated world and

emulated world. The scale factor relationships are described in table 1. Those factors have been choosen to fullfield three constaint: components voltage supply, bandwith of the analog grid computation and signal-to-noise ratio.

	Real world	Simulated	Emulated
U	380 [kV]	1[pu]	1[V]
I	263[A]	1[pu]	50[uA]
Z	1444[Ω]	1[pu]	20[kΩ]

Table 1. Electronic scaling factors

VI. System Architecture

The hardware architecture is based on two boards: a *mixed-signal board* and a pure digital *FPGA board* (Fig.6)

The *mixed-signal board* contains the reconfigurable components of the grid model through the PE approach. It also contains the ADC and DAC interfaces. The *FPGA board* provides the configuration of the mixed-signal board and an innovative pipeline architecture computing the load and generator models [4]. A high-speed USB connection is also included on the FPGA board. It provides connection to any computer for board configuring and signal measuring. A set of an FPGA and mixed-signal boards can emulate up to 24 nodes and up to 84 branches.

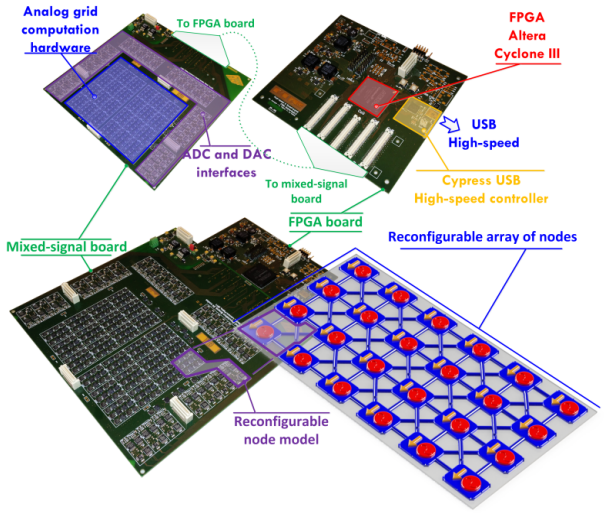

Fig. 6. Architecture of the mixed-signal architecture providing the PE approach computation platform

Each mixed-signal board contains also reconfigurable and vertical connections that model the lines. The stacking of multiple boards enables therefore to increase of the power system topology size. Fig. 7 illustrates a stacking system of 4 mixed-signal boards and 4 FPGA boards provide a 96 nodes and 336 branches platform thanks to the proposed 3D vertical connections.

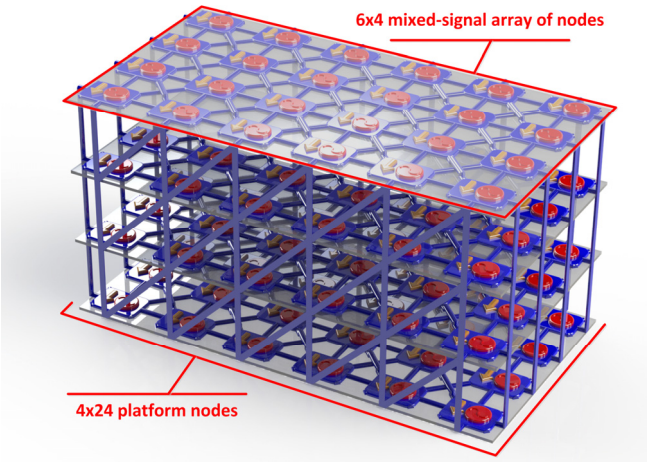

Fig. 7. Stacking of 4 mixed-signal board and 4 FPGA boards

VII. Calibration Process

Before using the mixed-signal platform it requires a full calibration process of the analog components. Indeed, programmable potentiometers are provided with a range of ±10%. An automatic calibration methodology has been therefore implemented and uses high-precision components connected to each node as references components. The calibration process (Fig.8) begins with the ADC offset and gain calibration to establish an accurate reference measure. It is followed by the offset and gain calibration of the nodal current source (real and imaginary part). Finally, a binary search algorithm is used for the calibration of every programmable resistor using 0.1% precision resistors as reference.

The full automatic calibration process takes less than 1500ms per board and only one calibration is necessary before a set of multiple emulations. Calibration is uniquely necessary when hardware temperature as changed.

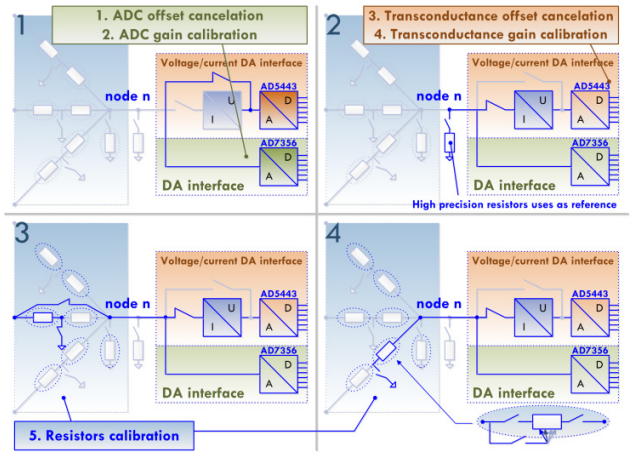

Fig. 8. Calibration process overview. (1) ADC offset and gain (2) DAC and transconductance offset and gain (3) Programmable resistors.

VIII. CONFIGURATION AND ANALYSIS SOFTWARE

Dedicated software has been realized for the management of the hardware platform. It includes communication drivers, the full calibration procedure and the results analysis. It contains an easy to use GUI for the power system configuration. The software core contains automatic mappers and a fitter which simplify the emulation configuration process. The mapper core aims to automatically map the power system topology on the 3D emulator architecture. The fitter core translates the power system parameters into electronic values using scale factors for resistances, currents, voltages and gains. The user can choose between digital software simulation and the hardware emulation platform. Finally, visualization and analysis coming from both platforms can be performed.

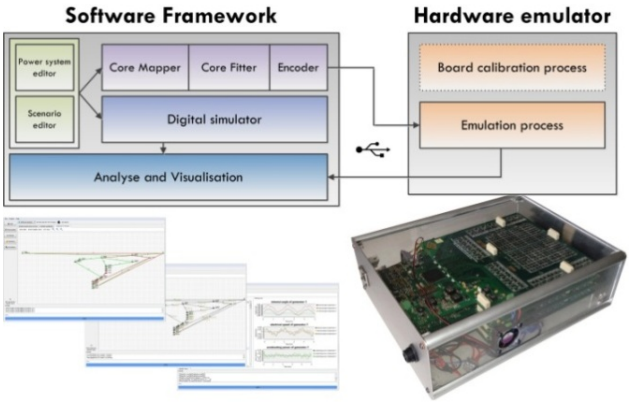

Fig. 9. Software architecture overview

IX. COMPARISON RESULTS BETWEEN DIGITAL SIMULATION AND MIXED-SIGNAL EMULATION

A. *Mapping of the IEEE 14 bus test case*

Comparison in term of accuracy has been done in order to validate the full concept. The IEEE 14 Bus Test Case [7] has been first chosen as a benchmark. Fig. 10 illustrates the mapping of this topology on 1 mixed-signal board.

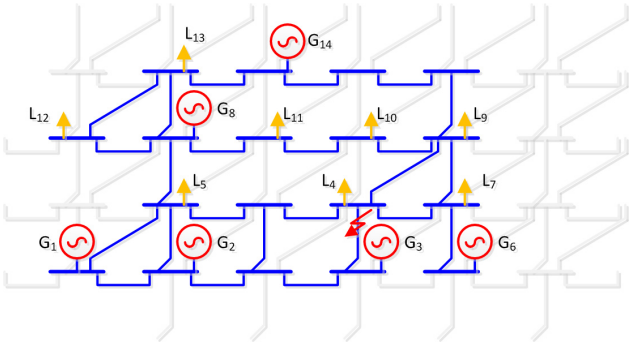

Fig. 10. Mapping of the IEEE 14 Bus test case on 1 mixed-signal board

B. *Calibration and accuracy results*

The IEEE 14 Bus Test case contains 6 generators, 8 loads and 24 branches. A digital simulator used as reference has been implemented on Labview. It has already been validated and compared with Eurostag software [2]. It includes exactly the same model equations than that of the hardware platform. The comparison scenario is based on a three-phases short-circuit on line G3-L4 with a clearing of 70ms after the fault. Fig. 11 and Fig. 12 illustrate the rotor angles of the generators. Fig. 11 shows a comparison between simulation (computed with Labview) and mixed-signal emulation without any component calibration. Fig. 12 provides the same comparison with a previous calibration of the analog components of the mixed-signal board.

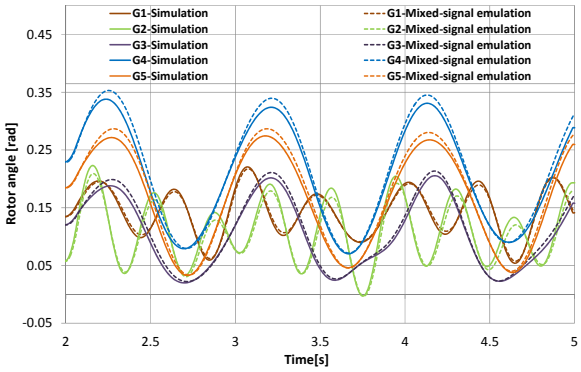

Fig. 11. Dynamic behavior of the rotor angles for the three-phases short-circuit without calibration of the mixed-signal board

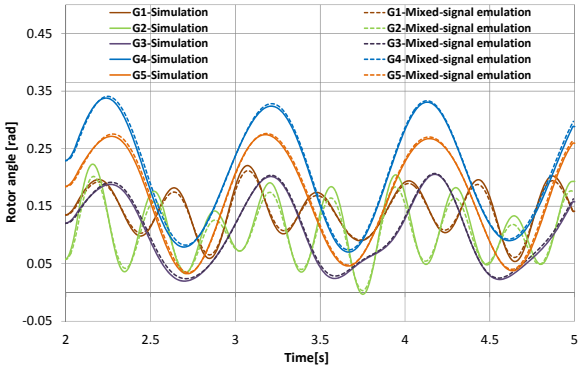

Fig. 12. Dynamic behavior of the rotor angles for the three-phases short-circuit with previous calibration of the mixed-signal board

Fig. 11 and Fig. 12 show that the analog components calibration significantly reduces the error between simulation and mixed-signal computation. Indeed, pre-calibration resistor error is in the range of ±10% and post-calibration resistor error is in the range of ±0.5%.

C. *Time-step modification*

The mixed-signal emulation time-step can be adjusted from the GUI. It can be set in the range of 1ms to 0.0625ms. A comparison scenario based on the same three-phases short-circuit with a clearing of 200ms after the fault has been

chosen as a reference in order to compare the different results. Fig. 13 shows a comparison between simulation (computed with Labview) and mixed-signal emulation for G2 and G8 rotor angles. Five different time-steps are illustrated: 1ms, 0.5ms, 0.25ms, 0.125ms and 0.0625ms.

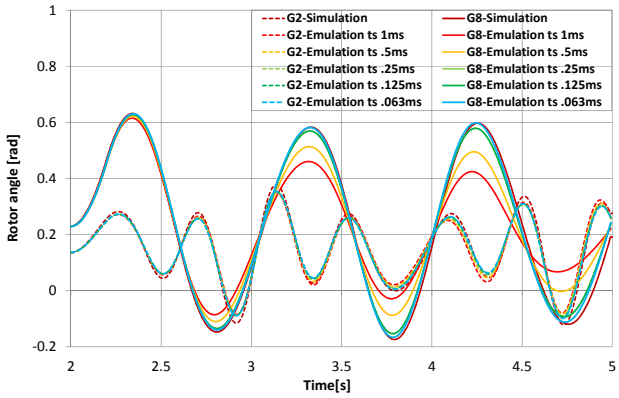

Fig. 13. Dynamic behavior of two rotor angles (G2 and G8) for a three-phase short-circuit (200ms) and different time-step emulation.

Fig.13 illustrates that dynamic behavior of rotor angles is damped when increasing the time-step. Indeed, bandwidth of the analog computation grid is slightly too low for providing the necessary analog feedback speed. This is due to parasitic capacitance of the printed circuit board (PCB). It creates RC filters with the configurable resistances computing the grid. A full computation time-step includes DA conversion, analog grid computation, AD conversion and digital model computation [4]. This computation scheme takes 1us at each time-step. The analog grid computation time between the DAC and ADC has been fixed to 200ns in order to obtain an equivalent ratio between analog and digital computation time. Enhancement of the system bandwidth is nevertheless possible by reducing the impedance scale factor. This modification has three consequences:

- Enhancement of the RC filter cutoff (reduction of R value);
- Reduction of the system accuracy (resistance resolution is decreased);
- Enhancement of the signal-to-noise ratio (higher current in the analog grid);
-

D. Impedance scale factor modification results

Based on the same comparison scenario than the previous paragraph, different impedance scale factors have been set through the developed GUI. This comparison aims to validate the enhancement of the grid computation bandwidth in order to cancel the effect illustrated in the previous paragraph. Table 2 shows the system characteristics when changing the impedance scale factor.

	Impedance scale factor	Line impedance resolution	Current scale factor	Volatage scale factor
1	20[kΩ/pu]	9 bit	50[uA/pu]	1[V]
2	15[kΩ/pu]	8 bit	66.7[uA/pu]	1[V]
3	10[kΩ/pu]	8 bit	100[uA/pu]	1[V]
4	5[kΩ/pu]	7 bit	200[uA/pu]	1[V]
5	3[kΩ/pu]	6 bit	333.3[uA/pu]	1[V]

Table 2. Characteristics of the analog grid computation when setting different impedance scale factors

Fig. 14 shows a comparison between simulation (computed with Labview) and multiple mixed-signal emulation for G2 and G8 rotor angles. The time-step computation is maintained at 1ms. Five different impedance scale factors are illustrated: 20kΩ/pu, 15kΩ/pu, 10kΩ/pu, 5kΩ/pu and 3kΩ/pu.

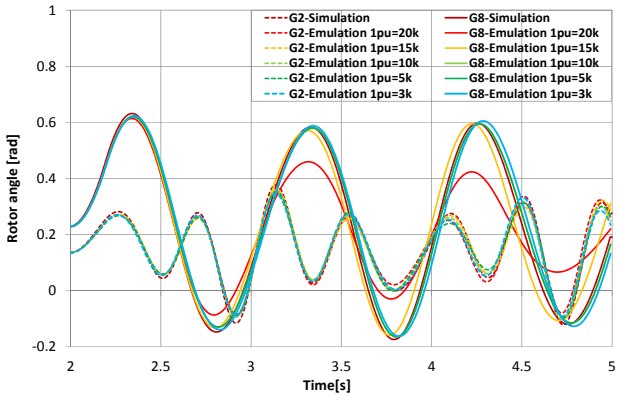

Fig. 14. Dynamic behavior of two rotor angles (G2 and G8) for the three-phase short-circuit (200ms) with different impedance scale factors.

Fig. 14 illustrates therefore that the rotor angle damping is cancelled when decreasing the impedance scale factor. This is due to the increase of RC filter cutoff frequency by means of resistance reduction. The rotor angles behavior shows that an impedance scale factor of 10kΩ/pu is sufficient for canceling the damping effects.

E. Critical Clearing Time (CCT) analysis

The platform is also able to perform a binary search algorithm that analyses the CCT of each branch in the topology. Critical Clearing Time (CCT) determination is concerned with the maximum sustained duration of a fault, for which the system maintains its stability. The CCT value is estimated by an upper and a lower bound. Table 3 shows a comparison between the simulated and emulated CCT of different lines of the topology.

	CCT Simulated lower bound	CCT Simulated upper bound	CCT Emulated lower bound	CCT Emulated upper bound
G3-L4	657ms	658ms	654ms	655ms
G6-L11	615ms	616ms	592ms	593ms
L13-G14	590ms	591ms	582ms	583ms
G1-G2	820ms	821ms	790ms	791ms

Table 3. CCT comparison of different lines of the topology

Fig. 15 shows rotor angles comparison between simulation and mixed-signal emulation for different clearing time (from 70ms to 175ms). A three phase short-circuit is applied in the middle of the line G3-L4.

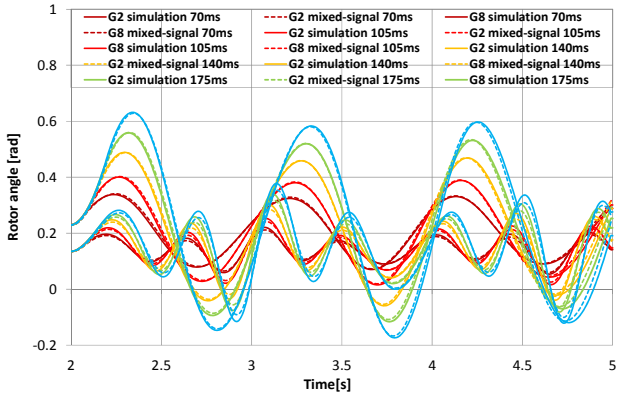

Fig. 15. Dynamic behavior of two rotor angles (G2 and G8) for different clearing time. Simulated and emulated results are compared.

F. Simulation and mixed-signal emulation speed comparison

Comparisons in term of speed have also realized. The IEEE 30 nodes reference topology [7] has been used as a benchmark. This topology has been mapped on two connected board sets. It contains 6 generators, 24 loads and 42 branches. The comparison scenario is based on a three-phases short-circuit on a line with a clearing of 70ms after the fault. Fig. 16 illustrates the rotor angles of the generators 5 seconds following the fault.

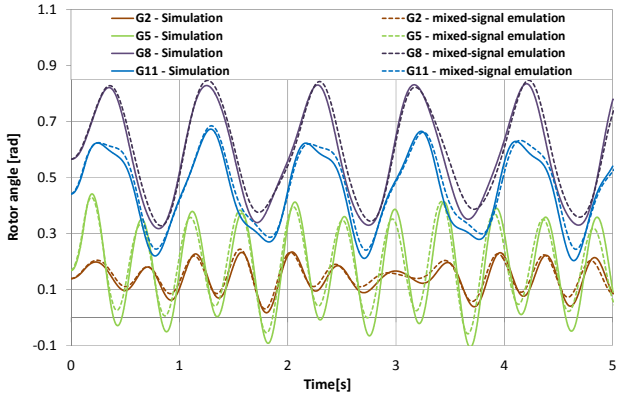

Fig. 16. Comparison between emulated and simulated rotor angles for a three-phase short-circuit (clearing after 70ms)

For the same line models, generator models, load models and for the same computation step (1ms), it takes 2.6s for the simulation process (IntelCore i7 64bit @ 3.40Ghz). The mixed-signal emulation process takes only 5ms. The platform speed is therefore 520 times higher than the simulator. The speed increase will also be higher for larger power system networks as analog computation speed is independent of the power system size.

X. CONCLUSION

This paper presents a novel 3D hardware platform for power system dynamics computation based on mixed-signal architecture. Thanks to the FPPNS concept, the proposed architecture is flexible in term of topology. Moreover, it can be stacked for increasing the number of the power system nodes. Comparison results between digital simulation and the proposed platform illustrates that computation speed is much higher. The computation speed is not related to the number of nodes. This is due to the instantaneous analog computation of the grid and the dedicated electronics. Thanks to high-speed USB connection capabilities this platform aims to be used as a co-processor unit for computing ultra-fast power system security assessment.

Applications such CCT and dynamic PSSA can be easily address with such a platform.

In order to further increase the number of node an integrated circuit has been developed on the same 3D connection strategy. It aims to emulate power systems containing hundreds of nodes

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