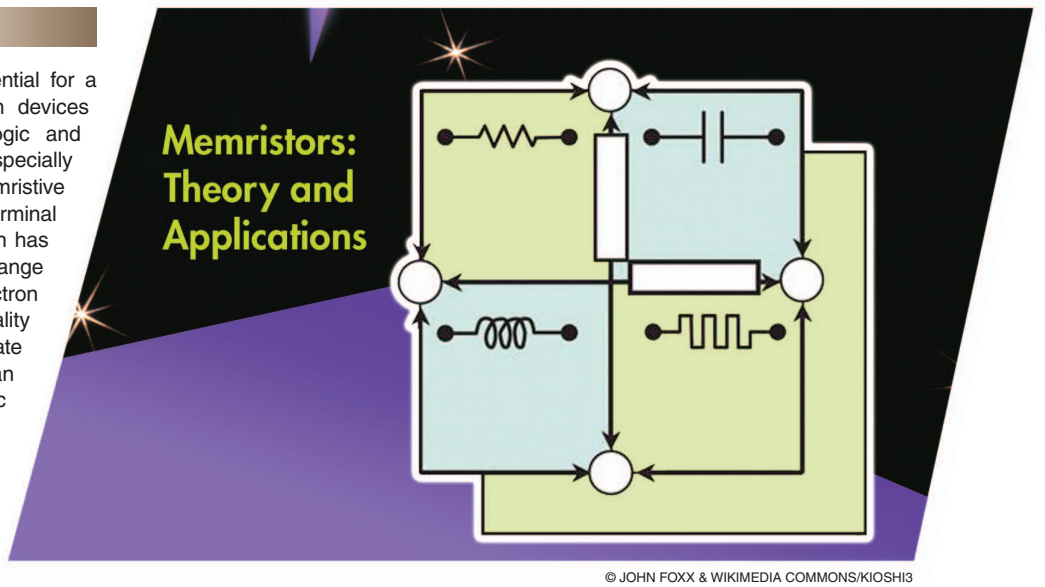
Applications of Multi-Terminal Memristive Devices: A Review

Davide Sacchetto, Pierre-Emmanuel Gaillardon, Michael Zervas,
Sandro Carrara, Giovanni De Micheli, and Yusuf Leblebici

Abstract

Memristive devices have the potential for a complete renewal of the electron devices landscape, including memory, logic and sensing applications. This is especially true when considering that the memristive functionality is not limited to two-terminal devices, whose practical realization has been demonstrated within a broad range of different technologies. For electron devices, the memristive functionality can be generally attributed to a state modification, whose dynamics can be engineered to target a specific application. In this review paper, we show examples of two-terminal *Resistive RAMs (ReRAM)* for standalone memory and *Field Programmable Gate Arrays (FPGA)* applications. Moreover, a *Generic Memory Structure (GMS)* utilizing two ReRAMs for 3D-FPGA is discussed. In addition, we show that trap charging dynamics can explain some of the memristive effects previously reported for *Schottky-barrier field-effect Si nanowire transistors (SB SiNW FETs)*. Moreover, the SB SiNW FETs do show additional memristive functionality due to trap charging at the metal/semiconductor surface. The combination of these two memristive effects into multi-terminal MOSFET devices gives rise to new opportunities for both memory and logic applications as well as new sensors based on the physical mechanism that originate memristance. Finally, the multi-terminal memristive devices presented here have the potential of a very high integration density, and they are suitable for hybrid CMOS co-fabrication with a CMOS-compatible process.



I. Introduction

Very different applications belonging to signal processing, memory and sensing are envisaged for multi-terminal memristive devices. The possibility to build very dense crossbar arrays of two-terminal memristive devices is often seen as a disruptive technology for ultra-dense *Resistive RAM (ReRAM)* or *Write at Once Read Many (WORM)* non-volatile memory storage [1]. In this concern, all the non-volatile two-terminal memristive technologies are suitable candidates to replace flash memory in the future, given their higher density storage per cost. This feature is especially interesting because it can be utilized to stack non-volatile memory elements in the *Back-End-of-the-Line (BEoL)*, increasing both density and access speed among logic and memory layers. Good examples are the recently proposed hybrid semiconductor/nanowire/molecular (CMOL) integrated circuits [2], as well as 3D *Field Programmable Gate Arrays* (*FPGA*) architectures with programmable *Through Silicon Vias* (*TSVs*) [3] (see Fig. 1). Moreover, the ReRAMs can be combined

Digital Object Identifier 10.1109/MCAS.2013.2256258
Date of publication: 22 May 2013

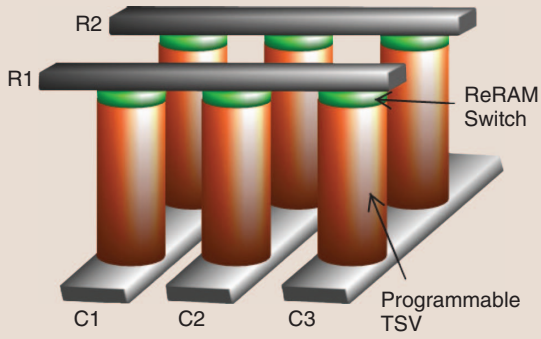


Figure 1. A crossbar architecture with programmable TSVs made of ReRAM stacks [3].

in new arrangements, as for instance, in the *Generic Memory Structure (GMS)* that enables faster data path with less area in 3D-FPGAs [4]. The two-terminal memristive crossbars can also be integrated into programmable logic array architectures to compute Boolean logic functions. The memristive crossbar architecture can be exploited to re-program itself. For instance in [5], a very dense nanowire crossbar with TiO_2 memristive junctions was used to perform logic functions and to store the result into another portion of the same crossbar. Moreover, memristive switches can be used to perform material implication function[1] and exploited to build latches that use resistance in place of voltage or charges as physical state variable [6]. Another application that can exploit the memristive functionality is related to the design of Cellular Neural Networks [7]. The Hodgkin-Huxley model for the synapse was one of the earlier examples reported by Chua and Kang [8] of systems that can be modeled with the memristor. Recently, the use of two-terminal memristive devices in combination with digital to analog converters demonstrated a way of reproducing the associative memory of animals [9]. The modification of the memristive characteristic to environmental conditions can also be utilized for different types of sensing. For instance, functionalization of nanowires with redox active molecules gives rise to the typical memristive pinched hysteresis loop [10]. Another example can be the sensing of temperature with spintronic memristor [11]. The temperature change can cause a variation of the domain-wall mobility that in turns is sensed thanks to a positive feedback loop electronics. This type of sensor has been reported to be very compact ($\leq 1\,\mu m^2$ cell size) and to operate with very low power.

Multi-terminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [12] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for bio-molecule detection in dry environment [13]. More specifically, in [13] the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all-around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authors [14]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [15]. For instance in [15], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing a hysteretical negative differential resistance [16]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel.

In Section II an example of fabrication and characterization of bipolar resistive RAM based on Al_2O_3 and Ta_2O_5 is discussed for standalone memory applications. Then a *Generic Memory Structure (GMS)* made of two ReRAM devices is presented and discussed for FPGA applications (Section III). Another example of ReRAM application is given in Section IV. Then, in Section V sensing applications for multi-terminal memristive SiNW devices are showcased. Finally, in Section VI we draw the conclusions.

II. Standalone Memories

A. Introduction

Future deeply scaled circuits will see their performances limited by the physical limitations of the materials. To keep pushing the performance of computation and the density of storage, the microelectronics industry envisages using more efficient state variable than the electronic charge. In this sense, the

[1]Here, the material implication is used for a fundamental Boolean logic operation on two variables p and q such that pIMPq is equivalent to (NOTp)ORq.

Davide Sacchetto, Pierre-Emmanuel Gaillardon, Michael Zervas, Sandro Carrara, Giovanni De Micheli, and Yusuf Leblebici are with EPFL—Ecole Polytechnique Fédérale de Lausanne, Switzerland. E-mail: davide.sacchetto@epfl.ch.

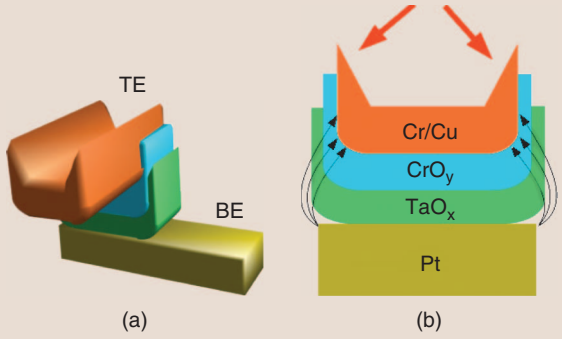


Figure 2. (a) 3D cross-point ReRAM concept with fence-like TE shape. (b) Lateral cross-section view of Pt/TaO_x/CrO_y/Cr/Cu cross-point ReRAM device. The fence-like TE enables better scalability of the cross-point device thanks to a reduction of the intense electric field distribution at the corners.

memristor is an attractive candidate for both computation and memory, thanks to its programmable resistive state. When considering the Resistive RAM (ReRAM) memories, which can be classified as memristors, excellent scalability and programming time can be obtained if compared to traditional Flash, which make ReRAMs suitable candidates for standalone memory applications.

In this section, a ReRAM technology demonstrating a *Multi-Level (ML)* forming-free Pt/TaO_x/CrO_y/Cr/Cu crossbars built with low thermal budget $< 200\,^{\circ}C$ is discussed. The devices show excellent scalability down to 2.5×10^9 bit/cm^2 with device half-pitch of 100 nm with projections of practical storage density of up to 10^{12} bit/cm^2 at the 10 nm technology node [17].

B. Fabrication

The basic device concept is a ReRAM composed of 2 metal lines crossing orthogonally and a transition metal oxide stack in between (see Fig. 2(a)). Moreover, the shape of the *Top Electrode (TE)* has been fabricated such that corners are smoothed (Fig. 2(b)). This feature reduces the fringing field intensity at the wire ends, thus improving both reliability and scalability of the devices. Two different ReRAM (Pt/TaO_x/CrO_y/Cr/Cu and Al/TiO_2/Al with the Bottom Electrode/Transition Oxide/Top Electrode order) stacks have been built and compared in terms of performance. Both stacks have forming-free property and as such they do not require special forming steps to form the devices. This is a considerable advantage for actual implementation on chip. Several devices have been built in a passive crossbar array fashion as explained in the following text. Si bulk wafers are first isolated by depositing 100 nm thick Al_2O_3 with *Atomic Layer Deposition (ALD)*

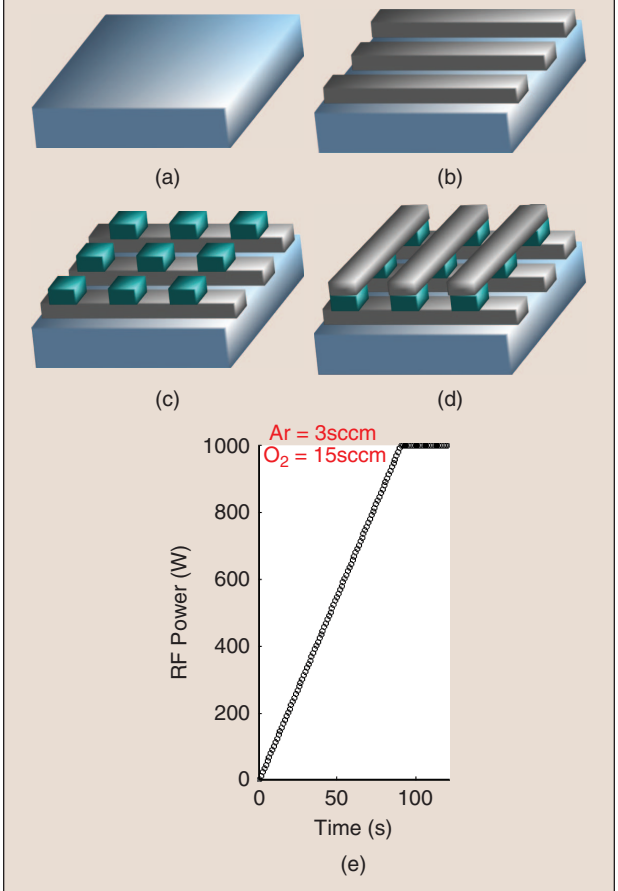


Figure 3. Process Flow. (a) Insulated Si substrate, (b) Pt bottom electrode lift-off, (c) TaO_x sputtering deposition, (d) TE lift-off, and (e) sputtering parameters of TaO_x, with increasing RF power and constant 3sccm/15sccm Ar/O_2 flows.

(Fig. 3(a)). Then, PMMA bi-layers are patterned with e-beam lithography as lift-off masks for 10 nm/80 nm Pt *Bottom Electrodes (BE)* deposition (Fig. 3(b)). In the next step, a second lift-off mask is defined and 15 nm TaO_x oxide layer (Fig. 3(c)) is deposited by sputtering from a Ta_2O_5 target with increasing RF power in Ar/O_2 atmosphere (Fig. 3(e)). Finally, 50 nm/100 nm thick Cr/Cu bi-layers TE are deposited by e-beam evaporation (Fig. 3(d)). For Al/TiO_2/Al devices, the Al electrodes are deposited with e-beam evaporation while 10 nm thick TiO_2 is deposited by ALD. In Fig. 4(a) and 4(b) SEM images of 100 nm wide BE lines and 64 bit passive crossbar are shown, respectively. In Fig. 4(c), a 3D reconstructed AFM profile is shown. About 250 individual Pt/TaO_x/CrO_y/Cr cross-points for area sizes varying from 100 nm $\times$ 100 nm to 1 μm $\times$ 1 μm, and 64 bit crossbars with half-pitch varying from 100 nm $\times$ 100 nm to 500 nm $\times$ 500 nm are built on the same sample following the proposed fabrication steps. In Fig. 5(a) and Fig. 5(b), a tilted SEM view, and a 3D reconstructed

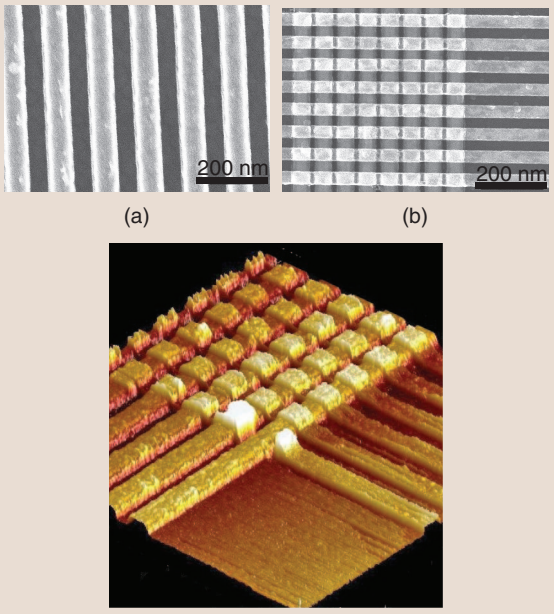


Figure 4. Top SEM view of: (a) bottom electrode lines, (b) complete 64 bit crossbar array of devices with 100 nm half-pitch, and (c) reconstructed 3D image from AFM profile.

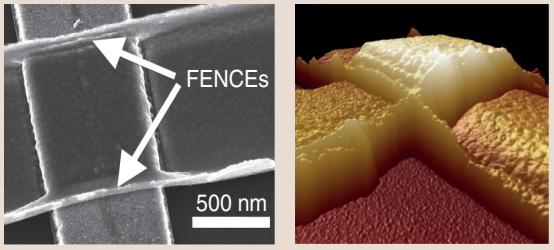


Figure 5. Pt/TaO_x/CrO_y/Cr/Cu cross-point device with 900 nm × 900 nm cross-point area. (a) Tilted SEM image view. Notice the fence-like structures at the edges of the TE line. (b) Reconstructed 3D AFM image of the pristine cross-point device. Average roughness on TE is $\sigma \approx 42.6$ nm.

AFM profile of a cross-point device with fence-like TE are shown, respectively.

C. Electrical Characterization

Electrical measurements are carried out with an Agilent B1500 semiconductor device analyzer. Pulse mode sweeps with pulses of 500 μs demonstrate forming-free *Bipolar Resistive Switching (BRS)* for Pt/TaO_x/CrO_y/Cr/Cu (Fig. 6(a)). The BRS is obtained for a voltage range of less than 1 V with pristine ON state in the same range of the *Low Resistance State (LRS)*. This is an important advantage compared with nonforming-free ReRAM devices, because the forming operation requires higher

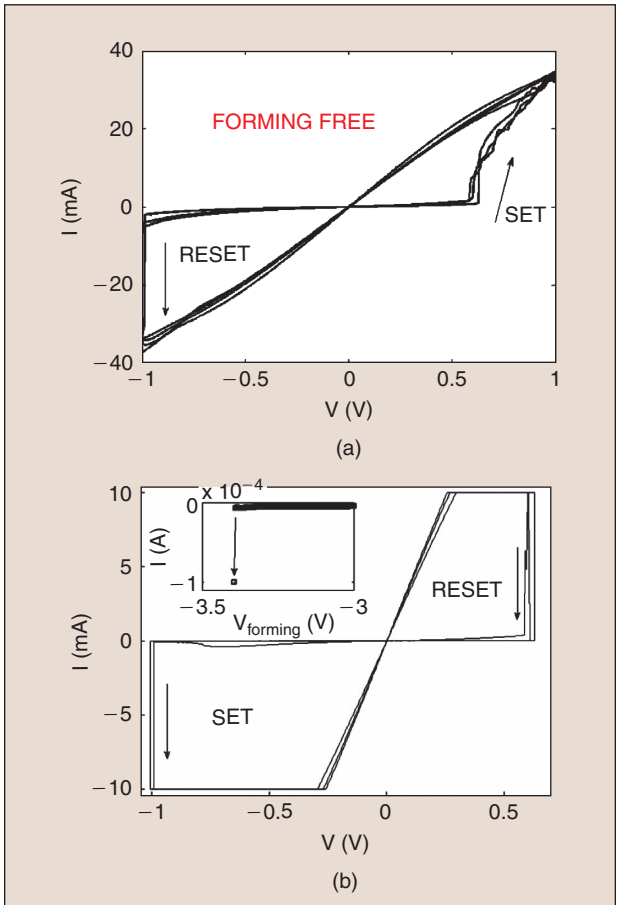
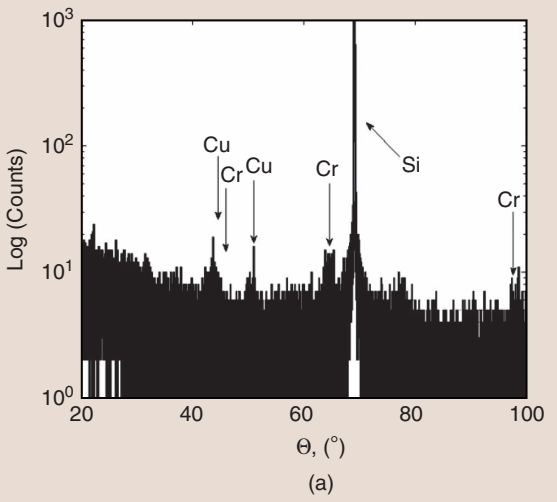


Figure 6. (a) Typical I-V characteristic of the Pt/TaO_x/CrO_y/Cr/Cu ReRAM cell showing resistance ratio of 10^4. Notice very low $V_{SET} = +0.8$ V and $V_{RESET} = -1$ V. After fabrication the devices are forming-free and in the ON state. (b) Typical I-V characteristic of the Al/TiO_2/Al ReRAM cell after forming with $V_{SET} = -1$ V and $V_{RESET} = +0.8$ V. Inset shows $V_{FORMING} = -3.4$ V.

voltages. A forming voltage of -3.4 V has indeed been necessary for the Al/TiO_2/Al (Fig. 6(b)), that then show similar performance as the Pt/TaO_x/CrO_y/Cr/Cu devices.

D. Discussion

Material characterization has been carried out to understand the pristine ON state of Pt/TaO_x/CrO_y/Cr/Cu. The X-ray diffraction pattern of Fig. 7(a) shows peaks from the TE and the Si substrate. The absence of any Ta_2O_5 or TaO_2 peaks indicates that the material is in amorphous state, due to the low deposition temperature. The visible peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. The pristine ON state excludes the conductive filament mechanism and observing the double logarithmic plot of the I-V curve (Fig. 8(a)), quasi-Ohmic regimes



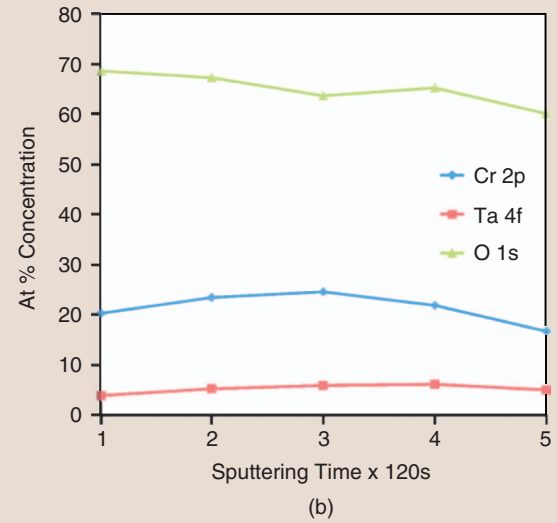
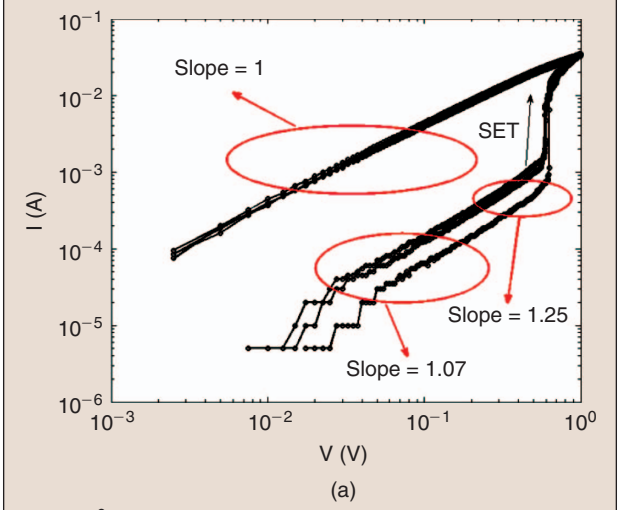


Figure 7. (a) X-ray diffraction pattern on an Si wafer demonstrating amorphous TaO_x/CrO_y. The peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. (b) XPS depth profile analysis showing the presence of both Cr and Ta in oxidized states. Both $Ta_2O_{5-\delta}$ and $TaO_{2-\gamma}$ are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE.



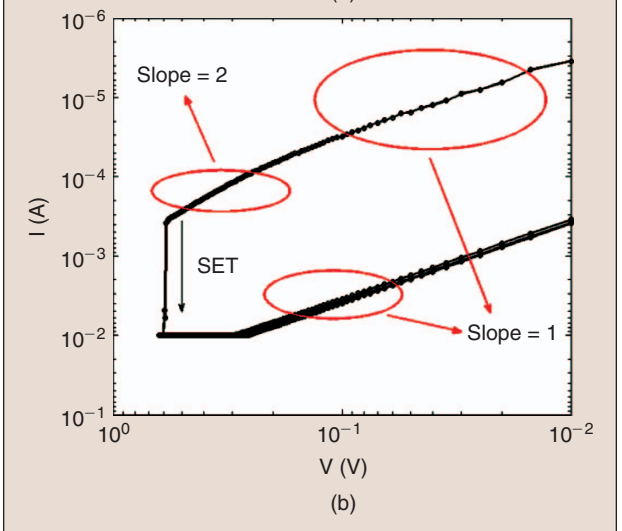


Figure 8. (a) The log(I)-log(V) plot of $Pt/TaO_x/CrO_y/Cr/Cu$ shows typical trap-controlled conduction of *Space-Charge-Limited-Conduction (SCLC)* before SET. In the SET region, the slope is about 25 and it is indication of gradual distribution of defects. (b) The log(I)-log(V) plot of the $Al/TiO_2/Al$ shows typical trap-controlled conduction of SCLC with quadratic V dependence before SET condition, thus following Childs law dependence. In the SET region, the slope is about 50, and it is indication of an abrupt distribution of defects.

with slopes ≈1 are obtained for regions far from the SET condition. Typical trap-assisted *Space-Charge-Limited-Conduction (SCLC)* is observed close to the SET condition. The SCLC conduction is also observed for $Al/TiO_2/Al$ devices (Fig. 8(b)) whose slopes indicate a more abrupt distribution of trap density, which can be related to the different deposition methods. In both devices, the resistive switching mechanism can be attributed to Redox reaction linked with the motion of oxygen-vacancies [18], [19]. Moreover, structural modification is observed from the roughness profile of $Pt/TaO_x/CrO_y/Cr/Cu$ cross-point after 100 cycles. As shown in Fig. 9(a) and Fig. 9(b), the $Pt/TaO_x/CrO_y/Cr/Cu$ average roughness (Ra) measured above the TE broadens. The Ra changes from a pristine 100 nm variation into a 200 nm broad window, indicating structural modification by the motion of oxygen vacancies upon switching. In addition, XPS-depth analysis (Fig. 7(b)) confirms that $Ta_2O_{5-\delta}$ and $TaO_{2-\gamma}$ phases are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE that is consistent with the Redox switching mechanism.

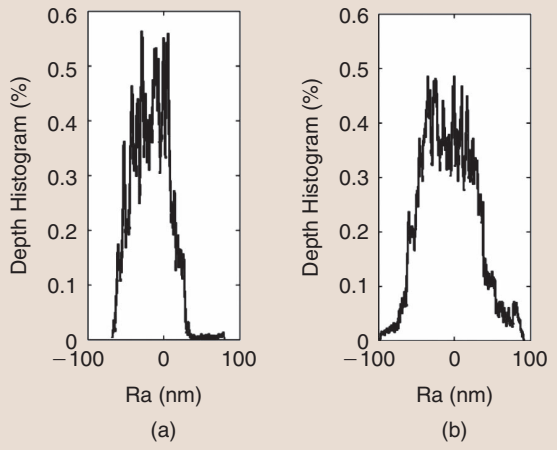


Figure 9. Average roughness profiles for TaO_x cross-points: (a) $\sigma \approx 42.6$ nm after fabrication; (b) $\sigma \approx 56.3$ nm after 100 cycles. The broadening is attributed to the structural change induced by the motion of oxygen-vacancies upon cycling.

1) High Density Multi-Valued Crossbars

Several resistance levels of $Pt/TaO_x/CrO_y/Cr/Cu$ devices can be programmed. As shown in Fig. 10(a), four levels of resistance (encoding 2 bits) are found within a 4 orders of magnitude range. A larger resistance window of 1 bit is found for $Al/TiO_2/Al$ devices, which show an LRS around 30 Ω and a *High Resistance State (HRS)* at 1 M Ω within 2 orders of magnitude variation (see Fig. 10(b)). The $Al/TiO_2/Al$ show stable LRS and HRS in a large V_{READ} voltage range (Fig. 11(a)). The $Pt/TaO_x/CrO_y/Cr/Cu$ devices demonstrate excellent scalability, as the HRS/LRS ratio improves for smaller device sizes (Fig. 11(b)). For instance, 2 bit can be written in a $Pt/TaO_x/CrO_y/Cr/Cu$ by using shorter SET pulses in order to program the cell in one of the stable Intermediate Resistance (IR) states. An example of 2 bit storage using LRS, HRS and 2 IRs is demonstrated in Fig. 12, each level is separated of about one order of magnitude from each other for various V_{READ}. The devices could be easily assembled into dense 2.5×10^9 bit/cm^2 passive crossbar arrays whose storage density improves to 10^10 bit/cm^2 thanks to ML capability of $Pt/TaO_x/CrO_y/Cr$ ReRAMs.

E. Conclusions

Bipolar Resistive Switching $Pt/TaO_x/CrO_y/Cr/Cu$ and $Al/TiO_2/Al$ devices built with thermal budget $< 200\,^{\circ}C$ have been fabricated and characterized. Very large storage density of TaO_x/CrO_y-based ReRAMs is demonstrated up to 10^{10} bit/cm^2 thanks to the excellent scalability of the fence-like top electrode lines.

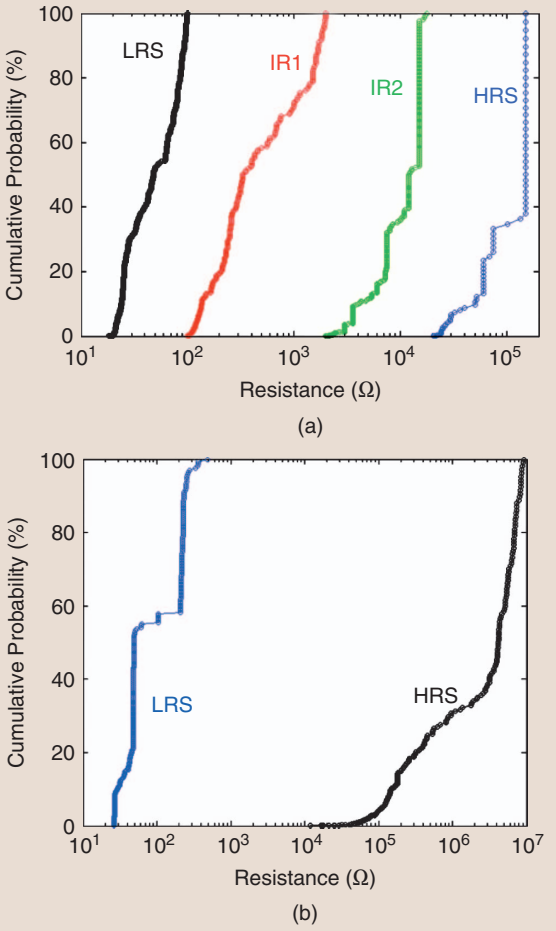


Figure 10. (a) Cumulative probability of *Low Resistance State (LRS)*, *Intermediate Resistance state 1 (IR1)* and *Intermediate Resistance state 2 (IR2)* and *High Resistance State (HRS)* for $Pt/TaO_x/CrO_y/Cr$ devices are shown. The LRS, IR1 and IR2 are obtained by using SET pulses of 2 ms, 1 ms and 500 μs at 1 V, respectively. The HRS is obtained with a 500 μs RESET pulse at −1 V. (b) Cumulative probability of LRS and HRS for $Al/TiO_2/Al$ devices are shown. The LRS and the HRS are obtained by using SET and RESET pulses of 500 μs at −1 V and +1 V, respectively.

III. Generic Memory Structure (GMS) for Non-Volatile FPGAs

A. Introduction

While a lot of research effort targets high density ReRAM-based standalone memories [20], the focus of this work is the usage of ReRAMs for Field-Programmable Gate Arrays (FPGAs). The reason behind this choice is that in reconfigurable logic, up to 40% of the area is dedicated to the storage of configuration signals [21]. Traditionally, the configuration data is serially loaded in SRAM cells, distributed throughout the circuit [22]. As a consequence, power up of the circuit is limited by the slow serial configuration.

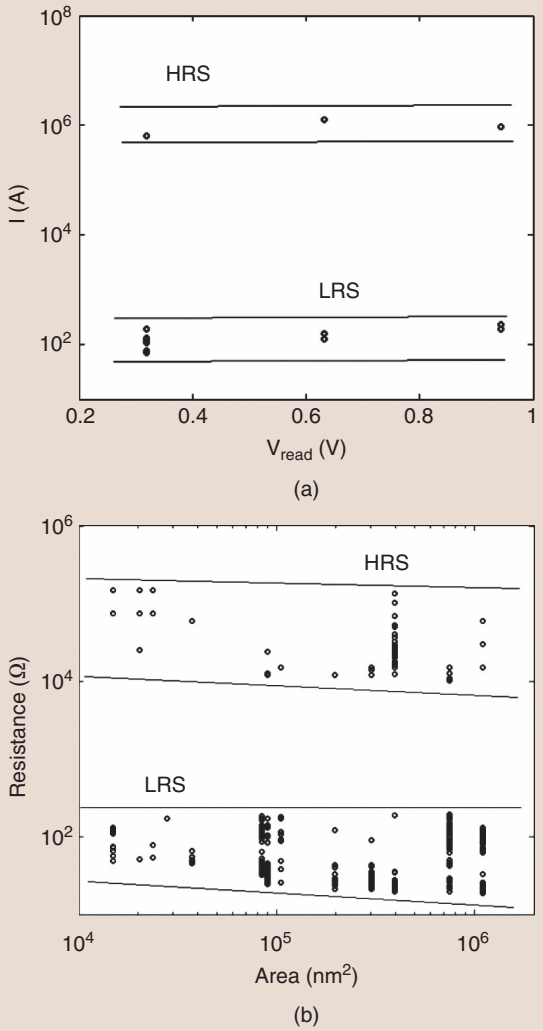


Figure 11. (a) LRS and HRS resistance distributions for increasing V_{READ} of the Al/TiO_2/Al cell. The 10^4 resistance ratio is constant over a large range of reading voltage. (b) Measured HRS and LRS values for the Pt/TaO_x/CrO_y/Cr cell devices with different cross-point area demonstrating excellent scalability, indicating local switching at the nanoscale.

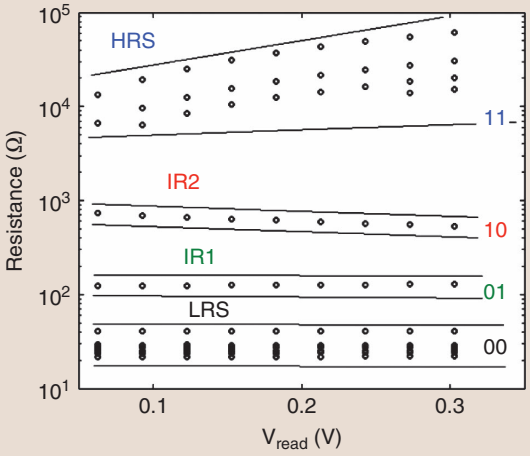


Figure 12. Resistance distributions for multi-value storages vs. increasing V_{READ} of the Pt/TaO_x/CrO_y/Cr cell. The HRS, IR2, IR1, LRS are encoded in 2 bit.

To overpass SRAM volatility and loading time issue, Flash NVM have been proposed [23]. Nevertheless, the use of an hybrid CMOS-Flash technology results in high fabrication costs. Conversely, ReRAMs are fabricated within the Back-End-of-the-Line (BEoL) metal lines, moving the configuration memory to the top of the chip and reducing the area utilization [24]. Similarly, the ReRAM cells can be utilized in combination with Through- Silicon-Via (TSVs), enabling 3-D stacked FPGA architectures [3]. In this paper, we propose a complete proof of concept of an ReRAM-based Generic Memristive Structure (GMS) circuit for FPGAs from technology development to architectural evaluation.

The main idea is to replace the pass-transistors in SRAM-based FPGAs by ReRAMs. Hence, the ReRAMs store the information in their resistive states and can be either used to route signals through low resistive paths, or to isolate them by means of high-resistive paths. Such a functionality is envisaged either to build routing Multiplexers (MUXs) or configuration nodes. In order to keep the programming complexity in the same range of SRAM-based FPGAs, we propose an efficient methodology based on the inherent GMS complementary programming. The proposed methodology, with GMS-based complementary programming has been validated by electrical measurements on a fabricated device.

B. BEoL Integration of ReRAMs

As per the previous section, ReRAMs can be fabricated within the BEoL processing. Hence, it is possible to fabricate them between two metal layers (e.g. in between Metal 1 and Metal 2). Because of the BRS of the ReRAMs of this study, depending on the forming polarity, either the Metal 1 or the Metal 2 terminal can be utilized as the positive electrode of the memory, giving two possible configurations (see Fig. 13(a)).

C. Device Description

In the GMS, two ReRAMs are interconnected as shown in Fig. 14(a). The positive terminal of the top memory is connected to the negative terminal of the bottom memory. This arrangement enables complementary programming of the two ReRAMs composing a GMS. We call the concurrent programming of the GMS a complementary programming operation.

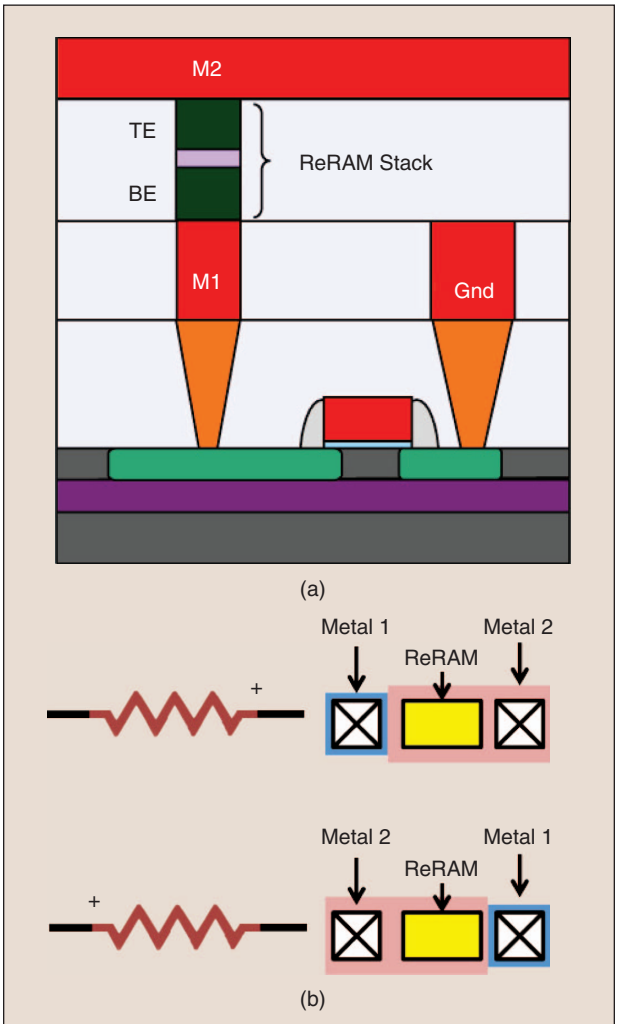


Figure 13. Cross sectional schematic showing the integration of a ReRAM integrated between the M1 and M2 interconnection levels in the back-end-of-line. (a) The bottom electrode is thus directly connected to a MOSFET selector (bottom) forming a 1-Transistor 1-Resistor (1T1R) memory node. (b) ReRAM polarity selection by physical design.

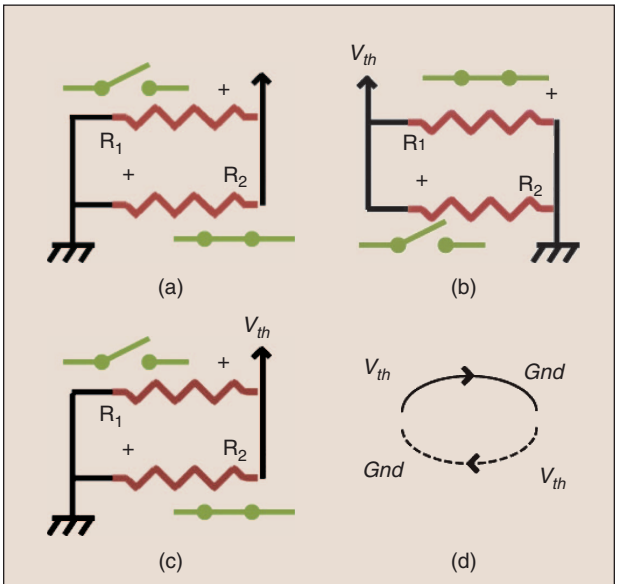


Figure 14. GMS complementary programming. (a) Two BRS resistive RAMs are in series connected after forming. (b) When V_{th} is applied, R_1 switches ON, while R_2 switches OFF. (c) When $-V_{th}$ is applied, R_1 switches OFF, while R_2 switches ON. (d) Graph representation of the complementary switching operation.

A similar programming scheme was previously used for low power crossbars [25]. Fig. 14(b) illustrates the programming of the top path (i.e. left to right arrow in the programming graph shown in Fig. 14(d)). R_1 and R_2 are switched simultaneously to R_{OFF} and to R_{ON} respectively. This operation is achieved by grounding the common right terminal and biasing the left terminal to Vth (which corresponds to the SET voltage –Vth for R_1 and to the RESET voltage +Vth for R_2). The programming of the bottom path (see Fig. 14(c)) is obtained by inverting the Vth and the Gnd (which corresponds to the RESET voltage for R_1 and to the SET voltage for R_2). In addition to speed up the programming operation, due to the complementary scheme, only two voltages are needed (Gnd and Vth).

The complementary programming operation has been validated by electrical measurements, while the MUX performances have been extracted by electrical simulations. Fig. 15 depicts the resistance values of R_1 and R_2 of a GMS-based MUX21. Resistances are read at $V_{READ} = +0.1$ V.

After a preliminary forming step, R_1 and R_2 are set to R_{ON}. The devices are then read for 10 cycles, showing a stable non-volatile resistance. Hence R_1 and R_2 are switched using the complementary programming operation presented in the previous section. During the first writing operation SET and RESET events are induced on R_2 and R_1, respectively (see Fig. 14(c)) by applying a voltage pulse for 500 μs. After reading the resistance values for another 10 cycles, again validating the non-volatility of the resistance states, a second complementary switching operation is performed as depicted in Fig. 6-b. Now the resistance states of R_1 and R_2 are complementary switching, as seen in the reading sequence of Fig. 15. As can be noticed the resistance values of R_1 and R_2 do not exactly match. This is due to the different ReRAM geometries and to the large variability of the cells utilized for the demonstrator. Nevertheless, improved variability of one order of magnitude has been demonstrated for ReRAM prototypes fabricated with industrial methods [26].

D. GMS Memory Node

In this section, we present an elementary circuit used to move most of the configuration part of reprogrammable

circuits to the back-end, reducing their impact on front-end occupancy. Such a memory node is dedicated to drive LUT inputs. The memory node is based on a unique GMS node and provides intrinsically the retained information as a voltage level. Furthermore, it shall allow a layout efficient line sharing.

1) Overall Structure

The basic memory node is presented in Fig. 16(c). The circuit consists of 2 ReRAMs connected in a voltage divider configuration between 2 fixed voltage lines (LA and LB). The memories are used in a complementary manner, in order to improve reliability. Reliability is required as far as the output is not restored by an inverter for compactness purpose. The output is designed to place a fixed voltage on a conventional standard cell input. Read operations are intrinsic with the structure, while programming is an external operation to perform on the cell.

2) Read Operation

A voltage divider is used in this topology to intrinsically realize the conversion from a bit of data stored in the variable resistance to voltage level. Fig. 16(b) presents a configuration example where the node stores a 1. Voltage lines LA and LB are respectively connected to Vss and Vdd. For the sake of example, consider that the resistive memory R1, connected to the Vdd line, is configured to the low resistivity state. The other memory R_2, connected to Vss, is in the high resistivity state. As a consequence, a voltage divider is configured and the output node is charged close to the voltage of the branch with a high conductivity. The logic levels depend on R_{ON} and R_{OFF} as in the following relations.

It is also worth noticing that in continuous read operation, a current will be established through the resistors. This leads to a passive current consumption through the structure based on the following relation.

This static current can be reduced by the choice of a memory technology like $Cu/TiO_2/Pt$ (Table 1) maximizing the R_{OFF} value.

3) Write Operation

Fig. 16(c) presents the programming phase of the node. First, the lines LA and LB are disconnected from the power lines and connected to the programming signals. The programming signals are chosen according to the GMS programming scheme. Fig. 17 presents the programming circuits required to program an array of GMS-based configuration memories. To provide individual access, each GMS has its own selection transistor. Thus, the different lines can be shared in a standalone-memory-type architecture, yielding an efficient layout strategy. The different modes and programming signals are selected by line-driving multiplexers.

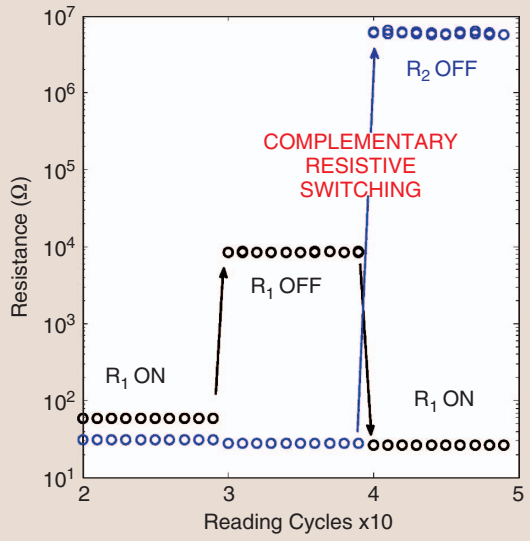


Figure 15. Complementary switching operation for the ReRAM-based GMS.

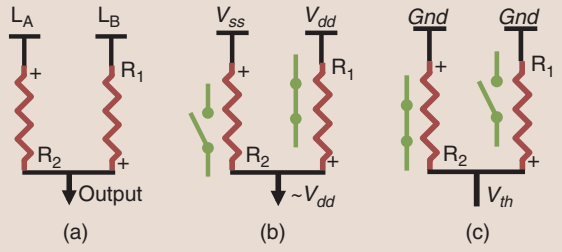


Figure 16. GMS complementary programming: (a) Two in-series connected BRS RAMs forming a voltage divider between 2 metal lines, LA, LB. (b) Voltage distribution to program a logic 1 into the GMS cell. (c) Voltage distribution to program a logic 0 into the GMS cell.

E. Conclusions

This section introduced a novel design, called GMS, based on resistive memories, designed to replace traditional routing resources in reconfigurable logic circuits. Resistive RAM memories combined into a complementary switching GMS cells were used to reduce the footprint and to improve the electrical performances of the data path. The GMS cell can also be used to replace standalone memories, leading to more compact LUTs and steering logic, due to the BEoL integration of ReRAMs.

Thanks to ReRAMs, the area and the delay are reduced by 7% and 58% respectively due to the compactness and the low on-resistance of ReRAMs.

Table 1.
Obtained ReRAM electrical parameters for the different devices.

Device	SET	RESET	HRS	LRS	HRS/LRS	Reading
Planar Pt/TiO_2/Pt	+1.8 V	−1.3 V	10 MΩ	10 Ω	10^5	+1 V
TSV—Pt/TiO_2/Pt	+0.6 V	−0.5 V	2 MΩ	666 Ω	3003	+0.2 V
TSV—Cu/TiO_2/Pt	−4.2 V	+5 V	500 MΩ	5 Ω	10^5	+1 V

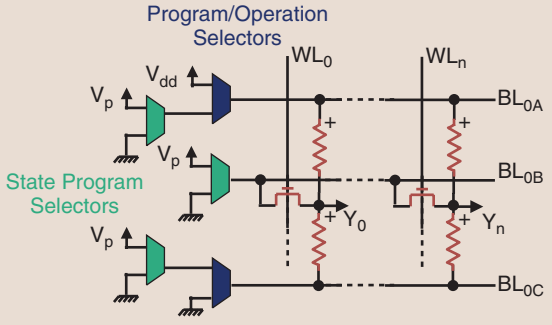


Figure 17. Complementary switching operation for the Re-RAM-based GMS.

IV. Resistive Programmable TSVs

In this section, Back-End-of-the-Line technology for 3D interconnects is addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in *three-dimensional (3D)* wafer/chip stacking solutions utilizing *Through Silicon Vias (TSVs)* [27] as well as in reconfigurable interconnect fabrics. The discussed BEoL demonstrate the co-integration of TSVs with ReRAM stacks, offering a new path for re-programmable 3D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3D chip interconnects. The fabrication and characterization of titanium dioxide (TiO_2)-based *resistive RAM (ReRAM)* co-integration with 380 μm-height Cu *Through Silicon Via (TSV)* arrays for programmable 3D interconnects is discussed. Non-volatile resistive switching of Pt/TiO_2/Pt thin films are first characterized with resistance ratio up to 5 orders of magnitude. Then co-integration of Pt/TiO_2/Pt or Pt/TiO_2 memory cells on 140 μm and 60 μm diameter Cu TSV are fabricated. Repeatable non-volatile bipolar switching of the ReRAM cells are demonstrated for different structures.

A. Fabrication

1) Planar ReRAM Devices

First, high resistivity p-type ($N_A \approx 10^{15}$ atoms/cm^2) bulk-Si wafers are prepared by 500 nm thermal oxidation in H_2O atmosphere. Then the deposition of the resistive switching materials is performed by sputtering of Pt/TiO_2/Pt layers with 270 nm/80 nm/270 nm thicknesses. A conceptual picture is shown in Figure 18(a). The top electrode area of 100 μm by 100 μm squares were patterned by standard lithography and etched by ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

2) TSV Devices

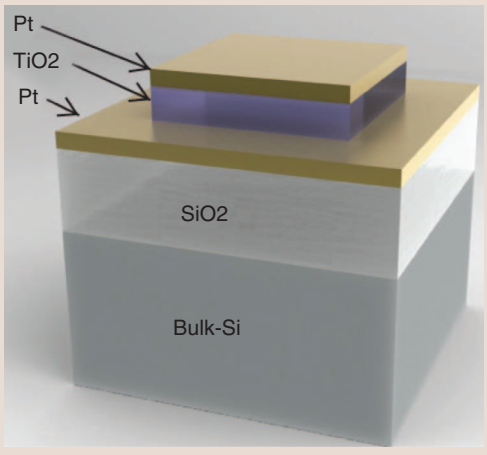
The resistive switching materials were integrated with TSVs producing two different devices:

- 140 μm TSV diameter in 380 μm thick wafer, using Pt/TiO_2/Pt memory stack
- 60 μm TSV diameter in 380 μm thick wafer, using Cu/TiO_2/Pt memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

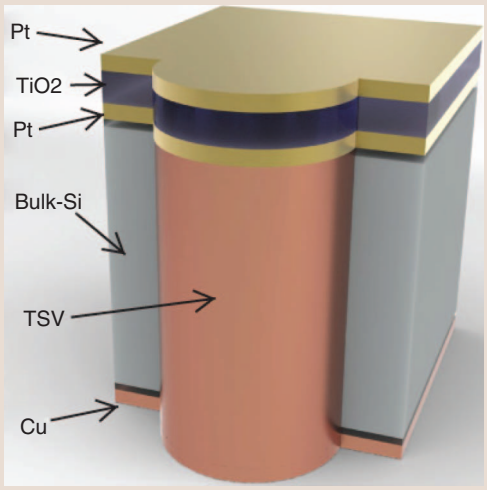
The TSVs are fabricated using the same process in both cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through wafer etch, RCA wafer cleaning and thermal oxidation in water atmosphere to grow a 3 μm thick oxide. A 750 nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

3) TSV with Pt/TiO_2/Pt ReRAM

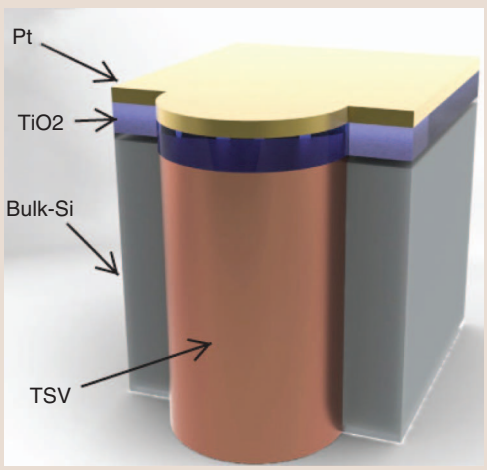
For the first type of devices, once the TSVs are fabricated the front side of the wafer is processed with *Chemical Mechanical Polishing (CMP)* technique to form a flat surface. The Pt/TiO_2/Pt stack is sputtered with layer thicknesses 270 nm/80 nm/270 nm accordingly. A concept picture of the fabricated structure can be seen in Figure 18(b).



(a)



(b)



(c)

Figure 18. (a) Concept image of planar ReRAM made of Pt/TiO_2/Pt stack. (b) Concept image of the ReRAM-TSV using Pt/TiO_2/Pt programmable fuse. (c) Concept image of the ReRAM-TSV using Cu/TiO_2/Pt programmable fuse.

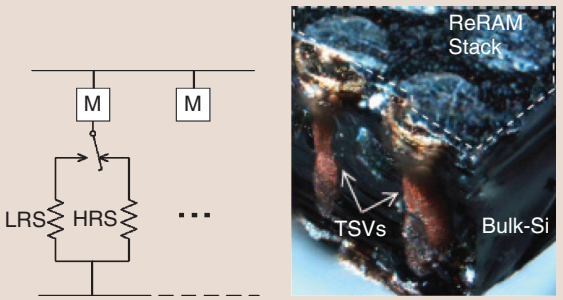


Figure 19. (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element M). (b) Reconstructed 3D photograph of the TSV - Cu/TiO_2/Pt device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

4) TSV with Cu/TiO_2/Pt ReRAM

For the second type of devices the wafer is polished using CMP on both sides to remove the seed layer and to planarize the surfaces. The Cu was then cleaned using an NH_4:H_2SO_4 etching solution at room temperature for 10 minutes. Then the wafer was loaded into a vacuumed sputtering chamber and a TiO_2/Pt layer was deposited with thicknesses of 80 nm and 270 nm respectively. The Cu of the TSV is acting as the bottom electrode of the ReRAM (see Figure 18(c)). Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Figure 19(a) and 19(b), respectively.

B. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station in dark conditions. For electrical contacts, standard tungsten needles with 15 μm apex diameter were placed on the top electrode area very softly, since a dependence of the switching with needle pressure has been observed, similarly to the observation of local pressure modulated conductance with AFM tips [28]. Then double I – V DC sweeps have been used to investigate the resistive switching behavior. In all the cases, bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table 1.

C. Planar ReRAM Devices

First the planar Pt/TiO_2/Pt are characterized and it showed stable and repeatable bipolar switching behavior between 10 Ω and 1 MΩ read or measured at

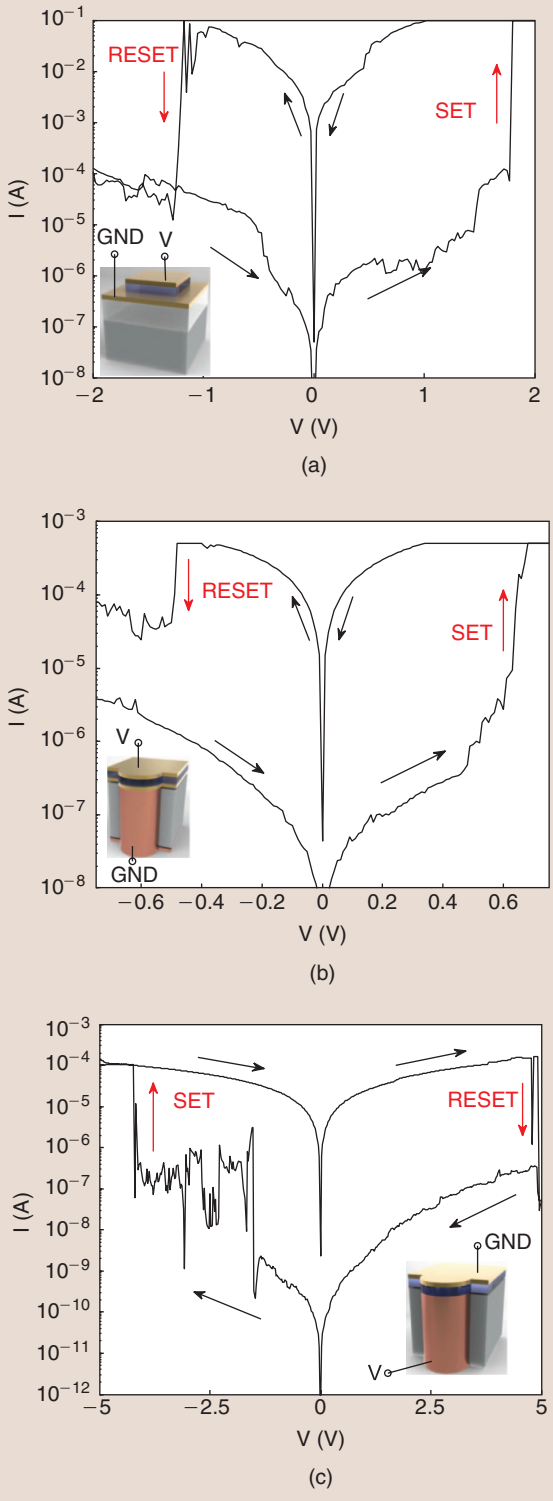


Figure 20. (a) Resistive switching through I – V sweeps for planar Pt/TiO_2/Pt. (b) Resistive switching through I – V sweeps using TSV - Pt/TiO_2/Pt programmable fuse. (c) Resistive switching through I – V sweeps using TSV–Cu/TiO_2/Pt programmable fuse.

+1 V (see Figure 20(a)). Originally the devices are in the high resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low resistance state (LRS) occurs at +1.8 V After the SET event, the voltage sweep continues until +2 V and then move backward toward negative voltage region. When −1.3 V is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about 5 orders of magnitude is read at +0.5 V.

D. TSV—Pt/TiO_2/Pt *Devices*

Next, TSV—Pt/TiO_2/Pt with the same layer thicknesses are measured, showing resistance switching below ±1 V (see Figure 20(b)). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks as well as to surface states acting as dopants for the TiO_2 [29]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only +0.6 V, while the RESET voltage is measured at −0.5 V. Using a reading voltage of +0.2 V, an HRS of 2 MΩ and an LRS of 666 Ω, with resistance ratio of 3000 are measured.

E. TSV—Cu/TiO_2/Pt *Devices*

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the TiO_2 layer [30], [31], that is a n-type semiconductor, an alternative device is obtained by depositing TiO_2 and Pt directly on top of the Cu–TSV. Thus, thanks to a larger Schottky barrier height at the Cu–TiO_2 interface, a larger programming window is obtained (Figure 20(c)). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. An HRS of 500 MΩ and LRS of 5 kΩ are read at +1 V.

F. Conclusion

In this study, Pt/TiO_2/Pt obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with LRS to HRS resistance ratio up to 5 orders of magnitude. The device is successfully integrated on top of 140 μm and 60 μm TSV arrays either in the full Pt/TiO_2/Pt stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The co-integration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3D chip interconnects.

V. Sensing

A. Temperature Sensing with Ambipolar Si Nanowire Transistors

This section reports on the fabrication and characterization of a pA current and temperature sensing device with ultra-low power consumption based on a Schottky barrier silicon nanowire transistor. Thermionic and trap-assisted tunneling current conduction mechanisms are identified and discussed on the base of the device sensitivity upon current and temperature biasing. In particular, very low current sensing properties are confirmed also with previously reported polysilicon-channel nanowire Schottky barrier transistors demonstrating that these devices are suitable for temperature and current sensing applications. Moreover, the process flow compatibility for both sensing and logic applications makes these devices suitable for heterogeneous integration. In this work we extend the application of Si nanowires to temperature sensing. A range of device operation conditions are investigated, showing how an ambipolar device can be used for different applications, the only requirement being the biasing condition.

B. Device Description

The device scheme consists of a suspended Si nanowire having NiSi silicide source/drain junctions with 2 parallel polysilicon gates having gate-all-around (GAA) configuration on an SOI substrate. Typical Si nanowire with drop-like cross-section shape has an average diameter of 100 nm. More details can be found in [14].

C. Device Fabrication

The process flow is based on a previously reported technique utilized for the fabrication of vertically-stacked Si nanowire FET arrays [32]. Here a deep reactive ion etching technique is adapted to form a single suspended Si ribbon over the buried oxide. A sacrificial oxidation is performed to reduce the cross-section down to a 100 nm. Then a 20 nm dry oxidation is performed followed by a 500 nm polysilicon layer deposited by low pressure chemical vapor deposition. Contact regions are etched in a low temperature oxide passivation layer. Then a 50 nm Ni + 10 nm Al bi-layer is evaporated and annealed to form a silicide/Si mid-gap Schottky junction. The Al is used as a cap layer to prevent Ni oxidation during the silicidation step and to provide a good interface with final metallization. Finally, 1 μm thick Al is patterned for electrical characterizations.

D. I-V Dependence

For Schottky barrier FETs, Ids can be described by the sum of a tunneling I_{tunnel} and a thermionic-emission I_{th} component [33]:

$$I_{ds} = I_{th} + I_{tunnel} \tag{1}$$

$$I_{th} = A_C A^* T^2 e^{\left(-\frac{\phi_{Beff}}{kT}\right)} \left\{ e^{\left(-\frac{\phi_{Va}}{kT}\right)} - 1 \right\} \tag{2}$$

$$I_{tunnel} = A_C \frac{q^2 F^2}{8\pi h \phi_{Beff}} e^{\left(-\frac{8\pi}{3hqF}\sqrt{2m(q\phi_{Beff})^3}\right)}, \tag{3}$$

where A_C is the contact area of the source to channel junction, F the electric field across the Schottky barrier, A* the Richardson's constant, h the Planck's constant, m the electron rest mass, q the elementary electron charge, ϕ_{Beff} the effective Schottky barrier height, T the temperature, Va the applied voltage across the Schottky junction, k the Boltzmann's constant.

1) Temperature Dependence

The Ids-Vgs dependence with T is mainly attributed to the I_{th}, however T also influences the I_{tunnel} since hotter carriers pass through a narrower Schottky barrier, leading to an increasing current level [33]. The I_{OFF} current is increasing exponentially with temperature and, as suggested by Eq. 2, its main contribution is a thermionic emission component. A different behavior has been observed for the I_{ON} current. Increasing the temperature makes the I_{ON} current to decrease until the temperature reaches 55 °C and then it rise exponentially with linear increase of T. At lower temperatures tunneling and trap-assisted tunneling are more important than thermionic emission. Rising T up to 70 °C makes the charges trapped into the gate oxide to un-trap, reducing the I_{tunnel} component. A different behavior is observed for the I_{ON} currents for 70 °C ≤ T ≤ 115 °C. In this range, the I_{ON} exponentially increases with T. This effect is evidence of two main current components, for which the I_{ON} changes from a tunneling to a thermionic emission dominated regime. A set of $I_{ds} - V_{ds}$ curves (Fig. 21(a)) taken at different temperatures at constant V_{ds} = 100 mV and V_{bg} = 5 V are used to extrapolate the Arrhenius plot shown in Fig. 22(a). The constant V_{bg} = 5 V is used to set the device operation more favorable for electron conductance at low Vgs. Constant subthreshold swings ≈ 110 mV/dec are observed independently from the temperature (see Fig. 21(b)). Low negative Vgs voltages ranging from −1 V to 0 V show an almost linear slope with inverse of temperature and can be correlated to a thermionic-emission regime. However, for this Vgs range the current level is on the order of fAs, which is comparable to the background noise, and it cannot be used to extrapolate the Schottky barrier height. Another

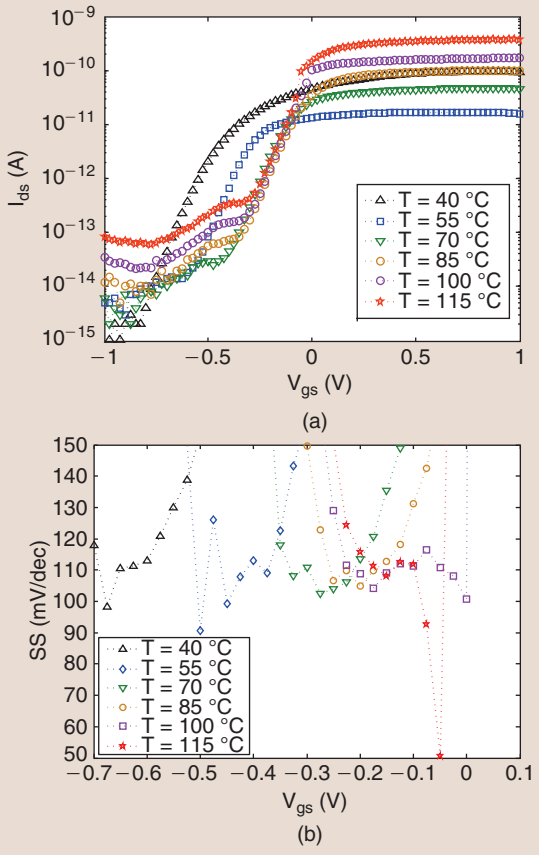


Figure 21. (a) Effect of the temperature on the ambipolar $I_{ds}V_{gs}$ at $V_{ds} = 100$ mV. (b) Subthreshold swings associated with the $I_{ds}V_{gs}$ plots. Very low swing minima are measured at 100 °C and 100 °C close to threshold voltages. Notice the voltage shift with temperature increase and the extremely low minima of 50 mV/dec for the highest temperature.

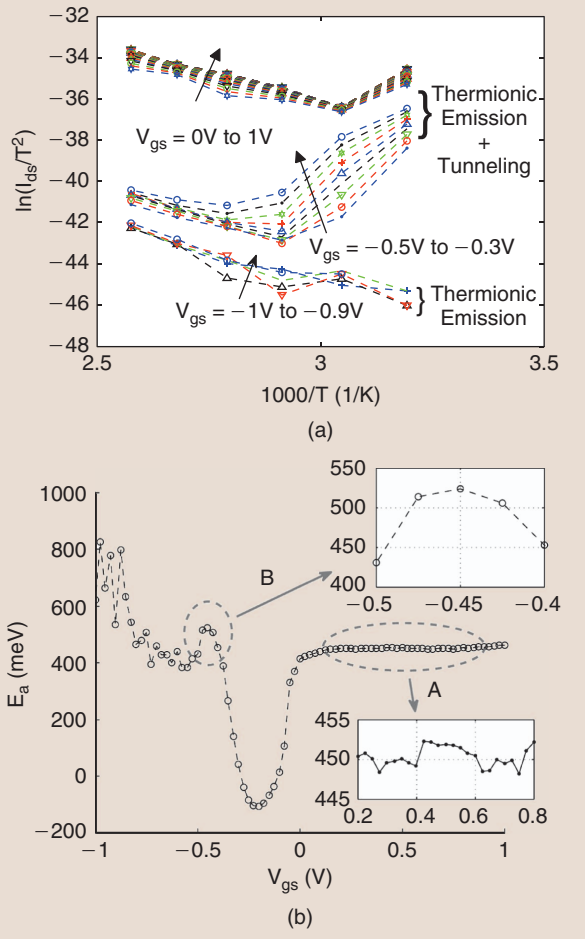


Figure 22. (a) Arrhenius plot for different V_{gs} extracted from the plots of Fig. 21(b) showing both thermionic emission and tunneling mechanisms. The linear decreasing slopes are associated with thermionic emission regimes. (b) Extracted E_a over a large range of V_{gs}. The inset A shows a constant $E_a = 450 \pm 5$ meV over $-0.2\,V \leq V_{gs} \leq -0.8\,V$. Inset B shows the maximum of $E_a = 525$ meV which is associated to the ϕ_{Beff}.

distinct regime is observed for $-0.3\,V \leq Vgs \leq -0.5\,V$, for which the slopes are greatly affected by tunneling. This regime shows a dominant tunneling component for the two lowest temperatures. Finally, an exponential dependence with T is observed again for $V_{gs} \geq 0$ V with the exception of the lower temperature. All these regimes demonstrate that the current in our device is mainly thermionic for $T \geq 70\,°C$ and that the tunneling contribution is trap assisted. The slopes from the Arrhenius plot are then used to extract the effective Schottky barrier height ϕ_{Beff} with the activation energy E_a method. As shown in inset A of Fig. 22(b), an average effective barrier height $E_a \approx 450 \pm 5$ meV is found over a large range of $V_{gs} \geq 0.2$ V. However, these values cannot be taken as Schottky barrier height since in this regime the device has both tunneling and thermionic components. As suggested by Svensson et al. [34], a better evaluation of the Schottky barrier height can be taken at the maximum of E_a for low current levels. As shown in the inset B of Fig. 22(b), this maximum corresponds to $V_{gs} = -0.45$ V and gives a $\phi_{Beff} = 525$ meV, confirming the mid-gap Schottky barrier height.

2) Current Sensing

Current biasing the devices with a constant Ids current makes the device to behave as a pseudo-inverter configuration with hysteretic transfer function. Thanks to the ambipolarity, the $V_{out} - V_{in}$ curves shift linearly with the applied current bias. For instance in Fig. 23(a), low pA current levels can be either read from the high-to-low or the low-to-high transition voltage with sensitivities of 17 mV/pA. A similar biasing scheme for polysilicon nanowires has been previously characterized by the authors show a similar trend. In Fig. 23(b), forward and

reverse threshold voltages for currents between 100 fA and 500 fA show a linear increase with current.

3) Temperature Sensing

Upon application of increasing temperature of operation, the hysteresis window observed in pseudo-inverter biasing scheme shrinks. The crystalline Si nanowire Schottky barrier FET shows different sensitivities at different temperature regimes, depending on which mechanism dominates the conductance. Since the hysteresis is attributed to the storage of charges in either gate oxide and/or at the Schottky barrier junctions [35], an increased hysteresis window is expected for the lowest temperatures. The highest sensitivity of 40 mV/°C is found in the T range around 40 °C at which the trap tunneling mechanisms dominates. For temperatures higher than 55 °C the sensitivity tends to saturate according to the dominance of thermionic current contribution, leading to lower sensitivity of 10 mV/°C. In Fig. 23(c) the hysteresis window shrink for increasing T when 70 °C ≤ T ≤ 100 °C is shown.

E. Bio-Sensing with Memristive Ambipolar Si Nanowires

1) Introduction

Recently, there has been an increasing interest in nano-bio-sensing applications, due to possibility for minimal invasive, real-time monitoring for preventive treatments and therapy personalization [37]. In particular, one-dimensional silicon nanowires are good candidates for sensing devices due to their very large surface-to-volume ratio and quantum properties [38]. However, the sensing with nanowires is only exploited by the ion-sensitive field-effect-transistor paradigm [39]. Due to the nanoscale of the fabricated geometries [40], the recent discovery in solid-state devices of the memristive effect has been source of renewed research efforts in applications for high-density memory device [1]. The physical phenomena governing the memristive behavior are attributed to the change of an internal state variable, which modifies the conductance in a non-volatile manner [8]. As reported by Duan et al., memory devices are possible also with molecule-gated nanowire transistors by using redox active molecules [10]. In this section, we report the first evidence of unexpected new insights for a novel molecular sensing in dry conditions based on nanofabricated memristors functionalized with bio-molecular thin films.

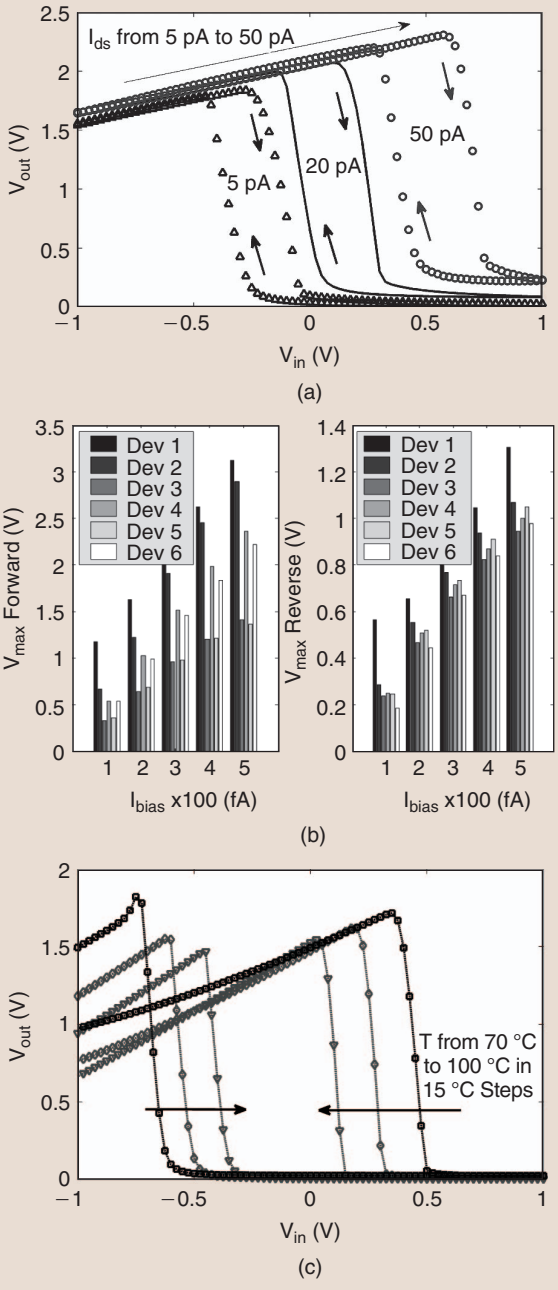


Figure 23. (a) Measured input-output transfer characteristics of a hysteretic inverter based on a single Si nanowire FET with low current bias, showing current-dependent thresholds. (b) Forward and reverse threshold voltages for polysilicon Schottky barrier FETs under constant current biasing from 100 fA up to 500 fA (adapted from ref. [36]). (c) The hysteresis window shrinks with increasing temperature. Within this T range, the temperature sensitivity of 10 mV/°C is related with the thermionic current regime.

F. Device Nano-Fabrication

The fabrication method utilizes some of the steps that were previously reported [35] for memristive Schottky-barrier silicon nanowire field-effect-transistors. The process starts from low resistivity Silicon-On-Insulator substrates, with 1.5 μm device layer and 3 μm SiO_2 insulating layer. After standard lithography, the silicon nanowire is carved anchored at the top of two silicon pillars. Then,

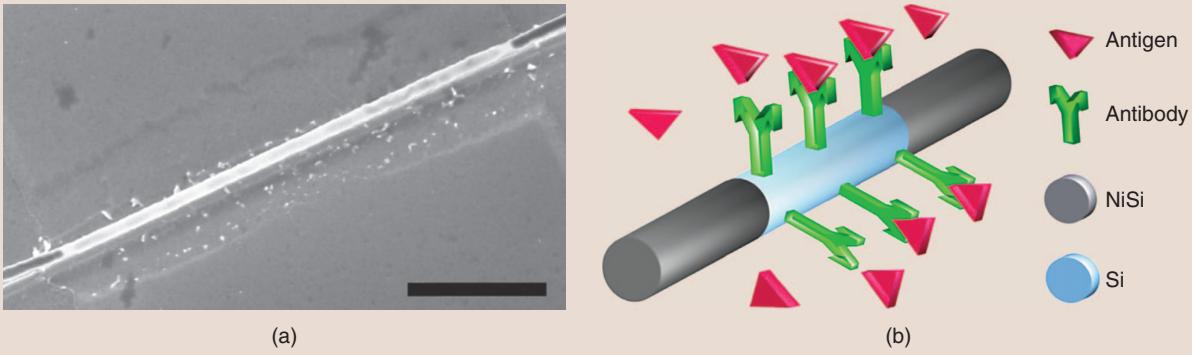


Figure 24. (a) Suspended functionalized silicon nanowire with NiSi extremities. Scale bar is 4 μm. (b) Concept model.

Ni is deposited on top of the pillars with overlap on the outer portions of the silicon nanowire. Hence, an annealing step at 450 °C in a horizontal wall furnace forms NiSi contacts. Figure 24(a) shows a nano-fabricated memristive silicon nanowire with NiSi contacts.

G. Biomolecule Self-Assembly

The silicon nanowire surface was derivatised with 3-glycidoxypropyltrimethoxysilane GPTS [41] and functionalized by covalent attachment of anti-rabbit polyclonal antibodies (AB) [42]. Antigen (rabbit antibodies, AG) interact with the functionalized wire as depicted in Figure 24(b).

H. Results and Discussion

Electrical measurements are carried out in a shielded probe station connected with HP4615C Semiconductor Parameter Analyzer and in dark, to avoid any photo-generated currents. Before functionalization with the AB layer, $I_{ds} - V_{ds}$ curves taken for forward and backward sweep do show a typical memristive behavior (see Figure 25(a)), where the current minima always occur for $V_{ds} = 0$ V; consistently with previously reported measurements [35] on non-functionalized devices. Conversely, functionalized silicon nanowires show different positions of the current minima for backward or forward regimes. This effect is observed after drying from: (a) de-ionized H_2O solution and (b) 5 pM AG solution. The $I_{ds} - V_{ds}$ curve before AG up-take shows an hysteresis (curve (1) in Figure 25(b)) due to charge trapping mechanisms at the Schottky junctions. The binding of an AG with the functionalized wire is responsible for a modification of the hysteresis (curve (2) in Figure 25(b)), in particular to a reduction of the current minimum gap between forward and backward V_{ds} sweeps. Coherently, the up-take of increasing amounts of AG (in the pM range) results on a further diminishing of this gap.

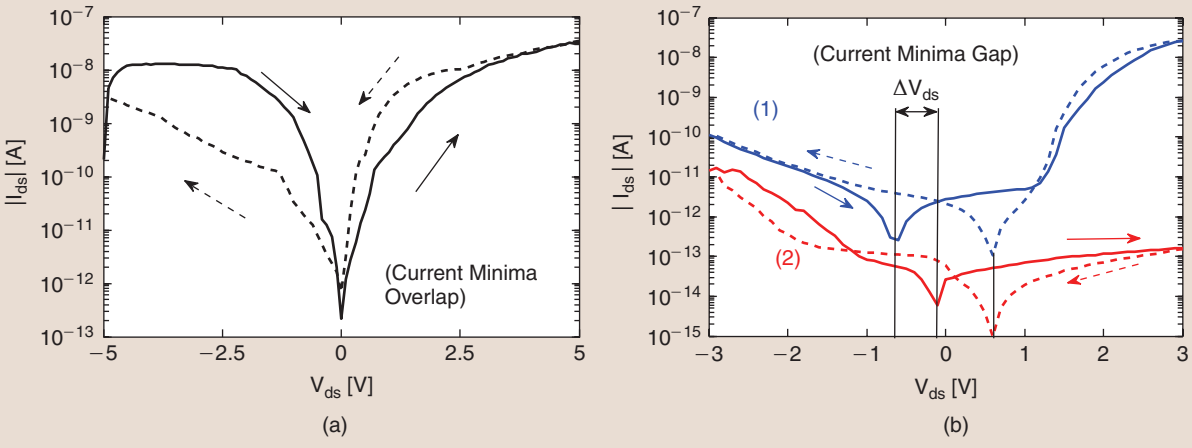


Figure 25. $I_{ds} - V_{ds}$ curves: (a) before functionalization with AB bio-layer. A typical memristive hysteresis is observed, with no ΔV_{ds} gap between I_{ds} minima in forward and backward regimes; (b) the blue curve (1) is measured after drying the sample from de-ionized water. The red curve (2) is measured after dipping in 5 pM AG solution and drying.

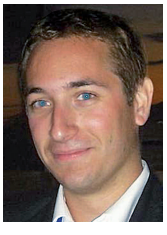
VI. Conclusions

Several applications of two-terminals and multi-terminal memristive devices are discussed. Specifically, fabrication of resistive RAM memories have been presented for their potential for standalone memories. The resistive RAM can also be exploited for increased FPGA functionality, such as lookup tables, datapath routing. In here we propose the use of a generic memory structure to replace the pass-transistor in SRAM-based FPGAs. Another application envisages the use of ReRAM on top of Through Silicon Via for fully-3D programmable interconnects. A low thermal budget fabrication scheme of resistive programmable TSV has been developed and discussed. In the last sections of this work, three-terminal memristive SiNW devices are exploited for sensing physical and biological quantities. Moreover, an innovative device exploiting the hysteresis of functionalized Si nanowires is a first-time approach for bio-sensing in a controlled dry environment.

Acknowledgment

The authors would like to thank Dr. Haykel Ben-Jamaa of CEA/LETI and Dr. Veronica Savu for useful discussions. The authors would also like to thank F. Puppo for her help with the bio-memristive nanowires. Moreover, the authors thank the CMI staff of EPFL for help with the fabrication. This work has been partially supported by the Swiss NSF Grant No 200021-122168, Swiss NSF Grant No 200021-132539, Nano-Tera Grant No 20NA21-128841, Nano-Tera Grant No 20NA21-128840 and grant ERC-2009-AdG-246810.

Davide Sacchetto received the B.S. degree in physics engineering from Politecnico di Torino (Italy) in 2007. In 2008 he received the jointed M.S. degree in Micro and Nano Technologies for Integrated Systems from Ecole Polytechnique Federale de Lausanne, the Institut National Polytechnique de Grenoble and the Politecnico di Torino. Since November 2008 he is working as a Ph.D. student at the Microelectronic System Laboratory (LSM) and the Integrated System Laboratory (LSI), EPFL. His research interests focus on novel devices, investigating issues ranging from solid-state microfabrication to circuit implementation.



Pierre-Emmanuel Gaillardon (S10M11) works for EPFL, Switzerland, as a research associate at the Laboratory of Integrated Systems (LSI). He holds an Electrical Engineer degree (CPE-Lyon, France, 2008), an M.Sc. degree (INSA Lyon, France, 2008) and a Ph.D. in Electrical Engineering (University of Lyon, France, 2011). Previously, he was research assistant at CEA-LETI. Involved in the Nanosys project, the research activities and interests of Dr. Gaillardon are currently focused on digital architecture design based on emerging devices. He is recipient of the C-Innov 2011 best thesis award and the Nanoarch 2012 best paper award. He has been serving as TPC member for Nanoarch 2012, 2013 conferences and is reviewer for several journals (IEEE TNANO, IEEE TVLSI), conferences (ICECS 2012, ISCAS 2013) and funding agencies (ANR).

Michael Zervas received his diploma (B.S. and M.S. degree in applied mathematics and applied physics from Athens Technical University, Athens, Greece in 2005), and the M.Sc. degree in Micro and Nano technologies for Integrated Systems, joint Master's degree awarded by Ecole Polytechnique Federale de Lausanne (EPFL), Institut National Polytechnique de Grenoble (ENSERG/MINATEC) and Politecnico di Torino in 2007. From 2007 till 2010 he has been working with Oerlikon first as management trainee and later as strategic procurement manger located in Singapore for Oerlikon Solar (2 years). As a procurement manager he help setup and was team leader of the procurement team in Asia from 2008 till 2010 (Distributed team in Korea, Japan, Taiwan, Singapore). In 2013 he received his Ph.D. degree in the Department of Electrical Engineering, EPFL, Lausanne, Switzerland, under the supervision of Prof. Leblebici. His research interests include micro/nanointegration techniques, micro fabrication and physical modeling of sensors based on nanowires as well as heterogeneous integration methods such as TSV.

Sandro Carrara is a lecturer and scientist at the EPFL in Lausanne (Switzerland). He is a former professor of optical and electrical biosensors at the Department of Electrical Engineering and Biophysics (DIBE) of the University of Genoa (Italy) and a former professor of nanobiotechnology at the University of Bologna (Italy). He is founder and Editor-in-Chief of the journal *BioNanoScience* by Springer, Topical Editor of the *IEEE Sensors Journal*, and Associate Editor of *IEEE Transactions on Biomedical Circuits and Systems*. He is an IEEE member for the Circuit and System Society (CASS) and member of the Board of Governors of the IEEE Sensors Council. He also has been recently appointed as CASS Distinguished Lecturers for the years 2013–2014. His scientific interests are on electrical phenomena of

nano-bio-structured films, and include CMOS design of biochips based on proteins and DNA. He has more than 130 scientific publications and 10 patents. He has several Top-25 Hottest-Articles (2004, 2005, 2008, 2009, and two times in 2012) published in highly ranked international journals such as *Biosensors and Bioelectronics*, *Sensors and Actuators B*, *IEEE Sensors* journal, and *Thin Solid Films*. His work received a NATO Advanced Research Award in 1996 for the original contribution to the physics of single-electron conductivity in nano-particles, two Best Paper Awards at the IEEE PRIME Conference in 2010 (Berlin), and in 2009 (Cork), a Best Poster Award at the Nanotera workshop in 2011 (Bern), and a Best Poster Award at the NanoEurope Symposium in 2009 (Rapperswil). He also received the Best Referees Award from the journal *Biosensor and Bioelectronics* in 2006. From 1997 to 2000, he was a member of an international committee at the ELETTRA Synchrotron in Trieste. From 2000 to 2003, he was scientific leader of a National Research Program (PNR) in the field of Nanobiotechnology. He is now an internationally esteemed expert of the evaluation panel of the Academy of Finland in a research program for the years 2010-2013. He will be the General Chairman of the Conference BioCAS, edition 2014.

Giovanni De Micheli is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He is program leader of the Nano-Tera.ch program. Previously, he was Professor of Electrical Engineering at Stanford University. He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), an M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983). Prof. De Micheli is a Fellow of ACM and IEEE and a member of the Academia Europaea. His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies, networks on chips and 3D integration. He is also interested in heterogeneous platform design including electrical components and biosensors, as well as in data processing of biomedical information. He is author of: *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994, coauthor and/or coeditor of eight other books and of over 500 technical articles. His citation h-index is 76 according to Google Scholar. He is member of the Scientific Advisory Board of IMEC and STMicroelectronics. Prof. De Micheli is the recipient of the 2012 IEEE/CAS Mac Van Valkenburg award for contributions to theory, practice and experimentation in design methods and tools and of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He received also the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000, the D. Pederson Award for the best paper on the IEEE Transactions on CAD/ICAS in 1987, and several Best Paper Awards, including DAC (1983 and 1993), DATE (2005) and Nanoarch (2010 and 2012). He has been serving IEEE in several capacities, namely: Division 1 Director (2008-9), cofounder and President Elect of the IEEE Council on EDA (2005-7), President of the IEEE CAS Society (2003), Editor in Chief of the *IEEE Transactions on CAD/ICAS* (1997-2001). He has been Chair of several conferences, including DATE (2010), pHealth (2006), VLSI SOC (2006), DAC (2000) and ICCD (1989).

Yusuf Leblebici received his B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, in 1984 and in 1986, respectively, and his Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1990. Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000-2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, Dr. Leblebici has been a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the coauthor of 6 textbooks, namely, *Hot-Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers, 1993), *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications* (Springer, 2007), *Fundamentals of High Frequency CMOS Analog Integrated Circuits* (Cambridge University Press, 2009), *Extreme Low-Power Mixed Signal IC Design* (Springer, 2010) and *Reliability of Nanoscale Circuits and Systems* (Springer, 2011), as well as more than 250 articles published in various journals and conferences. He has served as an Associate Editor of *IEEE Transactions on Circuits and Systems (II)*, and *IEEE Transactions on Very Large Scale Integrated (VLSI) Systems*. He has also served as the general cochair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference (ESSCIRC/ESSDERC). He is a Fellow of IEEE and has

been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010-2011.

References

[1] S. H. Jo, K. Kim, and W. Lu, "High-density crossbar arrays based on a Si memristive system," *Nano Lett.*, vol. 9, pp. 870–874, Feb. 2009.

[2] D. B. Strukov and K. K. Likharev. (2005). CMOL FPGA: A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices. *Nanotechnology* [Online]. *16(6)*, p. 888. Available: http://stacks.iop.org/0957-4484/16/i=6/a=045

[3] D. Sacchetto, M. Zervas, Y. Temiz, G. De Micheli, and Y. Leblebici, "Resistive programmable through silicon vias for reconfigurable 3D fabrics," *IEEE Trans. Nanotechnol.*, vol. 11, no. 1, pp. 8–11, Jan. 2012.

[4] P.-E. Gaillardon, D. Sacchetto, S. Bobba, Y. Leblebici, and G. De Micheli, "GMS: Generic memristive structure for non-volatile FPGAs," in *Proc. 2012 IEEE/IFIP 20th Int. Conf. VLSI and System-on-Chip (VLSI-SoC)*, pp. 94–98.

[5] J. Borghetti, Z. Li, J. Straznicky, X. Li, D. A. A. Ohlberg, W. Wu, D. R. Stewart, and R. S. Williams, "A hybrid nanomemristor/transistor logic circuit capable of self-programming," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 106, pp. 1699–1703, Feb. 2009.

[6] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, pp. 873–876, Apr. 2010.

[7] L. Chua, "Memristors: A new nanoscale CNN cell," in *Cellular Nanoscale Sensory Wave Computing.* New York: Springer-Verlag, 2010, pp. 87–115.

[8] L. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.

[9] Y. V. Pershin and M. D. Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Netw.*, vol. 23, no. 7, pp. 881–886, 2010.

[10] X. Duan, Y. Huang, and C. M. Lieber. (2002). Nonvolatile memory and programmable logic from molecule-gated nanowires. *Nano Lett.* [Online]. *2(5)*, pp. 487–490. Available: http://pubs.acs.org/doi/abs/10.1021/nl025532n

[11] X. Wang, Y. Chen, Y. Gu, and H. Li, "Spintronic memristor temperature sensor," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 20–22, Jan. 2010.

[12] T. Sakamoto, N. Banno, N. Iguchi, H. Kawaura, S. Kaeriyama, M. Mizuno, K. Terabe, T. Hasegawa, and M. Aono, "Three terminal solid-electrolyte nanometer switch," in *IEDM Tech. Dig.*, Dec. 2005, pp. 475–478.

[13] D. Sacchetto, M.-A. Doucey, G. De Micheli, Y. Leblebici, and S. Carrara. (2011). New insight on bio-sensing by nano-fabricated memristors. *Bionanoscience* [Online]. *1*, pp. 1–3. Available: http://dx.doi.org/10.1007/s12668-011-0002-9

[14] D. Sacchetto, G. De Micheli, and Y. Leblebici, "Ambipolar Si nanowire field effect transistors for low current and temperature sensing," in *Proc. 16th Int. Conf. Solid-State Sensors, Actuators and Microsystems*, 2011.

[15] S. Ecoffey, M. Mazza, V. Pott, D. Bouvet, A. Schmid, Y. Leblebici, M. Declereq, and A. Ionescu, "A new logic family based on hybrid MOSFET-polysilicon nanowires," in *IEDM Tech. Dig.*, Dec. 2005, pp. 269–272.

[16] S. Ecoffey. (2007). Ultra-thin nanograin polysilicon devices for hybrid CMOS-NANO integrated circuits. Ph.D. dissertation [Online]. Available: http://library.epfl.ch/theses/?nr=3722

[17] V. Zhirnov, R. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Brauhaus, C. Schindler, and R. Waser, "Memory devices: Energy-space-time tradeoffs," *Proc. IEEE*, vol. 98, no. 12, pp. 2185–2200, 2010.

[18] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, "Highly reliable TaOx ReRAM and direct evidence of redox reaction mechanism," in *Proc. IEEE Int. Electron Devices Meeting, 2008*, pp. 1–4.

[19] F. Miao, W. Yi, I. Goldfarb, J. J. Yang, M.-X. Zhang, M. D. Pickett, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams. (2012). Continuous electrical tuning of the chemical composition of taox-based memristors. *ACS Nano* [Online]. *6(3)*, pp. 2312–2318. Available: http://pubs.acs.org/doi/abs/10.1021/nn2044577

[20] S.-S. Sheu, M.-F. Chang, K.-F. Lin, C.-W. Wu, Y.-S. Chen, P.-F. Chiu, C.-C. Kuo, Y.-S. Yang, P.-C. Chiang, W.-P. Lin, C.-H. Lin, H.-Y. Lee, P.-Y. Gu, S.-M. Wang, F. Chen, K.-L. Su, C.-H. Lien, K.-H. Cheng, H.-T. Wu, T.-K. Ku, M.-J. Kao, and M.-J. Tsai, "A 4 Mb embedded SLC resistive-ram macro with 7.2 ns read-write random-access time and 160 ns MLC-access capability," in *2011 IEEE Int. Solid-State Circuits Conf. Digest Tech. Papers (ISSCC)*, pp. 200–202.

[21] M. Lin, A. El Gamal, Y.-C. Lu, and S. Wong. Performance benefits of monolithically stacked 3D-FPGA. presented at 2006 ACM/SIGDA 14th Int. Symp. Field Programmable Gate Arrays. [Online]. Available: http://doi.acm.org/10.1145/1117201.1117219

[22] V. Betz, J. Rose, and A. Marquardt, Eds., *Architecture and CAD for Deep-Submicron FPGAs*. Norwell, MA: Kluwer, 1999.

[23] K. J. Han, N. Chan, S. Kim, B. Leung, V. Hecht, B. Cronquist, D. Shum, A. Tilke, L. Pescini, M. Stiftinger, and R. Kakoschke, "Flash-based field programmable gate array technology with deep trench isolation," in *Proc. IEEE Custom Integrated Circuits Conf. 2007 (CICC'07)*, pp. 89–91.

[24] Y. Y. Liauw, Z. Zhang, W. Kim, A. Gamal, and S. Wong, "Nonvolatile 3D-FPGA with monolithically stacked RRAM-based configuration memory," in *2012 IEEE Int. Solid-State Circuits Conf. Digest Tech. Papers (ISSCC)*, pp. 406–408.

[25] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nat. Mater.*, vol. 9, no. 5, pp. 403–406, 2010.

[26] Y. Chen, H. Lee, P. Chen, C. Tsai, P. Gu, T. Wu, K. Tsai, S. Sheu, W. Lin, C. Lin, et al., "Challenges and opportunities for HfOX based resistive random access memory," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2011, vol. 31, pp. 1–31.

[27] [Online]. Available: http://www.itrs.net

[28] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nat. Nanotechnol.*, vol. 3, no. 7, pp. 429–433, July 2008.

[29] U. Diebold, "The surface science of titanium dioxide," *Surf. Sci. Rep.*, vol. 48, nos. 5–8, pp. 53–229, 2003.

[30] H. Y. Jeong, J. Y. Lee, and S.-Y. Choi, "Interface-engineered amorphous TiO2-based resistive memory devices," *Adv. Funct. Mater.*, vol. 20, no. 22, pp. 3912–3917, 2010.

[31] W.-G. Kim and S.-W. Rhee, "Effect of the top electrode material on the resistive switching of TiO2 thin film," *Microelectron. Eng.*, vol. 87, no. 2, pp. 98–103, 2010.

[32] D. Sacchetto, M. Ben-Jamaa, G. De Micheli, and Y. Leblebici, "Fabrication and characterization of vertically stacked gate-all-around Si nanowire FET arrays," in *Proc. European Solid State Device Research Conf., 2009 (ESSDERC'09)*, pp. 245–248.

[33] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ: Wiley, 2007.

[34] J. Svensson, A. A. Sourab, Y. Tarakanov, D. S. Lee, S. J. Park, S. J. Baek, Y. W. Park, and E. E. Campbell, "The dependence of the Schottky barrier height on carbon nanotube diameter for Pd–carbon nanotube contacts," *Nanotechnology*, vol. 20, no. 17, p. 175204, 2009.

[35] D. Sacchetto, M. Ben-Jamaa, S. Carrara, G. De Micheli, and Y. Leblebici, "Memristive devices fabricated with silicon nanowire Schottky barrier transistors," in *Proc. 2010 IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 9–12.

[36] D. Sacchetto, V. Savu, G. D. Micheli, J. Brugger, and Y. Leblebici, "Ambipolar silicon nanowire FETs with stenciled-deposited metal gate," *Microelectronic Engineering*, vol. 88, no. 8, pp. 2732–2735, 2011.

[37] S. Carrara, Ed., *Nano-Bio-Sensing.* New York: Springer-Verlag, 2010.

[38] F. Patolsky, G. Zheng, and C. M. Lieber, "Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species," *Nat. Protocols*, vol. 1, no. 4, pp. 1711–1724, Nov. 2006.

[39] G. Zheng, F. Patolsky, Y. Cui, W. Wang, and C. Lieber, "Multiplexed electrical detection of cancer markers with nanowire sensor arrays," *Nat. Biotechnol.*, vol. 23, no. 10, pp. 1294–1301, Oct. 2005.

[40] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, 2008.

[41] D. Kim, H. G. Lee, H. Jung, and S. H. Kang, "Single-protein molecular interactions on polymer-modified glass substrates for nanoarray chip application using dual-color TIRFM," *Bull. Korean Chem. Soc.*, vol. 28, no. 5, pp. 783–790, May 2007.

[42] W. Kusnezow, A. Jacob, A. Walijew, F. Diehl, and J. Hoheisel, "Antibody microarrays: An evaluation of production parameters," *Proteomics*, vol. 3, no. 3, pp. 254–264, Mar. 2003.