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Design methodology for ultra low-power analog circuits using next generation BSIM6 MOSFET compact model ☆

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ABSTRACT

The recently proposed BSIM6 bulk MOSFET compact model is set to replace the hitherto widely used BSIM3 and BSIM4 models as the de-facto industrial standard. Unlike its predecessors which were threshold voltage based, the BSIM6 core is charge based and thus physically continuous at all levels of inversion from linear operation to saturation. Hence, it lends itself conveniently for the use of a design methodology suited for low-power analog circuit design based on the inversion coefficient (*IC*) that has been extensively used in conjugation with the EKV model and allows to make simple calculations of, for example, transconductance efficiency, gain bandwidth product, etc. This methodology helps to make a near-optimal selection of transistor dimensions and operating points even in moderate and weak inversion regions. This paper will discuss the *IC* based design methodology and its application to the next generation BSIM6 compact MOSFET model.

1. Introduction

Analog circuit design is a complex exercise involving multiple tradeoffs, e.g. between power consumption and speed, and several degrees of freedom like the drain current and transistor dimensions. Design with advanced deep-submicron technology nodes is further complicated because of the short-channel effects [1]. The importance of accurate device models which stems from the fact that analog design has special modeling needs has long been recognized [2], and is all the more emphasized with the aggressive scaling of the CMOS technology and the short-channel effects becoming dominant.

The requirement that a model be accurate as well as computationally fast makes the development of advanced compact models quite complex. The modern circuit simulators coupled with sophisticated compact models are powerful tools for the design and analysis of circuits with advanced technology nodes, yet most experienced analog designers would still rely on their design intuition and do 'hand calculations' before performing any simulation. For this pre-simulation phase the designer should be able to use a stripped-down version of the model which is simple enough for initial design guidance, yet accurate enough to minimize trial-and-error simulations.

The new BSIM6 bulk MOSFET model scores on all these fronts. Adopting a charge based approach, it is more physics oriented; it is not only more accurate than its predecessors but can also be faster than the surface potential based models [3,4]. Even though the full compact model includes most of the real-device effects that are present in the advanced bulk CMOS technologies, the core model is based on simple analytical equations which are continuous in all regions of operation. This exempts the designer to use asymptotic approximations that may be valid in weak and strong inversion regions but are inaccurate in moderate inversion (the preferred operating region for low-power analog and RF circuits [5]) and do not account for short-channel effects.

The charge based BSIM6 model would extend elegantly to the existing design methodologies too. The inversion coefficient (IC) based design methodology [6] that has been extensively used in conjugation with the charge based EKV model [7] for the design of low power analog and RF circuits [8,5] can now also be used with the new BSIM6 model. It will be shown in Section 2 that the charge based model allows for a simple expression of the transconductance efficiency G_m/I_D, that is valid at all levels of inversion and accounts for velocity saturation (VS) and mobility reduction due to vertical field (MRVF).

2. Charge based analysis

2.1. Drain current and transconductance

The basic charge equation in a MOSFET is given by [7]

$$2q_i + \ln q_i = \upsilon_p - \upsilon. \tag{1}$$

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where q_i is the normalized inversion charge density ($q_i = Q_i/Q_{spec}$), normalized using specific charge Q_{spec}

$$Q_{spec} \triangleq -2nU_T C_{ox}. \tag{2}$$

υ_p and υ are the pinch-off and channel voltages respectively, normalized to the thermal voltage $U_T(\triangleq kT/q)$. The normalized drain current, normalized using the specific current I_{spec} [7]

$$I_{spec} = I_{spec_\square}\frac{W}{L} \quad \text{with} \tag{3a}$$

$$I_{spec_\square} \triangleq 2n\mu_0 C_{ox} U_T^2 \tag{3b}$$

where μ_0 is the constant low-field mobility, is given by [9]

$$i_d = 2q_i\frac{ue}{\lambda_c} - u\frac{dq_i}{d\xi}. \tag{4}$$

In (4) u is the effective mobility normalized to the low-field surface mobility μ_0, e is the longitudinal electric field normalized to the critical electric field E_c and λ_c is defined as

$$\lambda_c \triangleq \frac{2U_T}{E_c L} = \frac{2\mu_0 U_T}{\upsilon_{sat} L} \tag{5}$$

where υ_{sat} is the saturation velocity.

The normalized source transconductance

$$g_{ms} = \frac{G_{ms}}{G_{spec}} = \frac{nG_m}{G_{spec}}\bigg|_{saturation} \quad \text{with} \tag{6}$$

$$G_{spec} \triangleq \frac{I_{spec}}{U_T} \tag{7}$$

and G_m and n being the total gate transconductance and the slope factor, respectively, can then be calculated as

$$g_{ms} \triangleq -\frac{\partial i_d}{\partial q_s}\frac{\partial q_s}{\partial \upsilon_s}, \tag{8}$$

q_s being the value of q_i at the source.

2.2. Inversion coefficient

The inversion coefficient IC is the measure of the level of channel inversion and is equal to the drain current in forward saturation:

$$IC \triangleq \frac{I_D}{I_{spec}} = i_d\bigg|_{saturation} = i_{dsat}. \tag{9}$$

The different regions of operation in saturation can then be defined as

$IC \le 0.1$ weak inversion
$0.1 < IC \le 10$ moderate inversion
$10 < IC$ strong inversion.

2.3. Short channel effects

As discussed in Section 1, the short-channel effects become prominent at sub-micron channel lengths. Two of the especially important effects are drain induced barrier lowering (DIBL) and velocity saturation (VS). While DIBL pertains to weak inversion, velocity saturation is dominant at higher values of IC. In addition, there is mobility reduction due to the vertical field (MRVF). To maintain sufficient accuracy these effects should be accounted for even in the simplistic model for hand calculations. Both velocity saturation and mobility reduction due to vertical field are related to the mobility of the carriers and affect not only the magnitude but also the slopes of I_D vs. V_G and G_m/I_D vs. IC curves [7].

To include the velocity saturation effect we choose the simple piecewise linear velocity-field model for its simplicity [7], which gives the normalized effective mobility as

$$u_{eff} \triangleq \frac{\mu_{eff}}{\mu_z} = \begin{cases} 1 & \text{for } e < 1 \\ 1/e & \text{for } e \ge 1, \end{cases} \tag{10}$$

where μ_z includes the mobility reduction due to the vertical electric field and is related to the low field mobility μ_0 by [7]

$$\frac{\mu_z}{\mu_0} = \frac{1}{1+\theta(q_b + q_i/2)} = \frac{1}{k_1 q_i + k_2} \quad \text{for } e < 1, \tag{11}$$

where

$$\theta = \frac{Q_{spec}}{\epsilon_{Si} E_0}, \tag{12a}$$

$$k_1 = \theta\left(\frac{1}{2} - \frac{1}{1+\frac{2}{\gamma_b}\sqrt{\psi_p}}\right), \tag{12b}$$

$$k_2 = 1 + \frac{\theta\psi_p}{1+\frac{2}{\gamma_b}\sqrt{\psi_p}}, \tag{12c}$$

E_0 is the electric field intensity at which the mobility starts to decrease significantly, γ_b is the normalized body factor and ψ_p is the normalized pinch-off surface potential (corresponding to $q_i = 0$). In (4), u is the effective mobility normalized to low-field surface mobility:

$$u = \frac{\mu_{eff}}{\mu_0} = \frac{\mu_{eff}}{\mu_z}\frac{\mu_z}{\mu_0}. \tag{13}$$

Therefore, from (10) and (11),

$$u = \begin{cases} \dfrac{1}{k_1 q_i + k_2} & \text{for } e < 1 \\ 1/e & \text{for } e \ge 1. \end{cases} \tag{14}$$

DIBL is modeled as a shift in the threshold voltage [7] which can simply be accounted for in (1) as a shift in υ_p.

2.4. Effect of short channel on drain current and transconductance

Following the derivation in [9] for velocity saturation and in [7] for MRFV, we obtain the drain current in saturation

$$i_{dsat} = \frac{4(q_s + q_s^2)}{2 + \lambda_{ck} + \sqrt{4(1+\lambda_{ck}) + \lambda_{ck}^2 (1+2q_s)^2}}, \tag{15}$$

where

$$\lambda_{ck} = \frac{\lambda_c}{k_2} \tag{16}$$

accounts for mobility reduction due to vertical field and is slightly bias dependent because of the gate bias dependent parameter k_2 given by (12c).

The normalized source transconductance can then be calculated as

$$g_{ms} \triangleq -\frac{\partial i_d}{\partial q_s}\frac{\partial q_s}{\partial \nu_s} = \frac{2q_s}{\sqrt{4(1+\lambda_{ck}) + \lambda_{ck}^2 (1+2q_s)^2}}, \tag{17}$$

equivalently expressed in terms of i_d ($= i_{dsat} = IC$) as

$$g_{ms} = \frac{\sqrt{i_d^2\lambda_{ck}^2 + 2i_d\lambda_{ck} + 4i_d + 1} - 1}{i_d\lambda_{ck}^2 + \lambda_{ck} + 2} \tag{18}$$

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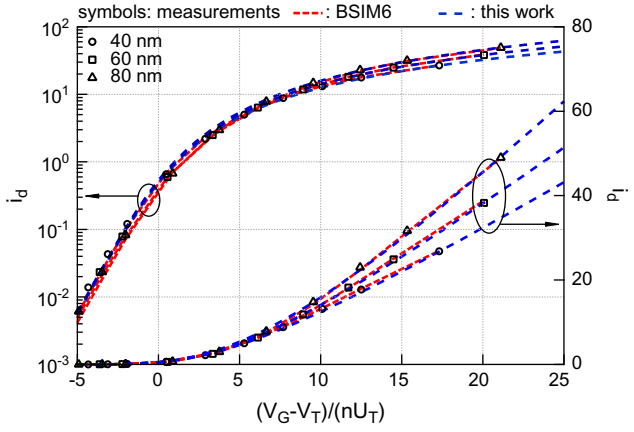

Fig. 1. i_d versus pinch-off voltage.

which gives

$$\frac{g_{ms}}{i_d} = \frac{\sqrt{i_d^2\lambda_{ck}^2 + 2i_d\lambda_{ck} + 4i_d + 1} - 1}{i_d^2\lambda_{ck}^2 + i_d\lambda_{ck} + 2i_d}. \tag{19}$$

Velocity saturation and mobility reduction due to vertical field slightly impact the drain current I_D and gate transconductance G_m even in weak inversion [9]. Nevertheless, the transconductance remains proportional to the drain current in weak inversion and hence G_m/I_D remains unaffected in this region.

2.5. Comparison of the simple analytical model with BSIM6 and measurements

Fig. 1 shows the transfer characteristics (variation of the normalized drain current with normalized gate over-drive voltage) for three different channel lengths, viz. 40, 60 and 80 nm. The analytical curves are nothing but a plot of (15) in which q_s is eliminated using (1). Each channel length corresponds to a different value of the parameter λ_{ck}. Measurements on NMOS transistors fabricated in a standard bulk 40 nm CMOS technology as well as the BSIM6 fitting results at the same channel lengths (shown on the same figure) compare very well with the simple model.

Eq. (19) for g_{ms}/i_d is plotted in Fig. 2(a) as a function of IC with $\lambda_c = 0.45$. The normalized G_m/I_D (g_{ms}/i_d), is equal to 1 in weak inversion and decreases on moving towards strong inversion. In strong inversion it varies as $1/\sqrt{IC}$ if no velocity saturation is present, otherwise it tends asymptotically to $1/(\lambda_c IC)$. The parameter λ_c, called the velocity saturation factor and defined in (5), is a measure of velocity saturation effect and hence is an important parameter for short-channel devices that have strong velocity saturation effects. For a given technology it depends only on the channel length; the shorter the channel, the higher the value of λ_c and the higher the velocity saturation effect. In Fig. 2(a) the asymptote $1/(\lambda_c IC)$ intersects the weak inversion asymptote $g_{ms}/i_d = 1$ at $IC = 1/\lambda_c$, which can be interpreted as the demarcation between weak inversion and velocity saturated strong inversion region.

Fig. 2(b) shows a comparison of the analytical plots of the normalized G_m/I_D with measurements and BSIM6. It can be seen that the simple analytical equation (19) is valid from weak to strong inversion regions and is reasonably close to the measurements and the BSIM6 model.

It should be re-emphasized that the purpose of this simple analytical model is to provide initial design guidelines and not to replace a numerically accurate full compact model like BSIM6.[1] Of course, the initial values should be reasonably accurate to justify their use. As an example, the relative error in G_m/I_D between the simple analytical model and the measurements is limited to 10%, as can be seen in the inset in Fig. 2(b).

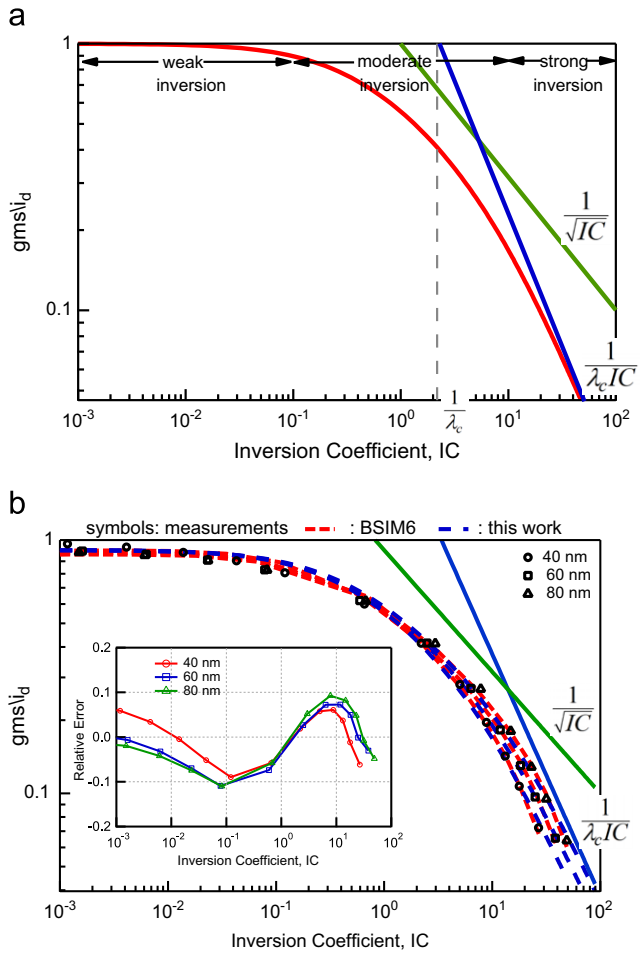

Fig. 2. g_{ms}/i_d vs. inversion coefficient. (a) The asymptotes at $1/\sqrt{IC}$ and $1/(\lambda_c IC)$ are shown. (b) Comparison of the simple analytical model with measurements and BSIM6. Inset: relative error between the simple analytical model and measurements.

It can be observed in Fig. 2(b) that for the 40 nm device, g_{ms}/i_d starts degrading as $1/(\lambda_c IC)$ already around $IC=3$ and that there is practically no region with $1/\sqrt{IC}$ dependence. For shorter devices this point would only move towards $IC=1$ or lower, implying a strong degradation of transconductance efficiency (due to velocity saturation) already at low biases. Evidently, to avoid this degradation the bias points for short-channel devices would need to be pushed from strong inversion towards moderate and eventually weak inversion.

3. Simple example of *IC* based design methodology

3.1. Current optimization in a common-source stage

Following [11], the goal is to optimize a capacitively loaded common-source stage, as shown in Fig. 3, to minimize its current consumption for a desired gain A_v at a given frequency of operation ω, which is assumed to be higher than the cut-off frequency ω_c, i.e., $\omega > \omega_c$.

The small-signal voltage gain of the circuit (loaded by an external load capacitance C_L) can then be approximated as

$$A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{G_m}{\omega C_{tot}} \tag{20}$$

[1] The interested reader is referred to [10] for an overview of the benchmarking of the scaling properties of BSIM6 against 40 nm CMOS technology.

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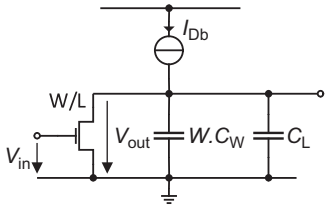

Fig. 3. A capacitively loaded common-source gain stage.

where

$$C_{tot} = C_w W + C_L. \tag{21}$$

Here C_w is the self-loading load capacitance per unit width of the gain transistor and W its width. At a given length L (usually taken as the minimum provided by the technology), the bias current through the transistor is

$$I_{D_b} \propto IC \cdot W. \tag{22}$$

Solving for W and normalizing, we obtain (see Appendix A for the detailed derivation)

$$w = \frac{\Omega}{g_{ms} - \Omega\ell} \cdot \ell; \tag{23}$$

$$i_{d_b} = \frac{\Omega}{g_{ms} - \Omega\ell} \cdot IC \tag{24}$$

where,

$$\Omega = \frac{\omega}{\omega_0} A_v \tag{25a}$$

$$\ell = \frac{L}{L_0} \tag{25b}$$

$$\omega_0 = \frac{I_{spec_\square}}{nU_T C_w L_0} \tag{25c}$$

and L_0 is the minimum channel length provided by the chosen technology. In Fig. 4, i_{d_b} is plotted as a function of IC for three different values of Ω at $L = 40$ nm ($\ell = 1$), using (18) for g_{ms}. The plots of i_{d_b} without including velocity saturation ($\lambda_c = 0$ in (18)) are also shown for comparison. We can observe that, to obtain a given Ω, higher bias current is needed in the device with velocity saturation than for the one without. This is especially prominent for high Ω and in strong inversion.

From Fig. 4, it is evident that the bias current I_{D_b} of the common-source stage can be minimized for a given gain and operating frequency, i.e. at a given Ω. For a target Ω at a given channel length (fixing λ_c and ℓ), the optimum inversion coefficient for achieving minimum bias current (IC_{opt}) can be obtained by minimizing (24) numerically and plotting the curve as in Fig. 4. Interestingly, this optimum lies in the moderate or the weak inversion region. Having obtained IC_{opt} we can calculate the required width W_{opt} by plugging-in IC_{opt} for i_d in (18) and using in (23). Finally, the required optimum bias current can be calculated as

$$I_{D_{bopt}} = I_{spec_\square} \frac{W_{opt}}{L} IC_{opt}. \tag{26}$$

3.2. Comparison with BSIM6

To verify the design methodology outlined above, we attempt the design of a common-source stage loaded with another common-source transistor of width 100 μm (implying a load capacitance $C_L = 18.5$ fF). We target a gain $A_v = 15$ dB and a working frequency $f = 24$ GHz, giving $\Omega = 0.83$. Choosing the minimum channel length, 40 nm ($\ell = 1$), provided by the 40 nm standard CMOS technology, we obtain the optimum value of IC, $IC_{opt} = 6.3$, that is in moderate inversion. The normalized optimum width $w_{opt} = 1.41$ is calculated using (23) and the normalized bias current $i_{d_{bopt}} = 8.78$ is calculated using (24). Knowing the values of technology parameters we can calculate the optimum bias current $I_{D_{bopt}}$ and width W_{opt}. Eventually, plugging the values of W_{opt} and $I_{D_{bopt}}$ for simulating with the BSIM6 model, we obtain a gain of 14 dB at 24 GHz, which is close to the target gain of 15 dB.

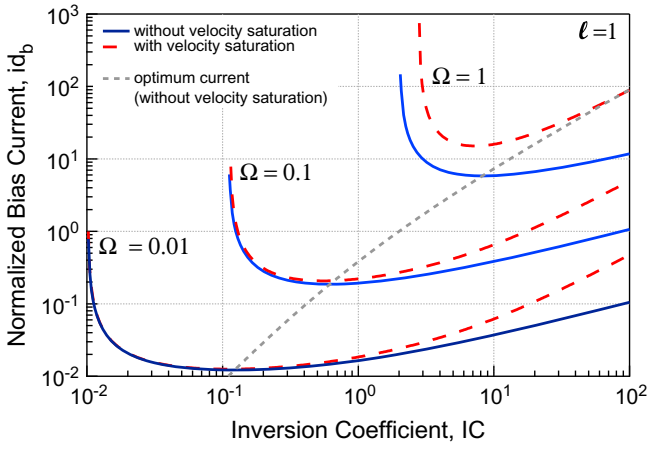

Fig. 4. Normalized bias current for the capacitively loaded common-source stage vs. inversion coefficient. $\ell = 1$.

4. Low-power RF design

A more practical requirement for low-power RF design would be not only to minimize the consumption to obtain a given gain but also to minimize the noise. Maximizing the gain, minimizing the noise and minimizing the consumption involves a mutual tradeoff. To quantify this tradeoff we can introduce a figure-of-merit and then optimize this FoM (rather than dealing with the gain, noise and current individually), as we show in the following.

Consider a common-source stage loaded with an identical transistor such that it presents a load C_{GS} to the first stage (see Fig. 5), we can write

$$A_v = \frac{G_m}{\omega C_{GS}} = \frac{\omega_t}{\omega} \tag{27}$$

where

$$\omega_t \cong \frac{G_m}{C_{GS}} \tag{28}$$

is approximately equal to the transit frequency. The noise factor is given by [7]

$$F \cong 1 + \frac{\gamma_{nD}}{G_m R_S} \tag{29}$$

where γ_{nD} is the excess noise factor of the gain transistor and R_S is the source resistance. In order to maximize the gain A_v and minimize the noise factor F at a given bias current I_D, we can define a FoM as

$$FoM_{GainNoise} \triangleq \frac{A_v}{(F-1) \cdot I_D} = \frac{R_S}{\omega\gamma_{nD}} \frac{G_m \omega_t}{I_D}. \tag{30}$$

$FoM_{GainNoise}$ is proportional to an important FoM for low-power RF

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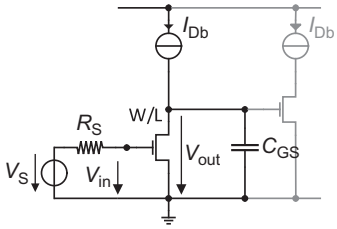

Fig. 5. A common-source gain stage loaded with an identical load stage.

design

$$FoM_{RF} \triangleq \frac{G_m \omega_t}{I_D} \tag{31}$$

which, in the normalized form [9], can be written as

$$fom_{rf} \triangleq \frac{g_{ms} f_t}{i_d}. \tag{32}$$

Both G_m/I_D and ω_t are important metrics in their own standing. Because G_m/I_D is maximum in weak inversion, it is advantageous to bias the device towards this region from the point of view of dc gain and power consumption. However, the linearity and noise of the device degrade in this region. The transit frequency ω_t is defined as the frequency at which the extrapolated small-signal current gain of the transistor in common-source configuration falls to unity. Devices are biased in strong inversion to obtain significant gain at RF, better noise and linearity, albeit at the cost of a higher current consumption.

FoM_{RF}, which combines these tradeoffs into a single metric, was introduced in [12] and discussed further in [13]. Since it combines the two quantities which have their maxima in opposite directions of the *IC* axis, it is particularly suited for low-power RF design, serving as a tool to locate the optimum operating point (*IC*) of the device. This optimum can be rapidly located by plotting the normalized fom_{rf} as a function of *IC* using (18) and (28),[2] as shown in Fig. 6. A comparison with measurements and BSIM6 simulations on 40, 60 and 80 nm, shown on the same figure, shows a reasonable match. Interestingly, for short channel devices, this FoM has a maximum in moderate inversion [9,12,13] indicating that the optimum operating point lies in this region. This corroborates the advantageous use of moderate inversion for low-power RF circuits as already mentioned in Section 1. The use of this FoM for RF design in moderate inversion region has been demonstrated in [13].

5. Conclusion

Accurate MOSFET compact models like BSIM6, integrated with sophisticated circuit simulators, place powerful tools in the hands of analog circuit designers to design circuits using the state-of-the-art technology nodes. However, most analog design cycles begin with simple hand calculations where tradeoffs (like that between power consumption, gain, operating frequency and noise) are evaluated and first-cut approximations about the operating points and dimensions of the transistors are made. Simple, yet sufficiently accurate, models are needed at this stage of the design cycle.

[2] The gate capacitance C_{GS} is a bias dependent parameter [7] but can be approximated by a constant value accounting not only for overlap and other extrinsic capacitances (such as fringing capacitances, which are becoming increasingly important in deep-submicron devices), but also for bias dependent intrinsic capacitances. Although this simplification obviously comes at the expense of accuracy (especially in strong inversion), it is acceptable for simple hand calculations.

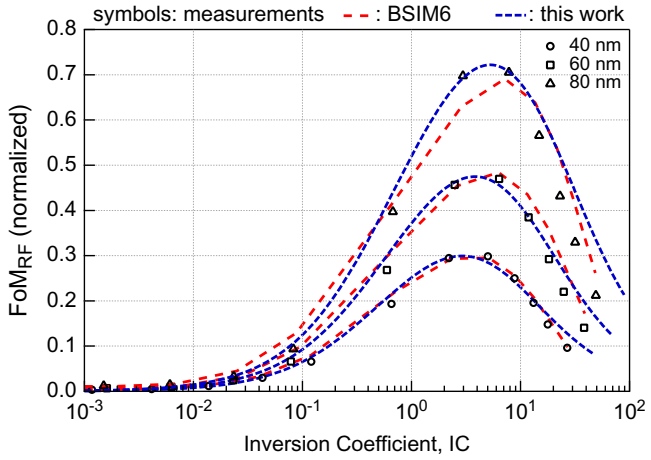

Fig. 6. *FoM* versus inversion coefficient.

This paper summarized a set of equations and figures-of-merit especially suitable for low-power analog and RF design derived from the charge based core of the BSIM6 model, that are simple enough for use with basic numerical tools, yet accurate enough to yield a good first-order approximation of the operating point, viz., inversion coefficient IC. It was shown that the optimum operating point for low-power RF circuits lies in the moderate inversion region emphasizing the importance of accuracy of the model in this region.

A comparison with the BSIM6 compact model and measurements from NMOS devices fabricated with 40 nm standard bulk CMOS technology was also presented. The comparison points out to the advantage of the charge based approach adopted in BSIM6: it can be used both as a full featured compact model and as a pre-simulation design methodology.

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Appendix A

The small-signal voltage gain of the capacitively loaded common-source transistor shown in Fig. 3 is given by

$$A_v = \frac{G_m}{\omega C_{tot}}. \tag{A.1}$$

Therefore

$$C_{tot} = \frac{G_m}{\omega A_v} = \frac{g_{ms} G_{spec}}{n \omega A_v} = \frac{g_{ms} I_{spec_\square} (W/L)}{n U_T \omega A_v}. \tag{A.2}$$

C_{tot} is the total load capacitance seen by the gain transistor and is the sum of the external load capacitance C_L and the load capacitance of the gain transistor itself (C_w per unit width):

$$C_{tot} = C_w W + C_L. \tag{A.3}$$

Let us define a constant

$$\omega_0 = \frac{I_{spec_\square}}{n U_T C_w L_0} \tag{A.4}$$

where L_0 is the minimum channel length provided by the chosen technology. Thus ω_0 is a parameter dependent entirely on the

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technology and temperature and independent of the operating point and frequency. Solving (A.2) and (A.3) for W and substituting using (A.4), we get

$$W = \frac{C_L}{C_w} \cdot \frac{\frac{\omega A_v}{\omega_0}\frac{L}{L_0}}{g_{ms} - \frac{\omega A_v}{\omega_0}\frac{L}{L_0}}. \tag{A.5}$$

Rewriting (A.5) in terms of normalized variables, we obtain

$$w = \frac{W}{W_0} = \frac{\Omega}{g_{ms} - \Omega\ell} \cdot \ell \tag{A.6}$$

where

$$W_0 = \frac{C_L}{C_w} \tag{A.7a}$$

$$\Omega = \frac{\omega}{\omega_0} A_v \tag{A.7b}$$

$$\ell = \frac{L}{L_0}. \tag{A.7c}$$

Now the bias current is then given by

$$\begin{aligned} I_{D_b} &= I_{spec_\square} \frac{W}{L} IC \\ &= I_{spec_\square} \frac{W_0}{L} \cdot \frac{\Omega}{g_{ms} - \Omega\ell} \cdot \ell \cdot IC \\ &= I_{spec_\square} \frac{W_0}{L_0} \cdot \frac{\Omega}{g_{ms} - \Omega\ell} \cdot IC. \end{aligned} \tag{A.8}$$

In the normalized form

$$i_{d_b} = \frac{I_{D_b}}{IC_0} = \frac{\Omega}{g_{ms} - \Omega\ell} \cdot IC \tag{A.9}$$

where,

$$IC_0 = IC_{spec_\square} \frac{W_0}{L_0}. \tag{A.10}$$

It should be remembered that g_{ms} in (A.6) and (A.8) is a function of IC through (18).

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