A-Si:H/c-Si heterojunctions: a future mainstream technology for high-efficiency crystalline silicon solar cells ?

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***Abstract* — In this contribution, we shortly review the main features of amorphous /crystalline silicon heterojunction (SHJ) solar cells, including interface defects and requirements for high quality interfaces. We show how a process flow with a limited number of process steps leads to screen printed solar cells of 2x2cm^2 with 21.8% efficiency and of 10x10cm^2 with 20.9% efficiency (n-type FZ). We show that the devices work in high injection conditions of 3x10^{15}cm^{-3} at the maximum power point, a factor two higher than the base doping. Several research labs and companies can now produce large area 6" cells well over 20% on CZ wafers and some of the critical cost factors, such a metallization can be overcome with suitable strategies. Based on the high quality coating tools and processes developed for thin films used for flat panel display or thin film solar cell coatings, the deposition of the layers required to make SHJ cells has the potential to be performed in a controlled way at low cost. Considering the few process steps required, the high quality n-type Cz wafers that can be obtained by proper crystal growth control, SHJ technology has several assets that could make it become a widespread PV technology.**

***Index Terms* — silicon heterojunction solar cells, amorphous silicon, crystalline silicon.**

I. Introduction

The combination of thin amorphous silicon layers on crystalline silicon wafers can be viewed as a combination of the best of two worlds, i.e. thin film technologies with their potential for ultra-low coating cost per m^2 and crystalline silicon as providing a quasi-perfect high quality absorber. This paper reviews some of the recent scientific and technological advances in the field and comments on the strength and potential weaknesses of the technologies.

II. Basic Principles

Silicon heterojunction (SHJ) technology, pioneered by Sanyo [1], is currently the only technology that relies on the full surface on the use of passivating contacts. As illustrated in Fig. 1, the i-p-TCO and i-n-TCO stacks at the front and back of an n-type wafer, respectively, play the role of semi-permeable membranes that controls the flow of carriers, maintaining a high density of carriers inside the wafer at the maximum power point, thereby ensuring a high V_{oc}. The thin intrinsic layers ensure a low interface state density, ($D_{it} < 10^{11}$ cm^{-2}) but still allow the carrier to cross the layers. Good SHJ cells rely on the use of high lifetime crystalline Si material, which can be achieved with n-type doping and well controlled CZ-crystal growth technique, for which bulk lifetime carrier in excess of several ms can be achieved over large part of the ingots. Indeed it is found that n-type CZ materials can reach even lifetime of 10 ms for moderate conductivity (> 1 Ohm cm). Good SHJ devices work at high injection and simulations (see part IV) show that the doping level, and hence doping variation along an ingot should not be an issue, relaxing some constraints for ingot doping linked to dopant segregation during growth. Hence it can be assumed that full CZ-n-type ingots can be produced at costs similar to those of p-type CZ wafers. Also, thanks to the high quality full area surface passivation, good SHJ cells display an increase of V_{oc} when thickness is reduced, thereby limiting efficiency losses, linked to current decrease strongly. The world record 23.7% SHJ devices of Sanyo was indeed achieved with a wafer only 98 micron thick [2]. The high V_{oc} translates into favorable temperature coefficient for the module performance, and values well below -0.3%/°C are reported [3].

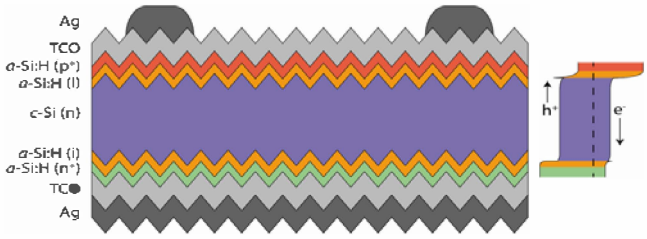

Fig. 1. Structure of SHJ cell, according to process flow and as manufactured by our group. A band digram is sketched on the right side.

III. Process Flow and Equipments

To achieve the device of Fig. 1, a typical process flow is the following:

1) Saw damage etch/texturing/cleaning
2) Deposition by plasma enhanced CVD of i-p stack (typically 10-15 nm)

3) Deposition by plasma enhanced CVD of i-n stack (typically 10-15 nm)
4) Deposition of front transparent conductive oxide (typically 70 nm ITO) by sputtering
5) Deposition of back contact (typically 70 nm TCO + 300 nm metal) by sputtering
6) Edge isolation
7) Screen-printing of front grid
8) Low temperature firing.

Note that the use of ion plating for the front contact and of various types of TCO/metal or TCO screen printed contacts for the back-side are also possible alternative.

The process sequence is arguably one of the most simple to realize devices above 20%. The major challenges are:

i) achieving a good surface cleaning, an excellent control of the deposition of the amorphous Si layers and a good control of the contacts the TCO makes with the amorphous layers,

ii) the reliability and cost of the coating processes (plasma processes),

iii) the possible high cost for the metallization (Ag paste) and TCO containing indium,

iv) finding module encapsulation schemes compatible with the used materials.

We'll comment here on the first three points. With respect to point i), several groups have shown excellent results recently, in line with those of Sanyo, showing that the expertise to master the process can be developed providing a suitable effort is done (see [4] for a complete review).

Concerning ii), thanks to the fantastic improvement of coating technologies both for flat panel displays and for thin film silicon, the technology to deposit on large areas uniform high quality amorphous Si layers by PECVD is now well mastered. This is similar for coating of layers by sputtering (PVD). It can be safely assumed that, in the long range, the cost for these processes can be reduced to extremely low level. Indeed for the parent thin film silicon technologies, full modules production costs of 0.35-0.4€/Wp at 10-11% module level should be achievable. Those include two TCO layers more than 1 micron thick, one amorphous and one microcrystalline cell of thickness in the 200 and 800 nm range. In this case, the cost for the coatings is below 0.2€/Wp. Hence it is straightforward to see that the cost of the PECVD and PVD layers for SHJ, with layers a factor 10-40 thinner and an efficiency doubled compared to thin film silicon can be extremely low cost. When ITO or In based TCO are used, the cost of indium remains also moderate (< 1€/m2) thanks to the low thicknesses used.

The challenges with metallization (iii), could be more critical, as low T silver pastes, even though they can be printed with higher aspect ratio than conventional high T pastes, are a factor typically 3-5 less conductive than high T paste. A 6" solar cells with 3 busbars pattern will hence be unattractive economically with front metalisation costs over 6 €cts/Wp. For this reasons schemes with e.g. 5 narrower busbars or arrays of wires have been recently demonstrated, e.g. by Roth and Rau CH [3, 5]. An elegant alternative is the use of plating, e.g. as demonstrated by Kaneka with 22.1%, 6" plated SHJ cells [6], providing likely an absolute 0.5 to 1% efficiency increase compared to screen printing thanks to reduced shadow losses. Recently copper based pastes were also introduced as possible candidates to replace Ag pastes [7]. In the last two cases the possible role of ITO as a known barrier to Cu diffusion has to be underlined.

IV. Nature and Realization Of High Quality a-si/c-Si Interfaces

Several fundamental works have recently addressed the fundamental properties of SHJ. A good interface is obtained when epitaxy is avoided [see e.g. 8, 9]. The low mobility of the carriers, the band alignment, the interface defects and the bandtails of a-Si play a critical role in controlling the carrier transport through the layers. For instance it is found that the conduction band offset of around 0.25eV remains essentially fixed when the hydrogen content is varied [10], whereas the valence band offset is adjusted accordingly. The defects at the interface are found very similar in nature to those of a-Si:H. They have been shown to have an amphoteric nature [11]. The reduction of defects by annealing follows a low similar to those of bulk a-Si defects [12], and a metastability effect at the interface under light soaking is also observed [13], similar to Staebler-Wronski effect, even though this effect impacts the cell performance only weakly. It is now assumed that the inteface defects are hence similar in nature to those found in bulk a-Si [4].

Even though passivation quality can be improved by annealing, it is usually found preferable that the films are already good in the as-deposited state [4]. Several factors are critical for achieving a high quality passivation in terms of processing. It was reported that working with plasma regimes close to depletion conditions would lead to a better surface passivation [14]. The use of Hydrogen plasma treatment on the thin i-layers [15] was also reported to give enhanced quality of surface passivation.

IV. Solar Cell Preparation And Results

Table I shows solar cells results according to the process flow of part II. The PECVD layers at 40 MHz were deposited in a KAI-M Reactor integrated in home-made system, whereas the PECVD layers at 13 MHz were deposited in an Octopus R&D multichamber cluster reactor from Indeotec SA. The TCO and metal layers were deposited by DC magnetron sputtering in an MRC system. All cells were screen-printed. Using 40 MHz frequency, an efficiency of 21.86% was obtained on a 2x2 cm^2 cells using a 3 Ohm cm 230 micron thick FZ wafers and close to 21% was achieved

on 10x10 cm^2 cells. The cells on CZ wafers were only 160 µm thick and showed higher Voc even though the performance was slightly reduced compared to the FZ case. The 2x2 cm2 best device at 13 MHz was at 20.9%, i.e. below the 40 MHz case. However less process optimization was made on the 13 MHz system and no final conclusion can be drawn for the effect of frequency in term of layer quality. This is similar for the results on Cz wafers. Results for rear emitter devices and results for p-type wafers will be discussed in another contribution [16].

TABLE I
SUMMARY OF MAJOR CELL RESULTS OBTAINED AT IMT

	FZ *n* c-Si 4 cm^2	FZ *n* c-Si 4 cm^2	FZ *n* c-Si 100 cm^2	CZ *n* c-Si 4 cm^2	CZ *n* c-Si 100 cm^2
PECVD	13 MHZ	40 MHz	40 MHz	40 MHz	40 MHz
V_{oc} [mV]	721	726	727	731	730
J_{sc} [mA/cm^2]	37	37.8	36.5	36.9	36.5
FF [%]	78.3	79.7	78.9	77.1	77.7
Eff. [%]	**20.9**	**21.86**	**20.95**	**20.80**	**20.71**

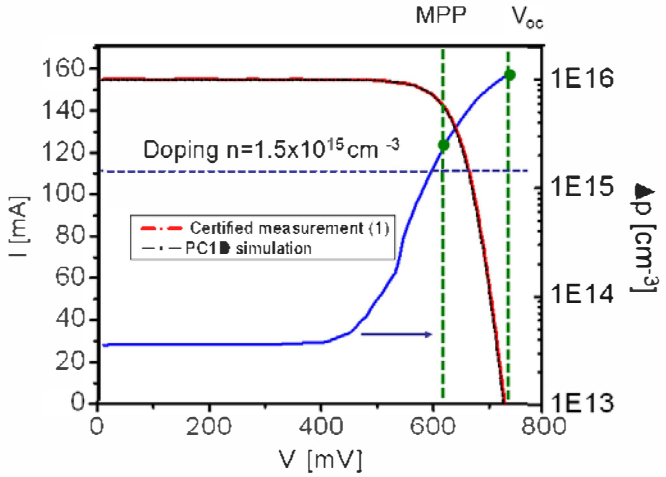

Fig.2. Experimental current-voltage (I-V) curve of a state-of-the-art devices and PC1D simulation of the devices. The blue line represents the injection level as a function of the voltage.

Figure 2 shows the experimental IV curve of a state-of-the art device (red curve), together with a PC1D simulation (black curve) using low lifetime, low mobility emitters and backcontact layers mimicking the a-Si layers with adjustment of the parameters for finding similar J_{sc} and V_{oc}. The PC1D curve reproduces perfectly the experimental curve. It is then possible form the PC1D simulation to extract the injection level in the middle of the wafer for the different voltage values. We find an injection level of $1.1x10^{16}$ cm^{-3} in V_{oc} conditions and of $3x10^{15}cm^{-3}$ at the maximum power point (MPP). This last value is a remarkably high value, which is twice as high as the background doping of $1.5x10^{15}$ cm^{-3}. In the simulation, there is no significant dependence of the efficiency on the doping going from 1 Ohm cm to intrinsic material, indicating that homogeneity of doping of n-type ingot might not be an issue for this type of devices.

V. INDUSTRIALIZATION AND PERSPECTIVES

Even though Sanyo (now Panasonic) was the first to start mass production [17], several new companies are starting productions at a few MW level such as CIC [18] in Japan or pilot production (EDF/Ines, France [19]). Intense R&D activities take place, for instance, at Kaneka [6], at Hyundai Heavy Industries [20], at LG Electronics [21] in Korea). Several equipment providers offer production solutions as well, including Roth and Rau, Switzerland/Germany [3,5]. Recently, CIC and Roth-and-Rau CH achieved 6" printed cells with over 21%. It can be assessed that the potential for "standard" SHJ in production with screen-printed contacts is, hence, between 21 and 22%. It could reach 22 to 23% if plated contacts are used. A next step will the realization of full interdigitated backcontacted (IBC) structures [19, 21,23], for which promising results up to 23.4% (not certified [21]) were already reported. For IBC, the important parasitic losses at the front created by the i-p-TCO stack [23], can be suppressed, leading to strong current increase. SHJ-IBC have the potential to surpass 25% efficiency. This should be possible, even though further work needs to be achieved to ensure FF as high as those achieved with state-of-the-art diffused cells.. Also the combination of high temperature steps and low temperature steps (e.g. rear emitter SHJ cells with highly transparent front [24]) could become an interesting alternative, even though the increased number of process steps will have to be compensated by a significant efficiency increase.

VI. CONCLUSION

In this work, we reported on the realization of high efficiency screen-printed full SHJ solar cells with 21.8% efficiency. In parallel several research groups and industry now report efficiencies well above 20%, even on 6" solar cells with a reduced number of processing steps compared to other techniques allowing high efficiencies. Based on the progress in production technologies for thin film silicon layers (homogeneity of reactors on large area, quality of layers), the manufacturing techniques of SHJ cells relying on thin film coating can be seen as an advantage for future low cost

manufacturing. Efficient production will require though good cleaning procedures, mastering of high quality n-type ingot, manufacture as well as metallization schemes which do require limited quantities of Ag. All these requirements seem within reach.

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