Multi-gate Si nanowire MOSFETs: Fabrication, strain engineering and transport analysis

THÈSE N^{O} 5507 (2012)

PRÉSENTÉE LE 2 NOVEMBRE 2012
À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DES DISPOSITIFS NANOÉLECTRONIQUES
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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FÉDÉRALE DE LAUSANNE
Suisse
2012

Acknowledgements

As a first step, I would like to thank Swiss Federal Institute of Technology in Lausanne-EPFL, the EDMI doctoral school and the Nanoelectronic Devices Laboratory (Nanolab) for doing this thesis in a competitive basis. It was a good opportunity to gain several knowledge in this thesis supported by extensive course works in microsystems and microelectronics as well, organized by EPFL, FSRM and MEAD Education SA. Thanks to Dr. Yoshishige Tsuchiya and Sheng Ye at Southampton University, UK, for the micro-Raman measurements (using a TERS setup) on deeply scaled cross-section Si nanowires and Dr. Di Wang and Dr. Robby Prang at Karlsruhe Institute of Technology (KIT), Germany, for the HRTEM cross-sections on my nanowires with 0.08 nm resolution. Thanks to Dr. Per-Erik Hellstrom at KTH Royal Institute of Technology, Stockholm, Sweden, for the poly-Si/SiO_2 gate stack, Dr. Sarah Olsen at Newcastle University, UK, for the micro-Raman measurement on sub-100 nm wide nanowires and Dr. Jean-Michel Sallese at EPFL to support the parameter extraction part of this thesis in the experiment, modeling and simulation steps. Thanks to Dr. Wladek Grabinski and Dr. Didier Bouvet (Dr. Paul Salet, Dr. Dimitrios Tsamados and Dr. Suyat Ayoz as well) for organizing the group meetings and providing feedbacks on the process, the electrical characterization and the simulation steps. Thanks to Matthieu Berthomé, for helps on the transport analysis steps in my nanowires, used for the three recent IEEE TED paper submissions (#1-3), and the other Ph.D. students, post-docs, all the secretaries and staff at Nanolab and EPFL for the happy moments.

Fabrication of bulk Si nanowires was pretty challenging, especially the isolation step, needing several process monitoring to minimize the process variation. Thanks to the CMi staff for the extensive technical supports during the various process steps, especially regarding several process issues for the first SOI Si nanowire run-card at EPFL including an ALD high-k/metal-gate stack. Note that we could fabricate the GAA sub-5 nm cross-sectional Si nanowires successfully and with 100% efficiency from our only two SOI wafers, dedicated to validate my first SOI Si nanowire run-card. Thanks to Mir-Enterprise Ltd., UK, and the Philips clean room at Eindhoven, the Netherlands, for performing the high-k/metal-gate ALD gate stack on mt 100 mm SOI wafers including suspended sub-5 nm cross-sectional Si nanowires. It was a pretty difficult task, performing all the steps in a few hours while monitoring and checking the actual process steps by EPFL at the same time as well. All the works went smoothly and with the highest possible quality and efficiency, only by perseverance, hardworking, precision and organization during the experiments, electrical characterization, publication and international conference presentations.

I would like to thank Prof. Andreas Schenk, the head of Nano-Device Physics Group at Swiss Federal Institute of Technology in Zurich-ETHZ, Dr. Jean-Michel Sallese from STI Scientists group at Swiss Federal Institute of Technology in Lausanne-EFPL, Prof. Adrian M. Ionescu, the head of Nanoelectronic Device Laboratory at Swiss Federal Institute of Technology in Lausanne-EFPL, the thesis director, Prof. Siegfried Mantl from Forschungszentrum Julich GmbH research center, Juelich, Germany, and finally, Dr. Catherine Dehollain, from the RFIC group, Swiss Federal Institute of Technology in Lausanne-EFPL, the jury director, for the high international level Ph.D. examination covering simulation, modeling and technology aspects in a competitive basis.

Performing the Ph.D. thesis at EPFL was an excellent opportunity to gain several experiences and knowledge on even the topics that I was not working directly considering various paper review requests from IEEE Transactions on Electron Devices (TED) and Institute Of Physics (IOP) e.g. Nanotechnology during my Ph.D. at EPFL. Thanks also to the Swiss National Science Foundation (SNSF) for the financial support to perform this project as well.

Abstract

Multi-gate devices e.g. gate-all-around (GAA) Si nanowires and FinFETs are promising candidates for aggressive CMOS downscaling. Optimum subthreshold slope, immunity against short channel effect and optimized power consumption are the major benefits of such architectures due to higher electrostatic control of the channel. On the other hand, Si nanowires show excellent mechanical properties e.g. yield and fracture strengths of 10±2% and 30±1% in comparison to 3.7% and 4.0% for bulk Si, respectively, a strong motivation to be used as exclusive platforms for innovative nanoelectronic applications e.g. novel strain engineering techniques for carrier transport enhancement in multi-gate 3D suspended channels or local band-gap modulation using $>$ 4 GPa uniaxial tensile stress in suspended Si channels to enhance the band-to-band tunneling current in multi-gate Tunnel-FETs, all without plastic deformation and therefore, no carrier mobility degradation in deeply scaled channels.

In this thesis and as a first step, a precise built-in stress analysis during local thermal oxidation of suspended Si NWs in the presence of a Si_3N_4 tensile hard mask was done. Accumulation of up to 2.6 GPa uniaxial tensile stress in the buckled NWs is reported. The contribution of hard mask/spacer engineering on the stress level and the NW formation was studied and buckled self-aligned dual NW MOSFETs on bulk Si with two sub-100 nm cross-sectional Si cores including ~0.8 uniaxial tensile stress are reported. Micro-Raman spectroscopy was widely used in this thesis to measure stress in the buckled NWs on both bulk and SOI substrates.

A process flow was designed to make dense array of GAA sub-5 nm cross-sectional Si NWs using a SOI substrate including a high level of stress. The NW stress level can be engineered simply using e.g. metal-gate thin film stress suitable for both NMOS and PMOS devices. Lately, highly and heavily doped architectures with a single-type doping profile from source to drain, called junctionless and accumulation-mode devices, are proposed to significantly simplify the fabrication process, address a few technical limitations e.g. ultra-abrupt junctions in order to fabricate shorter channel length devices. Therefore, in this process flow, a highly doped accumulation-mode was targeted as the operation mechanism.

Finally, extensive TCAD device simulation was done on GAA Si NW JL MOSFETs to study the corner effects on the device characteristics, from subthreshold to strong accumulation, report the concept of local volume accumulation/depletion, quantum flat-band voltage, significant bias-dependent series resistance in junctionless MOSFETs and finally, support the experimental data to extract precisely the carrier mobility in sub-5 nm Si NW MOSFETs.

keywords: Si nanowire, multi-gate, stressor, mobility enhancement, micro-Raman, TCAD simulation, nano-transport, ALD gate stack, accumulation, inversion, junctionless.

Résumé

Les dispositifs à plusieurs grilles de contrôle, par exemple nanofils de silicium à grilles enrobantes et FinFETs sont des candidats prometteurs pour la réduction agressive des dimensions pour les dispositifs CMOS. Une pente sous le seuil optimale, l'immunité contre les effets de canaux courts et une consommation de puissance optimisée sont des bénéfices majeurs de ce genre de dispositifs, cela grâce à un meilleur contrôle électrostatique du canal. D'un autre côté , les nanofils de silicium présentent des propriétés mécaniques excellents , par exemple des limites d'élasticité et de fracture de 10±2% et 30±1% en comparaison à 3,7 et 4% pour du silicium massif, c'est une motivation forte pour les utiliser comme unique plateforme pour des applications nanoélectroniques innovantes comme par exemple des techniques nouvelles d'ingénierie du stress pour une amélioration des qualités de transport dans une architecture 3D à multiples grilles et canaux suspendus, ou bien une modulation de la bande interdite via une contrainte de tension uniaxiale supérieure à 4GPa, permettant d'augmenter le courant tunnel de bande-à-bande dans une architecture Tunnel-FET, tout cela sans modification plastique et par la même occasion sans dégradation de la mobilité des porteurs dans des canaux fortement réduits en dimension.

Dans cette thèse et dans un premier temps, nous analyserons précisément les contraintes intrinsèques accumulées lors d'oxydation thermiques locales de nanofils de silicium suspendus en présence d'un masque dur de nitrure de silicium. Une accumulation de contraintes de tension jusqu'à 2,6 GPa dans des nanofils avec une déformation de type flambage induite par la tension est rapportée. La contribution de la technologie de masques dus et d'ingénierie des espaceurs sur le niveau de contraintes et sur la formation des nanofils est étudiée et des transistors auto-alignés à nanofils de silicium jumeaux formés sur des plaques de silicium massif présentant un canal de dimension sub-100nm sont présentés. La spectroscopie micro-Raman a été souvent utilisée dans cette thèse pour mesurer les contraintes mécaniques dans des nanofils de silicium courbés, à la fois sur des substrats SOI ou bulk.

Un déroulement des procédés a été créé pour permettre la création de réseaux denses de nanofils à grilles enrobantes avec un diamètre sub-5nm, en utilisant un substrat SOI avec un haut niveau de contraintes. Le niveau de contraintes peut être modifié, pa exemple, par l'ajout d'une grille métallique à contrainte intrinsèque adaptés à l'architecture NMOS ou PMOS. Récemment une architecture à base de silicium très et hautement dopé présentant un type de dopage constant de la source au drain, appelées MOS à accumulation et MOS sans jonctions (junctionless) ont été proposées pour simplifier fortement le procédé de fabrication et éviter quelques limitations techniques, comme par exemple la nécessité de jonctions ultra abruptes, dans le but de fabriquer des dispositifs avec des longueurs de canal encore plus petites. En conséquence, dans ce procédé de fabrication, un mode de fonctionnement à accumulation à base de silicium fortement dopé a été ciblé.

Enfin, une analyse du transport dans des transistors sans jonctions à base de nanofils de silicium à grille enrobantes a été effectuée, faisant usage de simulations TCAD complètes, pour rapporter l'effet des coins dans tous les modes d'opérations (depuis sous le seuil jusqu'à l'accumulation forte)., le concept d'accumulation/de déplétion de volume locale, le concept de tension de bandes plates quantique, l'importance de la résistance série et sa variation avec les tensions appliquées dans les architectures sans jonctions, et finalement une extraction précise de la mobilité des porteurs à faible champ dans des transistors à nanofils de silicium de dimensions sub-5nm.

Enfin, des simulations TCAD completes ont été faites sur des transistors MOS à nanofils de silicium à grille enrobante pour étudier l'effet des coins, depuis sous le seuil jusqu'en accumulation forte, décrire le concept d'accumulation et déplétion locales ainsi que la bande plate quantique, l'importance de la dépendance en biais des résistances parasites séries dans l'architecture de MOSFET sans jonctions, et enfin supporter les données expérimentales pour extraire précisément la mobilité des porteurs dans des MOSFET à nanofils de silicium de diamétre inférieur à 5nm.

Mots-cléfs : nanofils de silicium, multiples grilles, contraintes, augmentation de mobilité, micro-Raman, TERS, simulations TCAD, transport nanoélectronique, stack de grille ALD, accumulation, inversion, junctionless

Technical acronyms

Acronym	Description
AC	alternative current
ALD	atomic layer deposition
AM	accumulation-mode
AMOSFET	accumulation-mode metal-oxide semiconductor field effect transistor
BHF	buffered hydro fluoric acid
BOX	buried oxide (in a SOI substrate)
CE	classical electron
CED	classical electron density
CESL	contact etch stop layer
CMOS	complementary metal-oxide semiconductor
CMP	chemical mechanical polishing
CPD	crytical point dryer
CVD	chemical vapor deposition
DC	direct current
DHF	dilute hydrofluoric acid
DIBL	drain induced barrier lowering
DM	depletion-mode
EBL	e-beam lithography
EM	enhancement-mode
FB	flat-band
FET	field effect transistor
FIB	focused ion beam
GAA	gate-all-around
HH	heavy-hole band
HRTEM	high resolution transmission electron microscopy
HSQ	hydrogen silsesquioxane
IM	inversion-mode
IPA	isopropanol (or 2-propanol)
JL	junctionless
LH	light-hole band
LPCVD	low pressure chemical vapor deposition
LS	logic swing
LTO	low temperature oxide
MOS	metal-oxide semiconductor

Technical acronyms

Acronym	Description
MOSFET	metal-oxide semiconductor field effect transistor
NEMS	nano electromechanical systems
NW	nanowire
OIS	Oxidation-induced stress
PMA	post-metallization annealing
QE	quantum electron
QED	quantum electron density
QM	quantum mechanics
RF	radio frequency
RTA	rapid thermal annealing
SCE	short channel effect
SEM	scanning electron microscopy
SLO	stress-limited oxidation
SMT	stress memorization technique
SOI	silicon on insulator
SS	subthreshold swing
STI	shallow trench isolation
TCAD	technology computer aided design
TEM	transmission electron microscopy
TERS	tip-enhanced Raman spectroscopy
TH	threshold
TW	transition width
VTC	voltage transfer characteristics

Physical constants and prefixes

Metric prefixes

Yotta (Y)	10^{24}
Zetta (Z)	10^{21}
Exa (E)	10^{18}
Peta (P)	10^{15}
Tera (T)	10^{12}
Giga (G)	10^{9}
Mega (M)	10^{6}
kilo (k)	10^{3}
hecto (h)	10^{2}
deca (da)	10^{1}
	10^{0}
deci (d)	10^{-1}
centi (c)	10^{-2}
milli (m)	10^{-3}
micro (μ)	10^{-6}
nano (n)	10^{-9}
pico (p)	10^{-12}
femto (f)	10^{-15}
atto (a)	10^{-18}
zepto (z)	10^{-21}
yocto (y)	10^{-24}

Physical constants

Avogadro's number (N_A)	6.02×10^{23} mol^{-1}
Boltzmann's constant (k)	1.38×10^{-23} J/K
Electronic charge (q or e)	1.60×10^{-19} C
Free electron rest mass (m_0)	9.11×10^{-31} kg
Permittivity of free space (ϵ_0)	8.85×10^{-12} F/m
Planck's constant (h)	6.63×10^{-34} J·s
Speed of light in vacuum (c)	3.00×10^{8} m/s

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1 Thesis overview

Multi-gate architectures e.g. gate-all-around Si nanowires and FinFETs are promising candidates for CMOS downscaling. It is worth mentioning that recently Intel started to use FinFETs on bulk Si substrate for the 22 nm technology node including stressors and high-k/metal-gate stack. In this thesis we mainly focus on the multi-gate Si nanowire MOSFETs. We demonstrated buckled Si nanowire MOSFETs on both bulk and SOI substrates using local oxidation and metal-gate strain as the stressor technologies. Gate-all-around Si nanowires with sub-5 nm cross-sections are demonstrated as high temperature performance MOSFETs. Micro-Raman spectroscopy was used in this thesis to measure stress in the buckled Si nanowires on bulk and SOI substrates, via ALD gate stack and on naked Si nanowires. Inversion and accumulation-mode were chosen as operation mechanisms during the fabrication step.

Extensive TCAD device simulation was done in this thesis for transport analysis in nanoscale, especially for three dimensional sub-5 nm cross-section channels, to support the electrical characterization data and extract the key MOSFET parameters precisely. Transport and corner effect analysis was done on GAA Si nanowire accumulation-mode and junctionless nMOSFETs by TCAD device simulation.

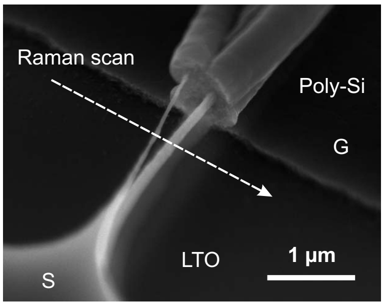
This thesis was done at the Nanoelectronic Devices Laboratory, Swiss Federal Institute of Technology in Lausanne-EPFL and mainly in the framework of Swiss National Science Foundation (SNSF) including several national/international partners e.g. Southampton University, Karlsruhe Institute of Technology, KTH Royal Institute of Technology, Newcastle University and EPFL (internal), providing several highly ranked articles in micro/nano-electronics e.g. IEEE TED (three), IEEE Transactions on Nanotechnology, Solid-State Electronics and several international conference presentations e.g. IEEE DRC, IEEE ESSDERC, IEEE ISDRS and INFOS.

A brief introduction to each chapter is provided below. Chapters 3, 4 and 7 are based on experiments including fabrication, optical/electrical characterization and key MOSFET parameter extraction. Chapters 5 and 6 include TCAD device simulations for corner effect study and transport analysis in GAA Si nanowire junctionless MOSFETs while in chapter 7, transport analysis on the fabricated devices was done using extensive TCAD device simulation.

Chapter 2: Introduction

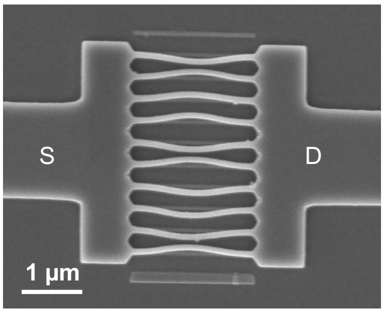
chapter 2 provides a brief introduction to the aggressive CMOS downscaling and the challenges to continue the Moore's law. The chapter includes a short introduction to the multi-gate architectures, strain engineering as a CMOS booster and finally, Si nanowire technology on both bulk and SOI substrates. This chapter provides an excellent motivation to the research on multi-gate Si nanowire MOSFETs and stressors for 3D suspended channels, will be followed by extensive fabrication, electrical characterization and TCAD device simulations in the next chapters.

Chapter 3: Multi-gate buckled Si NWs on bulk for high electron mobility and logic



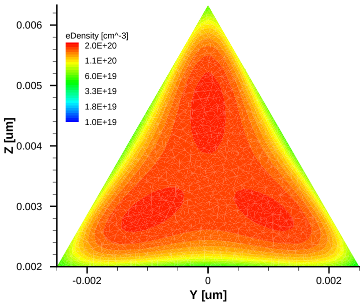
Chapter 3 describes built-in stress analysis during the oxidation process to make sub-100 nm cross-section Si NWs fabricated on bulk Si using 0.8 μm optical lithography, hard mask and spacer technology. We presented formation of buckled self-aligned dual Si NWs with two sub-100 nm Si cores using local oxidation in the presence of SiO_2 hard mask and spacer. The chapter includes fabrication, optical and electrical characterizations in nanoscale and key MOSFET parameter extractions.

Chapter 4: Buckled GAA deeply scaled cross-section Si nanowire MOSFETs



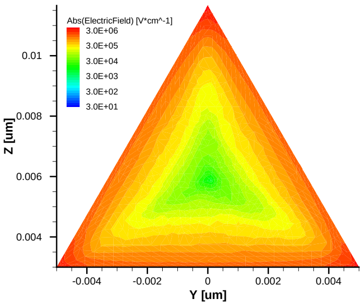
In chapter 4, a SOI Si nanowire platform was designed to provide dense array of sub-5 nm cross-section Si nanowires. Highly doped accumulation-mode was chosen as the operation mechanism. The devices were fabricated including an ALD gate stack and characterized electrically at various temperatures. Uniaxial tensile stress was induced to the Si nanowires using local oxidation and metal-gate strain. Such scaled cross-section devices are reported as high temperature performance MOSFETs and used for scattering mechanism study in nanoscale. More in depth studies, supported with extensive TCAD device simulations are reported in chapter 7.

Chapter 5: Local volume depletion/accumulation in GAA NW junctionless FETs



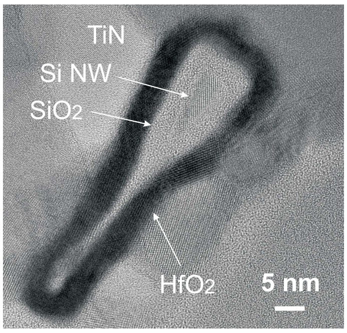
In chapter 5, extensive TCAD device simulation was done to report the new concept of local volume depletion/accumulation in the GAA Si nanowire junctionless nMOSFETs. The study was done using various doping levels and triangular Si nanowire cross-sections, considering local and total electron densities in the cross-section. The origin of local volume accumulation/depletion is reported in details using volume vs. surface conduction and majority vs. minority of carriers below and above flat-band. Such operation regimes can be used to suppress the typical corner effect in multi-gate MOSFETs, removing the subthreshold current path in the corners and therefore, reducing the OFF current.

Chapter 6: Transport analysis in triangular GAA Si NW junctionless MOSFETs



In chapter 6, we investigated transport analysis in GAA Si nanowire junctionless nMOSFETs with scaled cross-sections down to 5 nm in strong accumulation regime. Transport analysis was done in the presence of non-uniform accumulation of carriers and non-uniform normal electric field. The accuracy of the two main mobility extraction methods, split-CV and Y-function, are investigated. A significant bias-dependent series-resistance is reported in the junctionless MOSFETs. Contact engineering shows that this issue can be minimized, reporting the low-field carrier mobility values with acceptable accuracy while adding an extra S/D implantation step to the junctionless process flow.

Chapter 7: Transport enhancement in buckled GAA rounded triangular NW FETs



In chapter 7, transport analysis was done on the fabricated devices with sub-15 and sub-5 nm cross-section Si nanowires, considering electrical characterization supported by extensive TCAD device simulation. Note that applying the split-CV method is feasible only in the presence of a pretty large number of Si nanowires. Therefore, the Y-function was used to extract the carrier mobility in such devices. HRTEM was done on the samples with a 0.08 nm resolution and stress measurement was one on the buckled nanowires in the presence of ALD high-k/metal-gate stack using micro-Raman spectroscopy.

Chapter 8: Conclusion

In the last chapter, I provide a brief conclusion including the major works done in this thesis covering the process flows and process developments to make Si nanowire platforms on both bulk and SOI to even fabricate down to 4 nm cross-section NWs, integration of local stressors as CMOS boosters to such platforms to improve the carrier mobility and finally, TCAD device simulation to study the corner effects and support the transport analysis in deeply scaled channel cross-section NW MOSFETs. This thesis addresses some technological challenges e.g. including local stressors for 3D suspended channels, subthreshold behavior optimization in multi-gate devices using volume conduction mechanism and transport analysis in deeply scaled cross-section channels. This Ph.D. work includes extensive fabrication, optical/electrical characterization methods in nanoscale supported by extensive TCAD device simulations.

2 Introduction

The first transistor, a germanium-based PNP point-contact device, was demonstrated in 1947 at Bell Labs by W. Shockley, J. Bardeen and W. Brattain [1]. The first bipolar junction transistor (BJT) [2] and metal oxide semiconductor field-effect transistor (MOSFET) [3] were introduced in 1950 and 1959, respectively. The first integrated circuit (IC) [4] and complementary MOSFET (CMOS) logic [5] were demonstrated in 1958 and 1963, respectively. Since 1963, microelectronics has been one of the most promising technologies enabling further inventions of e.g. computers and mobile phones, growing exponentially according to the Moore's law [6]. Moore's law predicts that the number of transistors in an integrated circuit doubles every two years, a trend existed for about five decades and a base for International Technology Roadmap for Semiconductors (ITRS) [7] roadmap to make or invent smaller and faster transistors for every technology generation by both industry and academia (see Fig. 2.2).

2.1 Aggressive CMOS downscaling

Increasing the number of transistors to do faster computations is a desire, needing downscaling of the transistor dimensions to increase the circuit density. Dennard's rule [10] to shrink the key MOSFET parameters by a κ factor is reported in 1974, considering *a constant electric field* and summarized in table 2.1. Anyway, due to limitation on scalability of V_{TH} and OFF

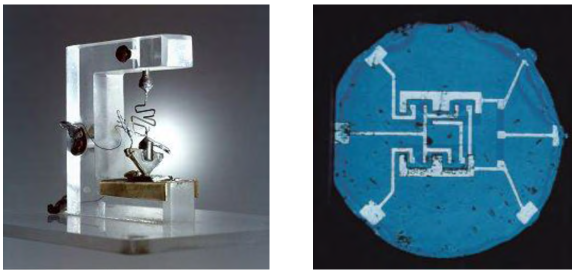


Figure 2.1: The first transistor, a germanium-based PNP point-contact device (left), the first complementary MOSFET (CMOS) logic (right) [8].

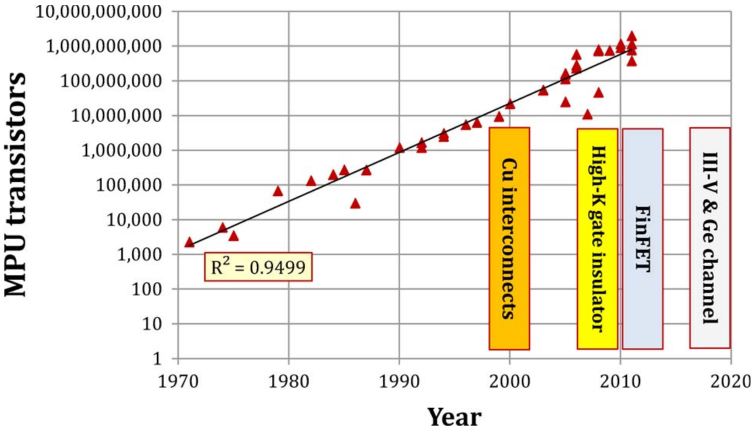


Figure 2.2: The number of transistors per microprocessor chip vs. time [9].

Key MOSFET parameter	Scaling factor (κ>1)
Device dimension (L, W, t_{ox})	$1/\kappa$
Channel doping (N_d, N_a)	κ
Current (I_D)	$1/\kappa$
Voltage (V_D)	$1/\kappa$
Gate capacitance ($\epsilon \cdot A/t_{ox}$)	$1/\kappa$
Circuit delay time ($\sim C_g \cdot V_D/I_D$)	$1/\kappa$
Clock frequency ($\sim I_D/C_g \cdot V_D$)	κ
Circuit power dissipation ($V_D \cdot I_D$)	$1/\kappa^2$
Circuit density ($\sim 1/A$)	κ^2
Power density ($\sim V_D \cdot I_D/A$)	1
Electric field	1

Table 2.1: The nominal MOSFET downscaling procedure for circuit performance enhancement considering a constant electric field.

current, considering non-scalable subthreshold swing of minimum 60 mV/dec. in the typical Si-based MOSFETs, it is not possible to downscale the bias voltage similar to the other parameters. On the other hand, the scaling rule down to ultimate dimensions is limited by various physical concepts e.g. quantum tunneling current in the case of ultra-thin films especially gate oxide. Therefore, high-k/metal-gate stack has been used for the 45-nm technology nodes and beyond to limit the tunneling current while e.g. a 0.7 nm EOT is needed (see Fig. 2.3). On the other hand, using metal-gate suppresses the poly-Si depletion issue, could cause a parasitic capacitance, degrading the MOSFET behavior.

2.2 Short-channel effects and multi-gate MOSFETs

Downscaling of the gate length in the planar MOSFETs leads to losing the channel potential control by the gate, mainly due to influencing the channel potential by drain. This results in several short-channel effects (SCE) e.g. increased OFF current, subthreshold slope degradation,

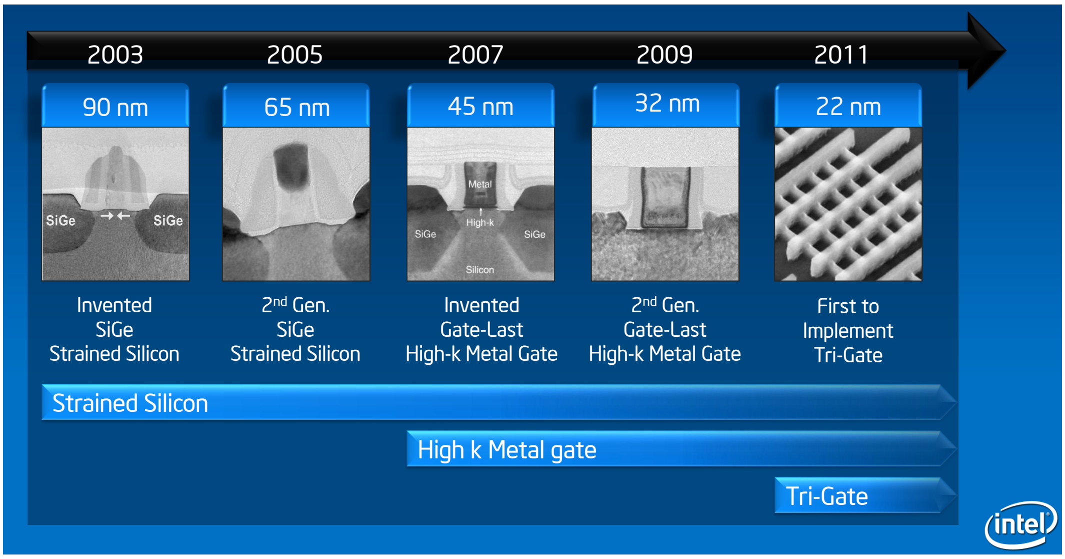

2003
2005
2007
2009
2011
90 nm
65 nm
45 nm
32 nm
22 nm
SiGe
SiGe
Metal
High-k
SiGe
SiGe
Silicon
Invented SiGe Strained Silicon
2nd Gen. SiGe Strained Silicon
Invented Gate-Last High-k Metal Gate
2nd Gen. Gate-Last High-k Metal Gate
First to Implement Tri-Gate
Strained Silicon
High k Metal gate
Tri-Gate
intel

Figure 2.3: Intel's 90 nm technology node and beyond to integrate stressor, high-k/metal-gate and a multi-gate architecture as CMOS boosters while downscaling [11].

threshold voltage roll-off (samller V_{TH} at shorter gate length) and drain-induced barrier lowering (DIBL, smaller V_{TH} at higher V_D). Note that increasing the OFF current is not a desire, causing a passive power consumption.

In order to suppress the short-channel effects in planar devices, including a retrograde (delta) profile under the channel, S/D extensions, halo implants under the S/D extensions, engineer the S/D extensions to minimize the junction depth (X_j) are suggested. In an aggressively scaled MOSFET architecture, the parasitic S/D to bulk substrate capacitances are becoming a major issue that can be significantly minimized using a SOI (Silicon-On-Insulator) technology. In extremely thin SOI (ETSOI) platforms, called also fully-depleted SOI (FDSOI) or ultra-thin body (UTB) SOI, due to a thinner silicon thickness (t_{Si}) than the channel depletion depth, the gate control on the channel is significantly enhanced in comparison to the planar bulk technology. SOI technology is being used for the 130 nm technology node and beyond by AMD. Obtaining sub-10 nm thick SOI devices in an appropriate way, performance issues due to the high series resistance, integration of stressors and finally, quantum confinement and scattering effects are the major challenges in a SOI-based technology.

An alternative way to improve the gate control on the channel and therefore, suppress the short-channel effects is using multi-gate architectures e.g. FinFETs or gate-all-around (GAA) Si nanowires. Note that such architectures can be implemented using a bulk substrate as well. Using the "natural length" parameter (λ), representing the extension of the electric field lines from the S/D into the channel, is a simple and effective way to compare the performance improvement due to the architecture [12]:

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{N \cdot \epsilon_{ox}} \cdot t_{ox} \cdot t_{Si}} \tag{2.1}$$

where N is the number of gates. ϵ_{Si}, ϵ_{ox}, t_{Si} and t_{ox} are the electrical permittivity of the channel and the gate oxide, the thickness of the channel and the oxide, respectively. An architecture would be assuemd to show minimum short-channel effects if the effective channel length, L_{eff}, is more than 6 times longer than the natural length. According to Eq. 2.1, the λ parameter can be reduced further by increasing the number of gates, shrinking the gate oxide and the channel thicknesses, increasing the oxide permittivity (high-k) and decreasing the channel permittivity (channel material engineering).

2.3 Stressors as CMOS boosters for carrier transport enhancement

To overcome the MOSFET performance limitations while downscaling e.g. short-channel effects, high leakage current, velocity saturation and dielectric breakdown, new device architectures (multi-gate) and concepts e.g. NEM and Tunnel-FETs, new materials and strain engineering should be explored. In this thesis, we mianly focus on strain engineering in multi-gate architectures. Note that strain engineering is being used for the 90-nm technology nodes and beyond.

Strain engineering is a low-cost and almost straight forward technique, compatible with the typical CMOS processes, while potentially enabling driving current enhancement up to ~2.0× and ~4.5× in Si-based nMOSFETs and pMOSFETs, respectively without a significant change in the leakage current. Experiments show that uniaxial compressive and uniaxial tensile stresses along the <110> channel orientation with (100) channel surface are the most helpful stresses to provide higher mobility of carriers in PMOS and NMOS Si-based devices, respectively [13].

2.3.1 Physics of strained classical Si-based MOSFETs

In this section, a brief introduction to the physics behind carrier mobility enhancement in nMOSFETs and pMOSFETs due to stress is provided. Further details can be found in [13].

n-type bulk Si: The bulk Si conduction band includes six equivalent degenerate valleys while the minimum energy band is located close to the X point. Applying stress shifts and splits the subbands e.g. <110> longitudinal tensile stress leads to downshift and upshift in the energy of Δ_2 and Δ_4 subbands (e.g. a 40 meV separation under 1 GPa), respectively, causing repopulation of electrons from the Δ_4 to the Δ_2 subband (see Fig. 2.4-a). The effective masses of Δ_2 and Δ_4 subbands are 0.19 m_0 and 0.315 m_0, respectively. Therefore, the electron repopulation helps to reduce the average effective mass and enhance the carrier mobility. Surface roughness and intervalley phonon are also the dominant scattering mechanisms in strained-Si. Conduction subband splitting suppresses the intervalley phonon scattering due to the smaller density of states and therefore, increases the carrier mobility as well.

nMOSFETs: Unlike bulk Si, the Δ_4 and Δ_2 subbands are non-degenerated in nMOSFETs while the energy splitting depends on the magnitude of electric field and the difference in their

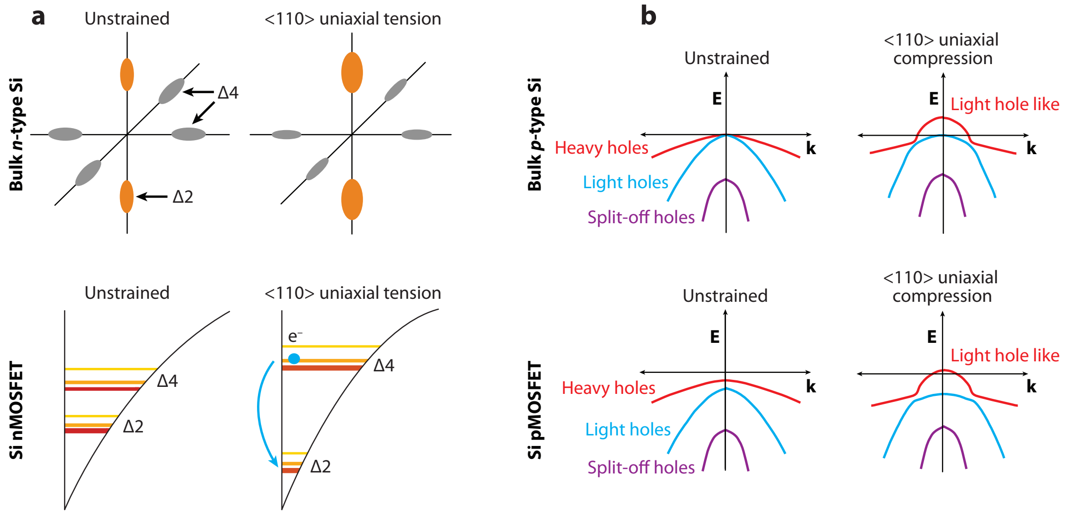

a
Unstrained
<110> uniaxial tension
Bulk n-type Si
Δ4
Δ2
Si nMOSFET
Unstrained
<110> uniaxial tension
e⁻
Δ4
Δ2
Δ4
Δ2
b
Unstrained
<110> uniaxial compression
Bulk p-type Si
E
k
Heavy holes
Light holes
Split-off holes
E
Light hole like
k
Si pMOSFET
Unstrained
<110> uniaxial compression
E
k
Heavy holes
Light holes
Split-off holes
E
Light hole like
k

Figure 2.4: Simplified conduction band engineering in n-type bulk Si and (100) Si nMOSFET by <110> uniaxial tensile stress (a), simplified valence band engineering in p-type bulk Si and (100) Si pMOSFET by <110> uniaxial compressive stress (b) [13].

out-of-plane confinement effective mass. Therefore, electrons already predominated the lower-energy Δ_2 subband causing a smaller stress-based effective mass change in comparison to bulk Si.

p-type bulk Si: In relaxed bulk Si, the minimum of valence band occurs at the Γ point. The heavy-hole (HH) and light-hole (LH) bands are degenerated while the spin-orbit split-off band, located 44 meV below, does not contribute significantly in the hole transport (see Fig. 2.4-b). HH and LH bands include 80 and 20% of holes, having effective mass of $0.59m_0$ and $0.15m_0$ along <110> orientation, respectively. Inducing <110> uniaxial compressive stress lifts the degeneracy and induces band warping, causing effective mass reduction and therefore, hole mobility enhancement. Note that the contribution on band split in comparison to band warping in the hole mobility enhancement at low stress level (>-1GPa) is negligible, due to the higher Si phonon energy (61.3 meV).

pMOSFETs: Lifting the degeneracy of HH and LH due to the surface electric field confinement, can be higher at higher electric fields, together with additional stress-based band split can be larger than the optical phonon energy and can enhance further the hole mobility. Therefore, suppressing the optical phonon scattering is more significant in comparison to p-type bulk Si.

2.3.2 Optimum channel strain engineering for NMOS and PMOS devices

<110> and <110> are the main orientations, being considered to induce uniaxial or biaxial tensile or compressive stress to the MOSFET channels. Note that the highest electron and hole mobility values in relaxed nMOSFET and pMOSFET devices correspond to the (100) and (110) surfaces in <110> orientation, respectively. Carrier mobility enhancement for each

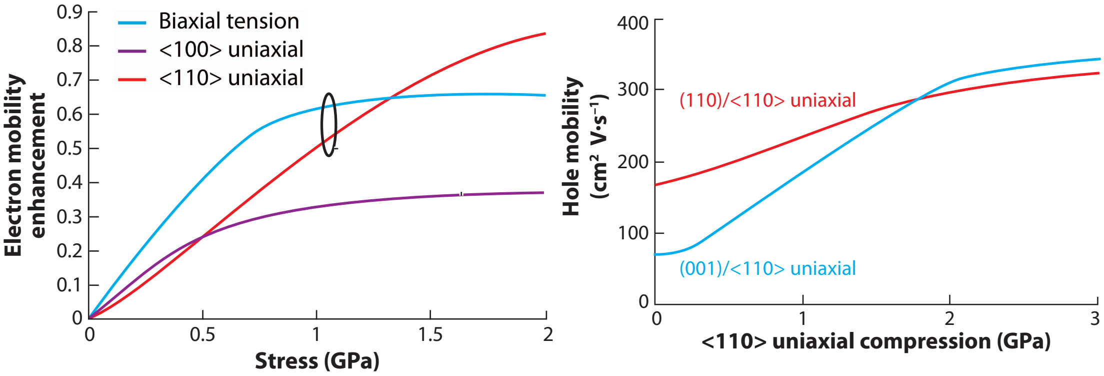


Figure 2.5: Electron mobility enhancement factor for various tensile stress types in (100) Si nMOSFET (left), hole mobility engineering in (100) and (110) Si pMOSFETs using <110> uniaxial compressive stress (right) [13].

surface and orientation can be described by band splitting, band warping, effective mass and scattering rate.

(100) nMOFETs: In general, electron repopulation in (110) surface nMOSFETs under uniaxial or biaxial tensile stress does not provide a significant effective mass change and therefore, does not reflect a desired electron mobility enhancement. Therefore, in the rest of this section, we only concentrate on the (100) nMOSFETs. At low stress (<0.5 GPa), biaxial, <100> and afterward, <110> tensile stresses show the highest electron mobility enhancement, respectively (see Fig. 2.5-left). Anyway, the mobility enhancement for both biaxial and <100> uniaxial tensile stresses saturates quickly due to the already repopulated Δ_2 low energy subband and therefore, the average effective mass does not change significantly at higher stress levels. On the other hand, at the same stress magnitude, the subband splitting for <110> uniaxial tensile stress is lower, leading to repopulation of electrons even at stress levels up to 2.0 GPa. Δ_2 band warping for <110> uniaxial tensile stress causes further decrease in the effective mass as well.

(100) pMOFETs: In this section we only concentrate on <110> uniaxial compressive stress, due to providing the most promising hole mobility enhancement in pMOSFETs. In relaxed pMOSFETs, (110) has almost twice hole mobility than (100) surface but as shown in Fig. Fig. 2.5-right, the saturated hole mobility values are almost the same at <-3 GPa uniaxial compressive stress. (100) has a higher effective mass change and therefore, higher hole mobility enhancement. On the other hand, a higher band splitting in (110) pMOSFETs, leading occupation of the ground state by holes, causes less stress-based hole repopulation in comparison to (100) pMOSFETs. Finally, ~4.5× and ~2.0× hole mobility enhancements for (100) and (110) pMOSFETs are reported, considering that the final saturated hole mobility values are almost similar.

2.3.3 Stress platforms for planar Si-based MOSFETs

Several methods are reported to include stress in the channel of planar MOSFETs. In this section, we provide a brief introduction to such stress platforms:

Strained substrate: Three methods can be used to make a strained Si layer on a substrate, providing a global stressor technique [14]:

- SiGe epitaxial growth on a Si substrate followed by Si growth on the SiGe layer to make a strained Si thin film (see e.g. [15]).
- Ge diffusion into a SOI layer to form a SiGe thin film, followed by Si growth to make a strained Si thin film.
- Transfer the strained Si layer of a strained substrate, e.g. fabricated using one of the methods above, to another substrate with an insulator layer on top using wafer bonding and afterward, removing the SiGe layer to make a strained SOI wafer without the presence of SiGe.

This technique induces biaxial tensile stress in the Si thin film while the stress level can be engineered by SiGe stoichiometry and thin film thicknesses.

Capping layer: Deposition of capping layers (called also Contact Etch Stop Layer, CESL) e.g. Si_xN_y with residual thin films can induce uniaxial stress to the channel, while the type of stress depends on the sign of stress in the capping layer [16]. Note that a thin film with a residual biaxial compressive or tensile stress tends to stretch or shrink, respectively, inducing a uniaxial stress to the channel. Therefore, the type of the uniaxial stress (tensile or compressive) is similar to the biaxial stress in the capping layer. The residual thin film stress in the Si_xN_y capping layer can be engineered by deposition method (e.g. PECVD, LPCVD), stoichiometry engineering in the thin film and deposition parameters e.g. temperature. Anyway, such a stress level in the Si_xN_y thin film can barely exceed ~2.5 GPa (biaxial compressive or tensile stress), inducing up to ~ ±1 GPa to the channel (e.g. see [17]). Therefore, other capping layers e.g. diamond-like carbon (DLC) can be deposited including higher levels of stress e.g. below -6 GPa is demonstrated in [18] to be able to induce a higher level of stress to the channel. Note that an appropriate stressor technology should be scalable, with minimum degradation of the stress level, parallel to the aggressive downscaling of the device dimensions.

Epitaxial thin film growth in the recessed S/D regions: Epitaxial growth of thin films e.g. SiGe or SiC in the recessed S/D regions can induce uniaxial compressive and tensile stress to the channel [19]-[21], respectively, mainly due to the lattice mismatch.

Stress Memorization Technique (SMT): Deposition of a capping layer including intrinsic tensile thin film stress and afterward, an annealing step e.g. spike annealing to e.g. activate the dopants was found to transfer stress from the capping layer to the channel. Interestingly, the stress remains even after removing the capping layer [22] while its origin is under various experimental investigations [23]-[24].

Shallow trench isolation (STI): Filling the STI gap with e.g. SiO_2, including residual biaxial thin film compressive stress can induce local biaxial compressive stress to the channel [25]. The oxide layer tends to expand horizontally, inducing local biaxial compressive stress to the channel. The smaller the distance between the STI and the channel, the higher the level of stress in the channel.

Silicidation in S/D: The silicidation process [26], due to intrinsic or growth stress, epitaxial thin film stress or thermal stress due to a higher thermal expansion coefficient (CTE) than Si for the common silicides e.g. NiSi can induce local biaxial stress to the channel [27]. Note that the final type of stress in the channel (compressive or tensile) depends on whether the stress-based silicidation or the isolation components are dominant [27].

2.3.4 Stress platforms for multi-gate MOSFETs

The mentioned stress platforms are compatible to the bulk and SOI planar CMOS processes. To enhance the performance of the multi-gate devices for the 32 nm technology nodes and beyond, innovative stressor technologies compatible with the scaled multi-gate devices with the capability of scaling down parallel to the downscaling of the channel should be developed. For the attached multi-gate devices to the BOX layer (e.g. Fin-FET but not GAA), four stressor technologies have been reported until now: epitaxial films in the S/D [28]-[29], CESL [30], strained substrate [31] and metal gate strain [32].

For the suspended GAA devices, because of a three-dimensional architecture, inducing stress in the channel properly is even more challenging than the attached multi-gate devices and until now, only six methods have been reported and summarized in table 2.2.

2.4 Si nanowire platforms

Si nanowires can be fabricated using a top-down [40] or a bottom-up approach [41]. In a top-down platform, Si nanowires are formed and positioned precisely using lithography and etching. The nanowires can be fabricated in a dense array format. On the other hand, a bottom-up includes synthesizing Si nanowires by catalytic growth and therefore, the precise position of nanowires is not well-defined and therefore, making a dense array is pretty challenging. The growth can be in various crystalline orientation as well but the surface roughness is minimized in such nanowires. Note that the surface roughness issue can be minimized in top-down approaches using hydrogen annealing [42] or stress-limited oxidation [43].

In this thesis, we focus on the top-down Si nanowires for strain engineering and transport analysis on bulk and SOI substrates considering both inversion and accumulation-modes. As an example, we provide three top-down Si nanowire platforms in horizontal and vertical

	Architecture	Cross-section (nm)	Stressor	Stress type	Stress (GPa)/ Strain (%)
Najmzadeh, ISDRS 2011 [33]	Buckled GAA Si NWs/ rounded triangular	4×9	Metal gate and local oxidation	Uniaxial tensile	~+5.6/3.3%$^{+}$
Singh, EDL 2007 [34]	Buckled GAA Si NWs/ circular	≈ 5-7 nm diameter	Metal gate	Uniaxial tensile	~+4.0/3.0%$^{+}$
Najmzadeh, INFOS 2009 [35] - Moselund, IEDM 2007 [36]	Buckled GAA Si NWs/ triangular	≥ 100×100	Local oxidation	Uniaxial tensile	+2.6/1.5%$^{\times}$
Hashemi, IEDM 2008 [37]	Straight GAA Si NWs/ rounded rectangular/circular	49×9 - 8×7	Strained SOI substrate	Uniaxial tensile	+2.0/1.2%$^{\times}$
Liu, EDL 2010 [38]	Straight GAA Si NWs/ rectangular	17×36	DLC liner	Uniaxial comp.	>-0.75/-0.44%$^{+}$
Li, IEDM 2007 [39]	Straight GAA Si NWs/ circular	8 nm diameter	SiGe S/D	Uniaxial comp.	>-0.80/-0.47%$^{+}$

Table 2.2: The available methods to integrate local or global stressors as CMOS boosters to include uniaxial stress (tensile or compressive) in multi-gate suspended Si nanowire platforms. Si Young's modulus of 169 GPa was used for the stress/strain conversion regarding the works not reporting both stress and strain or the used Young's modulus values.
$^{+}$: Stress estimation based on simulation, electrical characterization or visual buckling.
$^{\times}$: Stress measurement on the GAA Si NWs using micro-Raman spectroscopy.

direction.

2.4.1 Samsung bulk top-down Si nanowire platform - horizontal NWs

Fig. 2.6 illustrates the process flow. A damascene-gate process was used to define the gate length instead of sophisticated lithography. The process details can be found in [44], briefly including epitaxial SiGe/Si growth and STI trench formation (1), SiN hard mask trimming for the nanowire definition (2), DHP oxide filling in the STI and CMP (3), damascene gate formation (4), damascene gate etching (5-6), field oxide recess (7), SiGe removal and hydrogen annealing (8) and finally the gate stack step (9). The process provides twin Si nanowires on bulk Si substrate with a ~30 nm gate length and down to 4 nm Si nanowire diameter [45].

2.4.2 IBM SOI top-down Si nanowire platform - horizontal NWs

Fig. 2.7 shows a process flow to make top-down Si nanowires on a SOI substrate. The initial Si nanowire definition was done using e-beam lithography and RIE. Hydrogen annealing was performed to smooth the NW side-walls, realign the side-walls to the crystal planes, reshape the cross-section and thinning the NW by Si migration to the SOI S/D pads. A sacrificial thermal oxidation was done to shrink the NW cross-sections to even sub-3 nm. Gate stack (Hf-based dielectric, TaN metal-gate and poly-Si capping layer), gate definition, spacer, epitaxial Si growth at the S/D, ion-implantation of S/D and silicidation are the further steps. Following almost similar process flows while using a strained SOI substrate (a global stressor), GAA

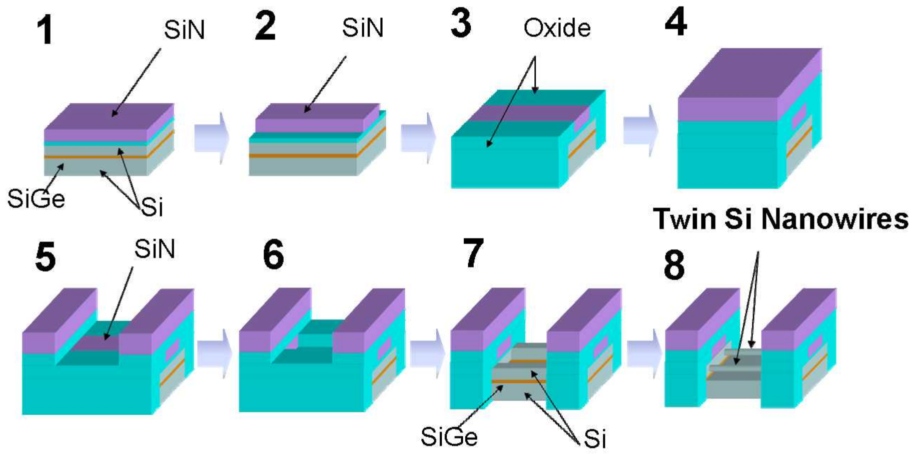


Figure 2.6: Samsung top-down bulk platform to make horizontal GAA twin circular Si nanowire MOSFETs using a damascene-gate process [44].

strained NW MOSFETs as well as multi-gate strained Si NWs attached to the BOX layer can be obtained (see e.g. [37] and [48]).

2.4.3 IME-Singapore bulk top-down Si nanowire platform - vertical NWs

According to Fig. 2.8, vertical Si pillars can be fabricated using a SiN hard mask, e-beam lithography and dry etching (a) [47]. Thermal oxidation at e.g. 1050 °C can convert the pillars into Si nanowires with smaller cross-sections and smoother side-walls (b). HDP oxide deposition (250 nm) followed by DHF wet etching (c) are the further steps. Due to the non-conformal HDP deposition, oxide is thinner on the Si side-walls and therefore, a controlled oxide wet etching can keep a thin oxide layer on the substrate to act as an isolation layer. Gate stack step (d) was done using ~5/30 nm of SiO_2/poly-Si followed by gate patterning (lithography and etching). HDP oxide deposition and wet etching, followed by Si dry etching was done to open up the poly-Si only on top of the nanowire (e-f). Stripping the oxide layers, ion-implantation, annealing to activate the dopants, and finally, metallization are the further steps (g-h). Note that the gate length in a vertical nanowire platform can be determined by deposition and etching steps but not lithography.

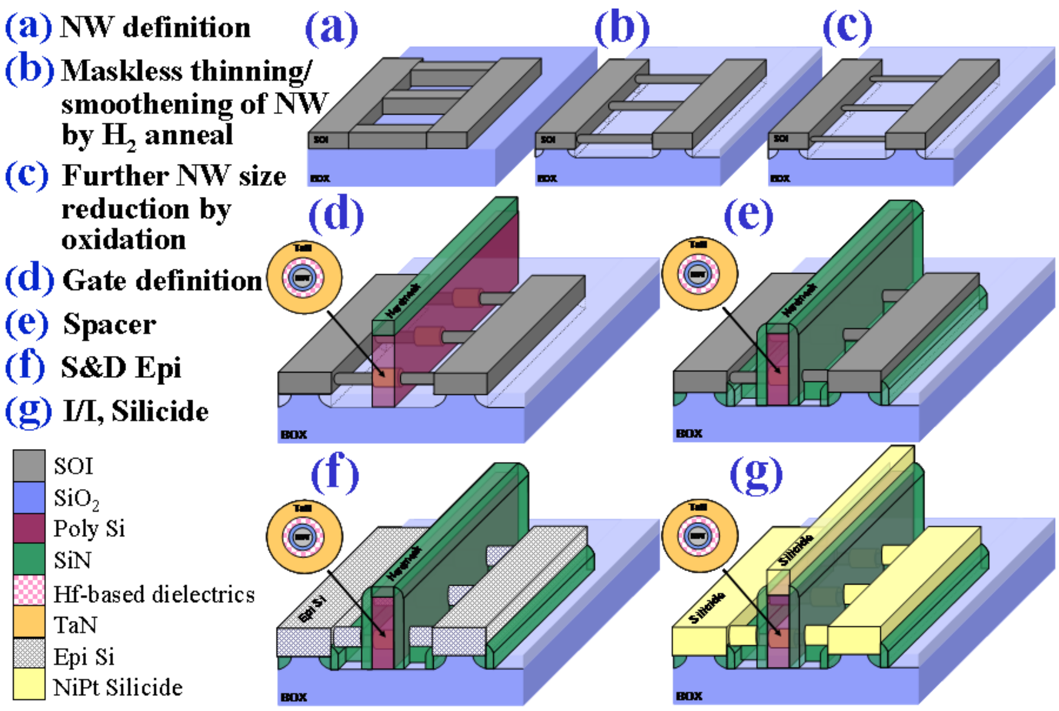

(a) NW definition
(b) Maskless thinning/ smoothening of NW by H_2 anneal
(c) Further NW size reduction by oxidation
(d) Gate definition
(e) Spacer
(f) S&D Epi
(g) I/I, Silicide
SOI
SiO_2
Poly Si
SiN
Hf-based dielectrics
TaN
Epi Si
NiPt Silicide
(a)
(b)
(c)
(d)
(e)
(f)
(g)
SOI
BOX
TaN
Hardmask
Epi Si
Silicide

Figure 2.7: IBM top-down SOI platform to make horizontal array of GAA Si nanowire MOSFETs with a circular cross-section [46].

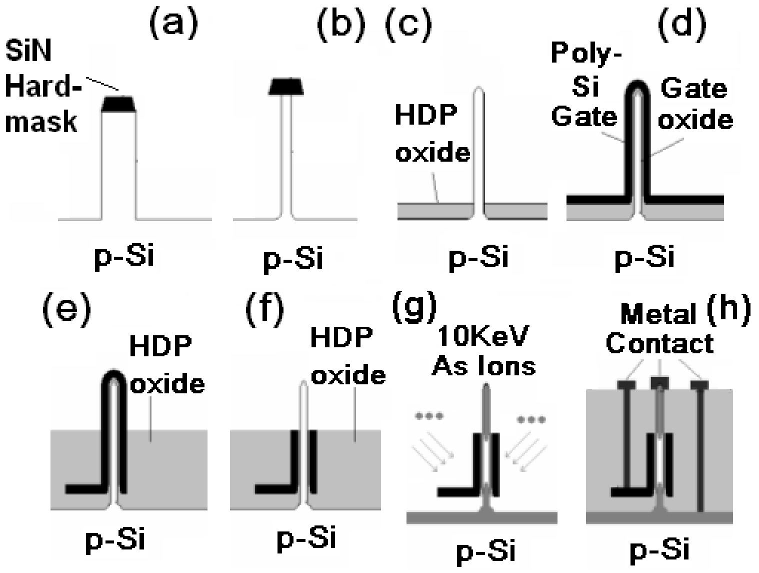

(a)
SiN Hard-mask
p-Si
(b)
p-Si
(c)
HDP oxide
p-Si
(d)
Poly-Si Gate
Gate oxide
p-Si
(e)
HDP oxide
p-Si
(f)
HDP oxide
p-Si
(g)
10KeV As Ions
p-Si
Metal Contact
(h)
p-Si

Figure 2.8: IME-Singapore top-down bulk platform to make vertical GAA Si NW MOSFETs [47].

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3 Multi-gate buckled Si NWs on bulk for high electron mobility and logic

The concept of oxidation-induced strain (OIS), accumulation of uniaxial tensile stress in suspended naked Si beams after thermal Si oxidation and stripping oxide, was originally reported in 2005 by the University of California, Santa Barbara in [1]. The origin of that stress was still unknown but it was assumed to be associated with the injection of self-interstitial silicon atoms from the oxidation front during oxidation [1]. It is worth mentioning that the maximum level of uniaxial tensile stress after stripping oxide was not exceeding 0.012%, after consumption of even 90% of total thickness of 50 μm long Si beams [2]. In another works, done by Swiss Federal Institute of Technology - EPFL in 2007 [3], accumulation of quite higher uniaxial tensile stress level, up to 2.0 GPa, in the Si nanowires is reported, by oxidation of Si nanowires with a hard mask on top and after stripping the grown oxide and the hard mask. In this chapter, the origin of such accumulation of uniaxial tensile stress is investigated and reported in details, using fabrication of Si nanowires on bulk Si by hard mask/spacer technology and 0.8 μm photolithography [4]-[5]. Extensive stress measurement was one on the suspended buckled Si nanowires using an optical micro-Raman spectroscopy setup and up to 2.6 GPa uniaxial tensile stress is reported in the buckled nanowires. Note that the electron mobility enhancement due to the uniaxial tensile stress is being saturated to ≈100% at >≈2.0 GPa [6]. Such high levels of uniaxial tensile stress in suspended Si channels can be used for further CMOS booster applications e.g. local Si band-gap modulation to enhance band-to-band tunneling current in multi-gate Si nanowire Tunnel-FETs, needing e.g. >4 GPa uniaxial tensile stress [7]-[8] considering no plastic deformation or fracture [9]. For this purpose, the stress level in the suspended Si nanowires can be engineered using integration of various local stressors e.g. local oxidation and metal-gate strain [10]-[13].

Electrical characterization of gate-all-around (GAA) buckled Si nanowire and non-strained relaxed multi-gate MOSFETs on bulk Si was done at room temperature and stress-based low-field electron mobility enhancement is reported [5]. Correlation of uniaxial tensile stress profile in the buckled Si nanowire channel with its I-V characteristics, to extract local carrier mobility enhancement in the channel, is reported [5].

As a first step to make vertical stack of Si nanowires, to enhance the current density, multi-gate buckled self-aligned dual Si nanowires were fabricated on bulk Si using SiO_2 hard mask/spacer technology and 0.8 μm photolithography [14]. Making a 3D stack of multi-gate devices using various techniques e.g. dual SOI wafer [15], epitaxial Si-SiGe stacks [16]-[17] and stress-limited oxidation [18] were previously reported. Among the 3D integration techniques, stress-limited oxidation is the simplest way used previously to make dual Si nanowires based on a vertical Fin on SOI [18] and vertical stack of Si nanowires from a pre-shaped vertical Fin using scalloping on bulk Si [19]. A well-controlled stress-limited oxidation can even cause keeping a thin Si bridge between the vertical Si nanowire cores, leading to a significant improve in the driving current [20] while keeping the nanowires in a more self-aligned manner and helping to suppress the sticking issue in the dense array of parallel nanowires due to the possible buckling in the case of e.g. using local stressors and therefore, providing more freedom to make a more dense array structure using the top-down Si nanowire platforms. Finally, a simple logic gate is demonstrated using multi-gate Si nanowires on bulk Si. This is a first step to investigate improvement of digital CMOS logic circuit characteristics using CMOS boosters e.g. local stressors in 3D stack of Si nanowires [21]. In this chapter, we only focus on lightly doped channel inversion-mode MOSFETs, since the nanowires are being fabricated on a bulk Si substrate, needing only one implantation step and therefore, a more straight forward process flow in comparison to [10]-[13].

3.1 Local oxidation as a local stressor technology

Including stress in the multi-gate suspended Si channels is a technology challenge and only a few techniques are reported until now: SiGe S/D by Samsung in 2007 [22], metal-gate strain by Institute of Microelectronics-Singapore in 2007 [23], local oxidation by Swiss Federal Institute of Technology - EPFL in 2007 [3], suspending Si nanowires from a strained SOI substrate, as a global stressor, by Massachusetts Institute of Technology in 2008 [24], diamond-like carbon (DLC) by National University of Singapore in 2010 [25] and finally, local oxidation and metal-gate strain by Swiss Federal Institute of Technology - EPFL in 2011 [10]-[12].

In this section, we investigate stress development during local oxidation of Si nanowires in the presence of a tensile Si_3N_4 hard mask on top (before oxidation, after oxidation and after stripping the Si_3N_4/SiO_2 thin films) considering two oxidation temperatures. The origin of stress development in the buckled Si nanowires, based on the extensive stress measurements using micro-Raman spectroscopy, will be discussed in details.

3.2 Process flow using Si_3N_4 hard mask and spacer

The process flow to make suspended buckled Si nanowires is schematically shown and described in Fig. 3.1. Note that this process is the adapted process flow reported originally in [3], considering suspension of W0.8 Si nanowires before oxidation by isotropic dry Si etching to investigate the effect of oxidation on suspended Si nanowires as well. The W1.0 Si nanowires

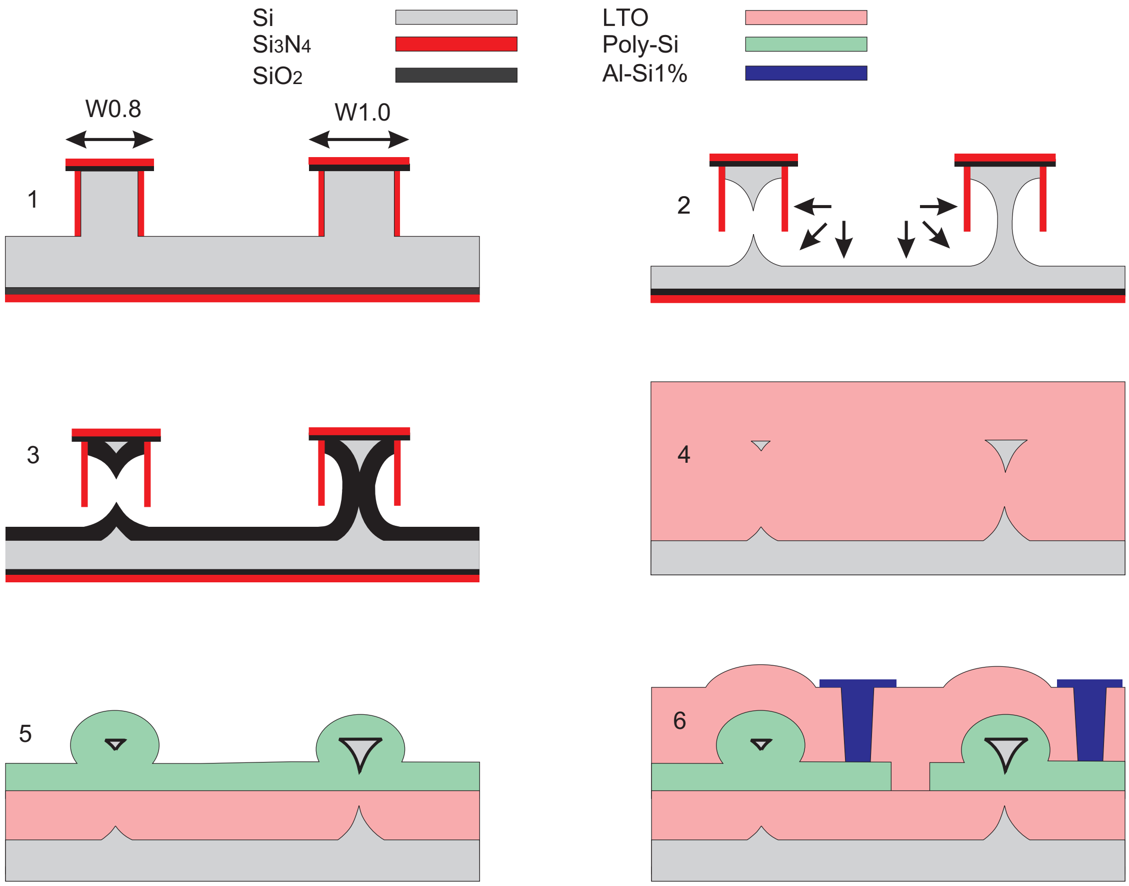

Figure 3.1: Process flow to make GAA suspended buckled Si nanowire MOSFETs using a top-down Si nanowire platform. W08 and W10 represent the initial 0.8 and 1.0 μm mask nanowire width, respectively.

are attached to the substrate before the oxidation step, while being suspended after the oxidation step. The wider structures e.g. W1.2 will be attached to the substrate even after the oxidation and stripping steps. The gate stack was chosen to be SiO$_2$/N$^+$ in-situ doped poly-Si to minimize the poly-Si depletion due to the challenging poly-Si implantation underneath the Si nanowire, can cause a weak gate control on the channel, leading to subthreshold slope, leakage current and driving current degradations [26].

All the process steps have been verified by 2D process simulations using TCAD Dios version 10.0 and TCAD Sentaurus Process version A-2007.12 in our earlier work [27]. As a first step, 100 mm (100) p-type (0.1-0.5 Ω·cm) bulk prime Si wafers were oxidized using dry oxidation at 950°C to grow 15 nm of SiO$_2$ and afterward, 80 nm of Si$_3$N$_4$ was deposited using LPCVD at 770°C to create the hard mask stack. The Si$_3$N$_4$ thin film includes 1.3 GPa biaxial residual tensile thin film stress. The designed pattern, all including the ⟨110⟩ channel direction, was transferred directly to the wafers using 0.8 μm photolithography. In the design, the width and the length of the wires vary from 0.8-1.8 μm and 2.0-20.0 μm, respectively. The hard mask was

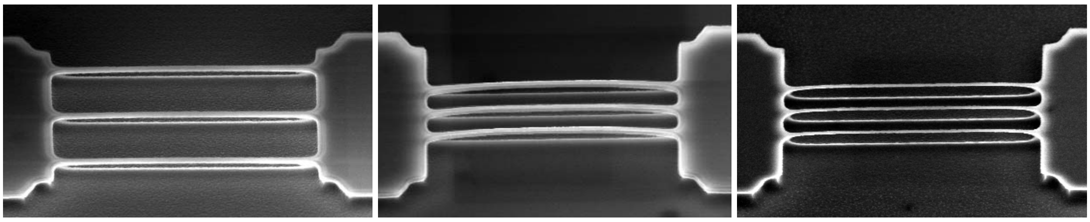

Figure 3.2: SEM micrographs (tilted view) of suspended 20 μm long W0.8 Si nanowires after different process steps: a tensile hard mask on top before oxidation (left), after sacrificial wet oxidation at 850 °C (middle) and after the stripping step (right), representing reproducibility and controllability of the local strain technique.

etched using anisotropic fluorine-based dry etching. Afterward, Si was etched anisotropically to create 300-400 nm high ribs. A sacrificial wet oxidation at 850 °C was done to nominally oxidize 135 nm of Si side-walls and the oxidized side-walls were etched using a BHF solution (NH_4F(40%) : HF(49%) [7:1]). 35 nm of Si_3N_4 was isotropically deposited on the wafer using LPCVD at 770°C. The Si_3N_4 thin film was etched anisotropically using a fluorine-based dry etching to keep the Si_3N_4 layer only on the side-walls and on the top of the ribs. Si was etched isotropically using dry etching to create the first NW shape and suspend the W0.8 NWs. To shrink further the cross-section dimension of the NWs and to oxidize the remained Si between the W1.0 NW and the substrate, the NWs were thermally oxidized to nominally consume 135 nm of (100) Si. In this step, two oxidation temperatures were investigated (wet oxidation at 850 and 1050°C). After stripping the hard mask and the grown oxide layer using a 49% HF solution, the W08 and W10 NWs were released. Fig. 3.2 shows the SEM micrographs of W0.8 nanowires before/after the oxidation at 850 °C and after the stripping steps.

The process flow was finalized using isolation (LTO deposition, CMP and LTO etching), gate stack deposition (15/200 nm of SiO_2/N^+ in-situ doped poly-Si), gate patterning (0.8 μm photolithography), S/D implantation and annealing, metallization (AlSi-1%) and sintering.

3.3 Direct stress measurement on buckled Si nanowires using micro-Raman spectroscopy

Micro-Raman spectroscopy can be used for direct stress measurement on the naked Si samples [28], [29] or on the Si samples typically covered by transparent thin films e.g. SiO_2. Uniaxial tensile and compressive stresses downshift and upshift the micro-Raman peak, respectively, and the strain value can be extracted directly from the wavenumber shift [28].

In this section and for the buckled Si nanowires on bulk Si substrate with cross-sections down to 100 nm, a micro-Raman optical setup was used initially with 0.2 cm^{-1} nominal resolution at 20 $°C$. Note that for the buckled deeply scaled cross-section Si nanowires (e.g. sub-5 nm) such measurements on a bulk substrate is pretty challenging due to the low Raman signal level of strained Si nanowires in comparison to the bulk Si or the Si carrier wafer Raman

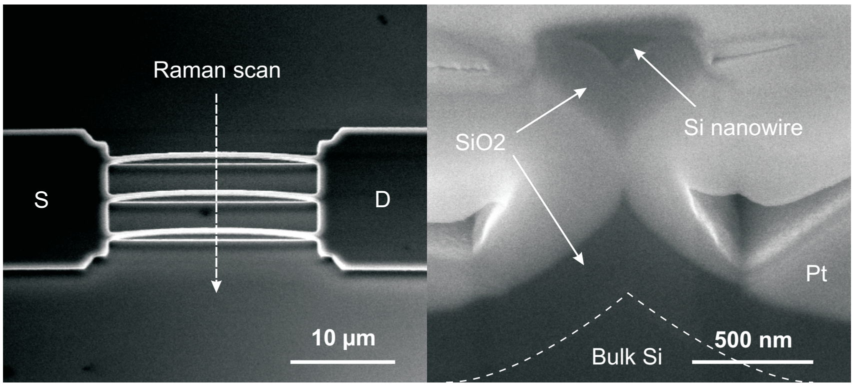

Figure 3.3: SEM micrograph from an array of Si nanowires with a tensile nitride hard mask on top after wet oxidation (left), the corresponding SEM nanograph cross-section from the middle of the suspended Si nanowire (right).

signal. Including a metal layer in the gate stack step e.g. as stressor is making even the stress measurement method based on only optical micro-Raman spectroscopy non-straight forward. Therefore, to magnify the obtained Raman signal from more scaled nanowires (sub-40 nm down to sub-4 nm cross-sections on a SOI substrate [10]-[13]) including ALD high-k/metal-gate stack as well, we modified our stress measurement method using an optical setup based on Tip-Enhanced Raman Spectroscopy (TERS) [30] to provide further rooms to obtain the needed Raman signal from deeply scaled cross-section strained Si nanowires.

In this section and using an optical micro-Raman spectroscopy, a laser beam with 514.5 nm wavelength was focused on the suspended Si nanowires (see Fig. 3.3), having 762 nm penetration depth in Si. Note that the penetration depth should be higher than the Si nanowire thickness (≥100 nm) to obtain both Raman spectra from the buckled Si nanowire and the relaxed bulk Si substrate underneath as a reference. According to Fig. 3.4, corresponding to the stress measurement at the middle of a 20 μm long W0.8 Si nanowire after stripping the Si_3N_4 and the SiO_2 thin films, only two peaks are detectable in the Raman spectra (using Lorentzian peak fitting [28]), corresponding both buckled Si nanowire and non-strained bulk Si. The shift in the wavenumber ($\Delta\omega$) can be translated to tensile stress (uniaxial or biaxial, depending on geometry) by [5]:

$$\sigma_{xx} + \sigma_{yy}[GPa] = -\frac{\Delta\omega[cm^{-1}]}{4.596} \tag{3.1}$$

Note that due to no micro-Raman peak upshift observation above ω>520.6 cm^{-1}, local buckling of the Si nanowire (due to a local stressor but not an external force e.g. wafer bending) provides a complete uniaxial tensile stress across the Si nanowire cross-section, even at the bottom side of the Si nanowire.

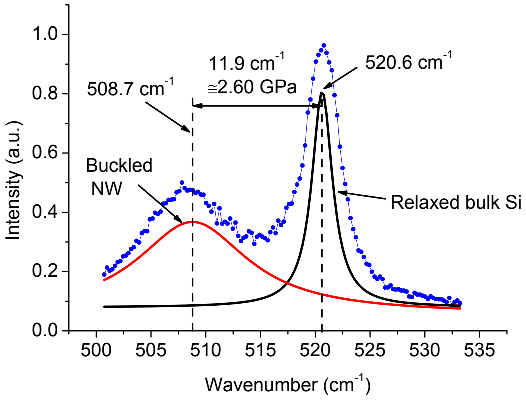

Figure 3.4: Micro-Raman spectra at the middle of a buckled 20 μm long naked W0.8 Si nanowire on bulk Si (850 °C wet oxidation). Only two peaks could be detected in the spectra (relaxed bulk Si and buckled Si nanowire), representing a pure uniaxial tensile stress across the Si nanowire cross-section even at its bottom side.

3.3.1 Stress profile along the buckled nanowires

Fig. 3.5 shows the measured strain values along two 5.0 μm long naked buckled W0.8 Si nanowires after oxidation at two different temperature (850 and 110 °C) and stripping steps. Both curves show a non-uniform and almost symmetric distribution of stress along the wires with a maximum almost at the middle of the wire, explained in part by a non-uniform and symmetric distribution of Si thickness along the nanowire (being thinner at the middle).

According to this study, the stress peak is occurring at the middle of the buckled Si nanowires and its value is becoming almost constant ≈1.5-2.0 μm far from the S/D anchors [38] for the longer nanowires. Therefore, in this chapter and for a straight forward built-in stress analysis during the process, we do stress measurement across the middle of buckled Si nanowires to report the maximum level of stress for the shorter nanowires or the approximate constant stress level at the middle parts of the long buckled nanowires.

3.4 Built-in stress analysis during the process

Fig. 3.6 shows the summary of the process flow together with the built-in stress analysis during the main process steps of the W0.8 nanowires (before oxidation, after oxidation and after the stripping step). Fig. 3.7 shows the measured peak of tensile stress along the W0.8 Si nanowires before/after wet oxidation at 850 °C and after the stripping step vs. nanowire length. In this part, we first analyze stress development in the W0.8 nanowires and afterward, we compare the results with the W1.0 buckled nanowires.

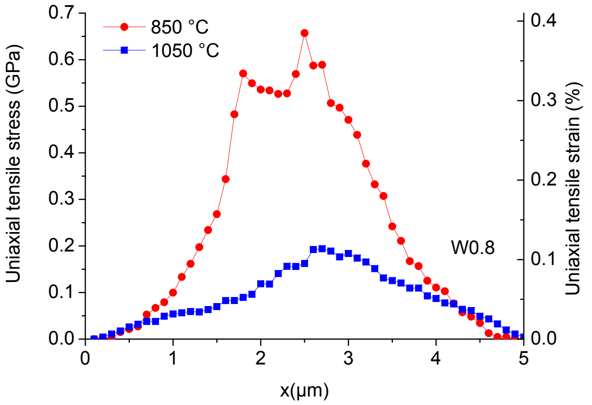

Figure 3.5: Tensile strain profiles along two 5 μm long W0.8 Si nanowires after wet oxidation (at 850°C and 1050°C) and stripping steps.

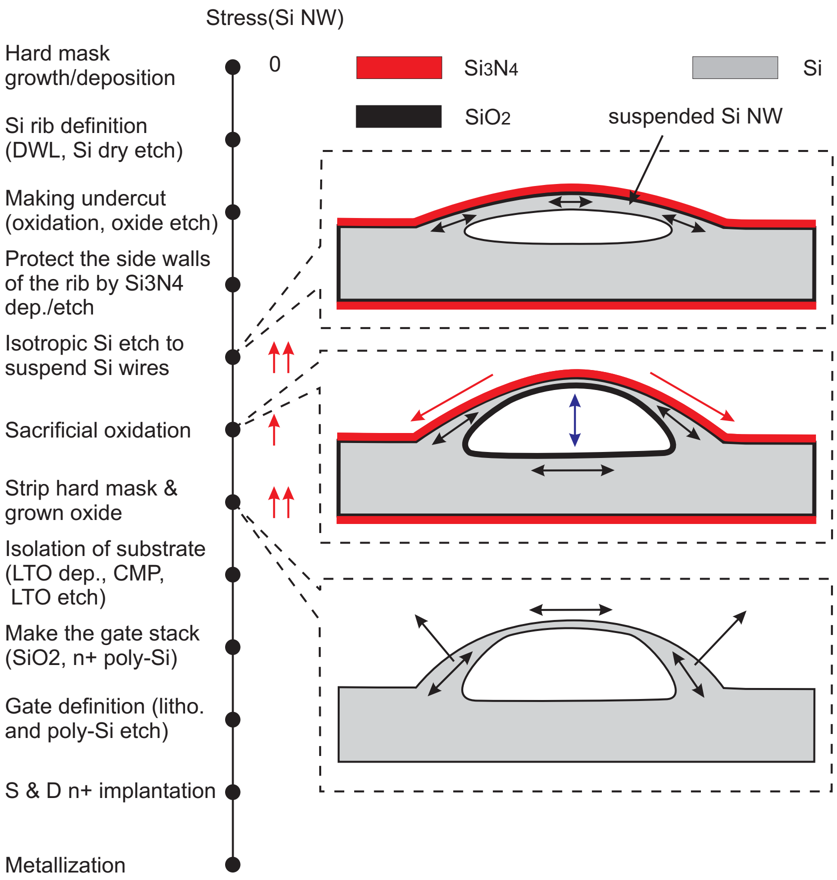
Stress(Si NW)
0
Si3N4
Si
SiO2
suspended Si NW
Hard mask growth/deposition
Si rib definition (DWL, Si dry etch)
Making undercut (oxidation, oxide etch)
Protect the side walls of the rib by Si3N4 dep./etch
Isotropic Si etch to suspend Si wires
Sacrificial oxidation
Strip hard mask & grown oxide
Isolation of substrate (LTO dep., CMP, LTO etch)
Make the gate stack (SiO2, n+ poly-Si)
Gate definition (litho. and poly-Si etch)
S & D n+ implantation
Metallization

Figure 3.6: Built-in stress analysis during the process to make GAA buckled Si NW MOSFET on bulk Si. The black arrows represent tensile stress in Si. The red arrows represent restrictions on out-of-plane mechanical buckling due to a tensile hard mask on top. The blue arrow represents upward vertical forces because of the grown oxide layer underneath the NW.

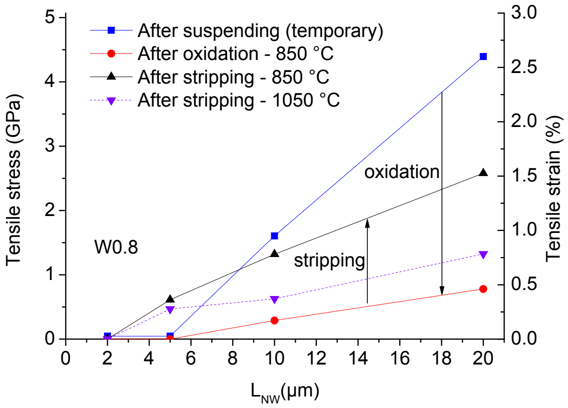

Figure 3.7: The peak of tensile stress along W0.8 Si nanowires before/after wet oxidation at 850 °C and after the stripping step vs. nanowire length. To obtain a highly strained Si nanowire after the stripping step, oxidation should be performed below $T_g(SiO_2) = 960°C$ [4].

3.4.1 Stress development during the oxidation step of W0.8 NWs

About zero initial biaxial strain value (ε_i) was found in the attached Si NWs to the substrate (a Si rib). Suspending the Si NW using isotropic dry Si etching temporarily induces a huge amount of tensile strain (ε_{Si-HM}) up to 2.6% (4.4 GPa uniaxial tensile stress) by in-plane lateral elongation as well as possible out-of-plane buckling perhaps due to relaxations of tensile stress in the Si_3N_4 hard mask across the Si NW as well as on the pads close to the anchor parts. Heating up the wafer to reach the oxidation temperature diminishes a significant amount of this temporary strain by α factor ($\alpha > 1$) due to viscoelastic relaxation of stress in the thin film layers of the hard mask at high temperature as well as geometrical reconfiguration of the Si NW during oxidation.

Thermal oxidation at high temperature induces a biaxial tensile stress into the Si NW, called growth strain (ε_g), due to lattice expansion during oxidation [2]. The increase in the level of tensile strain will be continued during cooling down the wafer to room temperature due to mismatch on thermal expansion coefficient of Si and SiO_2. The corresponding induced biaxial tensile strain to the Si NW is called thermal strain (ε_{th}) [2]. A small accumulation of uniaxial tensile strain in suspended Si nano-beams, called ε_{OIS-SF}, is also reported in [1] due to possible injection of self-interstitial Si atoms during oxidation to the oxidation front. However, as reported in [2], this strain value cannot exceed 0.012% after consumption of e.g. 90% of the thickness of 50 μm long Si beams. Therefore, the nominal value of biaxial tensile strain in the W0.8 Si NW after the oxidation step can be calculated by:

$$\varepsilon_{xx} + \varepsilon_{yy} = \varepsilon_i + \frac{\varepsilon_{Si-HM}}{\alpha} + \beta(\varepsilon_g + \varepsilon_{th}) + \varepsilon_{OIS-SF} \tag{3.2}$$

The grown SiO_2 thin film layer underneath the suspended Si nanowire (see Fig. 3.6) may also help to induce more lateral uniaxial tensile strain than expected to the Si nanowire due to the upward vertical forces during thermal oxidation and during cooling down to room temperature, causing consideration of a β factor ($\beta \geq 1$) in Eq. 3.2.

3.4.2 Stress development during the hard mask and oxide stripping step

According to Fig. 3.7 (see also Fig. 3.8-left for W1.0 nanowires), actual strain measurements on the Si nanowires with the tensile hard mask on top after the oxidation step represent saturation of the tensile strain to about 0.5-0.6% because of restriction on mechanical displacement of the Si NW due to *doubly-clamped design* (restriction on lateral in-plane elongation) and the *tensile hard mask* (restriction on out-of-plane displacement) causing storage of mechanical potential energy in the Si nanowire during the oxidation step. During stripping the hard mask and the grown oxide, the sources of strain because of hard mask, growth and thermal strain disappear [4] but the Si nanowire elongates more to release the stored mechanical potential energy causing an increase by 3-5 factor in the strain level of the Si nanowire (for $850°C$ oxidation temperature; see Fig. 3.7 for details). At this stage, the lateral uniaxial tensile strain in the Si nanowire can be calculated by:

$$\varepsilon_{xx} \approx \varepsilon_{xx} + \varepsilon_{yy} = \varepsilon_i + \varepsilon_{OIS-SF} + \varepsilon_{OIS-pot} \tag{3.3}$$

where $\varepsilon_{OIS-pot}$ represents the increase in strain during the stripping step because of the stored mechanical potential energy during oxidation.

3.4.3 Stress development during the rest of the process steps

After this stage, we believe that the possible further change in the strain level of the Si NW after the further thin film deposition and etching steps (e.g. LTO, poly-Si) can be in the order of the possible errors due to the process variation from wire to wire and from run to run, negligible in comparison to 2.6 GPa stress peak, obtained after the stripping step. Similar thermal properties of poly-Si gate and Si NW also can avoid accumulation of thermal stress during or after the SiO_2/poly-Si gate-stack deposition step. Obviously, the stress level can be significantly engineered using a high-k/metal-gate stack by inducing intrinsic thin film stress in the metal-gate layer.

3.4.4 Stress development in W1.0 nanowires

During the process, the W0.8 Si nanowires were suspended from the substrate, even before the oxidation step. According to the process flow (Fig. 3.1), the W1.0 nanowires are attached to the substrate before the oxidation step. The thin Si bridge between the nanowire and the substrate will be consumed during the oxidation step (see F.g 3.9) and the nanowire will be suspended after the stripping step. Fig. 3.8-left shows the stress development in the W1.0 nanowires, before and after the stripping step, following a similar trend to the W0.8 nanowires.

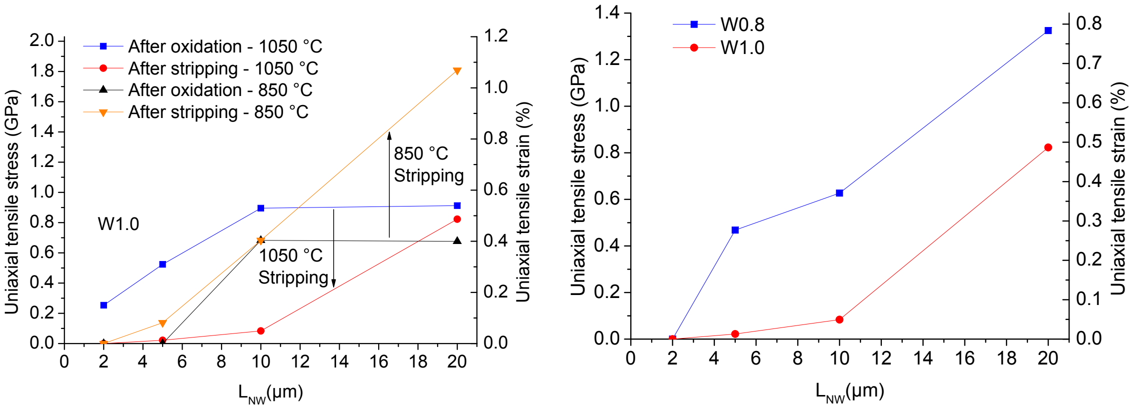

Figure 3.8: The peak of tensile strain along two W10 Si NWs after wet oxidation at 1050°C and after the stripping step (left). The peak of tensile strain along two W08 and W10 Si NWs after wet oxidation at 1050°C and stripping steps (right).

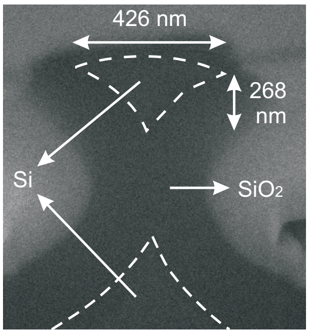

Figure 3.9: SEM cross-section nanograph of a W1.0 Si nanowire after the oxidation step. The remained Si between the Si nanowire and bulk was consumed during the oxidation step and the nanowire will be released right after the stripping step.

As a comparison, the stress peaks for the W0.8 and the W1.0 nanowires after the stripping step are plotted versus nanowire length in Fig. 3.8-right.

Note that stress development formulation in the W1.0 nanowires is similar to the W0.8 nanowires, neglecting the contribution of ε_{Si-HM} in Eq. 3.2 since the W1.0 NW was attached to the substrate before the oxidation step. Anyway, precise modeling of such complex nanowire buckling is not simple, needing consideration of stress profile analysis along the nanowires as well and approving later on using 3D process simulation (such large mesh displacements in 3D for the moment are not supported by e.g. TCAD Sentaurus and can be available in the future release by Synopsys).

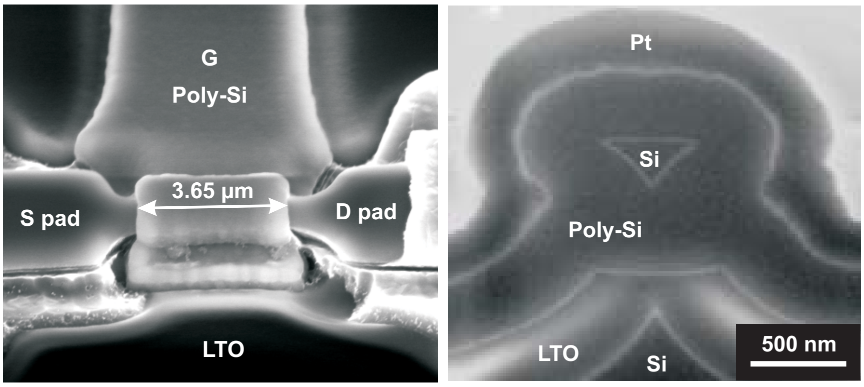

Figure 3.10: SEM picture of a GAA Si NW nMOSFET (left); Cross-section of the GAA triangular wire close to one of its anchors (right).

3.4.5 An additional oxidation step to shrink further the cross-section

In this chapter, we included an additional sacrificial oxidation step, wet oxidation to consume nominally 55 nm of (100) Si, to possibly shrink further the suspended buckled Si nanowires, after the stripping step. The oxidation temperature was chosen to be similar to the first oxidation step. The second oxidation step was found to oxidize significantly the buckled Si nanowires, due to the high level of uniaxial tensile stress, and almost all the buckled W0.8 and W1.0 nanowires were consumed during this step (higher oxidation rate in the presence of uniaxial tensile stress in Si). Therefore, due to the high level of uniaxial tensile stress, including only one oxidation step is recommended in the process flow and the further works in this project were done using only one thermal oxidation step to induce stress and as a sacrificial step, both at the same time.

3.5 Local versus global carrier mobility in the Si nanowire channel

Similar strained Si nanowires, fabricated earlier using low doped ≈6.0×10^{16} cm^{-3} p-type bulk Si with performed oxidation at 1000°C with the SEM top-view and the cross-section in Fig. 3.10, were used for micro-Raman measurement and electrical characterization after isolation, gate stack (SiO_2/poly-Si), S/D ion implantation and metallization steps. The electrical characterization was carried out at 293 K using a Cascade prober and an HP 4155B Semiconductor Parameter Analyzer.

Fig. 3.11-left shows normalized transfer and transconductance characteristics of the buckled device in Fig. 3.10 with the stress profile in Fig. 3.11-right, versus a non-bended one. According to the figure, the enhancements in normalized I_D and normalized transconductance are up to 38% and 50%, respectively. As it is shown in Fig. 3.11-left, the both enhancements decrease by increasing the gate overdrive voltage (V_{GS}-V_{TH}). Note that the threshold voltage and low-field mobility values are extracted using $I_D/\sqrt{g_m}$ method [31]-[32], quasi-independent of series resistance and mobility attenuation factor. It is worth mentioning that the observed 0.19 V

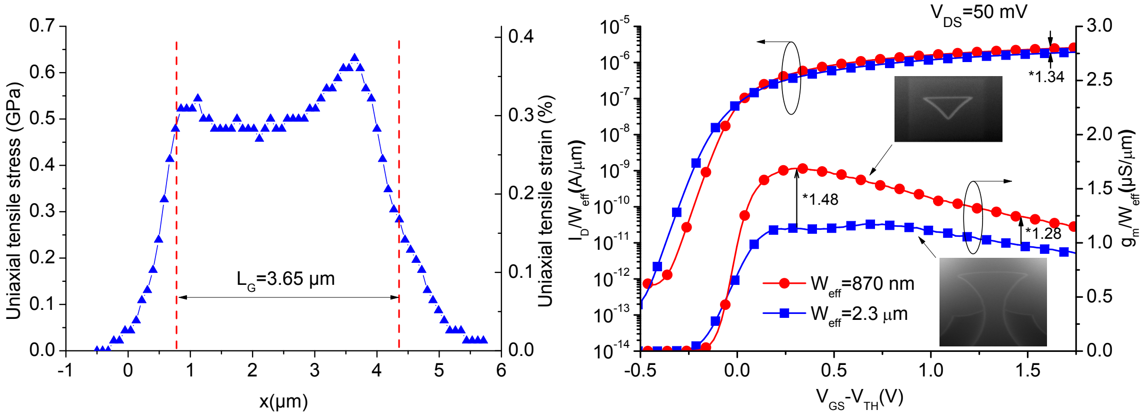

Figure 3.11: Stress profile along the 5.0 μm long Si nanowire, presented in Fig. 3.10, after the gate stack deposition step (left). Transfer and transconductance characteristics of strained and non-strained 5.0 μm long Si nanowire MOSFETs at V_{DS} = 50 mV (right). The smaller W$_{eff}$ corresponds to the strained device (for the strained device: V_T=-0.0384 V, SS=64 mV/dec; for the non-strained device: V_T=+0.1525 V, SS=66 mV/dec.).

downshift in the threshold voltage of the strained device is due to the strain-induced change in the electron affinity, band-gap and valence band density of states of the Si channel [33].

Low-field electron mobility extraction using $I_D/\sqrt{g_m}$ method represents 53% enhancement in average electron mobility, for the strained device in comparison to the non-strained one. Due to having one (100) face and two slanted non-well defined faces in the triangular GAA Si nanowire nMOSFET and by considering the fact that the highest possible electron mobility enhancement belongs to the (100) Si surface nMOSFET under $<110>$ uniaxial tensile strain [6], the highest possible local electron mobility enhancement due to strain in the triangular GAA structure is calculated using the actual strain profile, directly measured using micro-Raman spectroscopy through the gate stack, in Fig. 3.11-left and an experimental curve including electron mobility enhancement factor for the (100) surface nMOSFET vs. $<110>$ uniaxial tensile strain in [34], representing a peak of 54% enhancement in *nominal local electron mobility*, and afterward, plotted in Fig. 3.12 (curve B). However, the experimental electron mobility of the suspended architecture represents even 10% more than the average of our highest possible local electron mobility enhancement expectation due to uniaxial tensile strain. This is due to contribution of local volume inversion and corner effect [35], possible higher electron mobility enhancement factor than expected due to having a lower doping level in our wafer in comparison to the used doping level in [34] and possible cross-section variation along the channel. Finally, by considering the positive contribution of all the mentioned parameters together for the suspended architecture, the *actual local electron mobility* along the buckled Si nanowire channel is plotted in Fig. 3.12 showing a peak of 64% local electron mobility enhancement (curve C) in comparison to the non-strained device.

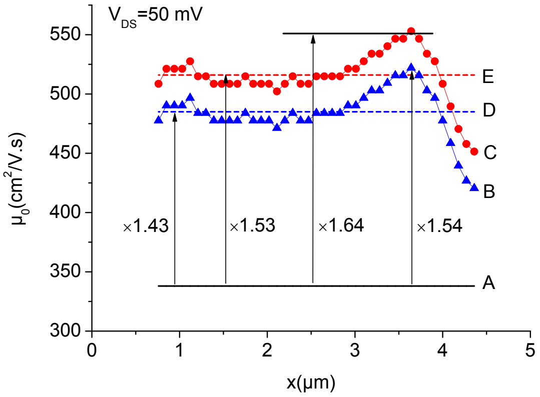

Figure 3.12: Local electron mobility enhancement along the buckled Si nanowire channel: Omega-gate non-strained Si nanowire MOSFET (A); *nominal local electron mobility* estimation based on local stress profile in Fig. 3.11-left (B); *actual local electron mobility* along the suspended buckled Si nanowire channel (C); average of nominal local electron mobility estimation based on local stress profile along the buckled channel (D); the extracted low-field electron mobility of the GAA buckled suspended Si nanowire nMOSFET (E).

3.6 Scalability of local oxidation as a local stressor

The shorter nanowires fabricated from this bulk top-down platform are thicker because of the pattern dependency of the isotropic Si etching process and therefore, less strained due to their higher critical-load-for-buckling values (see Figs. 3.7 and 3.8). But it does not reflect that such a local stressor is not scalable to e.g. sub-100 nm Si nanowire length. Prolongation of the isotropic Si etching step can be performed to shrink further the Si nanowire cross-sections before the oxidation step e.g. down to 300 nm to finally obtain e.g. 50 nm wide/thick Si nanowires after the sacrificial oxidation step. This will help to fabricate shorter buckled Si nanowires while causing consumption of longer nanowires on the wafer (see Fig. 3.13).

To suppress such process variations as well as minimize the cross-section variation along the channel, the buckled Si nanowires can be fabricated simply using a SOI top-down Si nanowire platform (see e.g. [10]-[13]). In this case, the Si nanowire thickness and width will be determined precisely by the SOI thickness and e-beam lithography (no need to spacer). Several parameters e.g. percentage of oxidation of the Si nanowire, oxidation conditions (wet or dry, oxidation temperature), uniaxial tensile stress level in the hard mask, etc. can influence the final stress level in such buckled Si nanowires as well and engineering of all the mentioned parameters, possibly can help to accumulate a similar sub-2.6 GPa uniaxial tensile stress level, demonstrated using a bulk substrate [4]. Note that since ALD high-k/metal-gate is an appropriate gate stack solution for the scaled devices, further stress engineering can be done simply using metal-gate strain to obtain possible higher level of stress (see e.g. our recent work in [11]).

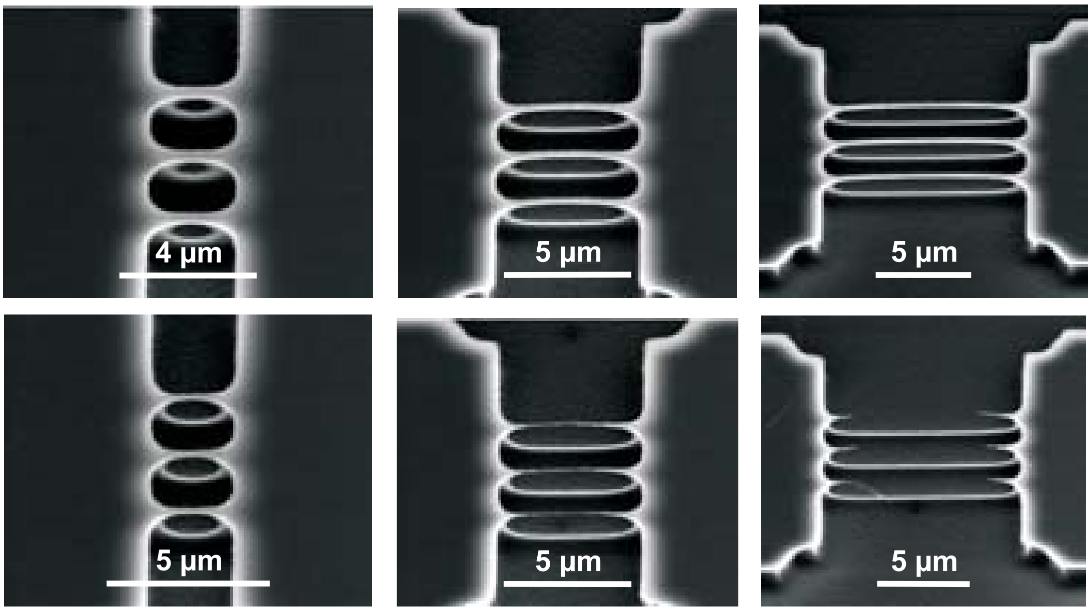

Figure 3.13: The Si nanowires with strain peaks represented in Fig. 3.7 after the stripping step (up); the Si nanowires after about 25% prolongation of the isotropic Si etching step and afterward the same oxidation and stripping steps (bottom). This Si etching prolongation induces a higher buckling to the shorter devices, validating the scalability potential of the local oxidation as a local stressor technique, while causing a complete consumption of the longer nanowires during the etching/oxidation steps as well. Such process variations can be minimized simply using a SOI Si nanowire platform [10]-[13].

An alternative approach to make scaled highly strained Si nanowires MOSFETs is fabrication of a short channel device at the highly strained region of the Si nanowire. This can be done using LTO to isolate the substrate, open up only the middle part of the wire and finally, gate stack deposition, implantation and metallization (see Fig. 3.14).

3.7 Multi-gate buckled self-aligned dual Si nanowires on bulk

In this section, we report making multi-gate buckled self-aligned dual Si nanowires including two sub-100 nm cross-section cores on bulk Si substrate using optical lithography, hard mask/spacer technology and local oxidation. ≈0.8 GPa uniaxial tensile stress was measured on the buckled dual nanowires using micro-Raman spectroscopy. The buckled multi-gate dual Si nanowires show excellent electrical characteristics e.g. 62 mV/dec. and 42% low-field electron mobility enhancement due to uniaxial tensile stress in comparison to the non-strained device, all at V_{DS}=50 mV and 293 K.

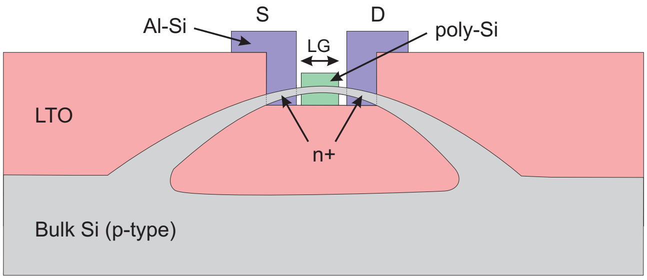

Figure 3.14: Implementation of a short channel length Si nanowire MOSFET centered on the highly strained nanowire region (e.g. sub-2.6 GPa lateral uniaxial tensile stress).

3.8 Fabrication process

The process flow to fabricate self-aligned dual Si nanowires from bulk Si substrate is demonstrated in Fig. 3.15. As a first step, the 100 mm (100) p-type (0.1-0.5 Ω·cm) bulk prime Si wafers were oxidized using wet oxidation at 1050 °C to grow 500 nm of SiO_2 including -310 MPa residual thin film biaxial compressive stress. Afterward, DWL200 was used to write the active resist pattern (S/D and wires) directly on the wafer using 0.8 μm resolution optical lithography. The length and the width of the wire masks were varying from 2.0 to 20.0 μm and 0.8 to 1.8 μm, respectively. To transfer the active layer to the wafer, the SiO_2 hard mask and Si were etched anisotropically using fluorine-based chemistry to make ≈1.1 μm high ribs. A 5 hour sacrificial wet oxidation at 850 °C was done to narrow the Si ribs from the two sides, smooth the Si side-walls and simultaneously grow an oxide spacer layer. A short fluorine-based dry anisotropic SiO_2 etching step was performed to remove the grown SiO_2 on the substrate. The higher oxidation rate for the Si side-walls in comparison to the (100) Si surface leading to grow a thicker oxide on the side-walls while due to the slightly slanted side-walls, the final SiO_2 spacer thickness right after the SiO_2 etching step is estimated to be ≤50 nm. Afterward, a fluorine-based isotropic Si etching was done to suspend the narrowest ribs (0.8 μm initial mask NW width, called W0.8) from the substrate while the rest of the Si ribs were still connected to the substrate.

A 4 hour wet oxidation at 850 °C (8.3 L/min O_2, 16.0 L/min H_2) was done to nominally consume 120 nm of (100) Si to reduce the nanowire dimensions, consume the remained Si between the wider nanowire (W1.0) and substrate to suspend the structures. The oxidation temperature was chosen to be below the glass transition temperature of SiO_2, 960 °C, to avoid relaxation of stress in the SiO_2 thin films to be able to accumulate mechanical potential energy in the nanowires during oxidation [4]-[5]. The higher oxidation rate of the Si side-walls in comparison to the top (100) Si surface as well as built-in stress in the growing oxide layer during the oxidation step yields to obtain two Si cores with rounded corners connected with a sub-10 nm thick Si bridge after oxidation of the narrowest Si ribs (W0.8).

Stripping the SiO_2 hard mask/spacer and the grown oxide was done using wet BHF etching (volume ratio of 7:1 of NH_4F 40% and HF 50%). Fig. 3.16 represents an array of Si nanowires

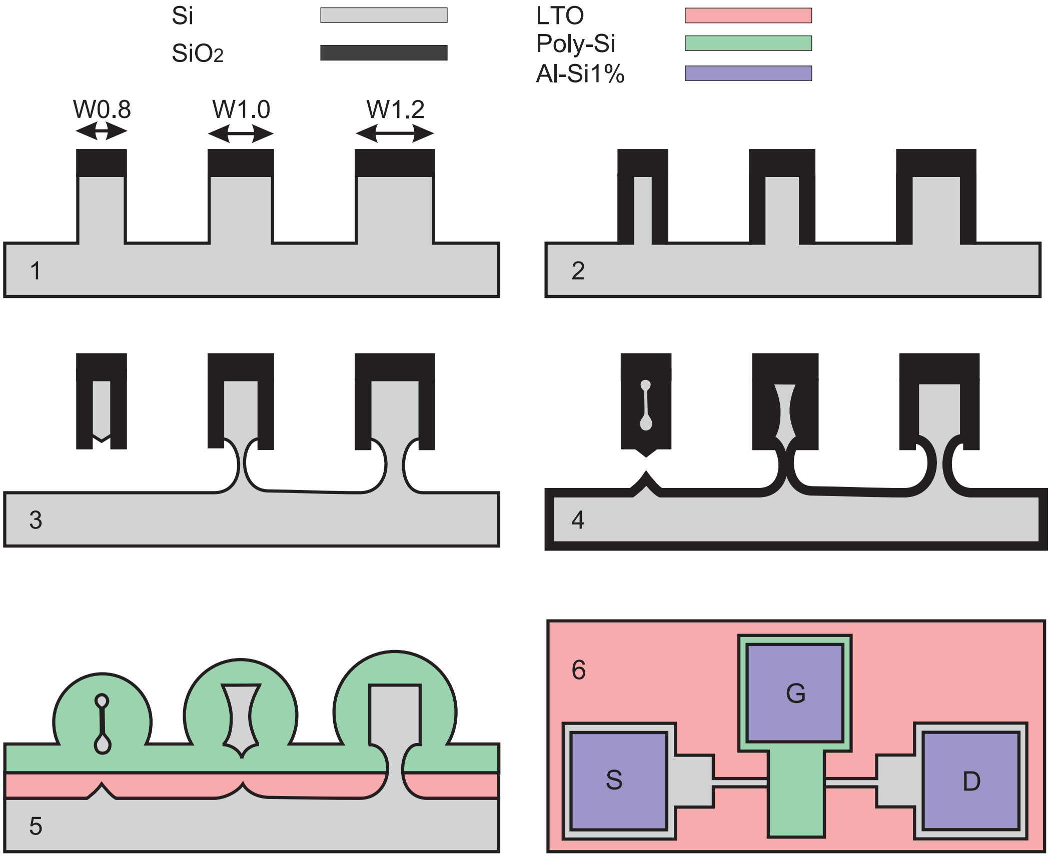

Figure 3.15: Process flow to obtain multi-gate Si nanowire MOSFETs on bulk. W0.8 corresponds to the initial 0.8 μm mask nanowire width.

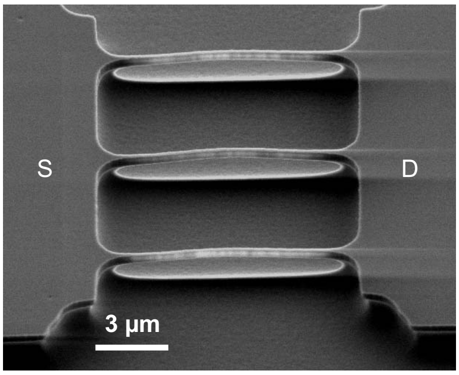

Figure 3.16: Tilted-view SEM micrograph of an array of 10 μm long buckled dual Si nanowires on bulk Si right after the SiO_2 stripping step, representing the reproducibility of the process flow from strain engineering and dual Si nanowire formation aspects. The two sub-100 nm cross-section nanowire cores are connected to each other using a thin Si bridge. The out-of-plane buckling is the signature of uniaxial tensile stress in the nanowire.

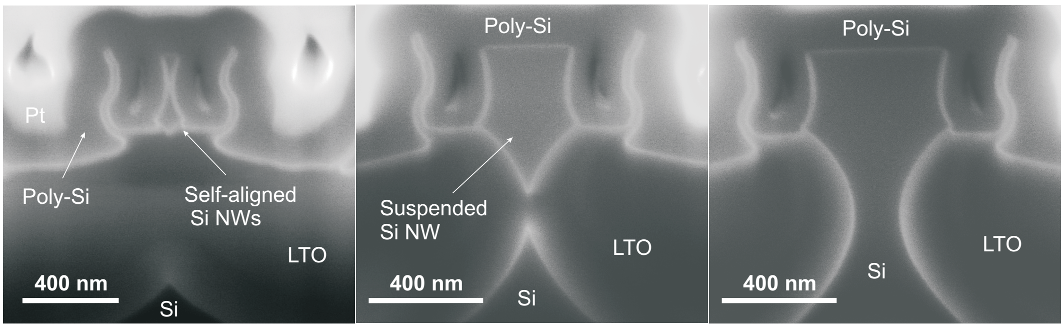

Figure 3.17: SEM nanograph from the cross-section of multi-gate MOSFETs on bulk Si: multi-gate suspended dual self-aligned Si nanowires (W0.8, left), multi-gate suspended Si nanowire (W1.0, center) and omega-gate MOSFET (W1.2, right)

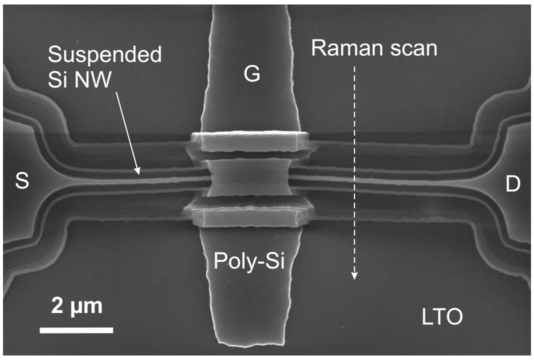

Figure 3.18: Top-view SEM micrograph of a multi-gate dual Si nanowire MOSFET on bulk Si. The in-plane nanowire buckling is a sign of uniaxial tensile stress in the channel. The arrow indicates the scan axis and direction of the laser spot in the micro-Raman measurement.

including two sub-100 nm cross-section self-aligned Si cores connected with a thin Si bridge right after the stripping step. The buckling in the nanowires after the stripping step is due to releasing the stored mechanical potential energy in the nanowires during the oxidation step [4]-[5], a clear sign of uniaxial tensile stress in the nanowire.

An isolation step including LTO deposition, CMP and isotropic LTO etching using BHF was done to isolate the suspended nanowires from bulk. The gate stack step includes RCA, dry oxidation to grow 15 nm of gate oxide at 850 °C and finally, 230 nm of LPCVD in-situ doped N^+ poly-Si (phosphorous: 2×10^{20} cm^{-3}) at 480 °C. The thin Si bridge during the gate stack step is being consumed and finally, two separated self-aligned sub-100 nm cross-section Si cores can be obtained (see Fig. 3.17).

To activate the dopants in the poly-Si thin film, a 5 min furnace annealing at 900 °C was done. The gate pattern was transferred to the wafer using optical lithography and fluorine-based isotropic poly-Si etching. Stripping the resist layer, S/D phosphorous ion implantation (2×10^{15} cm^{-2}, 30 keV) and annealing to activate the dopants, metallization and sintering (450 °C, 30 min) were the further steps.

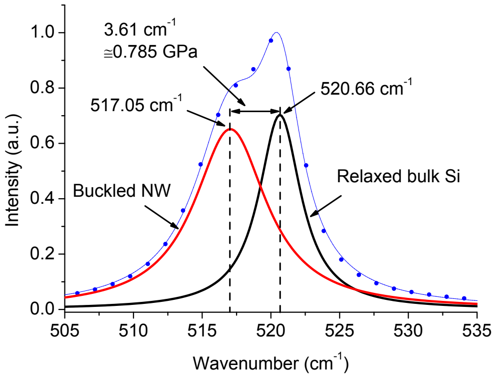

Figure 3.19: Micro-Raman spectrum taken on a 12 μm long buckled dual Si NW on bulk Si (SEM top-view in Fig. 3.18). The spectrum is well fitted with two Lorentzian peaks corresponding to the relaxed bulk Si at 520.66 cm^{-1} and the strained Si nanowire at 517.05 cm^{-1}.

3.9 Strain analysis in the buckled Si nanowires

3.9.1 stress measurement on the buckled dual Si NWs by micro-Raman spectroscopy

Micro-Raman spectroscopy was employed for measuring stress on a finalized dual Si nanowire MOSFET at 293 K (a TERS setup, using no AFM tip for the moment and as a first step to simplify the measurements). A Renishaw inVia spectrometer setup is used with a green laser of 532 nm in wavelength. As the penetration depth of the laser in Si (≈1 μm) is longer than the thickness of the Si nanowire (<500 nm), both Raman spectra of the strained Si nanowire and the relaxed Si underneath are observed while the laser beam is focused on the nanowire. The line scan with the step of 0.5 μm was done across the naked part of the Si nanowire between S/D pad and gate pattern (see Fig. 3.18) as the measurement on the Si channel via the poly-Si gate stack is challenging due to the broad spectra of poly-Si around the crystalline Si spectra.

A spectrum shown in Fig. 3.19 was taken at the 10th from the top out of 16 points along the scan axis. A considerable satellite peak is only observed at this point while just a single peak originated from relaxed bulk Si at 520.6 cm^{-3} is observed in the others except for a very subtle shoulder at the 9th and 11th. The result suggests that the buckled nanowire was spotted on in the measurement at the 10th point. As shown in Fig. 3.19, the corresponding two peaks are deconvoluted from the spectrum by using Lorentzian peak fitting [28]. 0.465%/0.785 GPa uniaxial tensile strain/stress in the buckled Si nanowire are estimated by assuming Young's modulus of 169 GPa in Si.

3.9.2 Process-based stress optimization in the top-down Si nanowire platform

Previously in [4]-[5], we reported in-depth stress analysis of local oxidation of the Si nanowires with a Si_3N_4/SiO_2 tensile hard mask on top. In this work, due to using a SiO_2 hard mask, grown

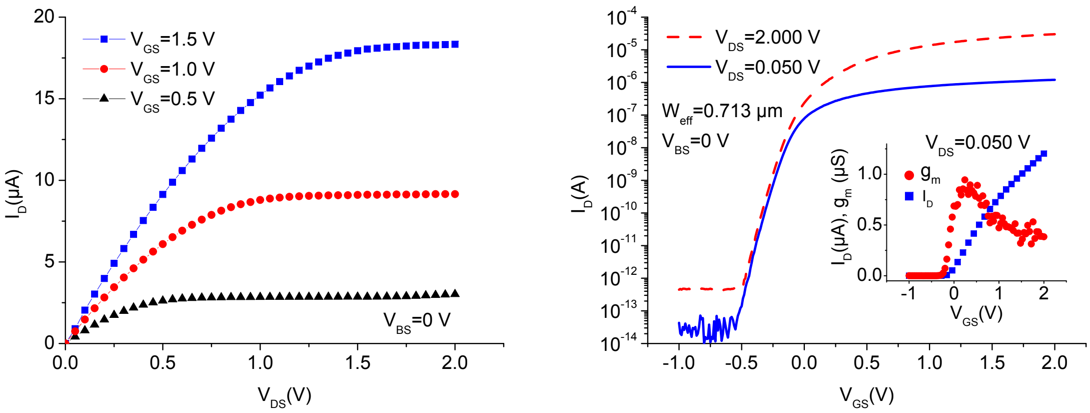

Figure 3.20: Output (left) and input (right) characteristics of the multi-gate dual Si nanowire MOSFET (W0.8, SEM cross-section in Fig. 3.17-left, W_{eff}=0.713 μm (top NW: 0.273 μm, bottom NW: 0.440 μm)). SS=62 mV/dec., V_{TH}=-0.061 V, μ_0=468 cm^2/V·s and R_{SD}=18.7 kΩ, all at V_{DS}=50 mV.

by wet oxidation, the sign of the stress in the hard mask is reverse because of volume expansion during oxidation. Less restrictions on out-of-plane buckling during the oxidation step due to having a compressive hard mask on top leads to a smaller accumulation of mechanical potential energy during oxidation and finally, a smaller amount of stress in the Si nanowires is expected in comparison to the Si nanowires with a tensile hard mask on top. On the other hand, using a SiO_2 hard mask and spacer has the advantage of further rounding the sharp corners of the Si nanowire channel. To improve further the level of uniaxial tensile stress in the Si nanowires, a high-k/metal-gate stack including an intrinsic compressive thin film stress in the metal-gate layer can be used [12], [23]. As a consequence, to even significantly relax the level of stress to make the Si nanowire platform suitable for the pMOS devices without hole mobility degradation, the thermal oxidation can be performed at temperatures higher than the glass transition temperature of SiO_2, 960 °C, for viscoelastic stress relaxation in the SiO_2 thin films on the wafer and further compressive stress can be induced to the suspended nanowire channel using a high-k/metal-gate stack including an intrinsic biaxial tensile stress in the metal-gate layer.

3.10 Electrical characterization and extraction of parameters

Electrical characterization was done at 293 K using a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer. Fig. 3.20 shows output (left) and input (right) characteristics of the multi-gate dual Si nanowire MOSFET with the shown SEM micrographs in Figs. 3.17(left) and 3.18. The threshold voltage and low-field mobility values were extracted using the $I_D/\sqrt{g_m}$ method [31]-[32], quasi-independent of series resistance and mobility attenuation factor reporting V_{TH}=-0.061 V and μ_0=468 cm^2/V·s at V_{DS}=50 mV. According to Fig. 3.20, the I_{on}/I_{off}

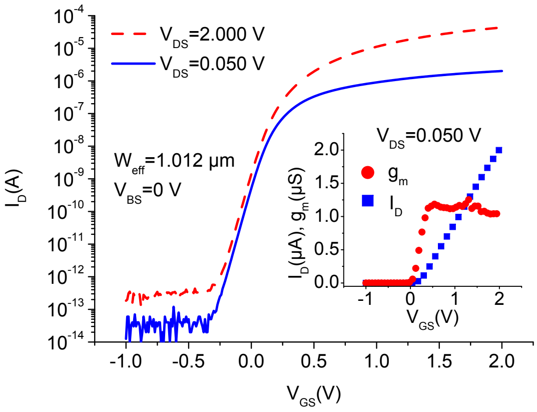

Figure 3.21: Input characteristics of the multi-gate Si nanowire MOSFET (W1.0, SEM cross-section in Fig. 3.17-center, W_{eff}=1.012 μm). SS=64 mV/dec., V_{TH}=0.213 V, μ_0=353 cm^2/V·s and R_{SD}=3.7 kΩ, all at V_{DS}=50 mV.

ratio at V_{DS}=2.000 V can be as high as $\approx 10^8$ in the case of tuning the threshold voltage using a metal-gate with a mid-gap work-function or channel doping modulation. During the extraction of parameters, only the covered faces of the nanowires with the poly-Si/SiO$_2$ gate stack in Fig. 3.17 were considered as the W_{eff} of the MOSFETs. Note that the bottom part of the suspended nanowires not covered with the gate stack, mainly due to its challenging isolation step, acts as an independent transistor with a thick gate oxide layer (>200 nm LTO) and using bulk Si as the back-gate. Due to its fairy thick oxide thickness and since V_{BS} is fixed to 0 V during all the measurements, this independent transistor cannot involve significantly in the conduction.

To compare the results, the wider MOSFETs with the SEM cross-sections in Fig. 3.17 and with the same gate length in Fig. 3.18 were also characterized (see Figs. 3.21 and 3.22). The omega-gate MOSFET shows V_{TH}=+0.255 V and μ_0=329 cm^2/V·s at V_{DS}=50 mV. The observed downshift in the threshold voltage of the dual-Si nanowire is mainly due to the local volume inversion, corner effect and uniaxial tensile stress in the channel [33]-[36]. The optimum values of the subthreshold slope as well as very low leakage current values are reflecting an excellent gate stack while the narrower channels represent a better value due to a better electrostatic control on the channel. A 42% low-field electron mobility improvement in the buckled dual Si nanowire in comparison to the omega-gate MOSFET is due to uniaxial tensile stress in the channel. The higher transconductance drop in Fig. 3.20-right in strong inversion regime in comparison to the wider devices is mainly due to the higher series resistance in the scaled Si nanowire MOSFETs.

The series resistance values reported in the caption of Figs. 3.20-3.22 are extracted and estimated using the y-intercept of total resistance (R_{tot}=V_{DS}/I_D) vs. 1/(V_{GS}-V_{TH}-V_{DS}/2) at V_{DS}=50 mV [37], assuming series resistance as the major transconductance drop mechanism in strong inversion regime. Note that the contribution of intrinsic mobility attenuation factor

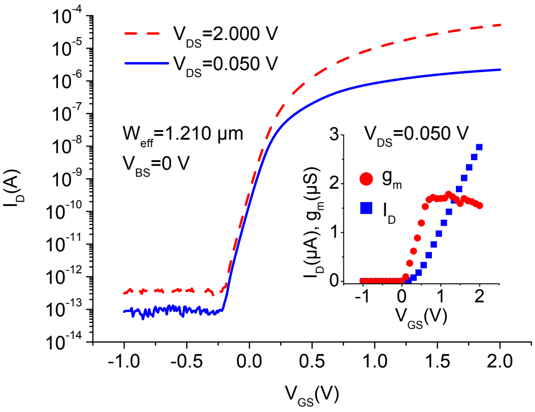

Figure 3.22: Input characteristics of the omega-gate MOSFET (W1.2, SEM cross-section in Fig. 3.17-right, W_{eff}=1.210 μm). SS=68 mV/dec., V_{TH}=0.255 V, μ_0=329 cm^2/V·s and R_{SD}=0.8 kΩ, all at V_{DS}=50 mV.

(θ_0, see [31], can be influenced mainly by channel-dielectric interface quality [38]) on the transconductance drop in strong inversion should be negligible due to having an excellent gate stack (optimum subthreshold slope and pretty low leakage drain current in a sub-100 fA range for all the multi-gate devices at V_{DS}=50 mV).

3.11 Si nanowires for low voltage digital logic

Due to the best electrostatic control on the channel, multi-gate Si nanowires are the best platforms to implement low power/low voltage CMOS digital circuits [39]-[40]. To address this as well as integration of CMOS boosters e.g. stressors to the nanowire platforms for further CMOS digital circuit optimization as a first step, we demonstrate various architectures of multi-gate NMOS inverters, using suspended Si nanowires as well as omega-gate MOSFETs, on bulk Si.

NMOS inverter is the simplest building block for digital logic circuits, having a simple process flow (a four-mask process flow and a single S/D implantation step). It consumes power while the driver is in the “ON” status but a necessary logic for some semiconductors e.g. CdS and CdSe, suffering from uniploarity and technically, not possible to make complementary inverters [41]. III-V materials are also showing a high electron mobility suitable for high speed/low voltage digital circuit applications while suffering from a very low hole mobility, causing a non-promising performance for a complementary architecture [42].

Fig. 3.24 shows the top-view SEM micrograph of a NMOS inverter (the driver SEM micrograph in Fig. 3.18). To simplify the mask design, all the pads are disconnected from each other on the wafer and depending on the threshold voltage sign, the enhancement-mode (V_{TH}>0, EM) and depletion-mode (V_{TH}<0, DM) architectures can be arranged while doing the measurements

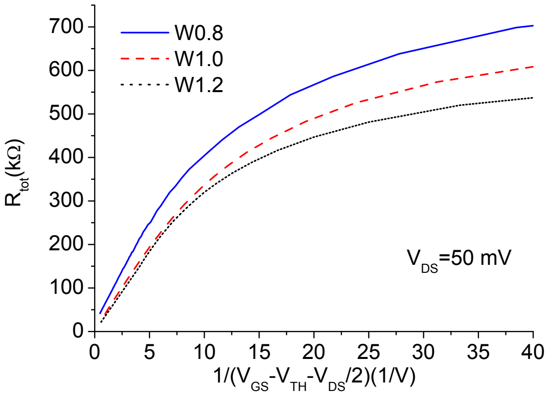

Figure 3.23: Total resistance (V_{DS}/I_D; which is sum of series and channel resistances) vs. $1/(V_{GS}$-V_{TH}-$V_{DS}/2)$ for the W0.8, W1.0 and W1.2 MOSFETs at V_{DS}=50 mV. The series resistance values can be approximately extracted from the y-intercept of each curve (least square approximation fitting e.g. below 2.5 V^{-1}) and reported in Figs. 3.20-3.22, captions.

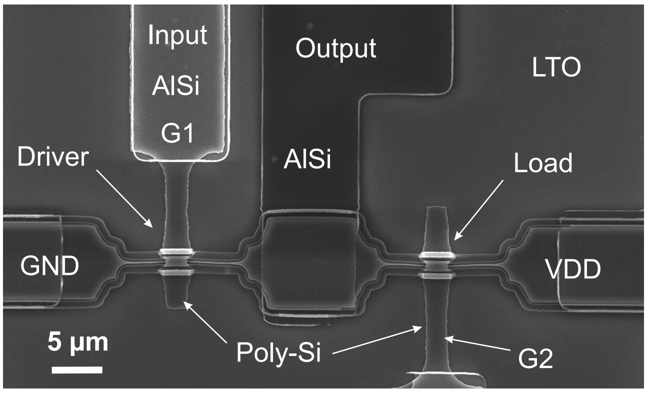

Figure 3.24: SEM picture of a NMOS inverter (W0.8). The nanowire length and gate length are 12.0 and 2.0 μm, repsectively.

using the prober and Semiconductor Parameter Analyzer (see Fig. 3.25-inset, regarding both logic architectures). The both driver and load transistors were designed to be nominally identical using the same NW length, width and gate length. The devices are from the same fabrication to make multi-gate self-aligned dual Si nanowires on bulk Si.

3.11.1 Electrical characterization of NMOS inverters

The electrical characterization was carried out at 293 K using a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer. Fig. 3.25-left shows the voltage transfer characteristics (VTC) of multi-gate MOSFETs (W0.8, W1.0 and W1.2), all at V_{DD}=0.400 V. The W0.8 NMOS inverter has the DM architecture, due to its negative threshold voltage, while the others have the EM architecture. According to the figure, it is clear that the scaled devices show a more

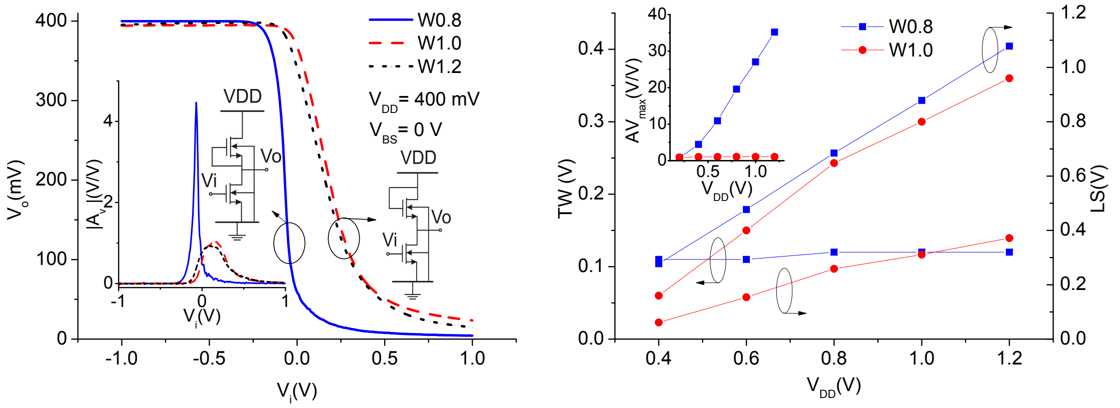

Figure 3.25: Voltage transfer characteristics (VTC) of the multi-gate W0.8, W1.0 and W1.2 Si nanowire NMOS inverters (inset: absolute value of the voltage gain, $|A_v|$=$|dV_o/dV_i|$, vs. input voltage) (left). W0.8 has the DM architecture while the others with positive threshold voltages have the EM architecture. Transition width (TW=V_{iH}-V_{iL}) and logic swing (LS=V_{oH}-V_{oL}) vs. V_{DD} for the multi-gate suspended (W0.8 and W1.0) Si nanowire NMOS inverters (inset: voltage gain peak vs. V_{DD})(right).

abrupt transition behavior. The DM architecture is providing the highest voltage gain, the largest output voltage swing and the lowest output voltage in the “ON” state. The observed characteristics can be described by small-signal and static analyses.

3.11.2 Small-signal analysis of multi-gate NMOS inverters

By considering the small-signal model of the NMOS devices [43] for the both load and driver in the saturation regime and in the transition region of the logic gate, the voltage gain of the multi-gate suspended dual nanowires in the DM architecture equals:

$$A_v = -g_{md} \cdot (r_{od} \| r_{ol}) \approx -g_{md} \cdot r_{od}/2 \tag{3.4}$$

where g_{md} is the transconductance of the driver. r_{od} and r_{ol} are the output resistances of the driver and load, respectively, assuming almost similar in this section. For the multi-gate suspended NW in the EM architecture, we have:

$$A_v = -g_{md} \cdot (1/g_{ml} \| r_{od} \| r_{ol}) \approx -g_{md}/g_{ml} \tag{3.5}$$

where g_{ml} is the transconductance of the load. Finally, for the omega-gate MOSFETs in the EM architecture:

$$A_v = -g_{md} \cdot (1/g_{ml} \| 1/g_{mbl} \| r_{od} \| r_{ol}) \approx -(g_{md}/g_{ml}) \cdot (1/(1+\eta)) \tag{3.6}$$

where, g_{mbl} is the body effect transconductance of the load and η=g_{mbl}/g_{ml}.

Due to having almost identical load and driver transistors, the voltage gain for the EM multi-gate suspended nanowire inverter should be around unity and for the EM omega-gate devices should be slightly smaller due to the body effect. The voltage gain for the DM architecture can be higher than unity. Suspending the NW from bulk removes the body effect, causing a more abrupt transition in the EM architecture. It is worth mentioning that the voltage gain for the omega-gate device was found to be higher than unity only for V_{DD} ≥1.4 V, due to the body effect.

3.11.3 Static analysis of the multi-gate suspended NMOS inverters

Fig. 3.25-right shows the key logic parameters of the multi-gate suspended NWs (W0.8 and W1.0) on bulk Si at different power supply voltages. Transition width (TW=V_{iH}-V_{iL}) and logic swing (LS=V_{oH}-V_{oL}) are plotted vs. V_{DD} for both devices. According to this figure, the DM architecture shows a narrower transition width and a higher logic swing (>69% V_{DD}). On the other hand, the EM architecture shows a wider transition width (<31% of V_{DD}) and a smaller logic swing (<30% of V_{DD}). Note that the GAA Si NW DM shows a fairy high DC load resistance, becoming even higher by V_{DD} while the GAA Si NW EM load DC resistance is much smaller, reducing even further by V_{DD} (6.6-17.5 MΩ vs. 870-183 kΩ at V_{DD}=0.400-1.200 V, respectively; all reported at V_i=1.000 V).

3.12 Summary

In this chapter, we reported the origin of high level of built-in stress during the oxidation of Si nanowires with the a tensile hard mask on top for the first time. Releasing the accumulated mechanical potential energy in the Si nanowire, stored in the NW during the oxidation step due to the tensile hard mask on top and a fixed-fixed design while released during the thin film stripping step, was found to be the main source of oxidation-induced buckling in the NWs, after the stripping step. We reported accumulation of up to 2.6 GPa uniaxial tensile stress peak in the buckled Si nanowires (20 μm long NW, sub-100 nm cross-section). The stress level can be modulated by NW length and NW width. To obtain a high level of stress, oxidation should be performed below glass transition temperature of SiO_2 (960 $^\circ C$), to avoid viscoelastic relaxation in the oxide layers. Since the stress level is almost constant along the NWs, about 2 μm far from the S/D anchors, while relaxing completely in the S/D anchors, it can be used in a controlled way as a CMOS booster to enhance the carrier mobility, placing the channel in the highly stressed NW part. We reported 53% low-field electron mobility enhancement in the buckled GAA Si NWs, with a measured stress peak of ~0.6 GPa uniaxial tensile stress via the poly-Si/SiO_2 gate stack and in comparison to the omega-gate relaxed MOSFET. Local stress profile along the channel was correlated to the I-V characteristics of the GAA buckled NW for the first time, revealing even a higher stress-based local mobility enhancement of 64% in the highly stressed part of the channel.

We reported a fabrication method to make multi-gate buckled self-aligned dual Si nanowires including two sub-100 nm cross-section cores on bulk Si substrate using 0.8 μm optical lithography, hard mask/spacer technology and local oxidation for the first time. ~0.8 GPa uniaxial tensile stress was measured in the buckled dual Si nanowires using micro-Raman spectroscopy. The gate stack includes 230/15 nm of LPCVD N^+ in-situ doped poly-Si/SiO_2. 62 mV/dec. and 42% stress-based low-field electron mobility enhancement in comparison to the non-strained device are reported, all at V_{DS}=50 mV and T=293 K. Almost ideal subthreshold slopes and pretty low leakage currents (in a sub-100 fA range) for all the multi-gate devices on the wafer reflect an excellent gate stack. A simple digital logic is demonstrated as well using multi-gate Si nanowire MOSFETs.

The original work carried out relative to this chapter includes:

- **Origin of built-in stress during oxidation of NWs**: Buckled sub-100 nm wide Si nanowires are fabricated on bulk Si using 0.8 μm lithography, Si_3N_4 hard mask and spacer technology in a controlled way to study and report the origin on oxidation-induced stress [4]-[5]. Stress was measured in the buckled NWs using micro-Raman spectroscopy. Correlation of local stress profile along a GAA buckled Si nanowire channel and I-V characteristics was done to extract local mobility along the channel [5].
- **Hard mask/spacer engineering to fabricate buckled dual Si nanowires on bulk**: Hard mask and spacer engineering together with local oxidation of a Si Fin can provide buckled dual Si nanowires. Using 0.8 μm optical lithography, buckled self-aligned dual Si nanowires with two sub-100 nm Si cores are fabricated on a bulk Si substrate and finalized in a multi-gate architecture using a N^+ in-situ doped poly-Si/SiO_2 gate stack [14]. Stress measurement was done on the buckled NWs using a TERS setup in micro-Raman mode and stress-based low-field electron mobility enhancement is reported. A simple logic gate (NMOS inverter) is demonstrated using multi-gate Si nanowire MOSFETs on bulk Si as well [21].

3.13 Future works

Further works can be done for in-depth study of local oxidation as a local stressor technology:

- **3D process simulation of NW buckling due to oxidation**: Thermal oxidation in the presence of different hard masks (compressive and tensile residual thin film stresses) on suspended and attached Si nanowires to the substrate (W0.8 and W1.0) and releasing the NWs after the stripping of the hard mask and the grown oxide. Note that TCAD Sentaurus for the moment does not support buckling eigenvalue analysis or non-linear analysis for large mesh displacements (can be available in a future release by Synopsys).
- **Study the effect of oxidation parameters on built-in stress**: The stress level during the oxidation and stripping steps can be influenced by oxidation temperature, percentage

of NW consumption during oxidation and the type of oxidation (wet, dry or other Si oxidation methods e.g. HNO_3 [44]). Note that the grown oxide thin film properties e.g. density can vary by the oxidation method. In this thesis, we mainly focused one temperature below glass transition temperature of SiO_2 while further investigation of oxidation temperature (<960 °C) can provide a better insight regarding optimization of the stress level in the NWs.

- **Fabrication of buckled Si nanowires using a SOI substrate**: This will help to have the best control on the Si nanowire cross-section dimension, no need to deposit spacer, making the built-in-stress studies more straight forward. Note that at a first glance, bulk technology seems to be cheap, but on the other hand, several extensive measurements and process monitoring are needed (e.g. FIB-cut for cross-section observation) to minimize the process variation, making such processes more financial support consuming than expected for straight forward research works. On the other hand, such precise built-in stress analysis including minimized process variation (e.g. nanowire thickness and width) along the channel will possibly help to model easier the built-in stress during the process as well.

Further works can be done regarding vertical stack of nanowires, as buckled multi-gate self-aligned dual Si nanowires was the first step to make more dense array of Si nanowires including stressors as CMOS boosters:

- **Fabrication of GAA vertical stack of buckled Si nanowires using scalloping**: Sub-10 nm cross-section Si nanowires can be fabricated using e-beam lithography on bulk or SOI substrates. The optimum gate stack is ALD high-k/metal-gate due to minimizing the Si channel consumption in comparison to a poly-Si/SiO_2 gate stack. The stress level can be engineered simply using intrinsic metal-gate strain (e.g. deposition temperature, thickness, deposition method and even strain engineering using a 2nd metal-gate capping layer).
- **Process optimization to make GAA NW PMOS devices with high mobility**: Since uniaxial tensile stress degrades the hole mobility, this stress type in the NWs should be suppressed using e.g. further annealing at temperatures higher than glass transition temperature of SiO_2 and before the stripping step). Metal-gate strain engineering can be also possible using a metal-gate including intrinsic biaxial tensile stress. This is necessary in single level and vertical array of Si nanowires.

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4 Buckled GAA deeply scaled cross-section Si nanowire MOSFETs

In this chapter, we demonstrate a process flow to make gate-all-around deeply scaled cross-section Si nanowires (down to 4 nm) from a top-down SOI platform using NW side-wall engineering and stress-limited oxidation. E-beam lithography together with a SOI substrate was used to have the best control on the dimensions of the nanowires. Local oxidation and metal-gate strain technologies were used to induce uniaxial tensile stress to the suspended Si nanowires mainly to boost the carrier mobility without affecting the I_{on}/I_{off} value. Local oxidation was used as a local oxidation and for stress-limited oxidation. Highly doped accumulation-mode was chosen as the operation mode to simplify the process (less need to a precise gate alignment since already the ON device needs to be turn off by the gate), obtain a high I_{on}/I_{off} as well as suppress the transistor performance dependency to the gate stack below the flat-band voltage and specially in subthreshold regime. The devices were characterized electrically and the key MOSFET parameters were extracted. 3D TCAD Sentaurus device simulation was used for initial transport mechanism study and parameter extraction in the deeply scaled cross-section Si nanowires. Note that more in-depth transport analysis will be reported in chapter 7.

4.1 Operation mode: Accumulation/junctionless vs. inversion

Lately, highly single-type doped Si devices such as accumulation-mode (AM) and junctionless (JL) MOSFETs are proposed as straightforward architectures to eliminate some technical limitations of the nano-scale MOSFETs such as ultra-abrupt junctions, allowing to fabricate even shorter channel devices [1]-[3].

Due to the lack of junctions, the AM and JL devices can show a pretty small leakage current, in the best cases even below the detection limit of the typical measurement systems (e.g. <1 fA) [1]. The AM and JL devices are less sensitive to the gate stack especially below the flat-band voltage, due to volume bulk conduction instead of surface conduction. Not a precise gate alignment is needed for the AM and JL devices, since the already on devices need to be mainly turn off. On the other hand, achieving a high driving current in heavily doped and especially

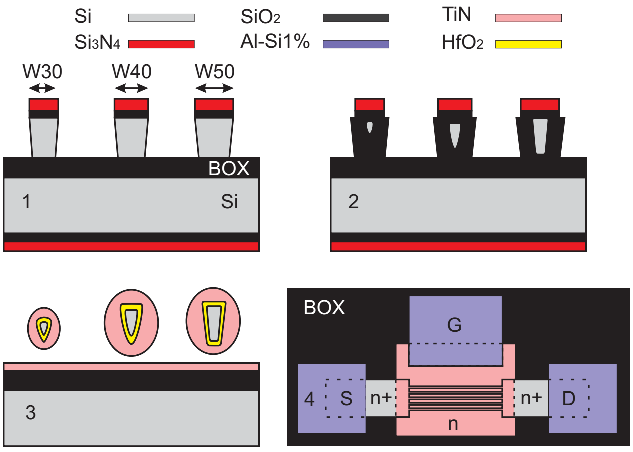

Figure 4.1: Process flow to make accumulation-mode GAA suspended uniaxially tensile strained Si nanowire nMOSFETs on a SOI substrate. W30 represents the initial 30 nm nanowire width on the mask.

in deeply scaled channels such as multi-gate nanowires and Fins is an engineering challenge due to the limitation of carrier mobility by ionized impurity scattering and the integration of mobility boosters such as local stressors in a CMOS process flow including suspended channels.

4.2 Fabrication and stress development during the process

Fig. 4.1 represents the process flow. The fabrication process is started using 100 mm (100) Unibond SOI wafers (SOI/BOX= 340/400 nm) with intrinsic p-type doping and 525 μm thickness. The SOI layer was thinned down to ≈100 nm by sacrificial dry oxidation. The oxide layer was stripped by BHF and afterward, phosphorous ion implantation (20 keV, 5×10^{13} cm^{-2}) was done in the presence of a 20 nm thick LTO layer as the implantation mask on top of the SOI layer. It followed by a 4 hour furnace annealing at 1000 °C to create a nominal 1.0×10^{18} cm^{-3} n-type SOI layer. A tensile hard mask including a stack of 80/15 nm of Si_3N_4/SiO_2 was deposited/grown by LPCVD/dry oxidation at 770 °C and 850 °C, respectively. The nitride layer includes a residual thin film stress of 1.3 GPa biaxial tensile stress, can be engineered by deposition temperature, stoichiometry and thickness [28]. The oxide layer was mainly used as a buffer layer to avoid generation of dislocations in the SOI active layer.

Afterward, dense arrays (≈8 nanowire/μm) of 10 parallel Si nanowires in <110> as well as <100> orientations, with 10-60 nm mask width and 0.5-3.0 μm length, together with the S/D pad patterns were written using e-beam lithography (150 nm thick negative tone XR-1541-006 HSQ, exposure parameters in Vistec EBPG5000: 100 keV, 3000 μC/cm^2 dose).

The hard mask was etched using an anisotropic fluorine-based dry etching and afterward, the SOI device layer was etched using a HBr/O_2-based dry etching to create slanted Si side-walls to

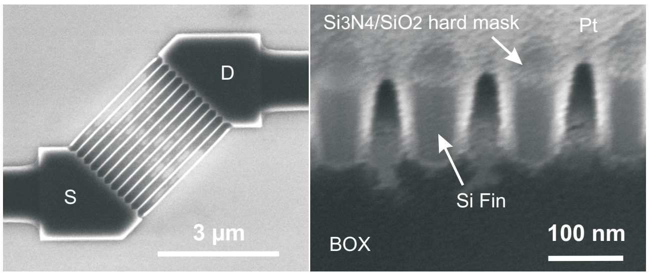

Figure 4.2: SEM micrograph of a HSQ pattern including 3.0 μm long and 25 nm wide array of nanowires in <100> orientation (left); SEM nanograph of Si Fins with ≈88.6° slanted side-walls, obtained using HBr/O_2 chemistry (right).

shrink the width further along the Fin to be able to deplete the highly doped channel properly (see Fig. 4.2). To reduce the Fin width even below 10 nm, round the sharp Si corners as well as accumulate uniaxial tensile stress in the suspended Si nanowire [4], a 7 hour stress-limited dry oxidation at 925 °C (0.500 L/min O_2, 10.00 L/min N_2), to consume nominally 9 nm of (100) Si, in the presence of the tensile nitride hard mask was done. It is worth mentioning that the Si consumption on the slanted Si side-walls was observed to be ≈40% higher than (100) Si surface. As Figs. 4.1, 4.3 and 4.4 represent, Si nanowires with triangular as well as trapezoidal cross-sections can be achieved from this process flow depending on the initial width of the Fins before oxidation.

Hot phosphoric acid (155 °C) was used to strip the nitride hard mask. Afterward, RCA (including 8 min HF dip to strip the grown SiO_2 and suspend the Si nanowires from the substrate), 5 nm HfO_2 deposition by ALD (ASM ALCVD Pulsar 2000, 265 °C), RTA (600 °C, 15 min) and finally, 50 nm TiN deposition by sputtering at room temperature (Veeco Nexus, target power: 500 W) including -2.0 GPa intrinsic biaxial compressive stress were done to make the gate stack as well as accumulate more uniaxial tensile stress in the suspended Si nanowires [5].

Gate patterning (including a 50/10 nm of LPCVD Si_xN_y/LTO mask, optical lithography and metal-gate/high-k etching), S/D ion implantation by phosphorous and annealing (2×10^{20} cm^{-3} nominal doping), metallization (Al-Si1%) and finally, post-metallization annealing (450 °C, 30 min) were the further process steps.

It is worth mentioning that the smallest GAA Si nanowire MOSFETs were achieved from W30 nanowires and all the W10 and W20 nanowires were consumed during the oxidation step. Therefore, in this chapter we mainly focus on the electrical characterization and transport analysis of GAA deeply scaled Si nanowire MOSFETs (W30).

4.2.1 Uniaxial tensile stress development during the process

Dry oxidation of fixed-fixed Si nanowires in the presence of a tensile Si_3N_4 hard mask on top at 925 °C helps to accumulate mechanical potential energy in the nanowires due to in-

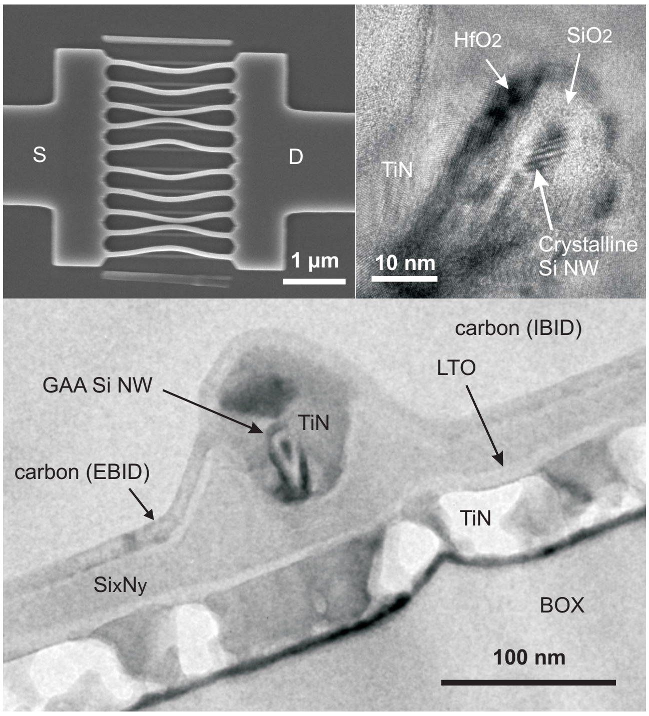
S
D
1 µm
HfO2
SiO2
TiN
Crystalline Si NW
10 nm
carbon (IBID)
LTO
GAA Si NW
TiN
carbon (EBID)
TiN
SixNy
BOX
100 nm

Figure 4.3: SEM micrograph of a buckled array of GAA Si nanowires after the gate stack step (left); TEM nanograph from the channel (right); TEM nanograph from the cross-section of a GAA Si nanowire (bottom). The cross-section of the Si nanowire is triangular with $W_{top} \approx 4$ nm. The TEM cross-section was obtained using FEI CM300 at EPFL.

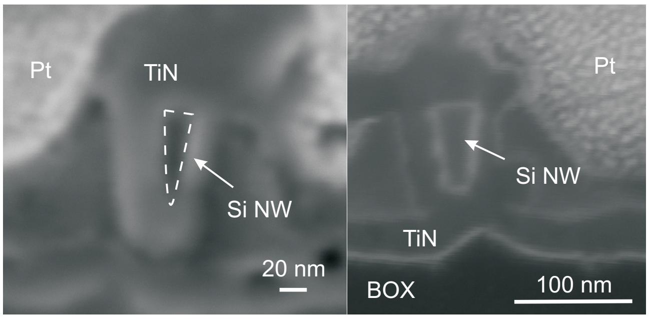
Pt
TiN
Si NW
20 nm
Pt
Si NW
TiN
BOX
100 nm

Figure 4.4: SEM micrographs from the cross-section of the GAA triangular (W40) and trapezoidal (W50) Si nanowires, after the gate stack step.

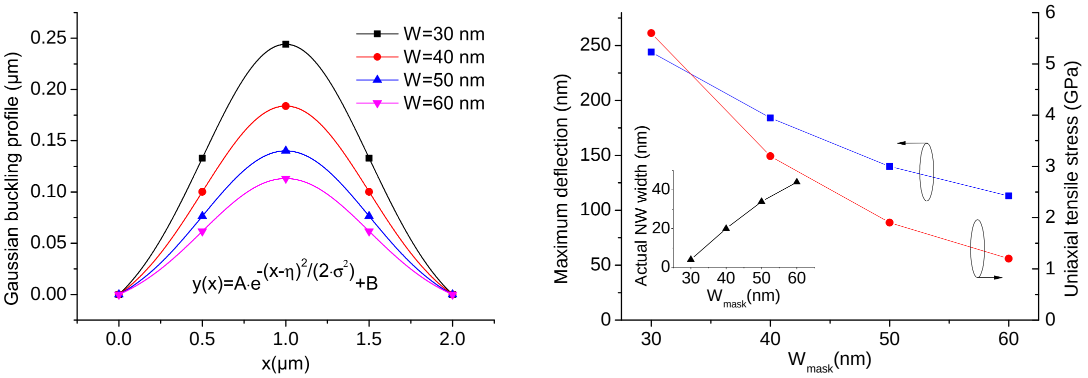

Figure 4.5: Left: approximate symmetric Gaussian buckling profiles along 2.0 μm long gate-all-around Si nanowires with different initial mask nanowire widths. Right: maximum deflection and uniaxial tensile stress level in the buckled Si nanowire vs. nanowire width on the mask. The inset shows actual nanowire width vs. mask nanowire width.

plane elongation and out-of-plane buckling restrictions during the oxidation process [4]. Thermal oxidation of Si below glass transition temperature of SiO_2 (960 °C) helps to avoid viscoelastic stress relaxation in the growing oxide layer and in the thin oxide layer of the hard mask to be able to store the optimum value of mechanical potential energy in the nanowires during oxidation [4]. This stored mechanical potential energy will be released in the form of nanowire mechanical buckling after stripping the hard mask, the grown oxide and the nanowire detachment from the substrate.

The thin film stress in the metal-gate layer can be engineered by sputtering power, thickness, deposition temperature [5] or changing the deposition method e.g. ALD. The metal-gate thin film with an intrinsic compressive stress (-2.0 GPa) tends to stretch, causing further elongation/buckling of the suspended Si nanowires.

4.2.2 Interfacial SiO_2 thin film layer between Si nanowire and HfO_2

Note that formation of a ≈5 nm SiO_2 interfacial thin film between the NW and the HfO_2 layer in Fig. 4.3 is due to the diffusion of oxygen atoms via the 50 nm thin metal-gate layer, can be suppressed using a thick conformal metal-gate capping layer right after the metal-gate deposition step [6]. The first metal-gate deposition using ALD for such 3D structures is more recommended, due to a more conformal metal thin film all around the suspended structures.

4.3 Stress estimation for the buckled gate-all-around Si nanowires

Fig. 4.3 represents the top-view SEM micrograph of an array of buckled deeply scaled Si NWs right after the gate stack step, with the depicted TEM cross-sections. Using micro-Raman

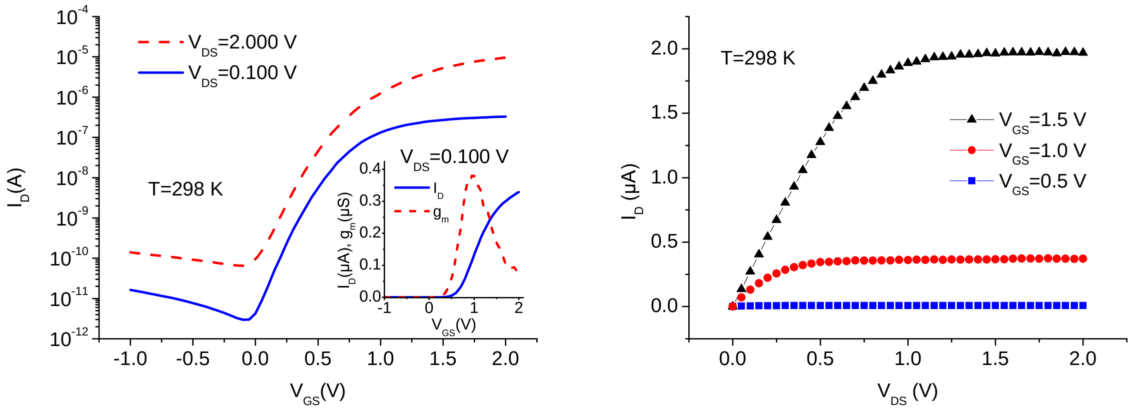

Figure 4.6: Output characteristics of a GAA uniaxially tensile *strained* Si nanowire AMOSFET (SEM and TEM nanographs shown in Fig. 4.3) at 298 K (left). Its transfer and transconductance characteristics at 298 K (right). The I_{on}/I_{off} ratio is 1.5× 10^5 at V_{DS}=2.000 V.

spectroscopy is pretty challenging to measure the stress value in the channel of such GAA Si nanowires with a high-k/metal-gate stack due to the non-transparency of the metal-gate layer. Therefore, by assuming a Gaussian buckling profile along the NW and considering only the represented in-plane buckling in Fig. 4.3, the average uniaxial tensile stress/strain value is estimated to be ≥ 2.5 GPa/1.5% (assuming Si Young's modulus of 169 GPa).

According to [7], the electron mobility enhancement is saturating in the Si-based MOSFETs by including > 2.0 GPa uniaxial tensile stress in the channel and therefore, the highest nominal electron mobility enhancement is already expected in such bended Si nanowires. A more in-depth stress study in [8] reveals that the uniaxial tensile stress/strain level for similar 2.0 μm long GAA Si nanowires can be up to ≈5.6 GPa/3.3% considering both in-plane and out-of-plane buckling using both top and tilted-view SEM micrographs. According to [9] and as expected from the buckling profile in the SEM micrograph in Fig. 4.3, such strained Si nanowires are in the elastic regime and therefore, no carrier degradation is expected due to no plastic deformation in the channel.

4.4 Electrical characterization

4.4.1 Room temperature (298 K)

A setup including a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer was used for electrical characterization at different temperatures. Fig. 4.6 shows the transfer, transconductance and output characteristic of a GAA AMOSFET including an array of 10 deeply scaled cross-section Si nanowires in <110> orientation, depicted SEM and TEM micro/nanographs in Fig. 4.3, at 298 K. The <110> orientated Si nanowire devices were chosen simply to investigate the highest uniaxial tensile stress-induced performance [7].

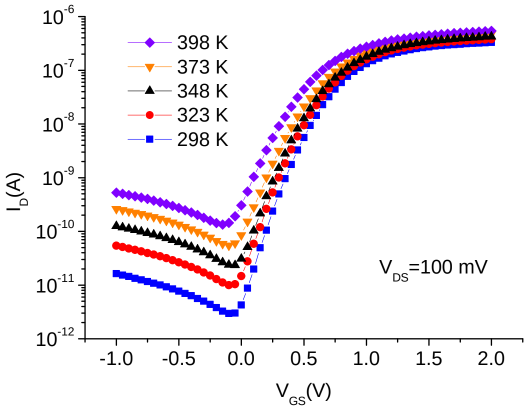

Figure 4.7: Transfer characteristics of a GAA uniaixially tensile *strained* Si nanowire AMOSFET at different temperatures (SEM and TEM nanographs shown in Fig. 4.3).

4.5 High temperature performance MOSFET demonstration

To investigate high temperature performance of GAA deeply scaled Si nanowire AMOSFETs, electrical characterization of the same device, depicted SEM and TEM micro/nanographs in Fig. 4.3, were done at 298-398 K with a 25 K step using the mentioned setup in 4.4.1 and the transfer characteristics were plotted in Fig. 4.7. Parallel to the high temperature performance MOSFET demonstration, this study will be used in 4.8 for further scattering mechanism detection in nanoscale.

4.6 Transport mechanism in the AM/JL MOSFETs

There is no junction in both AM and JL MOSFETs (a single type doping) while the doping level of the channel will nominally define the device type (heavily doped devices, $>1\times10^{19}$ cm^{-3}, called junctionless). The both devices have almost the same operation mechanism and the V_{FB}-V_{TH} difference can be engineered by doping level modulation in the channel. Therefore, the main operation regime for the heavily doped devices (JL) is usually bulk ($V_{TH}<V_{GS}<V_{FB}$), due to the large V_{FB}-V_{TH} difference, and for slightly or highly doped devices (AM) is accumulation ($V_{GS}>V_{FB}$). Operation in the bulk regime has the advantage of less degradation of carrier mobility due to the perpendicular field (conduction at the middle part of the channel) [10] but suffering from a non-straight forward analytical model in this region [11].

4.6.1 3D TCAD Sentaurus device simulation

TCAD Sentaurus Device simulation (V. 2010.12) was used for 3D simulation of a GAA deeply scaled rounded triangular NW AMOSFET (see Fig. 4.8), with a similar cross-section depicted in Fig. 4.3, similar channel and S/D doping but a shorter gate length (100 nm).

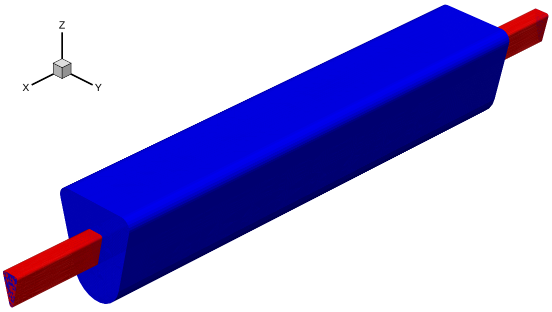

Figure 4.8: The 3D structure used for TCAD Sentaurus Device simulation. The gate length is 100 nm.

4.6.2 3D quantum mechanical confinement effect

The density-gradient model was used in the simulations to describe the 3D quantization effects in such a deeply scaled Si nanowire with sub-5 nm cross-section. The transfer characteristics with and without quantum correction at V_{DS}=100 mV were plotted in Fig. 4.9. The threshold voltage for each case was extracted from the simulation data using the derivative of g_m/I_D method [12], minimizing the effect of gate-voltage dependent mobility and series-resistance. Quantum confinement was found to upshift the threshold voltage by 45 mV, a similar trend to the inversion-mode devices due to the higher quantized subband energies [13]-[14], and degrade the drain current, as shown in Fig. 4.9-left, from 8% in strong accumulation (V_{GS}=1.300 V) to 90% in the subthreshold region (V_{GS}=0.200 V).

The flat-band voltage of the deeply scaled GAA Si nanowire AMOSFET was considered as a gate voltage that the electrostatic potential is almost constant across the channel cross-section (in both y and z directions) without considering any quantum mechanical effect, found to be 0.342 V (≈12 mV above the threshold voltage).

To study better the effect of quantum confinement on only the current degradation, the drain currents are plotted vs. gate overdrive voltage (V_{GS}-V_{TH}) in Fig. 4.9-right. The drain current was found to drop from 15% to 5% by increasing the gate overdrive voltage from 0.300 to 1.000 V. Therefore, the quantum effect was found to be significant at the first glance combining both threshold and drain current shifts in Fig. 4.8, but its effect on only the drain current degradation seem to be negligible in only strong accumulation regime leading to extract the key MOSFET parameters for a deeply scaled Si nanowire MOSFET, as an approximation using the classical extraction methods in the strong accumulation regime.

To understand better the conduction mechanism in such a deeply scaled cross-section channel with corners, the electron densities at the middle of the device were plotted in Fig. 4.10 for three different gate voltages representing subthreshold, above the threshold and above the

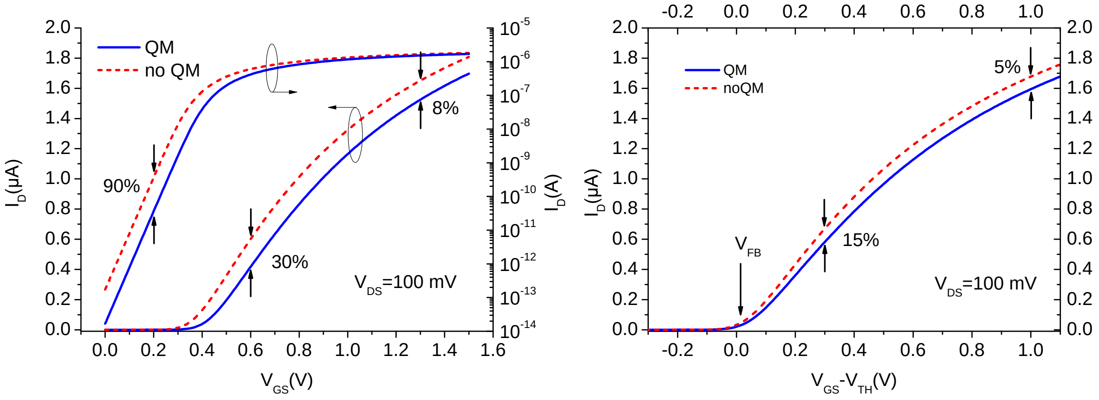

Figure 4.9: Transfer characteristics at V_{DS}=100 mV with and without considering quantum mechanical effect (V_{TH}(no QM)=0.330 V, V_{TH}(QM)=0.375 V) (left). Drain current vs. gate overdrive voltage (V_{GS}-V_{TH}) with and without considering quantum mechanical effect (right).

flat-band voltages. According to Figs. 4.10 and 4.11, bulk conduction is the main conduction mechanism below the flat-band voltage while in the strong accumulation regime, surface conduction as well as corner effect plays the major rule in the conduction mechanism. As shown in Fig. 4.11, the electron density distribution in the channel cross-section is mainly rearranged by quantum confinement in the strong accumulation regime.

4.6.3 I-V analytical model in the strong accumulation regime

At the first glance, the device represented in Fig. 4.3 can be seen as a degenerate double-gate architecture and therefore, an estimation of the accumulation current can be obtained from [11]. Indeed, noting that in the linear accumulation regime (V_{DS}<V_{GS}-V_{FB}), the log terms can be discarded in the charge versus potential and retaining only the highest order term in equations 16, 22 and 24 in [11] (an assumption valid only in strong accumulation), we obtain (using source as a reference):

$$I_D(V_{GS}) = I_{Bulk} + I_{Acc}(V_{GS}) \tag{4.1}$$

where I_{Bulk} does not increase further by V_{GS} and this fixed term in the strong accumulation regime represents the current carried out from a uniformly doped Si channel, ignoring the field effect. The accumulation current equals:

$$I_{Acc}(V_{GS}) = \mu \cdot C_{ox} \cdot W_{eff}/L \cdot [(V_{GS} - V_{FB}) \cdot V_{DS} - 0.5 \cdot V_{DS}^2] \tag{4.2}$$

where μ, W_{eff}, L and C_{ox} are mobility, effective channel width, channel length and gate oxide capacitance, respectively. Apart from these differences, such an asymptotic relationship derived for strong accumulation reverts to the one commonly used for bulk MOSFETs operating

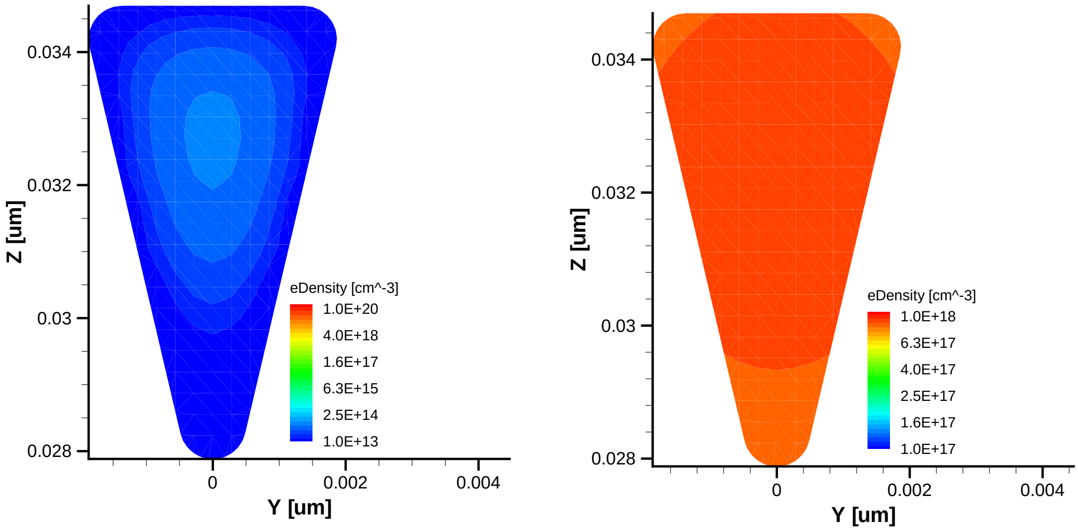

Figure 4.10: The simulated electron density in the cross-section of a GAA deeply scaled Si nanowire AMOSFET in different regimes (cut at the middle of the device shown in Fig. 4.8, the surrounding gate dielectric is not shown): Subthreshold (left, V_{GS}=0.100 V) and between the threshold and the flat-band voltage (middle, V_{GS}=0.340 V). The simulations exclude any quantum correction.

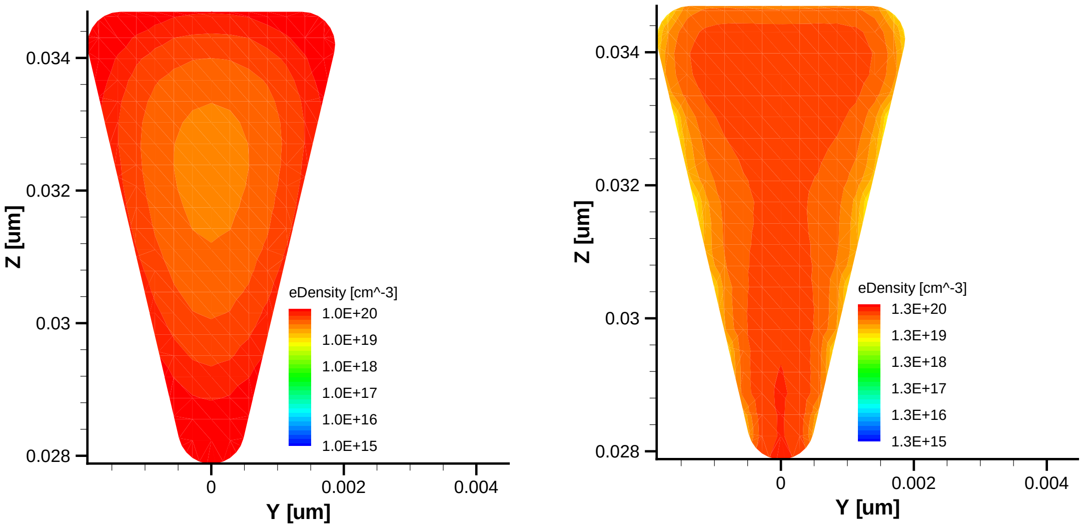

Figure 4.11: The simulated electron density in the cross-section of a GAA deeply scaled Si nanowire AMOSFET above the flat-band voltage and in the strong accumulation regime at V_{GS}=1.500 V: without considering quantum correction (left), considering quantum correction (right). The electron density in the channel cross-section is rearranged significantly by quantum confinement.

under high inversion. This property will serve as a basis to extract mobility related parameters considering W_{eff} as the channel electrical width.

4.6.4 Subthreshold swing

The subthreshold slope for the deeply scaled Si nanowire MOSFET was found to be 106 mV/dec. at V_{DS}=100 mV and 298 K. The accumulation-mode and junctionless devices have shown almost ideal subthreshold behavior [1]-[2] and since the conduction path in this regime is at the middle of the channel instead of surface or corner conduction (see Fig. 4.10-left, a simulation without considering quantum confinement), such devices are expected to be less sensitive to the gate stack below the flat-band voltage. Also, the prior highly strained MOSFETs in [5] and [27] have shown almost ideal subthreshold behavior and the subthreshold slope, especially for the devices with an ALD gate stack, can be improved using an excellent channel-dielectric interface [18].

4.6.5 I_{on}/I_{off} ratio

According to Fig. 4.6, the buckled GAA Si nanowire MOSFET shows excellent high performance MOSFET behavior at also a high drain voltage. The $\mathrm{I}_{on}/\mathrm{I}_{off}$ ratio was found to be $\approx 1.5\times10^5$ at V_{DS}=2.000 V (see Fig. 4.6). Due to having no junction in a single-type doped MOSFET, the leakage current is expected to be pretty small, even in the limit of our measurement setup [1]. Local strain engineering also leads to increase the driving current while not affecting the off current. Therefore, by optimizing the ALD gate stack step, even the observed sub-100 pA leakage current at V_{DS}=2.000 V can be reduced by more than two orders of magnitude [1].

4.7 V_{TH}, V_{FB} and low-field mobility extraction

4.7.1 Threshold voltage extraction

The threshold voltage of a MOSFET, in general, can be extracted using the transconductance change (TC) method [24], quasi-independent of series resistance and no need to any accurate analytical model. Interestingly, as shown in Fig. 4.12, the TC peak is located almost at the expected (theoretical) threshold voltage from the linear part of the transfer characteristic. It is worth mentioning that the derivative of $\mathrm{g}_m/\mathrm{I}_D$ method to extract the threshold voltage [12], used in section 4.6 for the simulation data could not provide consistent results using the measurement data.

Since the accumulation-mode and junctionless transistors work in a simple MOSFET-like manner only above the flat-band voltage but not above the threshold voltage [11], direct extraction of the flat-band voltage as a key MOSFET parameter from the characterization data seem to be pretty necessary. At the first glance, the V_{FB} value is expected to be extracted using the intersect of the two quasi-straight lines above the threshold voltage corresponding

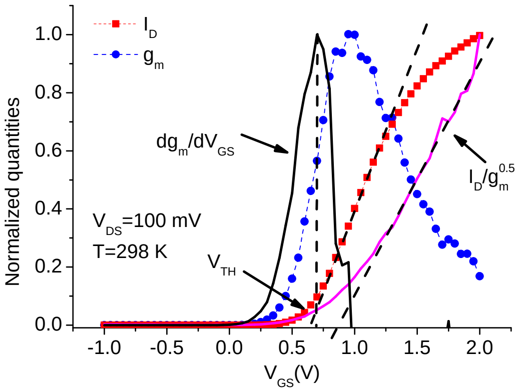

Figure 4.12: V_{TH} and low-field electron mobility extraction of an AMOSFET using the transconductance change [24] and $I_D/\sqrt{g_m}$ [15] methods.

to the bulk and accumulation regimes in the transfer characteristic [25] or using $I_D/\sqrt{g_m}$ in the strong accumulation regime as an approximation [21]-[22]. TCAD Sentaurus Device simulation reveals that the V_{FB}-V_{TH} difference for the deeply scaled cross-section in Fig. 5 is ≈12 mV at 1×10^{18} cm^{-3} phosphorous doping level and at 298 K. Therefore, the direct V_{FB} extraction from e.g. the transfer characteristic of our deeply scaled Si nanowire MOSFETs is almost beyond the accuracy of the extraction methods and the V_{FB} value simply should be approximated using the TCAD simulations at various temperatures. It is also worth mentioning that the both mentioned V_{FB} extraction methods seem to be pretty sensitive to the series resistance for the multi-gate scaled devices (see [26] and [12]) and several efforts should be addressed to the extraction methods for such multi-gate scaled devices.

4.7.2 Low-field electron mobility extraction in accumulation regime

Since the bulk current doesn't change above V_{FB} and not contributing significantly in the conduction in that regime, low-field electron mobility in the accumulation regime can be extracted simply using the $I_D/\sqrt{g_m}$ method [15] in the strong accumulation regime, independent of series resistance and mobility attenuation factor. To extract the low-field electron mobility, a cylindrical model, similar to [16], was used to expect the C_{ox} value for the GAA deeply scaled nanowires.

In this work, the extracted low-field electron mobility at V_{DS}=100 mV is 332 $cm^2/V{\cdot}s$, 32% higher than bulk Si electron mobility at the same level of doping (1×10^{18} cm^{-3}) [17], which is an evidence of including uniaxial tensile stress in the channel, and possibly a higher level can be achieved in this level of stress [7] in the case of an optimum dielectric-channel interface quality especially for the deeply scaled channel cross-sections [18].

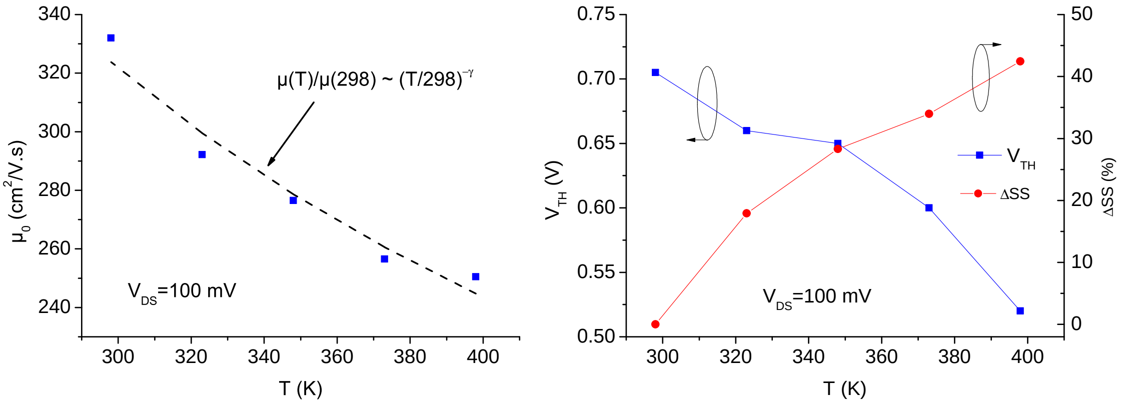

Figure 4.13: Low-field electron mobility dependence on temperature for a GAA uniaxially tensile *strained* Si nanowire AMOSFET (left). The extracted γ is 0.966. Temperature dependence of threshold voltage and subthreshold slope of a GAA uniaxially tensile *strained* Si Nanowire AMOSFET (right).

4.8 Scattering mechanism in the GAA highly doped Si nanowires

Fig. 4.13 depicts the low-field electron mobility at different temperatures for a single deeply scaled cross-section AMOSFET device. According to [19], the carrier mobility in the scattering regime (T>100 K) is varying by temperature according to the following trend:

$$\mu(T)/\mu(T_0) = (T/T_0)^{-\gamma} \tag{4.3}$$

where T_0=298 K. According to Fig. 4.13, γ=0.966 which is quite lower than 2.5, reported for the GAA Si nanowire MOSFETs with intrinsic doping level [20]. Our experiment in [21] is also reporting a similar γ value for the GAA triangular Si nanowires with a slightly bigger cross-section (sub-20 nm) with the same doping level. All the three studies in [20], [21] and [22] are in line with the previous reports for intrinsic or low-doped Si [23] being explained by the dominant role of ionized impurity scattering in highly doped Si MOSFETs, even for the deeply scaled Si nanowires.

4.9 V_{TH} drift by temperature in the GAA Si nanowire MOSFETs

Fig. 4.13-right shows a V_{TH} drift of -1.72 mV/K (smaller than -2.1 mV/K, the prior reported value for a deeply scaled GAA low doped Si nanowire in [20]) and a subthreshold slope change of 0.404%/K (with subthreshold slope of 106 mV/dec. at room temperature) for the 298-398 K temperature range.

4.10 Summary

In this chapter, we developed a process flow to make dense array of accumulation-mode gate-all-around deeply scaled cross-section (scalable down to 4 nm) top-down Si nanowire nMOSFETs on a SOI substrate using a high-k/metal-gate stack. The NW cross-section is varying from rounded triangular to trapezoidal, depending on the mask initial NW width. Both tensile and compressive stresses can be integrated to this platform using e.g. metal-gate strain while the integration of both local oxidation and metal-gate strain technologies are reported for the first time. The expectation level of stress, using top and tilted-view SEM pictures while assuming a Gaussian buckling profile and a uniform stress along the buckled NW, is up to ~5.6 GPa uniaxial tensile stress. We reported significant stress level modulation of ~5.6 to ~1.2 GPa uniaxial tensile stress using NW width modulation (4 to 44 nm, respectively) on the same wafer and for the first time. We demonstrated the GAA sub-5 nm cross-sectional NWs in a highly doped regime (1×10^{18} cm^{-3}) as high temperature performance MOSFETs (298-398 K) and the low-field mobility temperate dependence and afterward, the scattering mechanism was studied in those devices and an ionized impurity based scattering was reported. The low-field mobility values are extracted using the Y-function method, quasi-independent of series resistance and mobility attenuation factor, in strong accumulation regime, and 32% low field electron mobility enhancement is reported at V_{DS}=100 mV and T=298 K, in comparison to the electron mobility in bulk Si at the same doping level. The I_{on}/I_{off} ratio of 1.5×10^5 at V_{DS}=2.000 V and the subthreshold slope of 106 mV/dec. at V_{DS}=100 mV are reported for the mentioned device at T=298 K, can be improved further using an excellent channel-dielectric interface. Note that this is the first integration of e-beam lithography and ALD high-k/metal-gate stack at EPFL. The threshold voltage values are extracted using the transconductance change method, quasi-independent of the conduction mechanism and series resistance, we reported a threshold voltage drift of -1.72 mV/K for the measured device. TCAD device simulation was used to estimate the difference between the flat-band and the threshold voltages as well, based on the actual device cross-section.

The original work carried out relative to this chapter includes:

- **Development of a SOI Si nanowire platform with ALD gate stack**: I developed a SOI Si nanowire platform to make sub-5 nm cross-section Si nanowires using side-wall Si nanowire engineering and stress-limited oxidation [22], [29]. This was the first SOI Si nanowire platform at EPFL including an ALD high-k/metal-gate stack. Several process developments were done at EPFL e.g. EBL to pattern dense array of nanowires, NW pattern transfer to the SOI substrate in the presence of a Si_3N_4 hard mask, HBr/O_2-based Si etching to obtain minimized cross-sections before the oxidation step, appropriate ALD high-k/metal-gate stack recipes suitable for the 3D suspended structures and finally, HfO_2 dry etching and isotropic TiN etching recipes. Integration of local oxidation and metal-gate strain was done for the first time. Up to ~5.6 GPa uniaxial tensile stress is estimated in the buckled Si nanowires assuming a Gaussian buckling profile [8]. Local oxidation was used for stress-limited oxidation and as a stressor technology for the first time as well.

- **High temperature performance MOSFET demonstration**: Electrical characterization of GAA deeply scaled cross-section Si nanowire MOSFETs was done from 298-398 K using a cascade prober and Semiconductor Parameter Analyzer. The key MOSFET parameters were extracted from the electrical characterization data and the stress-based low-field electron mobility enhancement is reported in comparison to the non-strained bulk electron mobility at the same doping level. Scattering mechanism was studied in nanoscale and in a highly doped regime as well [22].
- **3D TCAD Sentaurus device simulation**: As a first step to use TCAD device simulation for transport analysis in GAA scaled cross-section Si nanowires, 3D TCAD Sentaurus device simulation was done based on the TEM cross-section of the electrically characterized device [29]. Device simulation was used to have an estimation of device behavior from subthreshold to strong accumulation as well as an estimation on the V_{FB}-V_{TH} parameter. Note that an accurate estimation on the flat-band voltage needs CV measurements on the devices, needing a pretty large array of nanowires.

4.11 Future works

- **ALD gate stack improvement**: This is needed to optimize the subthreshold slope as well as leakage current. The interfacial SiO_2 thin film between the channel and high-k should be suppressed by using a thick conformal second metal-gate deposition right after the first metal-gate deposition step. The first metal-gate deposition should be performed using ALD for the 3D structures as well.
- **Contact engineering:** This step helps to reduce significantly the series resistance, should be done using S/D ion implantation, annealing and S/D metallization (AlSi-1%). Minimizing the current sub-2 μm distance between S/D and gate can help further to reduce the series resistance as well.
- **Electrical characterization of various cross-section NWs**: Comparing the electrical characterization of different devices with various cross-sections is a pretty good idea. Note that the stress level can change significantly by NW length and width. Therefore, it can be used to study the flat-band voltage variation by stress. Study the effect of cross-section shrinkage on the mobility value in a highly and heavily doped regime can be performed as well (e.g. the effect of surface roughness scattering, quantum confinement, corner effect, etc.). The V_{FB}-V_{TH} difference can be studied by cross-section engineering to widen the bulk conduction regime (between threshold and flat-band) in a heavily doped regime. RF behavior of GAA Si nanowire MOSFETs at different channel doping level (especially AM/JL MOSFETs) and in the presence of stress can be done as well.
- **Investigate GAA Si NW MOSFETs as ultra-low power/low voltage switches**: This can

be done using appropriate threshold voltage engineering (e.g. sub-100 mV) to use the transistors with e.g. sub-100 mV power supply voltage. In such operation regimes, the contribution of strain engineering can be investigated as a CMOS booster (improve I_{on}/I_{off} ratio, etc.). This can be performed on inversion-mode, accumulation-mode and junctionless MOSFETs.

- **Implementation of GAA Si NW pMOSFETs including strain engineering**: Including uniaxial compressive stress can be done simply by metal-gate intrinsic thin film stress engineering to improve the carrier mobility in the PMOS devices. In the case of including both uniaxial tensile and compressive stresses on the same wafer, multi-gate CMOS architectures can be fabricated including appropriate stressors as CMOS boosters.

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5 Local volume depletion/accumulation in GAA Si NW junctionless nMOSFETs

Multi-gate architectures (except circular cross-sections that can be obtained by hydrogen annealing [1] or stress-limited oxidation [2]) have corners (e.g. see [3]-[7]). Therefore, an in-depth analysis of the corner effect on the electrical characteristics of the multi-gate devices is necessary. In this chapter, we report corner effect analysis in the gate-all-around equilateral triangular Si nanowire junctionless nMOSFETs, from subthreshold to strong accumulation regime using extensive TCAD device simulation (see [8]). This is a first clear step for transport analysis in GAA Si NW junctionless/accumulation-mode MOSFETs (single type doing profile from source to drain [9]-[10]) with various cross-sections and dimensions (circular, triangular, rectangular, etc.) from subthreshold to strong accumulation, can be supported by extensive experiments. We mainly focus on the junctionless/accumulation-mode MOSFETs for simulations and experiments due to their simpler fabrication method (e.g. one implantation step for the junctionless MOSFETs), less sensitivity to the gate stack in subthreshold regime (volume conduction below flat-band) and minimized the leakage current due to having no p-n junction.

To achieve the mentioned purposes, a parameterized GAA equilateral triangular Si nanowire architecture was designed to make a 3D TCAD device simulation platform considering an appropriate 3D meshing strategy due to having a 3D architecture including corners, can be simply adapted for various further device simulations as well. N-type channel doping levels of 1×10^{19}, 5×10^{18} and 1×10^{18} cm^{-3} were used for quasistationary device simulations of junctionless and accumulation-mode MOSFETs, and corner effect was studied for 5, 10 and 15 nm wide equilateral triangular Si nanowire MOSFETs with 2 nm SiO_2 gate oxide thickness (V_{DS}=0 V, T=300 K). To make a clear corner effect study in GAA Si NW junctionless MOSFETs with minimized short-channel effects on the device characteristics, 40 nm long channel length architectures were used for the simulations (> 6 times longer than the natural length of the widest NW, see e.g. [11]). This is a first step to make precise device and transport analysis in multi-gate junctionless architectures with short channel lengths including corners (see e.g. [12]). Note that various Si nanowire cross-sections can be experimentally achievable using bottom-up [13]-[14] or Si NW side-wall engineering by anisotropic Si etching in top-down [4],

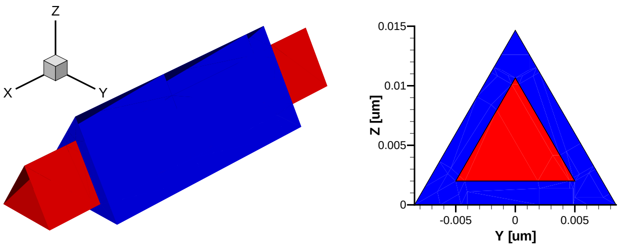

Figure 5.1: Equilateral triangular GAA Si NW MOSFET and its cross-section.

[15] platforms. In this chapter, we only concentrate on the equilateral triangular cross-sections, due to having the narrowest corner angle among the symmetrical architectures.

As a first step, the corner effect analysis was done considering both local and total electron densities in the Si nanowire channel cross-section (with and without channel quantization) at various channel doping levels in a 15 nm wide Si nanowire. The key MOSFET parameters were extracted for each device as well. The concept of local volume depletion and accumulation below and above flat-band, respectively, is analyzed and discussed in details, considering the contribution of volume and surface conduction and majority vs. minority of carriers and in comparison to the typical corner effect in the inversion-mode MOSFETs. Finally, the effect of channel cross-section shrinkage on the local and total electron densities is discussed in details at 1×10^{19} cm^{-3} channel doping level.

5.1 Numerical simulation

TCAD Sentaurus Device (G-2012.06) was used for quasistationary numerical simulation of GAA Si nanowire MOSFETs. Considering electrostatic and quasi-Fermi potential equations, the local carrier densities in a 3D structure can be extracted at each bias voltage. The electrostatic potential for the classic case is the solution of the nonlinear Poisson equation:

$$\nabla \cdot (\epsilon \nabla \psi) = -q(-n + p + N_D^+) \tag{5.1}$$

where q, n, p and N_D^+ are electron charge, electron density, hole density and ionized donor concentration, respectively (ionized acceptor concentration is neglected in our case). To include the 3D quantization effects in nanoscale, the density gradient quantization model is coupled to the Poisson equation [16]-[17]. The quantum correction procedure includes modification of the density of states [17]. The semi-classical Slotboom bandgap narrowing model was used for the highly and heavily doped Si channels [17]-[18]. The local carrier densities can be computed from the electron and hole quasi-Fermi potentials, considering Fermi-Dirac statistics covering both degenerate and non-degenerate regimes [17].

Fig. 5.1 shows the 3D GAA Si nanowire architecture, used for the device simulations (gate length: 40 nm, SiO_2 gate oxide thickness: 2 nm). The Si nanowire width is set to 15 nm (equilateral triangle), and three channel doping levels were investigated. The gate workfunction was set to 4.5 eV (a mid-gap workfunction). In all the simulations, V_{DS} was fixed at 0 V, to eliminate the effect of longitudinal electric field from source-drain potential difference on the local electron density distribution along the channel.

5.2 From subthreshold to strong accumulation in a 20 nm wide Si nanowire MOSFET

Quasistationary TCAD Device simulation was done on a 15 nm wide Si nanowire MOSFET at three channel doping levels (1×10^{19}, 5×10^{18}, 1×10^{18} cm^{-3}). The device characteristics can be studied using local electron density distribution in the channel at each gate voltage as well as charge on the gate vs. gate voltage characteristics (Q_G-V_{GS}, can be obtained directly from the simulations).

5.2.1 Operation of accumulation-mode/junctionless MOSFETs

The junctionless (JL) and accumulation-mode (AM) MOSFETs, unlike the typical inversion-mode (IM) MOSFETs, do not have any p-n junction and the channel doping level is nominally determining the device type (heavily doped devices, $>1\times10^{19}$ cm^{-3}, called junctionless) [9]. The both devices have the same operation mechanism while here we provide a brief explanation on this mechanism for a simple planar single-gate AM/JL nMOSFET.

Below the threshold voltage, the channel is fully depleted while the majority of the subthreshold current is passing through the channel volume (the closer to the channel-dielectric interface, the more depletion). There can be different definitions of threshold voltage. Whereas a simple extrapolation was proposed in [19], in this chapter we will adopt a slightly different condition. Assuming a full depletion approximation, our threshold voltage condition can be approximated when creating a neutral region at the middle of the fully-depleted channel (the corresponding local electron density almost equals the channel doping). The current passing through the neutral region is called bulk current. Applying a higher gate voltage extends the neutral region causing an increase in the bulk current.

The flat-band condition will be reached when the entire channel cross-section is neutral, implying that the bulk current will saturate at this point. Applying a higher gate voltage leads to creation of an accumulation layer close to the channel-dielectric interface. Therefore, the drain current includes one fixed (saturated bulk current) and one variable (accumulation current) component. Note that the V_{FB}-V_{TH} can be engineered by the channel doping, gate oxide thickness, channel cross-section geometry and dimension.

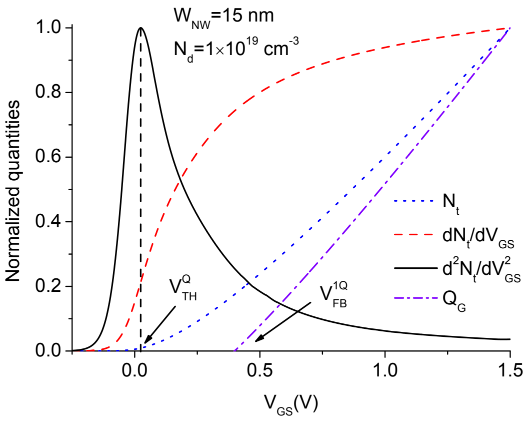

Figure 5.2: Normalized quantities of N_t, dN_t/dV_{GS}, d^2N_t/dV^2_{GS} and Q_G with respect to the maximum values vs. V_{GS} for the GAA 15 nm wide Si nanowire MOSFET at 1×10^{19} cm^{-3} channel doping including quantum confinement. The maximum values for each parameter are 5.46×10^7 cm^{-1}, 4.48×10^7 cm$^{-1}\cdot$V^{-1}, 1.29×10^8 cm$^{-1}\cdot$V^{-2} and 7.35×10^{-12} C$\cdot$cm^{-1}, respectively.

5.2.2 Threshold voltage extraction method

The threshold voltage can be extracted from the peak of the second derivative of the total electron density per unit length (N_t) vs. gate voltage [20] (similar to the transconductance change method [21]), while N_t can be calculated by integrating the electron density over the channel cross-section and at the middle of the channel (x=$L_G/2$; L_G equals gate length):

$$N_t = \int\int n(y,z)dydz \tag{5.2}$$

Fig. 5.2 shows the total electron density per unit length and the corresponding derivatives (normalized to the corresponding maximum values) for a GAA 15 nm wide Si NW MOSFET doped at 1×10^{19} cm^{-3}, including quantum confinement.

5.2.3 Flat-band voltage extraction method

In a standard planar MOSFET, the flat-band voltage is the gate voltage for which the electrostatic potential is being constant in the entire channel cross-section. However, due to the quantum confinement, the flat-band condition cannot be reached in the entire channel cross-section for a certain gate voltage when including corners. Nevertheless, we can still define an effective flat-band voltage for the entire channel cross-section (or quantum flat-band voltage) as a key device operation parameter which can be approximated from the x-intercept of the Q_G-V_{GS} curve as a first step (called V^{1Q}_{FB}), a direct output result from the presented gate charge-V_{GS} quasistatic simulations.

While the flat-band condition can be reached in the entire channel cross-section when dis-

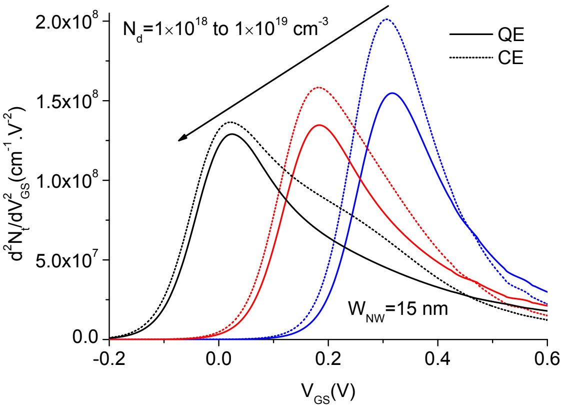

Figure 5.3: d^2N_t/dV_{GS}^2 vs. gate voltage for the GAA Si NW MOSFETs at various doping levels including or not quantization (QE or CE, respectively).

carding quantization, even in the corners, the observed slight difference between the actual flat-band voltage (V_{FB}^C) and the extracted one from the Q_G-V_{GS} curve for the classic case, $V_{FB}^{1C}-V_{FB}^C$, can be used to justify the flat-band voltage extraction method mismatch when quantum effects cannot be neglected. This slight inaccuracy, observed to be below a 13 mV range in table 5.1, is mainly due to the higher electron density in the channel parts close to the source and drain, as well as to the parameter extraction methodology. Based on this remark, we can estimate the effective flat-band voltage for the entire device (V_{FB}^Q or V_{FB}^C).

Note that flat-band condition may not be reached in the entire channel cross-section even for the classic case. This could be due to some local effective bulk doping concentrations in the corners, as reported previously in the subthreshold regime of the inversion-mode devices to describe the local threshold voltage downshift in the corners [20], [22]. But perhaps a much narrower corner angle is needed to significantly affect the local flat-band voltage variation between the corner and the side.

5.2.4 Gate-channel capacitance and effective channel width

Due to the quantization-based gate-channel capacitance [23] and effective channel width shrinkages in GAA NWs, instead of extracting each parameter separately, the CW_{eff} parameter, product of gate-channel capacitance and channel width, is introduced. This parameter can be extracted from the first derivative of the total electron density per unit length (N_t) vs. the gate voltage in strong accumulation regime:

$$CW_{eff}(V_{GS}) = (dN_t/dV_{GS})\cdot q \tag{5.3}$$

The CW_{eff}^{max} values, reported in table 5.1, are extracted at V_{GS}=1.500 V for all structures.

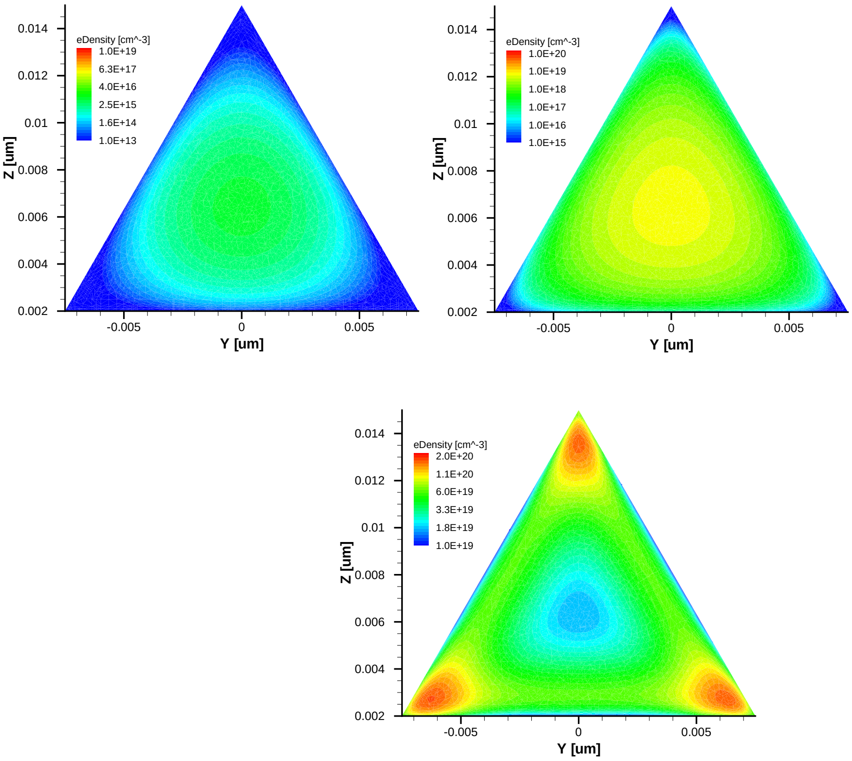

Figure 5.4: Cross-section quantum electron density at the middle of a GAA 15 nm wide Si nanowire junctionless MOSFET for three operation regimes (oxide is not shown, channel doping: 1×10^{19} cm^{-3}). Left: subthreshold (V_{GS}=-0.200 V), center: above threshold (V_{GS}=0.100 V), right: strong accumulation (V_{GS}=1.500 V). Note that V^{Q}_{TH}=0.027 V and V^{Q}_{FB}=0.399 V.

5.2.5 Key MOSFET parameters at different channel doping levels

Fig. 5.3 shows the second derivative of the total electron density per unit length (d^2N_t/dV^2_{GS}) vs. V_{GS} for the GAA 15 nm wide Si NW MOSFETs for three channel doping concentrations, considering classical and quantum effects. The results reported in table 5.1 show that the quantization is upshifting both the threshold and the flat-band voltages, due to the higher quantized subband energies [7], [24]-[25]. Note that even for the heavily doped structure and on the contrary to the IM devices [20], there is no hump effect below the gate voltage corresponding to the main peak in the d^2N_t/dV^2_{GS} vs. V_{GS} curve, thus representing a unique threshold voltage in the system. The hump appearing above the threshold voltage of the heavily doped device in the classical simulation is due to the non-linear operation of bulk regime between the threshold and the flat-band voltages as well as creation of accumulation conduction paths in the channel, reported before for the planar AM devices [10].

N_d (cm^{-3})	V^{C}_{TH} (V)	V^{Q}_{TH} (V)	V^{1C}_{FB} (V)	V^{1Q}_{FB} (V)	V^{C}_{FB} (V)	V^{Q}_{FB} (V)	CW^{Cmax}_{eff} (F/cm)	CW^{Qmax}_{eff} (F/cm)
1×10^{18}	0.306	0.316	0.332	0.351	0.319	0.338	7.62×10^{-12}	7.11×10^{-12}
5×10^{18}	0.181	0.183	0.349	0.379	0.345	0.375	7.63×10^{-12}	7.14×10^{-12}
1×10^{19}	0.025	0.027	0.360	0.399	0.360	0.399	7.65×10^{-12}	7.16×10^{-12}

Table 5.1: Key device parameter extraction from the quasistatic device simulations of the GAA 15 nm wide Si nanowire MOSFETs at different channel doping levels.

5.3 Local electron density distribution across the channel from subthreshold to strong accumulation

Figs. 5.4 and 5.5 show the quantum (QED) and classical (CED) electron density in the cross-section of a GAA 15 nm wide Si nanowire junctionless MOSFET (channel doping: 1×10^{19} cm^{-3}) in subthreshold, above threshold and strong accumulation regimes. According to the figures, the majority of electrons are accommodated in the corner regions only in strong accumulation. To study better the bias-dependent charge distribution mechanism in the channel cross-section, local quantum and classical electron density profiles as a function of gate voltage are plotted along y=0 (see e.g. Fig. 5.4) in Fig. 5.6. This provides a wide range of information on the local electron density variation in the corner, side and volume.

The maximum and minimum of the local classical electron densities in accumulation and depletion regimes are both occurring on the Si nanowire-dielectric interface, respectively. Therefore, a simple way to study the effect of corners on the local electron density variation can be the local classical electron density corner to side ratio at different channel doping and gate voltages. Note that due to the quantization effects, the peak of quantum electron density occurs inside the channel volume. Fig. 5.6-inset shows this ratio as a function of V_{GS}-V_{FB}. According to this figure (as well as from the local classical electron densities at different channel doping levels in Fig. 5.7), corners accumulate more electrons in comparison to the side in accumulation regime (>V_{FB}), while they deplete also further below flat-band.

5.3.1 Origin of local depletion/local accumulation in AM/JL MOSFETs

The different corner effects and device behavior in the IM and AM/JL MOSFETs come from distinct conduction mechanism, surface vs. volume conduction in different regimes, as well as conduction of minority vs. majority carriers. The effect of corners on the carrier density distribution in the channel cross-section is not simple. According to the simulations, it strongly depends on the channel geometry, doping level and dielectric thickness (see e.g. [20], [26]-[28]). There is no clear geometrical definition of the corner region while the analysis becomes even more complex including quantization.

The surface conduction by minority carriers is the only conduction mechanism in IM devices, while AM/JL MOSFETs exhibit surface conduction above V_{FB} and volume conduction below

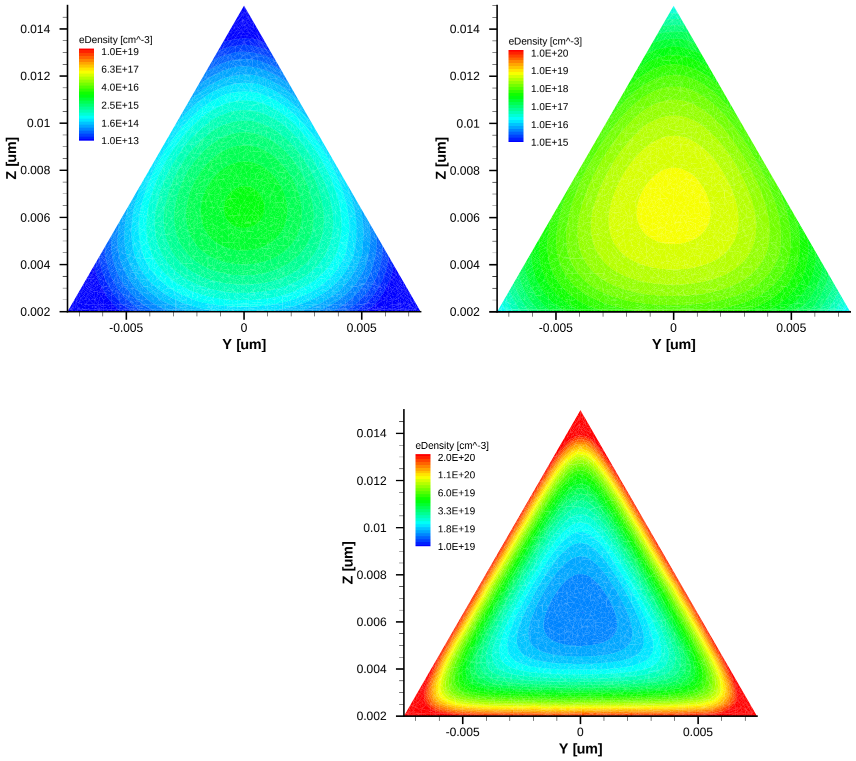

Figure 5.5: Cross-section classical electron density at the middle of a GAA 15 nm wide Si nanowire junctionless MOSFET for three operation regimes (oxide is not shown, channel doping: 1×10^{19} cm^{-3}). Left: subthreshold (V_{GS}=-0.200 V), center: above threshold (V_{GS}=0.100 V), right: strong accumulation (V_{GS}=1.500 V). Note that V_{TH}^{C}=0.025 V and V_{FB}^{C}=0.360 V.

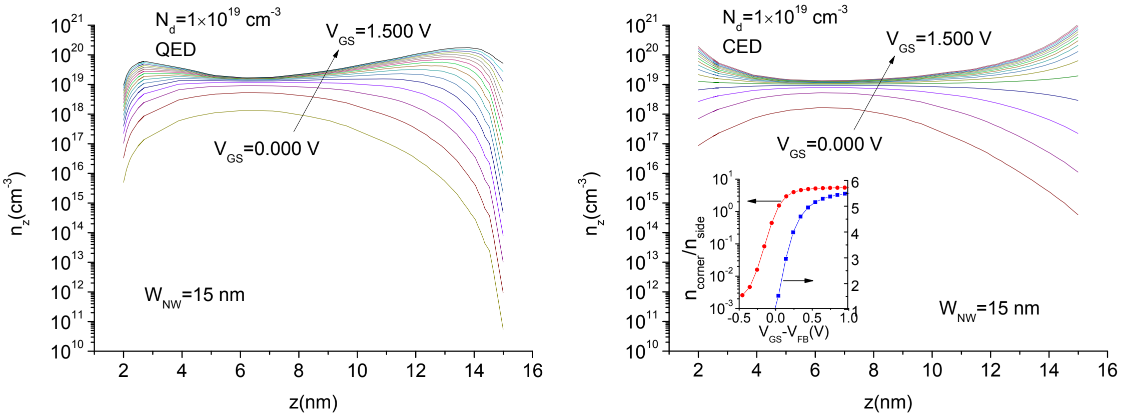

Figure 5.6: Local quantum (top) and classical (bottom) electron density profiles across the 15 nm wide NW channel volume at different V_{GS} (from subthreshold to strong accumulation, step: 0.100 V) at N_d=1×10^{19} cm^{-3} (cut at y=0, see e.g. Fig. 5.4). Inset shows local classical electron density to side ratio from subthreshold to strong accumulation.

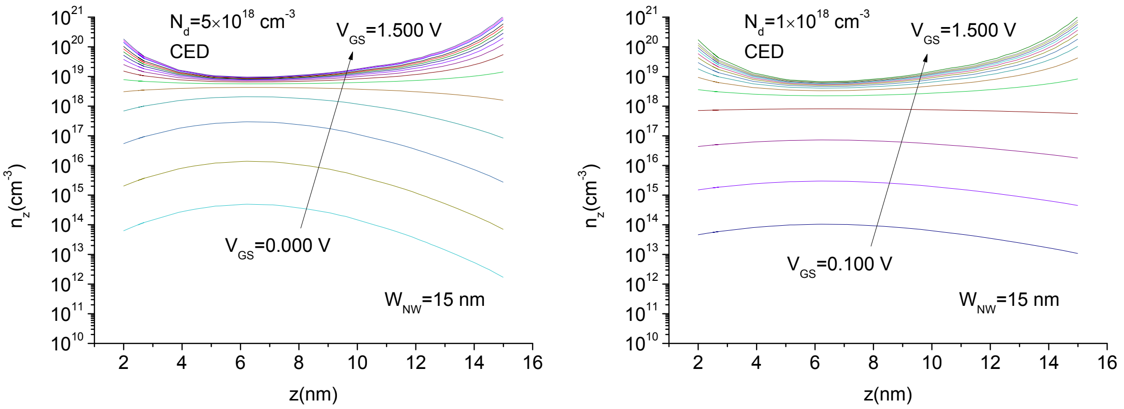

Figure 5.7: Local classical electron density profiles across the 15 nm wide Si nanowire channel volume at different gate voltages (from subthreshold to strong accumulation, step: 0.100 V) for N_d=5×10^{18} cm^{-3} (top) and 1×10^{18} cm^{-3} (bottom). The plots correspond to the cut at y=0.

V_{FB}, both involving majority carriers. Due to having a maximized surface to volume ratio in the corner region in comparison to the side region, the surface conduction mechanisms (above V_{FB} for AM/JL, all operation regimes for IM) should provide a higher local mobile charge density in the corner region (local volume inversion or local volume accumulation in IM and AM/JL devices, respectively). On the other hand, reduction of local effective channel doping in the corners because of side gates and the effective body thickness reduction in the corners were suggested previously to describe the local threshold voltage downshift and local volume inversion in the corners of the IM devices in the subthreshold regime as well [22].

Due to having a smaller effective channel body thickness in the corner region in comparison to the side, the volume conduction mechanism in the corner region is expected to be minimized with respect to the side region below the flat-band voltage, since the volume of corner is negligible. Therefore, no subthreshold conduction path in the corner regions of the AM/JL MOSFETs is expected to emerge from I_D-V_{GS} characteristics, as already observed in Fig. 5.3 (no hump below the main peak of the d^2N_t/dV_{GS}^2 vs. V_{GS} curves).

5.3.2 Corner versus global accumulation electron densities in accumulation regime

To assess corner effects on the global device characteristics, the normalized total accumulation electron density per unit length in the entire channel cross-section is defined as (V_{GS}>V_{FB}):

$$N_t^{acc}(V_{GS}) = N_t(V_{GS}) - N_t(V_{FB}) \tag{5.4}$$

Fig. 5.8 shows how this normalized accumulation electron density varies with respect to the gate voltage for the 15 nm wide Si nanowire MOSFETs, with three different channel doping levels at V_{GS}>V_{FB}. In order to study the effect of quantization and channel cross-section

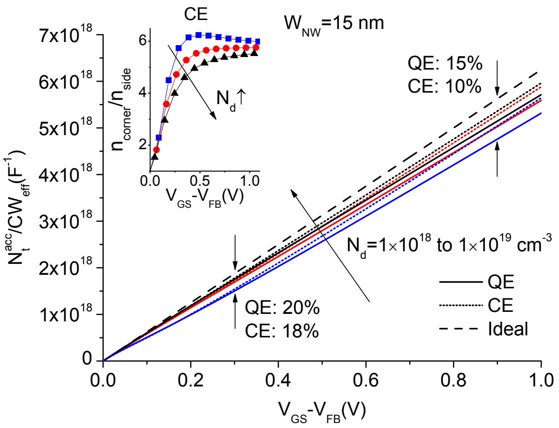

Figure 5.8: Normalized total accumulation electron density per unit length vs. V$_{GS}$-V$_{FB}$ at various channel doping levels including both quantum and classical electrons. The normalization factor is CW$_{eff}$(V$_{GS}$). Inset shows local classical electron density corner to side ratios in accumulation regime.

variation for various devices, accumulation electron densities are normalized to CW$_{eff}$(V$_{GS}$) at each bias voltage (see also section 5.4.1). According to Fig. 5.8, the normalized total accumulation electron density above the flat-band voltage is increasing with the channel doping while all the normalized values are slightly below the ideal limit, that can be calculated as below:

$$N_t^{acc}(V_{GS})/[CW_{eff}(V_{GS})] = (V_{GS} - V_{FB})/q \tag{5.5}$$

Therefore, corners clearly cannot be considered as CMOS boosters. Note that corner to side classical electron density ratio is increasing by channel doping reduction in accumulation regime (Fig. 5.8-inset). On the other hand and from Fig. 5.8, heavily doped structures represent a higher normalized total accumulation electron density per unit length and reveal characteristics closer to the ideal case, reflecting a more uniform distribution of the local electrons in the cross-section. This could be explained by electrostatic screening increase at higher doping levels in accumulation regime. In all cases, the normalized total accumulation electron density per unit length is slightly degraded by quantum confinement as well.

5.4 Cross-section shrinkage and corner effect

In this section, GAA equilateral triangular Si NW MOSFETs with 5 and 10 nm NW width were simulated at 1×10^{19} cm^{-3} channel doping level (2 nm SiO$_2$ gate oxide thickness). The second derivative of N$_t$ (d^2N_t/dV_{GS}^2) vs. the gate voltage curves are plotted in Fig. 5.9 and the extracted device parameters are reported in table 5.2 (the 15 nm wide nanowire with similar doping is added from table 5.1 for comparison). No hump exists below the threshold voltage while the one above the threshold voltage for the classical simulation disappears

W_{NW} (nm)	V^{C}_{TH} (V)	V^{Q}_{TH} (V)	V^{1C}_{FB} (V)	V^{1Q}_{FB} (V)	V^{C}_{FB} (V)	V^{Q}_{FB} (V)	CW^{Cmax}_{eff} (F/cm)	CW^{Qmax}_{eff} (F/cm)
5	0.267	0.344	0.360	0.447	0.360	0.447	2.86×10^{-12}	2.66×10^{-12}
10	0.153	0.171	0.360	0.408	0.360	0.408	5.25×10^{-12}	4.94×10^{-12}
15	0.025	0.027	0.360	0.399	0.360	0.399	7.65×10^{-12}	7.16×10^{-12}

Table 5.2: Key device parameter extraction from the quasistationary device simulations of the GAA Si nanowire MOSFETs with various nanowire widths, all at $N_d=1\times10^{19}$ cm^{-3}.

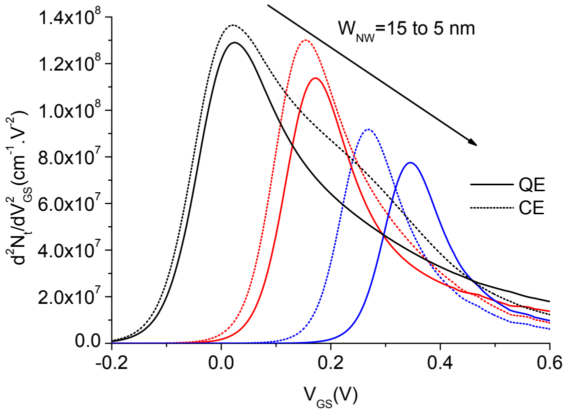

Figure 5.9: d^2N_t/dV_{GS}^2 vs. gate voltage for the GAA Si nanowire MOSFETs for various nanowire widths doped at $N_d=1\times10^{19}$ cm^{-3}, including both quantum (QE) and classical (CE) electrons.

by cross-section shrinkage as well, mainly due to the reduction of bulk conduction regime (V_{FB}-V_{TH}).

5.4.1 Local electron density for various cross-section dimensions

Fig. 5.10 shows the cross-section local electron density distribution in the channel with quantization for 10 and 5 nm wide Si NW JL MOSFETs in strong accumulation (V_{GS}=1.500 V). Significant charge redistribution in the 5 nm wide NW cross-section, can be called *volume accumulation*, in comparison to the wider ones together with 77 mV and 87 mV upshifts in the threshold and the flat-band voltages, respectively, are the typical quantization effects in such scaled 1DEG architectures. The local classical electron density profiles along y=0 are plotted in Fig. 5.11 for both devices at different V_{GS}. According to Fig. 5.12, the normalized total accumulation electron density per unit length becomes closer to the ideal limit for the wider structures. This corner effect is pretty close to the one occurring in the IM devices, simply due to less contribution of the corner regions on the electrostatics in the entire channel cross-section and less quantization effects for wider structures.

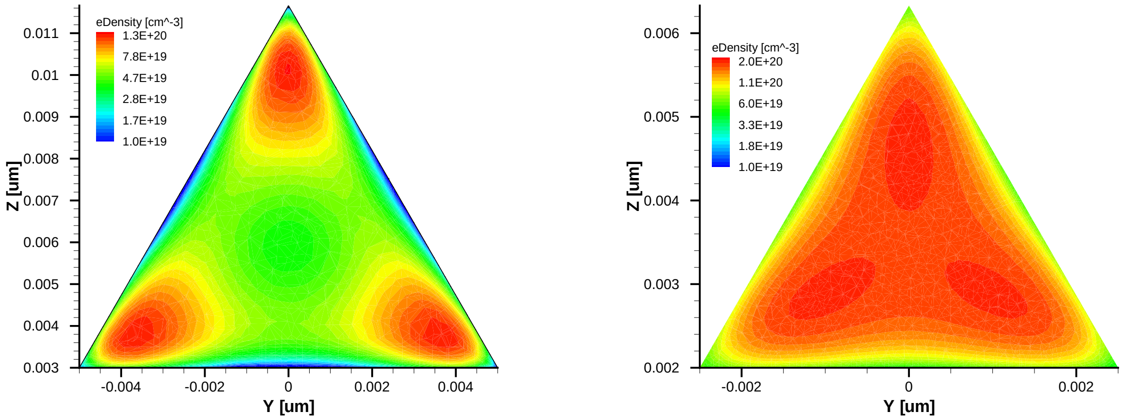

Figure 5.10: Cross-section quantum electron density at the middle of a GAA Si NW JL MOSFET in strong accumulation regime (V_{GS}=1.500 V) for 10 nm (top) and 5 nm (bottom) wide Si NW MOSFETs at N_d=1×10^{19} cm^{-3}.

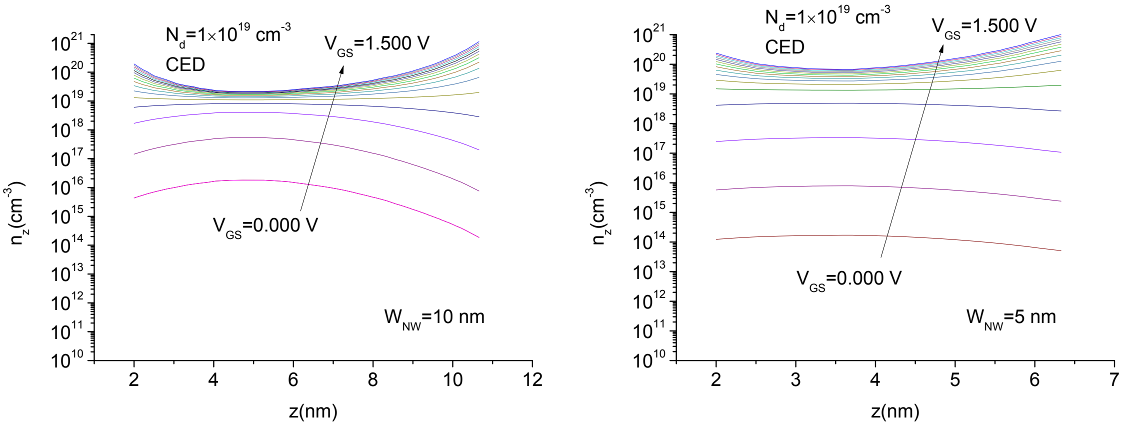

Figure 5.11: Local classical electron density profile across the Si nanowire channel volume at different gate voltages (from subthreshold to strong accumulation, step: 0.100 V) for 10 nm (top) 5 nm (bottom) wide Si nanowire MOSFETs at N_d=1×10^{19} cm^{-3}. Plots correspond to the cut at y=0.

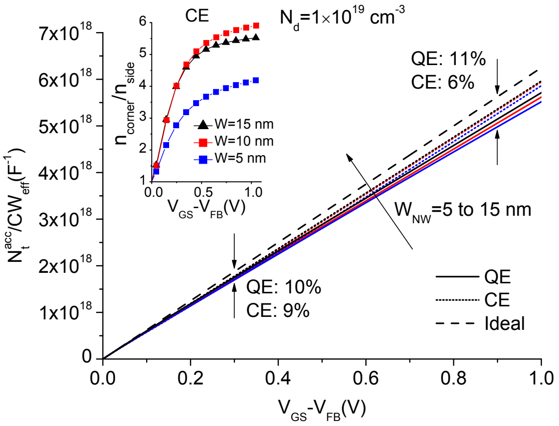

Figure 5.12: Normalized total accumulation electron density per unit length vs. V_{GS}-V_{FB} at various NW cross-section dimensions including both quantum and classical electrons. The normalization factor is $CW_{eff}(V_{GS})$. Inset shows local classical electron density corner to side ratios in accumulation regime.

5.5 Summary

In this chapter, we reported corner effect study in the single type doped (accumulation-mode and junctionless) GAA equilateral triangular Si nanowire nMOSFETs, using 15, 10 and 5 nm wide and 40 nm long Si NWs, 2 nm gate oxide thickness for the first time. The device simulations were done at V_{DS}=0 V, considering classical and quantized simulations and the key MOSFET parameters were defined and extracted using the total electron density per unit length (N_t) vs. V_{GS} and charge-voltage characteristics (Q_G-V_{GS}) as well. From the classical view, the corner regions deplete and accumulate more charges below and above flat-band in comparison to the sides. This is due to the fact that the corner regions have a higher surface to volume ratio in comparison to the side regions, leading to obtain a higher local charge in the corner regions in the case of a surface conduction mechanism (above flat-band, all operation regimes in the inversion-mode devices as well) and a lower local charge in the presence of a volume conduction mechanism (below flat-band). No secondary peak was observed below the main peak of d^2N_t/dV_{GS}^2, proving no subthreshold current path in the corner regions. Therefore, the typical well-known corner effect (local threshold voltage downshift in the corners and therefore, increased off current) is suppressed completely using accumulation-mode and junctionless architectures by having a unique threshold voltage in the system.

The effects of quantization are discussed in details, having a significant upshift in both the threshold and the flat-band voltages (e.g. 77 and 87 mV upshift, for the 5 nm wide NW at 1×10^{19} cm^{-3} channel doping, respectively) and strong charge redistribution in the channel cross-section. The product of the effective channel width and gate-channel capacitance, $CW_{eff}(V_{GS})$, a strong bias dependent parameter even in accumulation regime for the 3D architectures, was used to model better the quantized-effects on the device characteristics in comparison to the classical simulations. Note that both effective channel width and gate-channel capacitance parameters are bias-dependent while both shrink by quantization as well. This would be an efficient method to compare the device characteristics at different channel doping levels and cross-section dimensions. All the devices show a normalized total accumulation electron density per unit length (normalization factor: $CW_{eff}(V_{GS})$, $V_{GS}>V_{FB}$) slightly below the ideal MOSFET limit, even having a higher local accumulation in the corner regions in comparison to the side regions above the flat-band voltage. Therefore, the corners cannot be classified as CMOS boosters (e.g. stressors). The wider devices, at a constant channel doping of 1×10^{19} cm^{-3}, show a normalized total accumulation electron density per unit length characteristics closer to the ideal case, due to less contribution of the corner regions on the electrostatistics in the entire channel cross-section and less corner effects. On the other hand, the higher the channel doping level, the closer characteristics to the ideal case mainly due to increasing the electrostatic screening at a higher doping level in accumulation regime.

The original work carried out relative to this chapter includes:

- **3D device simulation of GAA Si NW JL MOSFETs**: In this chapter, I built a 3D TCAD device simulation platform in nanoscale (optimized meshing strategy in 3D, specified channel regions to get integral of various parameters e.g. charge, etc.) that we used for various publications in this direction [8], [29]- [30].
- **Reporting the new concept of *local volume depletion/accumulation***: The origin of local volume depletion/accumulation is described in details using TCAD device simulation results and based on volume vs. surface conduction below and above flat-band in multi-gate junctionless MOSFETs including corners. Note that local volume depletion below the threshold voltage prevents the issues corresponding subthreshold current path in the corners and therefore, such junctionless/accumulation-mode architectures will have a single threshold voltage in the system [8].
- **Reporting the new concept of *quantum flat-band voltage***: Since the flat-band condition cannot be satisfied for the quantum electrons in the channel cross-section especially including corners, the flat-band voltage is not a material-based parameter any more, depending on the channel geometry as well. In this chapter, we defined a methodology to extract the quantum flat-band voltage or the effective flat-band voltage as a key MOSFET parameter [8].
- **Corner effect study in JL/AM MOSFETs from subthreshold to strong accumulation**: The electron density profiles from corner to side and classical corner to side ratios were used to address the effect of corners on local electron densities at various bias voltages. To compare the characteristics of various devices, the $CW_{eff}(V_{GS})$ parameter was introduced, the product of effective channel width and gate-channel capacitance, that is a highly bias-dependent parameter. Even the charge accumulation occurs in

the corner regions above flat-band, we showed that the corners cannot be classified as CMOS boosters, comparing the normalized total accumulated electron densities per unit length. On the other hand, working in the JL and AM instead of IM helps to improve the device subthreshold behavior including corners (no OFF current degradation because of one threshold voltage in the system) [8].

5.6 Future works

- **Further study of corner effect for various architectures**: Compare the corner effect in accumulation-mode/junctionless with inversion-mode MOSFETs using a similar charge-based methodology. Investigate the effect of corner angle on charge accumulation and corner effect in AM/JL MOSFETs and finally, study the effect of rounding the corners on charge accumulation/depletion in AM/JL MOSFETs.
- **Corner effect to engineer key MOSFET parameters**: Since the corners deplete easier, they provide some rooms to fabricate heavily doped junctionless devices with bigger cross-sections with a similar leakage current. Therefore, as a possibility and in a new paper, one can investigate various cross-sections (including single-gate, planar double-gate, circular, rectangular, etc.) to provide a design guide to the maximum cross-section dimension to be able to turn off the heavily doped devices appropriately. Investigating the V_{FB}-V_{TH} engineering by the corner effect for various cross-sections in a GAA architecture (e.g. circular vs. rectangular, triangular, etc.) is another possibility. This can be used to widen the bulk conduction region in the AM/JL devices, since one of the main targets of these devices is working between the threshold and the flat-band voltage e.g. for ultra-low power and low voltage device and circuit applications.

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6 Transport analysis in triangular GAA Si nanowire junctionless nMOSFETs

Gate-all-around (GAA) Si nanowire MOSFETs including a circular cross-section can be achievable using hydrogen annealing [1] or stress-limited oxidation [2]. In other cases, such multi-gate architectures, including FinFETs as well, have corners (e.g. [3]-[8]). Transport analysis in such multi-gate devices especially with a deeply scaled cross-section is not simple due to non-uniform electron density [9] and normal electric field variation in the channel mainly due to the corners (see e.g. [10]-[14]). Two major mobility extraction methods were reported previously: Y-function ($I_D/g_m^{0.5}$) [15] and split CV [16]. Split CV is the most available accurate method for mobility and transport analysis, needing both C-V and I_D-V_G measurements but the CV measurements require a pretty large device (e.g. a large array of devices operating in parallel, see [17]), hardly feasible with a single nanoscaled device. On the other hand, applying the Y-function on a single scaled device is pretty straightforward, but requires an accurate estimation of the key device parameters such as the gate-oxide capacitance (C_{ox}) and the effective channel width (W_{eff}).

In this chapter, we report transport analysis in equilateral triangular GAA Si nanowire junctionless nMOSFETs. We intentionally mainly focus on strong accumulation regime, having a channel doping level of 1×10^{19} cm^{-3} and different channel cross-section dimensions (5 to 20 nm NW width) at V_{DS}=100 mV (channel length=100 nm, T=300 K), including the impact of corners. Two S/D doping levels will be considered: 1×10^{20} cm^{-3} (*contact engineered*) and 1×10^{19} cm^{-3} (the same doping as channel). No contact engineering causes a strong bias-dependent series resistance in strong accumulation (diffusion of electrons from the channel ends to the S/D extensions) and accounting for such series resistances in the I-V characteristics is not straight forward. Therefore and as a first step, transport analysis is done on the *contact engineered* MOSFETs, assuming a constant carrier mobility. Therefore, the effective series resistance in strong accumulation can be assumed constant, somehow similar to the typical inversion-mode (IM) devices. This is mainly to investigate the accuracy of the low-field mobility extraction procedures, using both split CV and Y-function methods in case of a highly non-uniform electron density in the channel cross-section due to the corner effects. In a second step, a more realistic transport analysis will be performed assuming an electric field

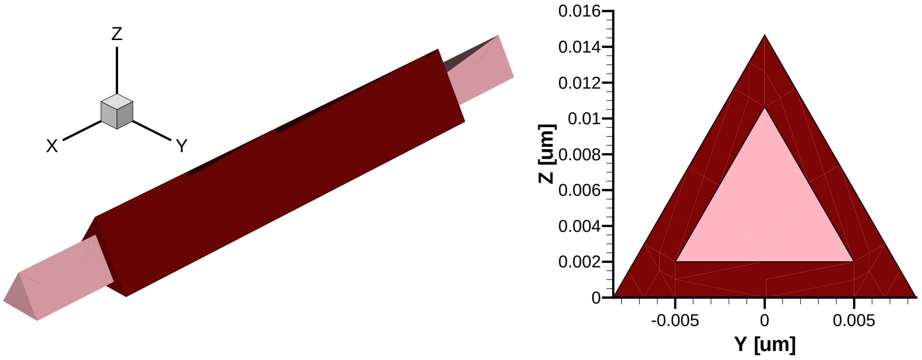

Figure 6.1: Equilateral triangular GAA 10 nm wide Si nanowire nMOSFET and its cross-section. The channel length is 100 nm.

dependent carrier mobility which will be impacted by the effect of non-uniform electric field in the channel cross-section, in strong accumulation regime. Lastly, transport analysis will be done on a JL MOSFET without *contact engineering*, performing a bias-dependent series resistance correction in strong accumulation using quasi-Fermi potentials over the channel.

6.1 Numerical simulation

TCAD Sentaurus Device (G.2012-06) was used for quasistationary numerical simulation of GAA NW MOSFETs. Using electrostatic and quasi-Fermi potential equations, the local carrier current and carrier density in a 3D architecture MOSFET can be extracted at each bias voltage. The density gradient quantization model is coupled to the Poisson equation [18]-[19] to include the 3D quantization effects. A Fermi-Dirac statistics was used as well, considering both degenerate and non-degenerate regimes [19].

Fig. 6.1 shows the equilateral triangular GAA NW MOSFET used in the device simulations (10 nm NW width). For all the NW widths (5, 10 and 20 nm), the gate length and SiO_2 gate oxide thickness are 100 and 2 nm, respectively. The channel doping is 1×10^{19} cm^{-3}. The source/drain extensions are 20 nm long and the doping levels are whether 1×10^{20} cm^{-3} (*contact engineered*) or 1×10^{19} cm^{-3} (similar to the channel). A fixed mid-gap gate workfunction of 4.5 eV was used as well.

6.2 Subthreshold to strong accumulation transport with a constant mobility model

In this section, quasistationary TCAD Device simulations were done on 5-20 nm wide Si nanowires including a constant carrier mobility of 100 cm^2/V·s in the entire channel cross-section, thus neglecting the mobility-electric field dependency, considering both classical (CE) and quantum (QE) electrons. The doping level of S/D extensions is 1×10^{20} cm^{-3} to minimize

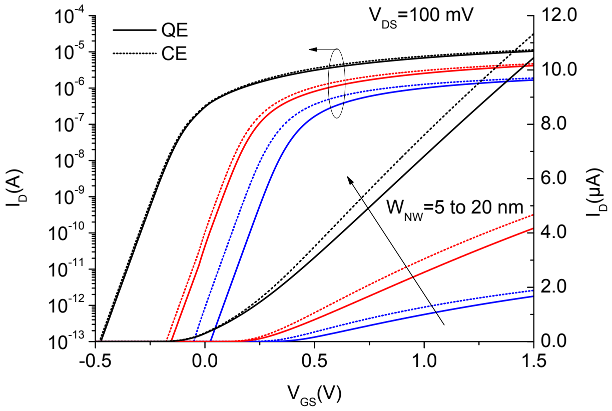

Figure 6.2: Transfer characteristics of GAA 5-20 nm wide NW JL nMOSFETs with *engineered contacts* at V_{DS}=100 mV and constant mobility (CE: classical, QE: quantum electrons).

the series resistances in strong accumulation. The transfer characteristics are plotted in Fig. 6.2 without any specific normalization in order to highlight the different effects that come into play, e.g. quantum confinement, gate-channel capacitance variation by V_{GS}, effective channel width variation due to quantization and finally, series resistance. Note that in this case, series resistance is the only effective channel mobility attenuation or transconductance degradation mechanism in strong accumulation regime.

6.2.1 Operation of GAA Si nanowire junctionless nMOSFETs

The flat-band voltage is the voltage where the conduction mechanism changes from depletion (below flat-band) to accumulation (above flat-band). In addition, below flat-band, most of the carriers flow inside the channel, while above flat-band, in addition to the bulk current, a surface conduction occurs. Therefore, the current in the accumulation regime is the sum of bulk and accumulation currents.

6.2.2 Threshold voltage extraction method

According to the transconductance change method [20], the threshold voltage of a MOSFET can be extracted from the peak of the second derivative of drain current, quasi-independent of the series resistance and transport mechanism. Fig. 6.3 shows the drain current and its first and second order derivatives at V_{DS}=100 mV (normalized to the maximum values) for a 20 nm wide NW MOSFET including quantization.

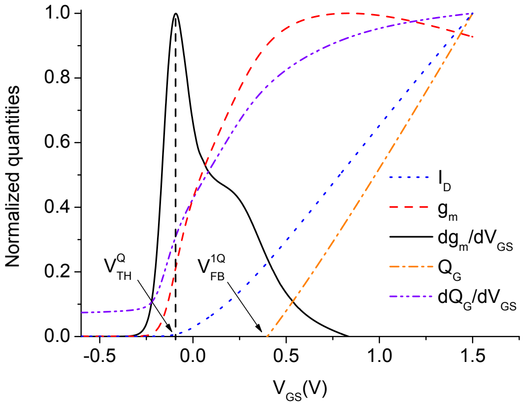

Figure 6.3: Normalized quantities of I_D, g_m, dg_m/dV_{GS} at V_{DS}=100 mV and Q_G and dQ_G/dV_{GS} at V_{DS}=0 V to the maximum values vs. V_{GS} for the GAA 20 nm wide Si nanowire MOSFET including quantum confinement. The maximum values for each parameter are 1.04×10^{-5} A, 7.52×10^{-6} A/V, 2.04×10^{-5} A/V^2, 1.00×10^{-16} C and 9.84×10^{-17} F, respectively. A constant mobility of 100 cm^2/V·s was used in the simulations.

6.2.3 Flat-band voltage extraction method

According to the typical flat-band voltage definition in a standard planar MOSFET, the flat-band condition is the gate voltage with no electric field (or constant electrostatic potential) in the entire channel cross-section. However, note that the actual flat-band condition cannot be satisfied in the entire channel cross-section when including quantum confinement, especially in a device having corners. Therefore, similar to [9], we can try to extract an effective flat-band voltage for the entire device from Q_G-V_{GS} simulations at V_{DS}=0 V (x-intercept, no fitting or extrapolation), called V^{1Q}_{FB} and V^{1C}_{FB} for both quantum and classical cases (see Fig. 6.3).

Obviously, the flat-band condition can be reached for the classical case in all the Si nanowires with various widths and at V_{GS}=0.360 V (uninform electrostatic potential in the entire channel cross-section, even in the corners), that is called V^{C}_{FB}. The slight difference between V^{1C}_{FB} and V^{C}_{FB} in a sub-1 mV range, due to the extraction methodology, can be used to report a more accurate effective flat-band voltage for the quantum electrons, called V^{Q}_{FB}.

6.2.4 Gate-channel capacitance and effective channel width

The total gate-channel capacitance (C_G) as a function of V_{GS} can be extracted directly from the Q_G-V_{GS} simulations at V_{DS}=0 V by:

$$C_G(V_{GS}) = dQ_G(V_{GS})/dV_{GS} \tag{6.1}$$

According to Fig. 6.3, this capacitance is varying by gate voltage, even in strong accumulation, while its bias dependency becomes more significant in the presence of quantization as well

W_{NW} (nm)	V_{TH}^{C} (V)	V_{TH}^{Q} (V)	V_{FB}^{1C} (V)	V_{FB}^{1Q} (V)	V_{FB}^{C} (V)	V_{FB}^{Q} (V)	$CW_{eff}^{0.5C}$ (F/cm)	$CW_{eff}^{1.0C}$ (F/cm)	$CW_{eff}^{0.5Q}$ (F/cm)	$CW_{eff}^{1.0Q}$ (F/cm)
5	0.320	0.397	0.361	0.454	0.360	0.453	2.94×10^{-12}	3.05×10^{-12}	2.61×10^{-12}	2.97×10^{-12}
10	0.202	0.219	0.361	0.413	0.360	0.412	5.32×10^{-12}	5.48×10^{-12}	4.72×10^{-12}	5.20×10^{-12}
20	-0.096	-0.092	0.361	0.399	0.360	0.398	9.99×10^{-12}	1.02×10^{-11}	9.22×10^{-12}	9.77×10^{-12}

Table 6.1: Key MOSFET parameters (1st table) extracted from device simulations of GAA NW JL MOSFETs with *engineered contact* and a constant mobility of 100 cm^2/V·s.

W_{NW} (nm)	μ_0^{C} (cm^2/V·s)	θ^{C} (1/V)	μ_0^{Q} (cm^2/V·s)	θ^{Q} (1/V)	R_{SD}^{C} (kΩ)	R_{SD}^{Q} (kΩ)	$R_{SD}^{0.5C}$ (kΩ)	$R_{SD}^{1.0C}$ (kΩ)	μ_0^{YC} (cm^2/V·s)	μ_0^{YQ} (cm^2/V·s)
5	92.0	0.593	92.4	0.547	21.56	21.23	21.71	21.65	89.1	76.4
10	91.6	0.275	90.6	0.239	5.55	5.31	5.29	5.26	89.0	80.0
20	92.5	0.143	91.2	0.122	1.53	1.41	1.35	1.35	89.9	84.7

Table 6.2: Key MOSFET parameters (2nd table) extracted from device simulations of GAA NW JL MOSFETs with *engineered contact* and a constant mobility of 100 cm^2/V·s.

(up to 13% variation from V_{GS}=1.0 to 1.5 V).

The gate-oxide capacitance is typically a geometrical parameter (depending on the gate-oxide thickness and geometry). Quantum confinement [21], Debye broadening effect [22] and the depletion layer below the flat-band voltage are the effects that modify the total gate-channel capacitance from subthreshold to strong accumulation. On the other hand, the effective channel width for both classic and quantum cases are not the same due to the modifications in the electron density pattern in the channel cross-section by quantum confinement. The effective channel width, even for the classical case, can vary with the gate voltage due to the corner effect (non-uniform local accumulation of electrons in the channel cross-section). Therefore, to simplify the transport analysis and the parameter extraction method, we consider an effective product of the channel-gate capacitance with the channel width, called CW_{eff}. This product will be a function of gate voltage and can be extracted directly from the total gate-channel capacitance (L: channel length):

$$CW_{eff}(V_{GS}) = C_G(V_{GS})/L \tag{6.2}$$

6.2.5 Key MOSFET parameters for different cross-sections

Table 6.1 reports all the key MOSFET parameters obtained from the mentioned extraction methods, for different channel cross-sections, considering both classical and quantum cases. The threshold and the flat-band voltage upshifts by the quantum confinement are due to the higher quantized subband energies [6], [23]-[24].

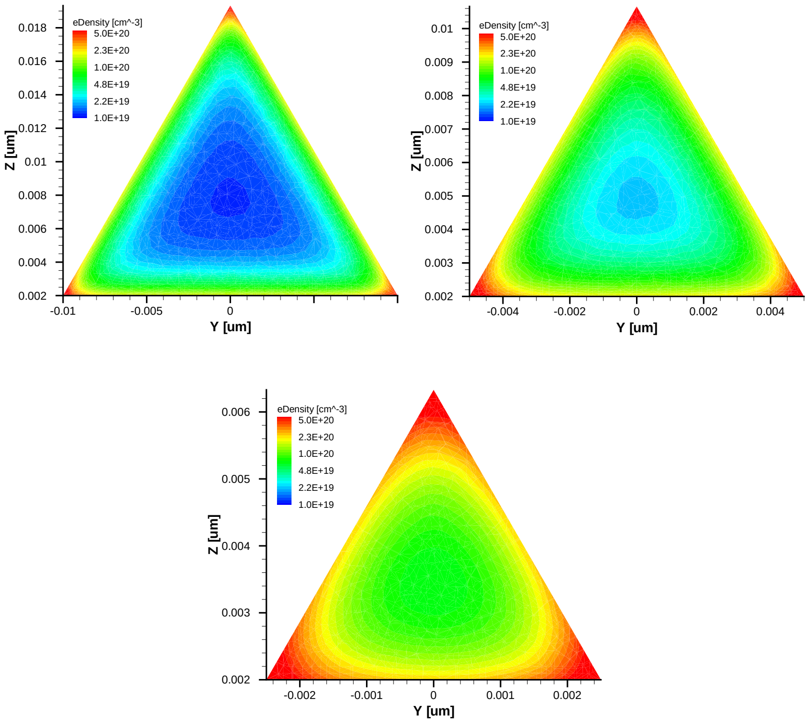

Figure 6.4: Cross-section local classical electron mobility pattern at the middle of the GAA Si nanowire JL MOSFETs with with *engineered contact* and different NW widths (left: 20 nm, center: 10 nm, right: 5 nm) in strong accumulation at V_{DS}=100 mV (oxide is not shown, V_{GS}=1.500 V).

6.3 Transport analysis in GAA Si nanowire MOSFETs with a constant mobility model

Figs. 6.4 and 6.5 show the local classical and quantum electron densities in the channel cross-sections and at the middle of the gate (x=L_G/2) in strong accumulation (V_{GS}=1.5 V). Quantization induces a higher accumulation of electrons in the corner regions together with a strong electron pattern redistribution in the 5 nm wide NW in comparison to the wider structures. To investigate the effect of non-uniform electron density distribution on transport, we assumed a constant mobility (in the whole channel) and extract the key MOSFET transport parameters such as low-field mobility as a first step. This will be used to assess the mobility extraction methodologies, aimed to investigate in such devices as well.

6.3.1 Transport analysis by split CV method

Similar to the split CV method in IM MOSFETs operating in linear regime [16], it is possible to show that using the initial derived I_D-V_{GS} analytical formula in [25], the effective carrier mobility in linear accumulation regime (V_{GS}-V_{FB}>V_{DS}, V_{GS}>V_{FB}) for an AM/JL MOSFET can be calculated using both transfer and charge-voltage characteristics by:

$$\mu_{eff}(V_{GS}) = \frac{I_D^{acc}(V_{GS})}{Q_G^{acc}(V_{GS})} \cdot \frac{L^2}{V_{DS}} \tag{6.3}$$

The contribution arising from the accumulation current above flat-band can be obtained by subtracting the drain current at flat-band (V_{FB}^{C} or V_{FB}^{Q} in table 6.1) from the total drain current.

Fig. 6.6 shows the bias dependency of the effective carrier mobility above flat-band. Since series resistance is the only transconductance or effective mobility drop mechanism in this section, a simple series resistance correction (see e.g. [26]) can be performed to estimate the low-field carrier mobility (μ_0). By neglecting slight MOSFET parameters bias-dependencies over strong accumulation regime, assuming a linear charge accumulation and almost symmetric source and drain series resistance on both channel sides and finally, the accumulation current as the dominant current component in strong accumulation regime, the bias dependency of the effective carrier mobility can be assumed as:

$$\mu_{eff}(V_{GS}) \approx \mu_0 / [1 + \theta \cdot (V_{GS} - V_{FB})] \tag{6.4}$$

The θ parameter, effective mobility attenuation factor, can be estimated by:

$$\theta \approx R_{SD} \cdot \mu_0 \cdot C W_{eff} / L \tag{6.5}$$

Both numeric values of μ_0 and θ parameters are extracted using least-square approximation fitting of the $1/\mu_{eff}$(V_{GS}) plot (Fig. 6.6) over 0.5 to 1.0 V of V_{GS}-V_{FB} range and reported in table 6.2. As observed, this method is providing almost a precise estimation of low-field mobility (sub-10% inaccuracy) for the three architectures when assuming a constant carrier mobility of 100 $cm^2/V{\cdot}s$. Note that such a slight inaccuracy is due to neglecting all key MOSFET parameters bias-dependencies over strong accumulation regime, slight actual V_{GS} variation by series resistance at a low V_{DS} (100 mV) while using both I_D-V_{GS} and Q_G-V_{GS} characteristics and extraction methodologies.

6.3.2 Series resistance and effective mobility attenuation

The approximate effective series resistance values for each architecture are calculated using eq. 6.5 and the extracted θ values in section 6.3.1 and finally, reported in table 6.2. According to these data, the effective series resistance is increasing by cross-section shrinkage. Note that the reported effective series resistances do not vary exactly by the cross-section scaling factor mainly due to the slight bias-dependency of MOSFET parameters e.g. slight actual gate length variation vs. gate bias voltage due to fringing electric fields at the gate ends.

As a comparison, the total resistance of S/D extensions using classical quasi-Fermi potentials at the gate ends at both 0.5 and 1.0 V of V_{GS}-V_{FB}, called $R_{SD}^{0.5C}$ and $R_{SD}^{1.0C}$, respectively, are

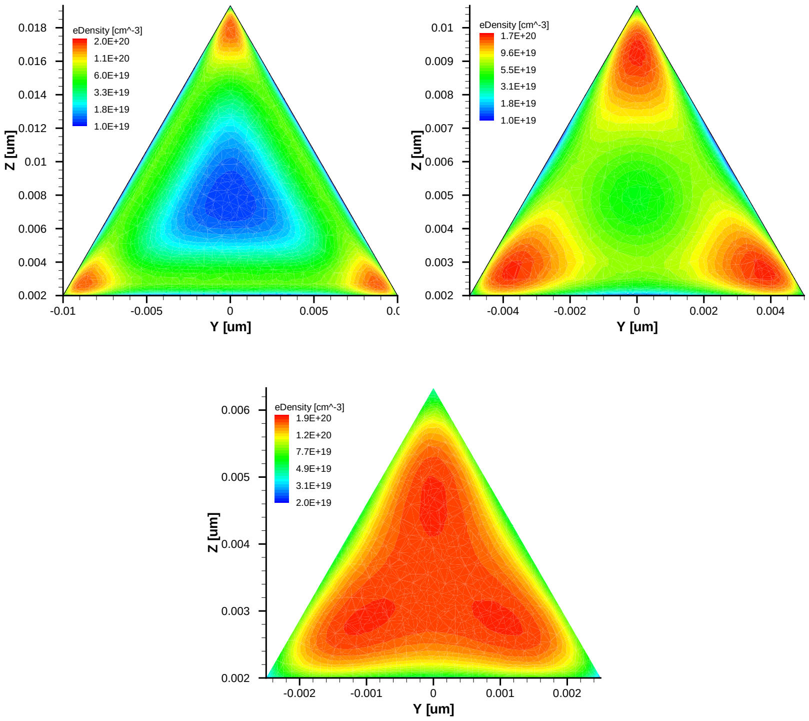

Figure 6.5: Cross-section local quantum electron mobility pattern at the middle of the GAA Si nanowire JL MOSFETs with *engineered contact* and different NW widths (left: 20 nm, center: 10 nm, right: 5 nm) in strong accumulation at V$_{DS}$=100 mV (oxide is not shown, V$_{GS}$=1.500 V).

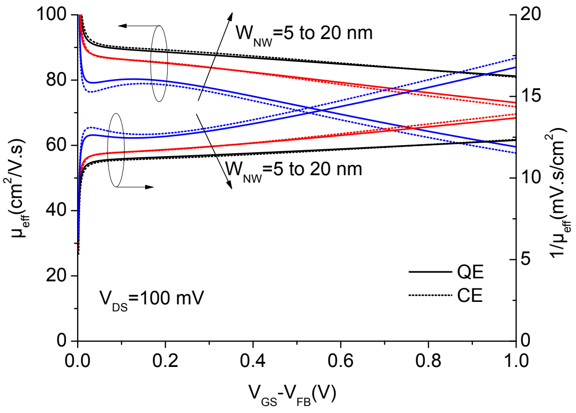

Figure 6.6: Effective electron mobility and its reverse vs. V$_{GS}$-V$_{FB}$ for GAA Si nanowire junctionless nMOSFETs with *engineered contact* (5, 10, 20 nm Si nanowire width).

calculated and reported in table 6.2. Note that the total resistance of S/D extensions is slightly bias-dependent, a sub-0.7% change for all the architectures.

6.3.3 Transport analysis using Y-function

Using the asymptotic form of the current in linear accumulation for the JL MOSFET [25], the strong similarity with inversion-mode MOSFETs supports that the Y-function at each bias voltage can be calculated by:

$$Y(V_{GS}) = \frac{I_D^{acc}(V_{GS})}{\sqrt{g_m(V_{GS})}} \approx \sqrt{\mu_0 \cdot C_{gc} \cdot V_{DS} \cdot \frac{W}{L}} \cdot (V_{GS} - V_{FB}) \tag{6.6}$$

where W is the channel width. Note that despite the split CV method (which uses the actual accumulated charges to estimate the effective mobility), a linear charge accumulation in the channel over strong accumulation regime is considered, neglecting the slight bias-dependency of effective channel width and gate-channel capacitance in this regime.

The Y-function is calculated for all the Si NW MOSFETs and plotted vs. V_{GS}-V_{FB} in Fig. 6.7-left Y axis. Obviously, an accurate low-field electron mobility extraction by this method needs a precise estimation of both W and C_{gc}. Due to the strong link between the actual channel width and gate-channel capacitance, instead of using an approximate analytical formula to extract both separately (see e.g. [27]), the average value of CW_{eff} over 0.5 to 1.0 V of V_{GS}-V_{FB} bias range from the Q_G-V_{GS} simulations (see eq. 6.2) can be used in eq. 6.6 to extract the low-field mobility values (called $CW_{eff}^{0.5}$ and $CW_{eff}^{1.0}$ in table 6.1). According to table 6.2, the extracted classical low-field mobility values (μ_0^{YC}) are almost close to the actual constant carrier mobility value (up to 11% under-estimation) and a sub-3% difference from the μ_0^C values extracted by the split CV method, for the three architectures. On the other hand, due to the strong quantization effect in the 3D structures with sharp corners and therefore, the higher bias dependency of CW_{eff}, specially for the 5 nm wide NW, the Y-function shows a higher deviation from the actual constant carrier mobility value (up to 24%).

6.4 Transport analysis in GAA NW MOSFETs with an electric field dependent mobility model

In this section, TCAD Sentaurus device simulation was done on the devices with *engineered contacts* (low source/drain access resistance) assuming an electric field dependent channel mobility. Fig. 6.8 shows the local electron mobility pattern in the channel cross-sections in strong accumulation regime (V_{GS}=1.5 V) when quantum effects are included. According to Figs. 6.4 and 6.5, corner regions accumulate more electrons in the channel cross-section in strong accumulation regime but they also suffer from a lower local mobility due to the higher normal electric field in strong accumulation (see Fig. 6.9). Note that the key MOSFET

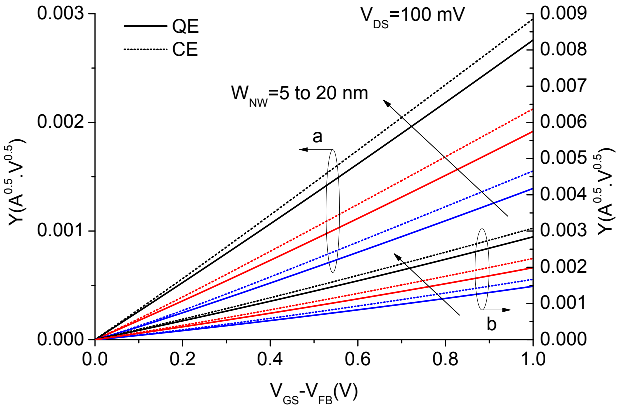

Figure 6.7: Y-function vs. V_{GS}-V_{FB} for GAA Si nanowire junctionless nMOSFETs with *engineered contact* (5, 10, 20 nm Si nanowire width). "a" and "b" correspond to the JL MOSFETs with a field free (section 6.3.3) and field dependent carrier mobility (section 6.4.3) model, respectively.

W_{NW} (nm)	μ_0^C (cm^2/V·s)	θ^C (1/V)	μ_0^Q (cm^2/V·s)	θ^Q (1/V)	θ_0^C (1/V)	θ_0^Q (1/V)	μ_0^{YC} (cm^2/V·s)	μ_0^{YQ} (cm^2/V·s)
5	105.4	1.520	107.4	1.478	0.531	0.566	110.5	91.6
10	100.0	0.794	97.2	0.697	0.336	0.300	105.5	90.6
20	98.4	0.510	94.9	0.412	0.271	0.209	103.0	94.8

Table 6.3: Extraction of carrier mobility parameters for GAA Si nanowire junctionless MOSETs with engineered contact using a field dependent carrier mobility.

parameters e.g. the threshold and flat-band voltages, reported in table 6.1, are assumed to be unchanged by including the field dependent mobility model, neglecting the possible slight error due to the extraction methodology.

6.4.1 Transport analysis using split CV method

The effective electron mobility values of the GAA Si nanowire MOSFETs vs. V_{GS}-V_{FB} are calculated using the split CV method (eq. 6.3) and plotted in Fig. 6.10. The extracted low-field mobility and mobility attenuation factors are also reported in table 6.3.

6.4.2 Normal electric field on mobility degradation

Considering eq. 6.5 as a first step, similar to the typical long single-gate MOSFETs [15], the contribution of normal electric field on effective mobility attenuation can be assumed as:

$$\theta \approx \theta_0 + R_{SD} \cdot \mu_0 \cdot CW_{eff}/L \tag{6.7}$$

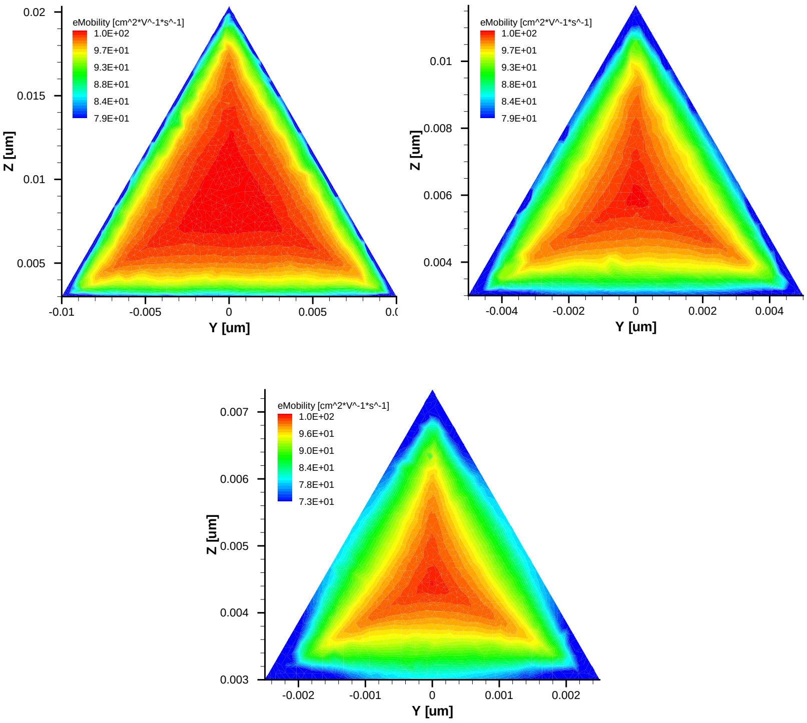

Figure 6.8: Cross-section local electron mobility pattern at the middle of the GAA Si nanowire JL MOSFETs with with *engineered contact* and different NW widths (left: 20 nm, center: 10 nm, right: 5 nm) in strong accumulation at V_{DS}=100 mV (oxide is not shown, V_{GS}=1.500 V, classical simulations).

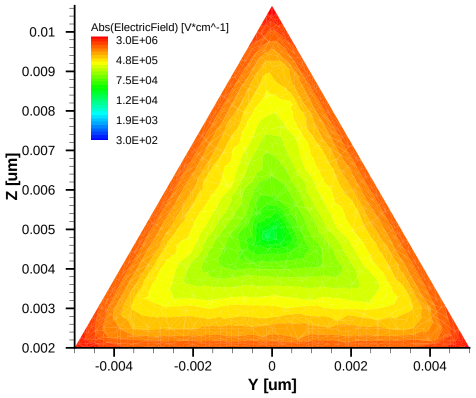

Figure 6.9: Cross-section absolute electric field pattern at the middle of a GAA 10 nm wide Si NW JL MOSFET with *engineered contact* in strong accumulation at V_{DS}=100 mV (oxide is not shown, V_{GS}=1.500 V, classical simulation).

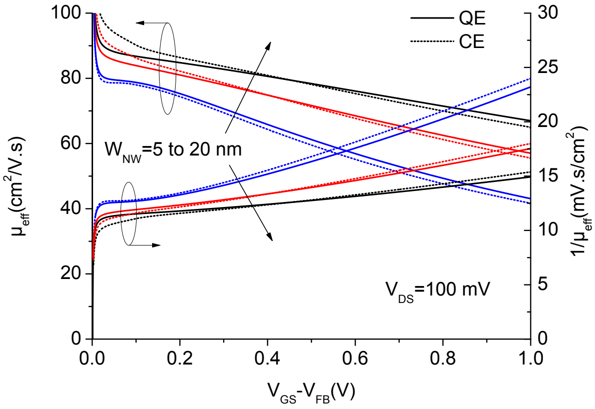

Figure 6.10: Effective electron mobility and its inverse vs. V_{GS}-V_{FB} for GAA Si NW JL nMOSFETs with *engineered contact* (5, 10, 20 nm Si NW width).

where, θ and θ_0 can be called mobility and intrinsic mobility attenuation factors, respectively. Using the extracted series resistance values from eq. 6.5 obtained while a constant mobility (table 6.2), the intrinsic mobility attenuation factors are extracted and reported in table 6.3. According to these data, θ_0 is increasing with channel cross-section shrinkage due to increasing the contribution of corners in transport (higher normal electric field in the corners). The observed general quantization-based decrease in θ_0 is due to the redistribution of the charges, placing the electron density peak inside volume but not in the sharp corner regions with higher normal electric field. Anyway, there is no significant difference between the estimated θ_0 values of classical and quantum electrons for the narrowest nanowire, possibly due to the stronger bias dependency of the key MOSFET parameters e.g. CW_{eff} and extraction methodology.

6.4.3 Transport analysis using Y-function

Using the method described in 6.3.3, the low-field mobility values can be calculated from the slope of Y-function vs. V_{GS}-V_{FB}, using the extracted CW_{eff} values from the Q_G-V_{GS} simulations in strong accumulation (see table 6.1 and Fig. 6.7-right Y axis). The corresponding values are reported in table 6.3. The classical values are pretty close to the low-field mobility values extracted from the split CV method (below 6% inaccuracy) for the three architectures. Similar to 6.3.3, the Y-function shows a larger deviation to estimate the the low-filed mobility values while including quantization (up to 15% in comparison to the split-CV method), mainly due to the higher bias-dependency of the key MOSFET parameters in the presence of quantization in the architectures with sharp corners.

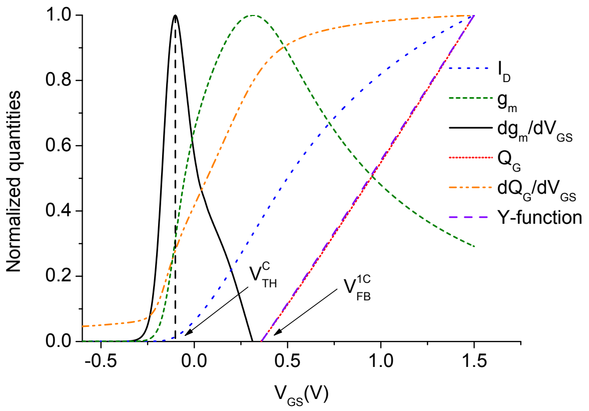

Figure 6.11: Normalized quantities of I_D, g_m, dg_m/dV_{GS}, Y-function at V_{DS}=100 mV and Q_G and dQ_G/dV_{GS} at V_{DS}=0 V to the maximum values vs. V_{GS} for the GAA 20 nm wide Si nanowire MOSFET without contact engineering. The maximum values for each parameter are 4.80×10^{-6} A, 4.63×10^{-6} A/V, 1.88×10^{-5} A/V^2, 2.59×10^{-3} A$^{0.5}$·V$^{0.5}$, 1.13×10^{-16} C and 1.03×10^{-16} F, respectively. A constant mobility of 100 cm^2/V·s was used in the simulations (V^C_{TH}=-0.102 V, V^C_{FB}=0.360 V).

6.5 Transport analysis in a JL MOSFET without engineered contact

Fig. 6.11 shows the classical I_D-V_{GS} and Q_G-V_{GS} characteristics together with the corresponding derivatives for a GAA 20 nm wide NW JL MOSFET without contact engineering (1×10^{19} cm^{-3} doping from source to drain) and a constant mobility of 100 cm^2/V.s. Direct split CV method was applied to the electrical characteristics and the effective carrier mobility values are plotted in Fig. 6.12. Unexpectedly, there is a significant effective mobility drop in comparison to Fig. 6.6 over strong accumulation regime. The extracted low-field mobility value from eq. 6.4 is also 56 cm^2/V.s, 44% below the actual constant mobility value. The Y-function method (see Fig. 6.11) also represents a low-field mobility value of 48 cm^2/V.s, 52% inaccuracy from the constant mobility value.

The correction of bias-dependent series resistance is not simple. It can be done using the actual source and drain quasi-Fermi potentials (V_D^* and V_S^* in Fig. 6.12-inset) at each bias voltage. Afterward, the effective mobility value at each bias voltage is calculated from eq. 6.3 considering the actual bias voltages over the transistor element and plotted in Fig. 6.12. Due to cancelling the series resistance effect, the effective mobility values are now pretty close to the constant mobility value, a sub-5% inaccuracy over 0.5 to 1.0 V of V_{GS}-V_{FB} range for the 20 nm wide Si NW MOSFET, mainly due to the inherent parameter extraction methodology. Note that the total S/D extension resistance changes from 13.2 to 13.4 kΩ, over the mentioned bias range, ~30 times higher than the the observed similar variation in the case of contact engineering (sub-7 Ω, see table 6.2).

The same doping level along source-channel-drain leads to diffusion of electrons from the

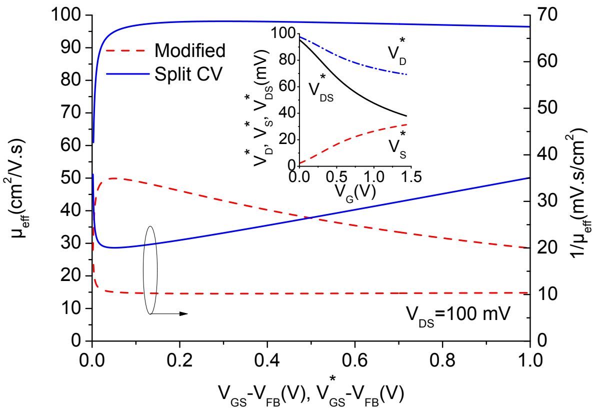

Figure 6.12: Effective electron mobility vs. V_{GS}-V_{FB}, direct split CV, or V^*_{GS}-V_{FB}, modified split CV using S/D quasi-Fermi potentials (shown in inset), for the GAA 20 nm wide NW JL MOSFET without contact engineering.

channel to the source/drain extensions in strong accumulation and therefore, having a highly bias-dependent series resistance. Note that such gate voltage-based resistance modulation of the S/D extensions in strong accumulation can be considered as channel length modulation as well, assuming a device with a longer actual channel length than the physical channel length. Since both the split-CV and the Y-function methods to extract the low-field mobility values are based on a constant series resistance, can be translated to a constant gate length as well, further transport analysis would be non-straight forward using both methods. Contact engineering, increasing the S/D doping level, may help to solve this issue, but needs an additional implantation step in the process flow.

6.6 Summary

In this chapter, we reported transport analysis in the equilateral triangular GAA Si nanowire junctionless nMOSFETs in strong accumulation regime for the first time. 20 to 5 nm wide Si nanowires with 100 nm gate length, 1×10^{19} cm^{-3} channel doping and 2 nm thick gate oxide thickness were used for quasistatic device simulations. The transport analysis was done as a first step using *contact engineering*, S/D doping level of 1×10^{20} cm^{-3}, to minimize the bias dependency of series resistance. The split-CV method shows sub-10% inaccuracy to report the low-field carrier mobility values, at a constant carrier mobility, for both classical and quantized simulations. The Y-function shows sub-11% inaccuracy to report the classical low-field mobility values, at a constant carrier mobility, as well (sub-3% difference from the values extracted by the split-CV method). Due to the higher bias dependency of the gate-channel capacitance and the effective channel width product (CW$_{eff}$) while including quantization (up to 14% variation over 0.5 to 1.0 V of V_{GS}-V_{FB} range while being sub-4% for the classical cases), the Y-function shows a larger deviation of 16-24% to report the quantum low-field mobility values at a constant carrier mobility, in comparison to the classical cases.

Regarding the simulations with a field-dependent mobility model, the Y-function shows sub-6% and 15% inaccuracies to estimate the classical and quantum low-field mobility values, respectively, in comparison to the split-CV method. Reducing the quantization-based bias dependency of the key MOSFET parameters e.g. CW_{eff} in the 3D channels with sharp corners, using possibly rounded corners, might improve further the accuracy of the Y-function to estimate the low-field mobility values in the presence of quantization. Note that applying the Y-function method to a device in nanoscale is simple, needing only I_D-V_{GS} characteristics, while the estimation on the channel width and gate-channel capacitance can be performed by device simulation based on the actual channel cross-section.

Finally, transport analysis was done on a 20 nm wide Si nanowire junctionless MOSFET without engineered contact, a uniform doping level of 1×10^{19} cm^{-3} along source-channel-drain, using classical device simulations and a constant carrier mobility. The split-CV and the Y-function methods show 44% and 52% inaccuracies, respectively, to estimate the low-field mobility values mainly due to the diffusion of carriers to the S/D extensions in strong accumulation regime, leading to a high bias dependency of the series resistance in strong accumulation regime.

The original work carried out relative to this chapter includes:

- **Device simulation of GAA Si NW JL MOSFETs**: Quasistationary device simulation was done using equilateral triangular GAA Si nanowire junctionless nMOSFETs from sub-threshold to strong accumulation. Extraction of the key MOSFET parameters was done precisely for various cross-section dimensions, based on the Q_G-V_{GS} and the I_D-V_{GS} simulations at V_{DS} of 0 and 100 mV, respectively. [28].

- **Transport analysis using a constant mobility model**: Investigate the accuracy of the split-CV and the Y-function methods in strong accumulation to extract the carrier mobility in GAA Si nanowire MOSFETs with 20-5 nm channel cross-sections, using a constant mobility model. Both classical and quantum simulations were considered.

- **Transport analysis using a field-dependent mobility model**: Compare the estimated low-field mobility values by the Y-function and the split-CV methods using a field-dependent mobility model.

- **Transport analysis in JL MOSFETs without contact engineering**: Examine the accuracy of both the Y-function and the split-CV methods to estimate the low-field carrier mobility in a JL MOSFET without contact engineering. Due to the significant bias-dependent series resistance in strong accumulation regime, reported for the first time, both the split-CV and the Y-function methods show a large deviation, up to 52%, from the used constant carrier mobility in the simulations. Such bias-dependencies can be minimized by increasing the S/D doping level, adding a few process steps, but strongly needed to perform precise transport analysis on such devices in strong accumulation regime.

6.7 Future works

- **Modeling of the bias-dependency of series-resistance in GAA JLMOSFETs:** Note that due to the bias-dependency of series resistance (smaller resistance at higher gate voltages), the drain current is increasing further, having a positive impact on the device performance but this issue prevents to extract the key device parameters e.g. low-field mobility in strong accumulation.
- **Transport analysis in GAA JLMOSFETs in bulk regime:** Due to volume instead of surface conduction between threshold and flat-band, the channel width and gate-channel capacitance are significantly bias-dependent in bulk regime. Transport analysis for such architectures with various cross-sections, e.g. circular, rectangular and triangular, are pretty interesting and can be the next step.
- **Transport analysis in GAA JL MOSFETs in subthreshold regime:** Since the corners deplete faster, such transport analysis below the threshold voltage is possibly more straight forward than the bulk regime (possible minimized contribution of corners in electron density modification in the channel cross-section, since the majority of carriers flow at the middle of the channel but not in the corner regions). One application of GAA Si nanowire MOSFETs (AM/JL) can be ultra-low power/low voltage device and circuit implementation in subthreshold regime and such studies can be supported by extensive experiments (simple fabrication) later on.
- **The effect of rounding corners on the accuracy of Y-function:** Due to the high bias-dependency of the CW_{eff} parameter while including quantization in accumulation regime, the Y-function shows a larger deviation from the constant mobility value in comparion to the classical simulations. Rounding the corners, while not changing the rest of the device configuration e.g. EOT, can possibly diminish slightly such bias dependent quantization effects and therefore, possibly improve the accuraty of the Y-function in the quantum simulations as well. Note that, experimentally, partial rounding of the cross-sections can be performed using a short thermal dry oxidation step or hydrogen annealing.

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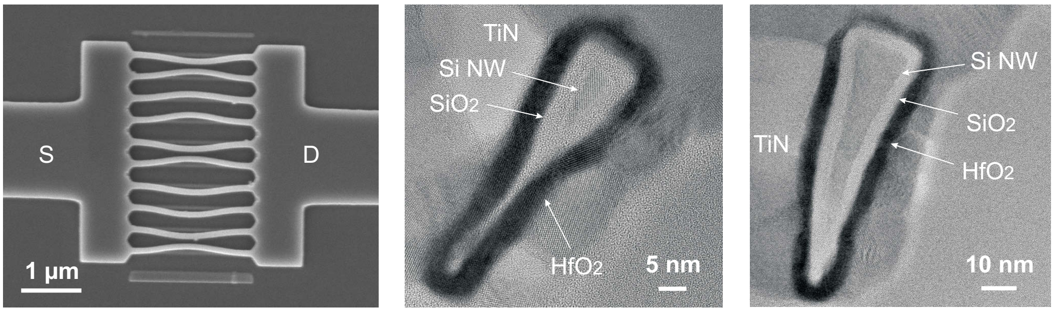
7 Transport enhancement in buckled GAA rounded triangular NW AMOSFETs

In this chapter, we report more precise transport analysis in the GAA buckled rounded triangular Si nanowires with sub-5 and sub-15 nm cross-sections supported by extensive TCAD device simulations (the fabrication process in chapter 4). HRTEM was done on the finalized and electrically characterized devices using FEI Titan 80-300 with 0.08 nm resolution to provide clear inputs for TCAD device simulations and transport analysis. Stress was measured on the buckled GAA Si nanowires via ALD high-k/metal-gate stack using micro-Raman spectroscopy. As a first step, the accuracy of the Y-function method was compared to the split-CV method using TCAD device simulation based on the experimental cross-sections. Afterward, the Y-function method was applied to extract low-field mobility from I-V characteristics of each buckled device and the stress-based low-field electron mobility values are reported for each device. The buckled sub-5 and 15-nm Si nanowires show 88 and 99 mV/dec. subthreshold slopes and stress-based low-field electron mobility enhancements of 50% and 54% vs. the electron mobility in bulk Si at the same doping level using the Y-function method, all at V_{DS}=100 mV and T=300 K, respectively.

7.1 Fabrication and stress development during the process

7.1.1 Fabrication of buckled GAA Si nanowire MOSFETs

The process flow to fabricate top-down buckled GAA Si nanowire accumulation-mode MOSFETs (AMOSFETs) down to ~4 nm rounded triangular cross-section is reported previously in chapter 4 (see also [1]-[4]). Fig. 7.1(a) shows an array of GAA buckled 2.0 μm long Si nanowire MOSFET, after the high-k/metal-gate stack step. As shown in HRTEM nanographs in Fig. 7.1(b) and (c), obtained by FEI Titan 80-300 with 0.08 nm resolution, the cross-section of the Si nanowires is rounded triangular due to using a HBr/O_2-based Si dry etching followed by stress-limited dry oxidation before the gate stack step. The sub-5 nm and 15-nm cross-sections, called in this chapter W05 and W15, respectively, can be obtained from the initial mask nanowire width of 30 and 40 nm [1], [3]. The n-type channel doping level is 1.0×10^{18} cm^{-3}.



(*a*) (*b*) (*c*)

Figure 7.1: SEM top-view micrograph of a dense array multi-gate buckled 2.0 μ m long Si nanowire nMOSFET on a SOI substrate after the high-k/metal-gate stack step (a). HRTEM cross-section nanographs of sub-5 nm (b) and sub-15 nm (b) Si NW MOSFETs, obtained by FEI Titan 80-300 with 0.08 nm resolution.

Note that formation of a sub-4 nm SiO_2 interfacial thin film between the NW and the HfO_2 layer in Fig. 7.1(b)-(c) is due to the diffusion of oxygen atoms via the 50 nm thin metal-gate layer. It can be suppressed using a thick conformal metal-gate capping layer right after the metal-gate deposition step [6].

7.2 Stress measurement via ALD gate stack using micro-Raman spectroscopy

Micro-Raman spectroscopy was employed to measure stress on the finalized GAA W05 and W15 Si nanowire MOSFETs at 293 K. A Renishaw inVia spectrometer setup is used with a green laser of 532 nm in wavelength and 55 mW. The green laser was chosen to have enough penetration depth in both Si ($\approx$1 μm) and the surrounding TiN metal-gate layer (not transparent) to obtain both Raman spectra of the strained Si nanowire and the relaxed Si carrier wafer underneath while focusing the laser beam on the nanowire. The Raman scan was done across the Si nanowire array and Fig. 7.2 shows the micro-Raman spectra of the W05 (left) and the W15 (right) NWs. Using the Lorentzian peak-fitting procedure [5], the downshift in the Raman peak wavenumber can be translated to the stress value, reporting 3.10 GPa and 1.64 GPa uniaxial tensile stress in the W05 and the W15 NWs, respectively.

7.3 Numerical device simulation

Transport analysis in scaled cross-section Si nanowires including corners especially with a sub-5 nm cross-section is not simple. In this section, 3D TCAD device simulation was done using similar GAA rounded triangular Si nanowire cross-sections in Fig. 1(b) and (c), with ~4×12 and ~15×23 nm×nm NW cross-sections, respectively. TCAD Sentaurus Device (G-2012.06) was used for quasistationary numerical simulations. Equivalent gate oxide thickness (EOT)

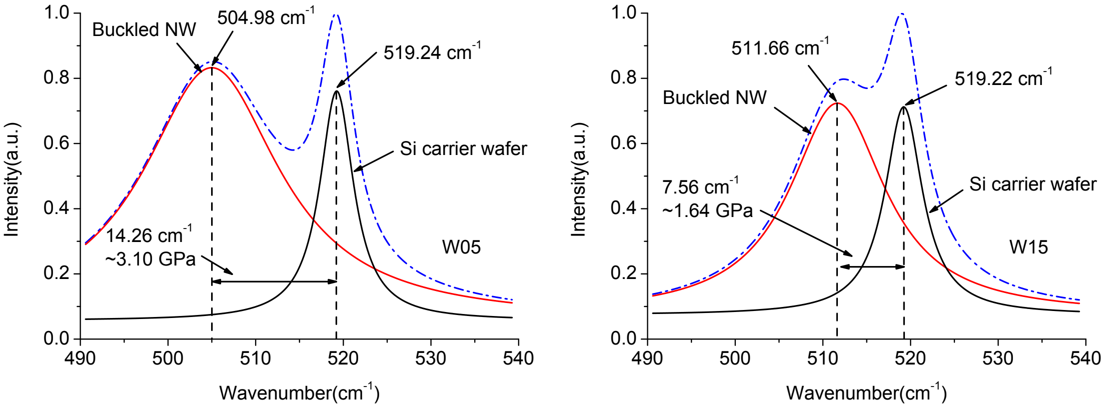


Figure 7.2: Micro-Raman spectra on the finalized W05 (left) and W15 (right) nanowires via ALD high-k/metal-gate stack. The Lorentzian peaks correspond to the buckled NW (downshifted curve) and the relaxed Si carrier wafer underneath (with a peak at ~519.2 cm^{-1}).

of 4.4 nm was used for both structures, considering both HfO_2 and SiO_2 interfacial layers in Figs. 7.1(b) and (c). A channel length of 100 nm with a n-type doping level of 1.0×10^{18} cm^{-3}, a metal-gate workfunction of 4.5 eV were used in the simulations (T=300 K and V_{DS}=100 mV). The source/drain extensions were 20 nm long with a n-type doping level of 1.0×10^{20} cm^{-3}.

The local carrier current in a GAA 3D MOSFET structure can be calculated at each bias voltage using electrostatic and quasi-Fermi potential equations. 3D density gradient model can be coupled to the Poisson equation as well to include 3D quantization effects in nanoscale [7]-[8] while considering the Boltzmann statistics [7]. The semi-classical Slotboom bandgap narrowing model was used for the highly doped Si channels [7]-[9]. Fig. 7.3 shows the transfer characteristics of the GAA W05 and the W15 Si nanowire AMOSFETs, considering both classical and quantum simulations.

Fig. 7.4 shows the cross-sectional local quantum electron density in the W15 MOSFET (a) together with local quantum (b) and local classical (c) electron densities in the W05 MOSFET, all at V_{GS}=1.5 V and V_{DS}=100 mV. Fig. 7.5 shows the cross-sectional local electric field (d) and local carrier mobility (e) in the W05 MOSFET, all at V_{GS}=1.5 V and V_{DS}=100 mV (classical simulation). As shown, the corner regions suffer from a higher normal electric field and therefore, have a smaller local electron mobility; but on the other hand, have a higher local electron density due to the corner effect making the transport analysis not straight forward.

7.4 Extraction of key MOSFET parameters in an AMOSFET

AM/JL MOSFETs operate in accumulation regime above flat-band and in depletion regime below flat-band. Below flat-band, the conduction current is mainly inside the channel volume, called bulk current. Above flat-band, both surface and volume contribute in conduction

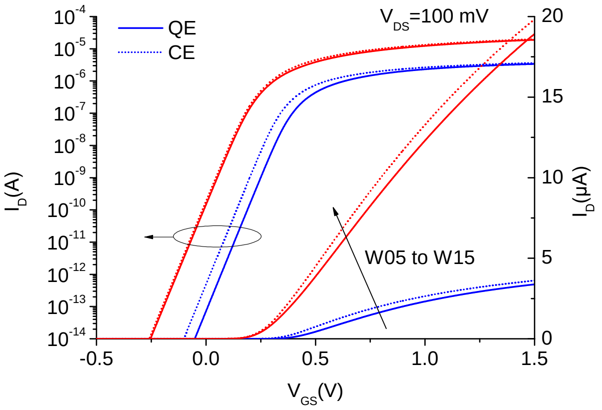


Figure 7.3: Transfer characteristics of GAA W05 and W15 Si nanowire AMOSFETs at V$_{DS}$=100 mV, considering both classical and quantum electrons.

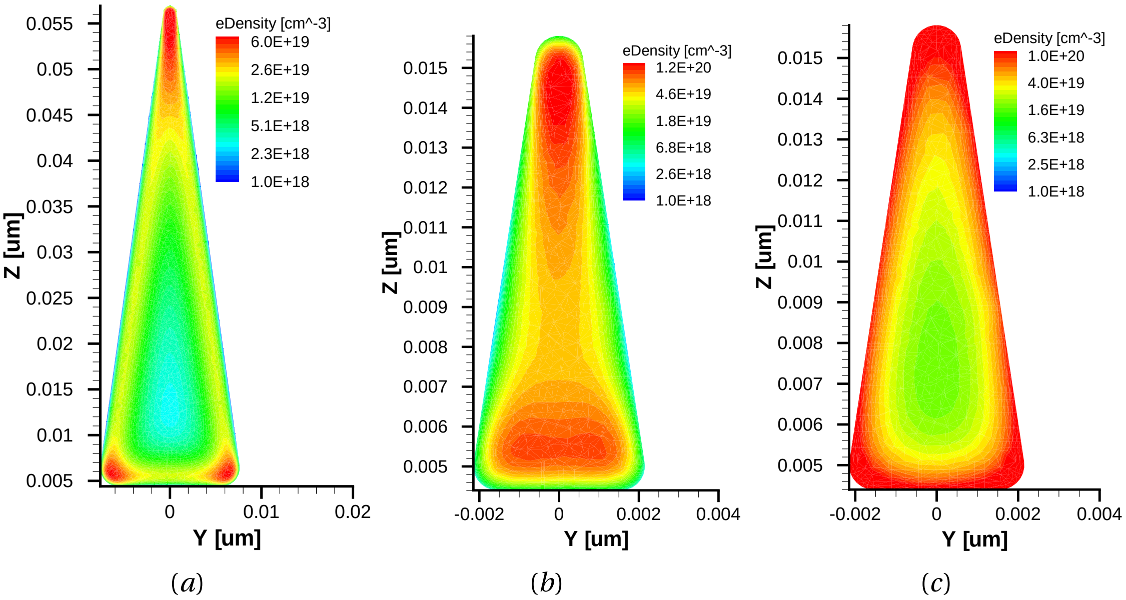


Figure 7.4: Cross-sectional quantum electron density in W15 (a) and W05 (b), classical local electron density in W05 (c) GAA Si nanowire AMOSFETs, all at the middle of the channel (oxide is not shown, V$_{GS}$=1.500 V, V$_{DS}$=100 mV).

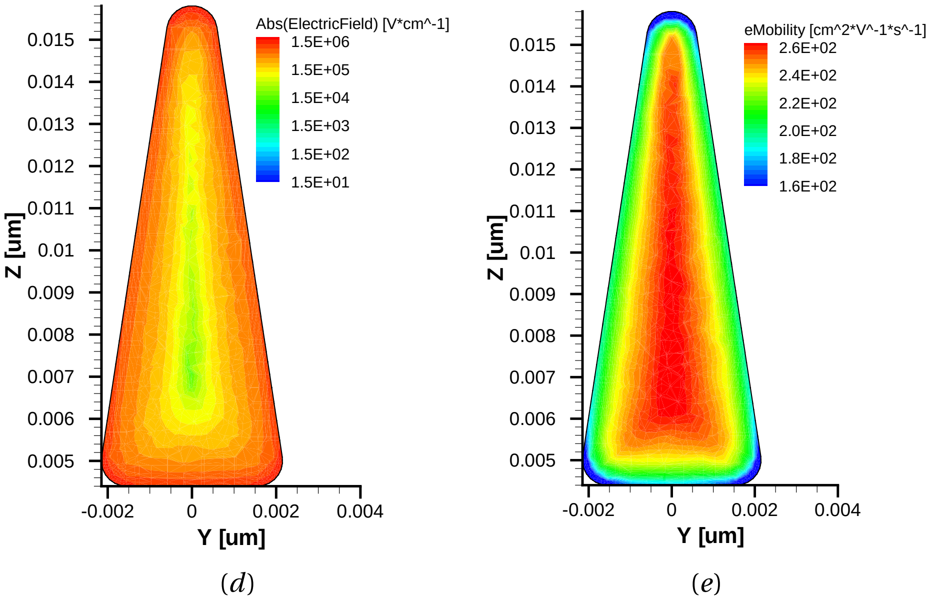


Figure 7.5: Cross-sectional absolute electric field in W05 (d) and local electron mobility in W05 (e) GAA Si nanowire AMOSFETs, all at the middle of the channel considering classical simulation (oxide is not shown, V_{GS}=1.500 V, V_{DS}=100 mV, classical simulation).

and the surface current component is called accumulation current. Obviously, the threshold voltage in this case occurs below the flat-band voltage [10], can be considered approximately as the bias that the channel starts to switch from fully-depleted to partially-depleted. Since below flat-band, the volume bulk current is the only current component, the channel cross-section dimension, geometry and channel doping level can be used to engineer the V_{FB}-V_{TH} difference.

7.4.1 Threshold voltage extraction method

The threshold voltage of a MOSFET can be extracted, quasi-independent of series resistance and conduction mechanism, using the transconductance change (TC) method [11]. Fig. 7.6 shows the drain current of the W15 MOSFET and its derivatives at V_{DS}=100 mV. The numeric V_{TH} values are reported in table 7.1 for both W05 and W15 structures. Note that the quantization-based threshold and flat-band voltage upshifts are due to the higher quantized subband energies [12]-[13].

7.4.2 Flat-band voltage extraction method

Initially, the flat-band voltage can be extracted from the x-intercept of Q_G-V_{GS} simulation at V_{DS}=0 V, called V_{FB}^{1C} and V_{FB}^{1Q} for both classical and quantum electrons (see Fig. 7.6). Note that due to quantization, the flat-band condition (e.g. uniform channel quasi-Fermi potential) cannot be satisfied in the entire channel cross-section [14], [15]. The slight difference between

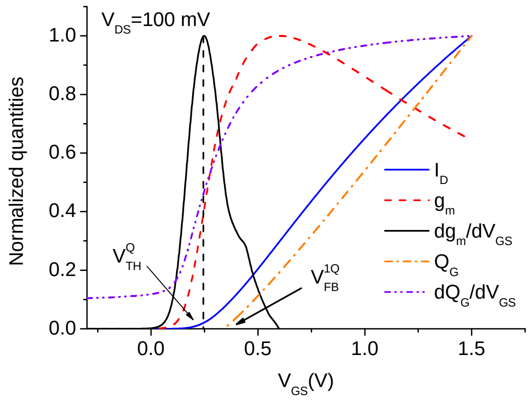


Figure 7.6: Normalized quantities of I_D, g_m, dg_m/dV_{GS} at V_{DS}=100 mV, Q_G^{acc} and dQ_G/dV_{GS} at V_{DS}=0 V to the maximum values vs. V_{GS} for the GAA W15 Si nanowire MOSFET including quantum confinement. The maximum values for each parameter are 1.89×10^{-5} A, 1.77×10^{-5} A/V, 8.06×10^{-5} A/V^2, 1.02×10^{-16} C and 9.51×10^{-17} F, respectively.

W_{NW} (nm)	V^C_{TH} (V)	V^Q_{TH} (V)	V^{1C}_{FB} (V)	V^{1Q}_{FB} (V)	V^C_{FB} (mV)	V^Q_{FB} (mV)	CW^{AC}_{eff} (F/cm)	CW^{AQ}_{eff} (F/cm)	μ_0^{AC} (cm^2/V·s)	μ_0^{AQ} (cm^2/V·s)	μ_0^{AYC} (cm^2/V·s)	μ_0^{AYQ} (cm^2/V·s)
W05	0.321	0.368	0.327	0.380	0.319	0.372	2.84×10^{-12}	2.62×10^{-12}	234	230	239	221
W15	0.244	0.247	0.322	0.340	0.319	0.337	9.47×10^{-12}	8.90×10^{-12}	244	236	234	226

Table 7.1: Key MOSFET parameters extracted from the quasistationary device simulations for W05 and W15 Si nanowire MOSFETs.

W_{NW} (nm)	CW^{BC}_{eff} (F/cm)	CW^{BQ}_{eff} (F/cm)	μ_0^{BC} (cm^2/V·s)	μ_0^{BQ} (cm^2/V·s)	μ_0^{BYC} (cm^2/V·s)	μ_0^{BYQ} (cm^2/V·s)
W05	2.97×10^{-12}	2.98×10^{-12}	283	289	271	262
W15	9.90×10^{-12}	9.41×10^{-12}	261	255	262	251

Table 7.2: Key MOSFET parameters extracted from the quasistationary device simulations for W05 and W15 Si nanowire MOSFETs (region B).

V_{FB}^{1C} and the actual bias voltage to obtain the flat-band condition in the cross-section for the classical electrons (V_{FB}^{C}) is due to the extraction methodology. This slight difference can be used to extract a more accurate quantum flat-band voltage (V_{FB}^{Q}) in table 7.1. The observed 47 and 53 mV upshifts in the threshold and the flat-band voltages of the W05 NW MOSFET, respectively, are due to the strong two dimensional confinement in the entire of the sub-10 nm channel cross-section in comparison to the wider device.

7.4.3 Product of gate-channel capacitance and channel width

Drain current in strong accumulation regime directly depends on gate-channel capacitance and channel width [10]. The total gate-channel capacitance can be extracted at any gate bias voltage using the derivative of the gate charge in Q_G-V_{GS} simulation at V_{DS}=0 V. As shown in Fig. 7.6, the total gate-channel capacitance (dQ_G/dV_{GS}) is a bias-dependent parameter from subthreshold to strong accumulation, depending on the depletion layer thickness below flat-band, quantization [16] and Debye broadening effect [17].

The effective channel width in a GAA architecture can vary for classical and quantum electrons especially in the presence of corners. The gate-channel capacitance be a bias-dependent parameter over strong accumulation regime as well. On the other hand, quantization shrinks both gate-channel capacitance and effective channel width of GAA architectures. Therefore, instead of defining each parameter separately, the product of gate-channel capacitance and channel width, called CW_{eff} in this chapter, can be extracted directly from the gate charge simulation (L: channel length):

$$CW_{eff}(V_{GS}) = \frac{1}{L} \cdot \frac{dQ_G(V_{GS})}{dV_{GS}} \tag{7.1}$$

Two bias regions of V_{GS}-V_{FB}, 0.4-0.5 V and 1.0-1.1 V, labeled A and B, respectively, are considered for further device analysis and key MOSFET parameter extractions in accumulation regime. Note that the CW_{eff} values reported in tables 7.1 and 7.2 correspond to the average value over the A and B bias regions, respectively.

7.4.4 Low-field electron mobility extraction by the split-CV method

Using the initial I_D-V_{GS} analytical formula for AM/JL MOSFETs in [10], it is possible to show that in linear accumulation regime (V_{GS}-V_{FB}>V_{DS}, V_{GS}>V_{FB}), the effective carrier mobility using the split-CV method [18] can be calculated by:

$$\mu_{eff}(V_{GS}) = \frac{I_D^{acc}(V_{GS})}{Q_G^{acc}(V_{GS})} \cdot \frac{L^2}{V_{DS}} \tag{7.2}$$

The accumulation current in strong accumulation can be calculated from the difference between the total drain current and the current at flat-band. Considering the effect of series

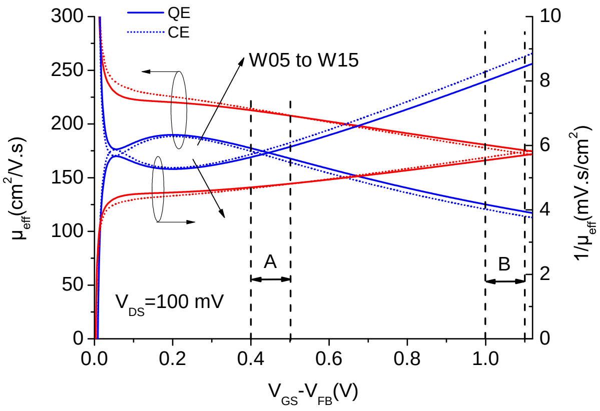


Figure 7.7: Effective electron mobility and its reverse vs. V$_{GS}$-V$_{FB}$ for the GAA W05 and the W15 Si nanowire AMOSFETs, using the split-CV method.

resistance and normal electric field on transconductance or effective carrier mobility drop in strong accumulation, the bias-dependency of the effective carrier mobility can be simply assumed as (see also [19]):

$$\mu_{eff}(V_{GS}) \approx \frac{\mu_0}{1+\theta\cdot(V_{GS}-V_{FB})} \tag{7.3}$$

where μ_0 and θ are low-field carrier mobility and mobility attenuation factor, respectively. The μ_0 values for both W05 and W15 MOSFETs are extracted from the slope of $1/\mu_{eff}$(V$_{GS}$) vs. V$_{GS}$-V$_{FB}$ plots in both A and B regions (see Fig. 7.7) and are reported in tables 7.1 and 7.2, respectively (μ_0^C and μ_0^Q).

7.4.5 Low-field electron mobility extraction by the Y-function method

Applying the split-CV method to a nanoscale device is barely feasible, needing a pretty large array of devices [20]. On the other hand, the Y-function method is based on a simple I$_D$-V$_{GS}$ experiment [19], applicable on every device, but needs a precise estimation of channel width and gate-channel capacitance. Using the initial I$_D$-V$_{GS}$ analytical formula for AM/JL MOSFETs in [10], it is possible to show that in linear accumulation regime, the Y-function can be calculated by:

$$Y(V_{GS}) = \frac{I_D^{acc}(V_{GS})}{\sqrt{g_m(V_{GS})}} \approx \sqrt{\frac{\mu_0\cdot V_{DS}\cdot CW_{eff}}{L}}\cdot(V_{GS}-V_{FB}) \tag{7.4}$$

Neglecting the slight CW$_{eff}$ variation in each A and B regions and using the average values reported in tables 7.1 and 7.2 over each bias region, the μ_0 values for both W05 and W15 MOSFETs in each bias region are extracted from the slope of Y-function (see Fig. 7.8) and

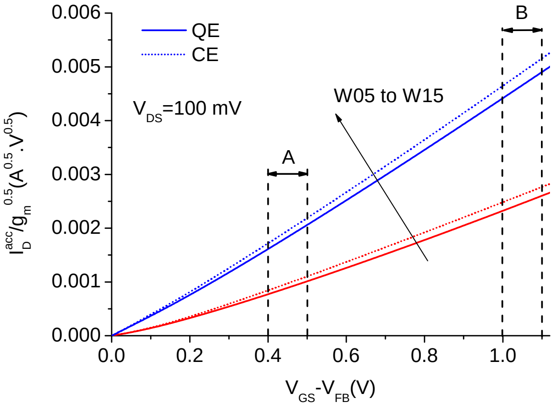


Figure 7.8: Y-function vs. V$_{GS}$-V$_{FB}$ for the GAA W05 and the W15 Si nanowire AMOSFETs.

reported in tables 7.1 and 7.2 (μ_0^{YC} and μ_0^{YQ}). In both A and B regions, the Y-function and split-CV low-field mobility values are pretty close to each other, sub-4 and 9% inaccuracies, respectively, also mainly due to neglecting the bias-dependency of the MOSFET parameters, assuming a linear charge accumulation in the devices with rounded corners, assuming the accumulation current as the main current component in accumulation regime and extraction methodology. The slight difference between the extracted low-field mobility values in the A and B regions can be addressed by the bias-dependency of the key MOSFET parameters over accumulation regime, resulting the bias-dependency of the θ parameter as well.

7.5 Electrical characterization

Electrical characterization was carried out using a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer at 300 K. The W05 and W15 devices include 10 nanowires, with 2.0 μm length, in parallel (see top-view SEM micrograph in Fig. 7.1(a)). The HRTEM cross-sections of the electrically characterized devices are reported in Fig. 7.1(b) and (c). Fig. 7.9 shows the transfer and transconductance characteristics of the W05 and the W15 Si nanowire MOSFETs. The key MOSFET parameters were extracted using the methods mentioned in section 7.4 and reported in table 7.3. The numeric values of the threshold and the flat-band voltages together with the subthreshold slope correspond to V$_{DS}$=100 mV, while the I$_{on}$/I$_{off}$ ratios are reported at V$_{DS}$=1.500 V. Note that the V$_{FB}^{Q}$-V$_{TH}^{Q}$ difference from the TCAD device simulations were used to estimate the V$_{FB}$ values of the GAA nanowires from the extracted V$_{TH}$ values.

Fig. 7.10 shows the Y-function for both the W05 and the W15 MOSFETs at V$_{DS}$=0.100 V. The low-field electron mobility values are extracted using the slope of Y-function and the CW$_{eff}$ values based on the device simulation data in table 7.1, corresponding to region A, the common linear regime for both Y-functions in Fig. 7.10, and reported in table 7.3. The low-field mobility enhancements in comparison to the bulk Si electron mobility at the same

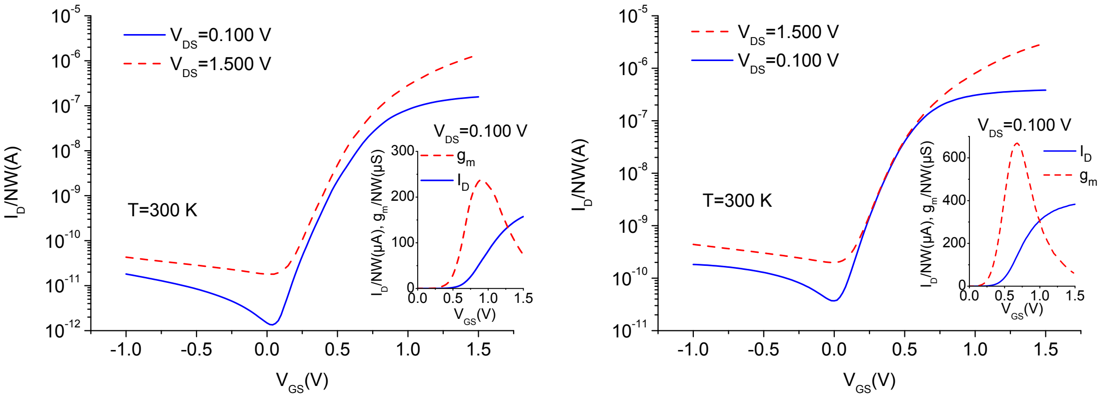


Figure 7.9: Transfer characteristics of the W05 (left) and the W15 (right) Si nanowire MOSFETs at 300 K at V_{DS}=0.100 and 1.500 V. The insets show the transfer and transconductance characteristics at V_{DS}=0.100 V in linear scale.

W_{NW} (nm)	V_{TH} (V)	V_{FB} (V)	SS (mV/dec.)	μ_0 (cm^2/V·s)	μ_0/μ_0^{Bulk} (%)	I_{on}/I_{off} (A/A)
W05	0.640	0.644	88	379	50	1×10^5
W15	0.480	0.570	99	388	54	2×10^4

Table 7.3: Key MOSFET parameters extracted from the electrical characterization of W05 and W15 buckled GAA Si nanowire MOSFETs.

doping level (252 cm^2/V·s) [21] are reported in table 7.3, representing 50% and 54% carrier mobility enhancement in the buckled W05 and the W15 MOSFETs, respectively. Note that the stress-based electron mobility can be even higher, up to ~100% [22] as reported for lightly doped Si channels, using an excellent channel-dielectric interface [23], while considering the carrier mobility boost value is becoming smaller in highly and heavily doped devices [24].

7.6 Summary

In this chapter, we reported precise transport analysis in the fabricated buckled GAA rounded triangular Si nanowire nMOSFETs with sub-5 and sub-15 nm NW cross-sections, electrical characterization supported by extensive TCAD device simulation for the first time. High resolution TEM cross-sections from the fabricated devices, with 0.08 nm resolution, were used as inputs to estimate the product of effective channel width and gate-channel capacitance, all obtained by FEI Titan 80-300. As a first step, the accuracy of the Y-function to estimate the low-field carrier mobility was compared to the split-CV method over the linear region of the experimental Y-function for both devices, V_{GS}-V_{FB} of 0.4-0.5 V, using TCAD device simulation, showing a sub-4% inaccuracy. Afterward, the Y-function was applied to the electrical characterization data, using the CW_{eff} values from the TCAD simulations to estimate

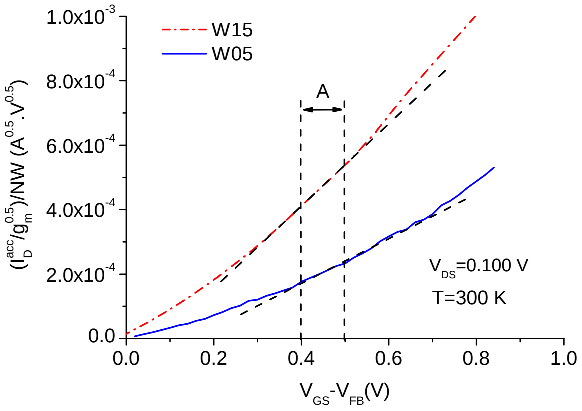


Figure 7.10: Y-function for both W05 and W15 nanowire MOSFETs at V_{DS}=0.100 V.

the experimental low-field mobility values. The buckled GAA sub-5 and sub-15 nm NWs show 50% and 54% electron mobility enhancement in comparison to the electron mobility in bulk Si at the same doping level (1×10^{18} cm^{-3}, 252 $cm^2/V{\cdot}s$), respectively, all at V_{DS}=100 mV and T=300 K. After finalizing the electrical characterization step, micro-Raman spectroscopy was used to measure the actual stress in the buckled GAA Si NWs and 3.10 and 1.64 GPa uniaxial tensile stresses were measured in the Si NWs with sub-5 and sub-15 nm cross-sections, respectively.

The original work carried out relative to this chapter includes:

- **Electrical characterization of buckled GAA Si NW nMOSFETs**: Electrical characterization of buckled GAA Si NWs with sub-5 and sub-15 nm NW cross-sections was done at 300 K. The key MOSFET parameters e.g. V_{TH}, SS, I_{on}/I_{off} are extracted for both devices [25].

- **HRTEM on buckled GAA Si NWs**: HRTEM cross-section of the electrically characterized devices were done using a FEI Titan 80-300 with 0.08 nm resolution [25]. Note that a high resolution TEM picture with clear boundaries between the various materials in nanoscale are needed to extract the key MOSFET parameters from the electrical characteristics.

- **Stress measurement on the buckled NWs via ALD gate stack using TERS**: Stress measurement was done on the buckled GAA Si NWs via ALD high-k/metal-gate stack using micro-Raman spectroscopy for the first time [25].

- **TCAD device simulation on the HRTEM cross-sections**: TCAD device simulation was done using the HRTEM cross-section inputs to extract some key MOFET parameters precisely from the experimental I-V characteristics e.g. V_{FB} and estimate the product of the gate-channel capacitance and the effective channel width. Using the device simulation data, the accuracy of the Y-function was compared to the split-CV method, for both channel cross-sections [25].

- **I-V based transport analysis and mobility extraction**: The Y-function was finally applied to extract the low-field mobility values from the experimental I-V characteristics of both devices supported by extensive TCAD device simulations. Note that a precise estimation on the gate-channel capacitance and the effective channel width is needed to estimate the carrier mobility accurately using the Y-function method [25].

7.7 Future works

- **Experiments on the accuracy of the Y-function and the split-CV methods**: A large array of buckled GAA Si nanowires should be fabricated. The ALD gate stack process should be improved to minimize the interfacial sub-4 nm SiO_2 layer to improve the device performance (subthreshold slope, leakage current, surface mobility). This helps also to estimate the low-filed mobility on wide range of devices (e.g. GAA to attached wide structures to the BOX layer) more precisely since the thickness of the interfacial SiO_2 layer can vary slightly from e.g. GAA NWs to the wider attached structures to the substrate.
- **Study the stress-based bulk mobility enhancement**: Since the conduction mechanism below flat-band is due to the bulk current (volume conduction mechanism), study the bulk carrier mobility enhancement due to stress is interesting. Note that the stress-based bulk carrier mobility due to stress can be higher than surface mobility [22].
- **3D stress development in the GAA NWs**: Stress measurement via the ALD high-k/metal-gate stack is challenging, due to the non-transparency of the metal gate layer and a pretty scaled Si nanowire cross-section. In this chapter, we showed the first stress measurements on such nanowires using micro-Raman spectroscopy. Due to the freedom on buckling (and shrinking as well) in the suspended channels, the stress level can be tuned easier in comparison to the attached devices to the substrate. One of the future works can be studying the stress development in the suspended nanowires, various length and cross-section dimensions. Note that both tensile and compressive stresses can be achievable simply in the nanowires using metal gate strain. TERS can be used to improve the level of local Raman signal as well, if needed, using e.g. the current setup. Note that parallel to carrier mobility improvement in the typical MOSFETs, a high level of local stress can be used to improve the band-to-band tunneling current in Tunnel-FETs, as CMOS boosters.

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8 Conclusion

Multi-gate architectures together with strain engineering and high-k/metal-gate stack are being used for the 22 nm technology nodes and beyond. The target of this thesis is to address innovative fabrication methods to make sub-5 nm cross-sectional Si nanowires on both bulk and SOI substrates, optical/electrical characterization methods in nanoscale, integration of ALD high-k/metal-gate for suspended channels, study the device behavior in inversion/accumulation-mode and junctionless MOSFETs (experiments supported by extensive TCAD device simulation), integration of local stressors as CMOS boosters for carrier mobility and current enhancement, transport analysis in nanoscale and finally, precise key MOSFET parameter extraction methodologies.

In this thesis, we targeted to make GAA Si nanowire MOSFETs with minimized cross-section to obtain the optimum subthreshold slope of ~60 mV/dec. (a fundamental limit for classical MOSFETs) at room temperature including stressors as CMOS boosters to improve the ON current without the OFF current degradation. Such devices can be used to make ultra-low power/low voltage MOSFETs and circuits working e.g. in subthreshold regime. This is the first clear step from simulation to experiment to implement sub-60 mV/dec. in such GAA Si nanowire platforms as well in the future, getting boost from the best electrostatic control of the channel and high level of stress engineering as a CMOS booster.

8.1 Summary

The main achievements in the present work include:

- **Origin of built-in stress during oxidation of Si nanowires**: Built-in stress during the oxidation of suspended Si nanowires in the presence of hard mask and spacer is addressed in details. This part includes fabrication of suspended sub-100 nm cross-section Si nanowires with a tensile Si_3N_4 hard mask on top, fabricated using 0.8 μm optical lithography, hard mask and spacer technology. Micro-Raman spectroscopy was used to measure stress in sub-100 nm Si nanowires and accumulation of up to 2.6 GPa is reported in the buckled naked NWs [1]-[2]. The contribution of hard mask on the nanowire formation and built-in stress is discussed in details. Using the hard mask and spacer engineering, buckled self-aligned dual Si nanowires with sub-100 nm cross-section are fabricated together with stress-based low-field electron mobility enhancement [3]. Finally, correlation of stress profile and I-V characteristics of buckled GAA Si NWs is reported in [2].

- **Development of a SOI Si NW platform to make GAA sub-5 nm cross-section NWs**: A SOI Si nanowire platform is developed considering side wall engineering, using HBr/O_2, and stress-limited oxidation in the presence of a tensile Si_3N_4 hard mask on top to make sub-5 nm cross-section Si nanowires. Both tensile and compressive stresses can be included in the platform using various oxidation conditions and metal-gate strain. Buckling was induced to the NWs using oxidation, at 925 °C, and metal-gate strain. I successfully developed and finalized the first GAA Si nanowire MOSFET run-card at EPFL including a SOI platform and ALD high-k/metal-gate stack. I demonstrated GAA sub-5 nm cross-section Si nanowires as high temperature performance MOSFETs, helpful to study the scattering mechanism in deeply scaled cross-section and in a highly doped accumulation regime [4]-[7].
- **Local volume accumulation/depletion in GAA Si NW junctionless MOSFETs**: TCAD device simulation was done to perform a charge-voltage based study of the corner effect in triangular GAA Si nanowire junctionless MOSFETs. The new concept of local volume accumulation/depletion is reported and described precisely using volume vs. surface conduction above and below flat-band [8]. The key MOSFET parameters were extracted precisely and the concept of "quantum flat-band voltage" is highlighted and its extraction method is described in details [8].
- **Transport analysis in GAA Si NW junctionless MOSFETs**: TCAD device simulation was done to study the transport in triangular GAA Si NW MOSFETs. Note that non-uniform accumulation of charges and normal electric field in especially deeply scaled cross-section channels would make the transport analysis non-straightforward. The accuracy of both the split-CV and the Y-function methods are discussed in details for transport analysis in the junctionless MOSFETs with and without contact engineering. A significant bias-dependent series-resistance in junctionless MOSFETs above flat-band is reported, making the transport analysis non-straightforward, without contact engineering [9].
- **Transport enhancement in buckled GAA Si NW accumulation-mode MOSFETs**: The Y-function was used to extract low-field mobility from the I-V characteristics of the buckled GAA sub-15 and sub-5 nm cross-section Si nanowires, supported by extensive TCAD device simulations. HRTEM cross-section of the GAA Si nanowires was done with 0.08 nm resolution, as the inputs for TCAD simulation and precise key MOSFET parameter extraction. Stress in the buckled NWs is measured via the ALD high-k/metal-gate stack using micro-Raman spectroscopy. The stress-based low-field electron mobility

enhancement is reported for both structures in comparison to the electron mobility in bulk Si at the same doping level [10]-[11].

8.2 Future work perspectives

In this thesis and especially for the developed SOI Si nanowire platform, we targeted to perform several device and circuit analysis, at the first glance. In an experiment-based Ph.D. thesis, should be supported by extensive external partnership e.g. sophisticated optical/electrical characterization setups as well, almost all the results will be available in the last 15 months of the thesis, needing several treatments for clear highly ranked publications (manuscript preparation and the reviewing procedure) and international conference presentations. In parallel, extensive TCAD device simulation is needed for precise device analysis and key MOSFET parameter extraction, overloading the tasks especially in the last months. In this thesis framework, I targeted the following tasks initially (even some included in the mask design), can be done as future works in this direction.

- **Study the effect of stress in DC/AC/RF characteristics of GAA NW devices**: Since both uniaxial tensile and compressive stresses can be simply integrated in the SOI Si nanowire that I developed, such CMOS boosters can be used to improve carrier mobility in both NMOS and PMOS devices. Considering the effect of stress on DC/AC/RF characteristics of GAA Si nanowire MOSFETs on a SOI substrate in inversion-mode, accumulation-mode and junctionless can be an excellent future work. Note that such designs were done already in my Ph.D. framework (not shown in this thesis yet, in progress fabrication, a simple logic gate is presented in [12]). The effect of stress on circuit performance (CMOS/NMOS/PMOS logic, ring oscillator, etc.) can be studied in details as well.

- **Transport analysis below flat-band in GAA Si NW junctionless MOSFETs**: TCAD device simulation can be used for precise transport analysis in GAA Si nanowire junctionless MOSFETs with various cross-sections below flat-band. Note that the channel width changes significantly in this regime, especially in the presence of corners and such studies can be pretty interesting for a pretty close TED paper submission.

- **Ultra-low power/low voltage circuit implementation using GAA Si NW JL MOSFETs**: Based on TCAD device simulations and experiments, we showed that the threshold voltage of accumulation-mode and junctionless MOSFETs can be engineered significantly by cross-section (dimension, corner effect) and stress engineering. Note that an appropriate ALD high-k/metal-gate stack can be used to tune the threshold voltage as well using e.g. metal workfunction engineering (metal type or annealing in the presence of hydrogen or oxidation in the case of having e.g. an Ru/HfO_2 gate stack [13]). An interesting work can be a simple ultra-low power/low voltage circuit implementation (e.g. simple logic, ring oscillator, etc.) using GAA Si NW junctionless MOSFETs with sub-100 mV power supply voltage, working below flat-band and even in subthreshold regime. The GAA Si NW accumulation-mode or junctionless MOSFETs are among the best candidates (among the architectures with minimum 60 mV/dec. subthreshold slope) to achieve this target since such devices are less sensitive to the gate stack below flat-band and it is more appropriate to obtain almost sub-62 mV/dec. at room temperature. Note that there are a few works in this direction, needing several efforts for an appropriate threshold voltage engineering and optimum subthreshold device behavior (excellent gate stack, a GAA architecture with minimized channel dimension and contact engineering). Such experiments can be supported by extensive TCAD simulations as well.

- **Using local stressors to boost the current in asymmetrically strained Tunnel-FETs**: Based on local stressors e.g. oxidation and metal-gate strain, a high level of stress (>4 GPa) can be engineered in the Si nanowire channel. Note that placing the source/channel junction at the highly stressed region of the nanowire while the drain/channel junction is placed on the relaxed drain anchor can improve the tunneling current without affecting the OFF current [14]. Implementation of such devices need several experimental treatments e.g. ultra-abrupt junction (sophisticated implantation and annealing) in the nanowires, excellent ALD gate stack and appropriate strain engineering should be performed in part via external partnership to obtain excellent results.

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A Process flow of buckled NWs on bulk

The following table presents a typical process flow to make suspended buckled triangular Si nanowires with sub-100 nm cross-sections using 0.8 μm optical lithography and bulk Si substrate.

Step	Process	Details
1	substrate	(100) prime Si substrates, p-type, 0.1-0.5 Ω·cm, 100 mm
2	hard mask	RCA, 15 nm SiO_2 (dry ox., 800 °C), 80 nm LPCVD Si_3N_4 (770 °C, residual thin film stress: +1.3 GPa biaxial tensile)
3	NW pattern	HMDS, Ritetrack1 (coat 0.8 μm ECI), DWL200 (KRY4.04x, defous: 0, filter: 30%, energy: 185, layer: NW), Ritetrack2 (ECI develop.); Note: NW width: 0.8-1.8 μm, NW length: 2-20 μnm.
4	hard mask etch	Oxford (O_2 plasma, 30 s), A601E (SiO2, 20 s)
5	Si etch	A601E (Si-opto, 20 s)
6	Alphastep	inspection (Si rib height: ~300-400 nm)
7	strip resist	Oxford (O_2 plasma, 30 min)
8	wet oxidation	RCA, wet Si oxidation (300 nm thick oxide growth on (100) surface, 950 °C)
9	strip SiO_2	BHF (~4 min)
10	Si_3N_4 spacer	RCA, LPCVD Si_3N_4 dep. (35 nm, 770 °C)
11	Si_3N_4 open	A601E (anisotropic Si_3N_4 etch by SiO2, 15 s)
12	Si etch	A601E (isotropic Si etch by Si-opto, ~75 s); Note: 0.8 μm wide NWs should be suspended.
13	wet oxidation	RCA, wet Si oxidation (300 nm thick oxide growth on (100) surface , 850 °C)
14	strip Si_3N_4/SiO_2	Reclaim (HF 49%, 30 min)
15	isolation	2 μm LTO dep. (LPCVD, 425 °C), densification (900° C, 30 min), 2 μm LTO dep. (LPCVD, 425 °C), dens. (900° C, 30 min), CMP, BHF (LTO etch to uncover completely the NWs)
16	gate stack	RCA, 15 nm SiO_2 (dry oxidation, 850 °C), 300 nm LPCVD poly-Si (N^+ in-situ doped, phosphorous: 2×10^{20} cm^{-3}, 480 °C), furnace annealing (900 °C, 5 min)

Step	Process	Details
17	gate pattern	HMDS, Ritetrack1 (coat 0.8 μm ECI), MA6 (Gate mask, 4 s), Ritetrack2 (ECI development), 30 s O_2 plasma
18	gate stack etch	A601E (isotropic Si etch by Si-opto, ~1 min), BHF (SiO_2 etch, 15 s)
19	strip resist	Oxford (O_2 plasma, 30 s)
20	implantation LTO	10-20 nm LTO deposition (LPCVD, 425 °C)
21	S/D ion imp.	P or As ion implantation (to obtain $>2\times10^{20}$ cm^{-3})
22	activation	furnace annealing
23	LTO strip	BHF (5-10 s.)
24	passivation	~0.5 μm LTO deposition (LPCVD, 425 °C)
25	Via contacts	HMDS, Ritetrack1 (coat 0.8 μm ECI), MA6 (Contact mask, 5 s), Ritetrack2 (ECI development)
26	LTO etch	A601E (SiO2, 1 min), BHF (30-60 s)
27	strip resist	Oxford (O_2 plasma, 30 min)
28	metallization	Pfeiffer Spider 600 (Al-Si1%, 300 nm)
29	metal pads	Oxford (O_2 plasma, 30 s), Ritetrack1 (coat 0.6 μm ECI), MA6 (Metal mask, 4 s), Ritetrack2 (ECI development)
30	dry Al etch	STS ICP (Al-etch, 90 s)
31	strip resist	Oxford (O_2 plasma, 30 min)
32	sintering	450 °C, 30 min

B Process flow of self-aligned NWs on bulk

The process flow to make more than one Si core on a Si substrate from oxidation of a Si Fin, called self-aligned dual Si nanowires in this thesis, is described in details here. The approximate cross-section dimension of Si nanowires is sub-100 nm, using 0.8 μm optical lithography on bulk Si substrates. The cross-section can be reduced to e.g. sub-5 nm, using e-beam lithography and SOI substrate (having the best control on the Si Fin cross-section before the stress-limited oxidation step). More than two Si cores can be achievable using pre-shape Fin engineering by scalloping.

Step	Process	Details
1	substrate	(100) prime Si substrates, p-type, 0.1-0.5 Ω·cm, 100 mm
2	hard mask	RCA, 500 nm SiO_2 (wet ox., 1050 °C, residual thin film stress: -310 MPa biaxial compressive)
3	NW pattern	HMDS, Ritetrack1 (coat 0.8 μm ECI), DWL200 (KRY4.04x, defous: 0, filter: 30%, energy: 185, layer: NW), Ritetrack2 (ECI develop.); Note: NW width: 0.8-1.8 μm, NW length: 2-20 μnm.
4	hard mask etch	Oxford (O_2 plasma, 30 s), AMS200 (SiO2-PR-5:1, 3 min)
5	Si etch	A601E (anisotropic Si etch by Si-opto, ~30 s)
6	Alphastep	inspection (Si rib height: ~600 nm)
7	strip resist	Oxford (O_2 plasma, 30 min)
8	wet oxidation/ SiO_2 spacer	RCA, wet Si oxidation (300 nm thick oxide growth on (100) surface, 950 °C)
9	SiO_2 open	A601E (anisotropic etch by SiO2, 1 min)
12	Si etch	A601E (isotropic Si etch by Si-opto, ~100 s); Note: 0.8 μm wide NWs should be suspended.
13	wet oxidation	RCA, wet Si oxidation (250 nm thick oxide growth on (100) surface , 850 °C)
14	strip SiO_2	BHF (8 min) or Reclaim (HF 49%, 30 s)
15	isolation	2 μm LTO dep. (LPCVD, 425 °C), densification (900° C, 30 min), 2 μm LTO dep. (LPCVD, 425 °C), dens. (900° C, 30 min), CMP, BHF (LTO etch to uncover completely the NWs)

Step	Process	Details
16	gate stack	RCA, 15 nm SiO_2 (dry oxidation, 850 °C), 300 nm LPCVD poly-Si (N^+ in-situ doped, phosphorous: 2×10^{20} cm^{-3}, 480 °C), furnace annealing (900 °C, 5 min)
17	gate pattern	HMDS, Ritetrack1 (coat 0.8 μm ECI), MA6 (Gate mask, 4 s), Ritetrack2 (ECI development), 30 s O_2 plasma
18	gate stack etch	A601E (isotropic Si etch by Si-opto, ~1 min), BHF (SiO_2 etch, 15 s)
19	strip resist	Oxford (O_2 plasma, 30 s)
20	implantation LTO	10-20 nm LTO deposition (LPCVD, 425 °C)
21	S/D ion imp.	P or As ion implantation (to obtain $>2\times10^{20}$ cm^{-3})
22	activation	furnace annealing
23	LTO strip	BHF (5-10 s.)
24	passivation	~0.5 μm LTO deposition (LPCVD, 425 °C)
25	Via contacts	HMDS, Ritetrack1 (coat 0.8 μm ECI), MA6 (Contact mask, 5 s), Ritetrack2 (ECI development)
26	LTO etch	A601E (SiO2, 1 min), BHF (30-60 s)
27	strip resist	Oxford (O_2 plasma, 30 min)
28	metallization	Pfeiffer Spider 600 (Al-Si1%, 300 nm)
29	metal pads	Oxford (O_2 plasma, 30 s), Ritetrack1 (coat 0.6 μm ECI), MA6 (Metal mask, 4 s), Ritetrack2 (ECI development)
30	dry Al etch	STS ICP (Al-etch, 90 s)
31	strip resist	Oxford (O_2 plasma, 30 min)
32	sintering	450 °C, 30 min

C Process flow of sub-5 nm SOI Si NWs

The following table presents a typical calibrated and validated process flow to make rounded triangular Si nanowires with sub-5 nm cross-sections from a SOI substrate. The process includes a high-k/metal-gate stack. The lithography steps for the gate pattern and metallization can be done using DUV or e-beam lithography as well.

Step	Process	Details
1	substrate	(100) Unibond SOI substrates (SOI/BOX: 340/400 nm)
2	SOI thin down	RCA, dry oxidation (1000 °C), BHF oixde etch to obtain ~100 nm thick SOI
3	implantation LTO	RCA, 20 nm LTO deposition (LPCVD, 425 °C)
4	ion implantation	P or As (tune the SOI active layer doping)
5	activation	furnace annealing or RTA
6	strip LTO	BHF or DHF
7	ZEP coat	substrate dehydration (2 min bake at 180 °C, 10 s cool down), 450 nm ZEP coat (ZEP dispense, 2500 rpm, 2 min bake at 180 °C)
8	e-beam exp.	Vistec EBPG5000 (100 keV, 200 mC/cm^2 dose, ALI mask)
9	ZEP devel.	1 min into AMZL, rinse (IPA, 30 s), dry (N_2 gas flow)
10	optical microscope	inspection
11	alignment mark etch	Oxford (PMMA descum, 8 s), AMS200 (SOI etch by Si-opto, 15 s), AMS200 (BOX etch by SiO2-PR-5:1, 2 min), AMS200 (~1 μm Si etch by Si-opto, 75 s)
12	Alphastep strip resist	inspection (after each etching step) Oxford (O_2 plasma, 30 min)
13	hard mask	RCA, 15 nm SiO_2 (dry ox., 800 °C), 80 nm LPCVD Si_3N_4 (residual thin film stress: +1.3 GPa biaxial tensile)
14	HSQ coat	pre-process adhesion (1 min into MFCD26), rinse (water), dry (N_2 gas flow), 5 min bake at 180 °C, 1 min cool down, 50-150 nm thick HSQ (HSQ dispense, e.g. 3000 rpm)
15	e-beam exp.	Vistec EBPG5000 (e.g. 100 keV, 3000 μC/cm^2 dose, NW mask); Note: NW width: 10-60 nm, NW length: 0.5-2.0 μm.

Step	Process	Details
16	HSQ devel.	60 s in MFCD26, rinse (water), dry (N_2 gas flow)
17	SEM	inspection
18	hard mask etch	A601E (Nitrure1, 20-40 s)
19	SOI etch	STS ICP (15 s breakthrough, 95 s HBr/O_2); Note: priming the chamber and etch rate test is needed.
20	Alphastep	inspection
21	FIB/SEM	inspection
22	gate stack	RCA (dip HF to release the NWs), CPD, 5 nm ALD HfO_2, RTA (600 °C, 15 min), 50 nm TiN (sputtering or ALD)
23	mask deposition	10 nm LTO, 50 nm low stress LPCVD Si_xN_y deposition
24	gate pattern	HMDS, Ritetrack1 (coat 0.6 μm ECI), MA6 (Gate mask, 4 s), Ritetrack2 (ECI development), 30 s O_2 plasma
25	hard mask open	A601E (isotropic Si_xN_y etch by Si-release, 2 min), BHF (LTO etch, 15 s), CPD
26	gate stack etch	RCA1 (isotropic TiN etch, 20 °C, ~30 min), AMS200 (anisotropic HfO_2 etch by Ar Ion Milling, 20 s)
27	SEM	inspection
28	implantation LTO	10-20 nm LTO deposition (LPCVD, 425 °C)
29	S/D ion imp.	P or As ion implantation (to obtain $>2\times10^{20}$ cm^{-3})
30	activation	furnace annealing or RTA
31	LTO strip	BHF (5-10 s.) or DHF (to avoid BOX over-etching)
32	passivation	30-50 nm LTO deposition (LPCVD, 425 °C)
33	Via contacts	HMDS, Ritetrack1 (coat 0.6 μm ECI), MA6 (Contact mask, 5 s), Ritetrack2 (ECI development); DUV or e-beam as alternative.
34	LTO etch	BHF (10 s) or DHF
35	strip resist	Oxford (O_2 plasma, 30 min)
36	metallization	Pfeiffer Spider 600 (Al-Si1%, 100-200 nm)
37	metal pads	Oxford (O_2 plasma, 30 s), Ritetrack1 (coat 0.6 μm ECI), MA6 (Metal mask, 4 s), Ritetrack2 (ECI development)
38	dry Al etch	STS ICP (Al-etch, 30 s)
39	strip resist	Oxford (O_2 plasma, 30 min)
40	sintering	450 °C, 30 min

D TCAD simulations

TCAD Sentaurus was widely used in this thesis mainly for 3D device simulations. Process simulation was only used in this thesis to expect the ion implantation parameters to obtain the appropriate doping levels. The following table shows the simulation tools used in this thesis.

TCAD simulation tool	Description
Sdevice	2-3D electrical device simulation (classical and quantum)
Sprocess	2-3D process simulation (mainly 2D ion implantation/annealing)
Noffset3D	3D meshing strategy in GAA Si NWs
Inspect	General device characteristics (Q-V and I-V)
Tecplot	Extract local device parameters in the NW cross-section
Stucture editor	Design 2-3D GAA Si NW MOSFET structures

Table D.1: TCAD Sentaurus tools used in this thesis.

In chapter 5, I developed a gate-all-around Si nanowire simulation platform based on TCAD Sentaurus version G-2012.06, a parameterized design with an appropriate 3D meshing strategy in both channel and oxide and therefore, an optimized number of mesh points, suitable for both classical and quantized device simulations. It was used in the three chapters (5-7) of this thesis. Note that the 3D quantized device simulations need a pretty dense mesh in both channel and oxide, especially in the corner regions, to provide realistic results. All the used models are described in details in the Sentaurus Device manual, cited in each chapter. But in general, the density gradient model was used to include 3D quantization effects (MLDA as another alternative). Bandgap narrowing at high doping levels by the Slotboom model, the Fermi-Dirac statistics to cover both degenerate and nondegenerate regimes, the Masetti carrier mobility model (DopingDependence, Enormal, HighFieldSaturation) and a simple constant mobility model are the typical key models for such extensive device simulations, done in this thesis. Note that the 3D meshing strategy is playing a key rule especially in the quantized 3D device simulations, minimizing the possible convergence issues and save the simulation time as well.

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- Nano-electronics/systems, Elec. eng., solid-state device physics.
- >20 technical articles in micro/ano-electronics (h index: 4).
- 4.5 year optical/electrical characterization experience in nanoscale.
- 6.0 year work experience in the clean room class 100.
- Competitive national/international rankings/standings.
- Fluent in English (C2), French: Basic understanding.

PRESTIGIOUS EDUCATION

2008-2012	**Ph.D. in Elec. Eng./Nanoelectronics**, Swiss Federal Institute of Technology-EPFL, Lausanne, Switzerland. **Thesis:** Multi-gate Si nanowire MOSFETs: fabrication, strain engineering and transport analysis. **Extensive courses:** Venture challenge, Management of innovation and technology transfer, Nanoscale CMOS and Si-based beyond CMOS nanodevices, Nano-Bio-Sensing, RF MEMS, Power MEMS, Ultimate CMOS devices, modelling micro/nano-electron devices, MEAD advanced engineering circuit courses.
2005-2007	**M.Sc. in Microsystems (Full-GPA)**, Chalmers University of Technology, Gothenburg, Sweden. **Extensive courses:** Semiconductor materials physics.
1999-2004	**B.Sc. in Electrical Eng./Microelectronics**, Sharif University of Technology, Tehran, Iran. **Relevant courses:** Electronics II-III, Physical electronics, Electromagnetics, Thermodynamics, Superconductivity, Electrical machines I-II, Computer architecture and language, Computer programming.
1998-1999	**Prep. courses for the XXXI International Chemistry Olympiad**, Young Scholars Club, Tehran, Iran.
1995-1999	**Mathematics and Physics Diploma**, Brilliant Talent High School (NODET), Arak, Iran.

SELECTED PRESTIGIOUS AWARDS/HONOURS

- **Prospective Researcher Fellowship Award**, Swiss National Science Foundation, EPFL Research Council, 2012.
- **Referee for journal articles in micro/nano-electronics:** Nanotechnology, IEEE Transactions on Electron Devices (TED), Journal of Micromechanics and Microengineering (JMM), Electrochemical and Solid-State Letters (ESL), various IOP journals and special issues.
- **EPFL Ph.D. scholarship** (almost the highest academic Ph.D. salary in the world), Swiss Federal Institute of Technology - EPFL, Lausanne, Switzerland, 2008-2012.
- **IEEE DRC conference travel award** to attend the 69th IEEE Device Research conf., Santa Barbara, USA, 2011.
- **Travel supports** to attend various international conferences in USA and Europe, 2007-2012.
- **1st with Full-GPA 5.0/5.0** in the international Microsystems master program, Chalmers University of Technology, Gothenburg, Sweden, 2007.
- **Presidential Award** as a member of National Olympiad team, Tehran, Iran, 2000.
- **Exceptional Admission** to the EE department of Sharif University of Technology (the best undergraduate engineering program in Iran) without university entrance examination, a member of National Olympiad team, Tehran, Iran, 1999.
- **1st** at the Brilliant Talent High School (NODET) with 4 year GPA 19.10/20.00, Arak, Iran, 1999.
- ***Gold medal*** in the 8th National Chemistry Olympiad **(top 0.01% of eligible participants)**, Tehran, Iran, 1998.
- **2nd** in the 2nd NODET National Chemistry Olympiad **(top 0.1% of eligible participants)**, Iran, 1996.

SELECTED COMPETITIVE TECHNICAL SKILLS

- Strong background in **Micro/Nano-electronics and systems, Electrical Eng. and Solid-state device physics. Software:** TCAD Sentaurus (sdevice, sprocess, 2-3D), TCAD Dios, CoventorWare products (Memulator, Etch3D), Comsol, Pspice, OrCAD, Workbench, Protel, Matlab, Mathcad, L-Edit, Cadence, LaTeX, Microsoft Visio, Corel Draw, Photoshop, Google SketchUp, Freehand, Microsoft Office (Word, Excel, PowerPoint, Access, OneNote), Microsoft Project, C, Pascal, Basic, HTML, Assembly, IC-CAP, Origin.
- **6.0 year professional work experience in the clean room class 100:** thin film (CVD, PVD, ALD), lithography (optical, e-beam), dry/wet etch, CMP, SEM, HRTEM, FIB, RTA, Si-Si fusion bonding, ion implantation, corner-compensation techniques, metrology techniques. **Topics:** Top-down bulk/SOI Si nanowires, local stressors, strained Si nanowires, ALD gate stack, stress-limited oxidation, bridge resonators, fluid-conveying Si microtubes, highly accurate microfluidic density/mass flow sensors.
- **4.5 year optical/electrical characterization in micro/nano-scale:** Laser Doppler Vibrometry (LDV), DC/AC/CV measurements, Cascade prober, PMC150 cryo-prober, Karl Suss PM8, Micro-Raman spectroscopy.

SELECTED ONE PAGE PUBLICATION LIST

- **Nanoelectronics, Si nanowire, Local stressors, Transport in nanoscale, CMOS downscaling:**

1. M. Najmzadeh, Y. Tsuchiya, J.-M. Sallese, M. Berthomé, D. Wang, R. Prang, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Transport enhancement in buckled gate-all-around rounded triangular Si nanowire AMOSFETs”**, IEEE Transactions on Electron Devices, 2012 (under submission).
2. M. Najmzadeh, J.-M. Sallese, M. Berthomé, W. Grabinski, A.M. Ionescu, **”Transport analysis in triangular GAA Si nanowire junctionless nMOSFETs”**, IEEE Transactions on Electron Devices, 2012 (under submission).
3. M. Najmzadeh, J.-M. Sallese, M. Berthomé, W. Grabinski, A.M. Ionescu, ”**Local volume depletion/accumulation in GAA Si nanowire junctionless nMOSFETs”**, IEEE Transactions on Electron Devices, 2012, DOI:10.1109/TED.2012.2220363.
4. M. Najmzadeh, Y. Tsuchiya, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Elastic local buckling as a CMOS booster for GAA Si nanowire nMOSFETs”**, IEEE Electron Device Letters, 2012 (under review).
5. M. Najmzadeh, Y. Tsuchiya, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Multi-gate buckled self-aligned dual Si nanowire MOSFETs on bulk Si for high electron mobility”**, IEEE Transactions on Nanotechnology, vol. 11, pp. 902-906, 2012.
6. M. Najmzadeh, Y. Tsuchiya, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Gate-all-around buckled dual Si nanowire nMOSFETs on bulk Si for transport enhancement and digital logic application”**, MNE 2012 (38th international conference on Micro and Nano Engineering), Toulouse, France, 2012 (oral).
7. M. Najmzadeh, D. Bouvet, W. Grabinski, J.-M. Sallese, A.M. Ionescu, ”**Accumulation-mode gate-all-around Si nanowire nMOSFETs with sub-5 nm cross-section and high uniaxial tensile strain”**, Solid-State Electronics (selected papers from the IEEE ESSDERC 2011 conf.), vol. 74, pp. 114-120, 2012.
8. M. Najmzadeh, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Local stressors to accommodate 1.2 to 5.6 GPa uniaxial tensile stress in suspended gate-all-around Si nanowire nMOSFETs by elastic local buckling”**, IEEE ISDRS 2011 (the **biennial** International Semiconductor Device Research Symposium), University of Maryland, College Park, USA, pp. 1-2, 7-9 Dec. 2011 (oral).
9. M. Najmzadeh, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Accumulation-mode GAA Si NW nFET with sub-5 nm cross-section and high uniaxial tensile strain”**, IEEE ESSDERC 2011 (the 41st European Solid-State Device Research Conference), Helsinki, Finland, pp. 311-314, 12-16 Sep. 2011 (oral).
10. M. Najmzadeh, D. Bouvet, W. Grabinski, A.M. Ionescu, **”Uniaxially tensile strained accumulation-mode gate-all-around Si nanowire nMOSFETs”**, IEEE DRC 2011 (the 69th IEEE Device Research Conference), Santa Barbara, California, USA, pp. 145-146, 20-22 June 2011 (poster).
11. M. Najmzadeh, K. Boucart, W. Riess, A.M. Ionescu, **”Asymmetrically strained all-silicon multi-gate n-Tunnel FETs”**, Solid State Electronics, vol. 54, pp. 935-941, 2010.
12. K. E. Moselund, M. Najmzadeh, P. Dobrosz, S. H. Olsen, D. Bouvet, L. De Michielis, V. Pott, A.M. Ionescu, **”The high-mobility bended n-channel silicon nanowire transistor”**, IEEE Transactions on Electron Devices, vol. 57, pp. 866-876, 2010.
13. M. Najmzadeh, L. De Michielis, D. Bouvet, P. Dobrosz, S. Olsen, A.M. Ionescu, **”Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs”**, Microelectronic Engineering, vol. 87, pp. 1561-1565, 2010.
14. M. Najmzadeh, L. De Michielis, D. Bouvet, P. Dobrosz, S. Olsen, A.M. Ionescu, **”Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs”**, MNE 2009 (the 35th international conference on Micro Nano Engineering), Ghent, Belgium, 28 Sep.-1 Oct. 2009 (oral).
15. M. Najmzadeh, D. Bouvet, P. Dobrosz, S. Olsen, A.M. Ionescu, **”Investigation of oxidation induced strain in a top-down Si nanowire platform”**, Microelectronic Engineering, vol. 86, pp. 1961-1964, 2009.
16. M. Najmzadeh, D. Bouvet, P. Dobrosz, S. Olsen, A.M. Ionescu, **”Investigation of oxidation induced strain in a top-down Si nanowire platform”**, INFOS 2009 (the 16th **biennial** conference on Insulating Films on Semiconductors), Cambridge, UK, 28 June-1 July 2009 (oral).
17. M. Najmzadeh, K. E. Moselund, P. Dobrosz, S. Olsen, A. O’Neill, A.M. Ionescu, **”Investigation of strain profile optimization in gate-all-around suspended silicon nanowire FET”**, IEEE ESSDERC 2008 (the 38th European Solid-State Device Research Conference), Edinburgh, Scotland, UK, 15-19 Sep. 2008 (poster).

Research highlights:

1. **Front cover of IEEE Transactions on Nanotechnology**, vol. 11, 2012 (impact factor 2011: 2.292).
2. **Special interest to the engineering community** paper selection (SSE 2012), Advances in Engineering, 2012.

- **Bridge resonator, Fluid-conveying Si microtubes:**

18. M. Najmzadeh, S. Haasl, P. Enoksson, **“A silicon straight tube fluid density sensor”**, Journal of Micromechanics and Micro-engineering, vol. 17, no. 8, pp. 1657-1663, 2007.
19. M. Najmzadeh, S. Haasl, P. Enoksson, **“Silicon straight tube fluid density sensor”**, IEEE Sensors 2007, Atlanta, USA, pp. 1185-1188, 28-31 Oct. 2007 (oral).