Local Volume Depletion/Accumulation in GAA Si Nanowire Junctionless nMOSFETs

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***Abstract*—In this paper, we report, for the first time, corner effect analysis in the gate-all-around equilateral triangular silicon nanowire (NW) junctionless (JL) nMOSFETs, from subthreshold to strong accumulation regime. Corners were found to accumulate and deplete more electrons than the flat sides or the channel center, when above (local accumulation) and below (local depletion) the flat-band voltage, respectively. On the contrary to the corner effect in the inversion mode (IM) devices, there is no major contribution of corners in the subthreshold current, and therefore, there is no subthreshold device behavior degradation (only one threshold voltage in the system). N-type channel doping levels of 1×10^{19}, 5×10^{18}, and 1×10^{18} cm^{-3} were used for quasi-stationary device simulations of JL and AM MOSFETs, and corner effect was studied for 5, 10, and 15 nm wide equilateral triangular Si NW MOSFETs with a 2 nm SiO_2 gate oxide thickness ($V_{DS} = 0$ V; $T = 300$ K). While the local quantum and classical electron density peaks are located in the corner regions above the flat-band voltage, reducing the channel doping and the channel cross-section was found to slightly suppress the normalized total accumulation electron density per unit length, $N_t^{acc}/(CW_{eff})$, in strong accumulation regime.**

***Index Terms*—Accumulation mode (AM), corner effect, gate-all-around (GAA), junctionless (JL), local accumulation, local depletion, quantum confinement, Si nanowire (NW), 3-D TCAD Sentaurus Device simulation.**

I. Introduction

MULTI-GATE architectures such as gate-all-around nanowires and FinFETs are promising candidates for aggressive CMOS downscaling, due to an almost optimized subthreshold slope, immunity against short channel effects, and optimized power consumption. Recently, highly and heavily single-type doped Si devices along the source–channel–drain, called accumulation mode (AM) and junctionless (JL), have been proposed [1], [2]. These devices present a simpler fabrication method to overcome some technical limitations of junction-based devices like ultra-abrupt junctions, which are issues for ultra short channel devices. The multi-gate architectures (except circular cross-sections that can be obtained by hydrogen annealing [3] or stress-limited oxidation [4]) have corners (e.g., see [5]–[9]). Therefore, an in-depth analysis of the corner effect on the electrical characteristics of the multi-gate devices is necessary. In this paper, we report, for the first time, corner effect analysis of the GAA Si NW JL nMOSFETs using a GAA equilateral triangular Si NW architecture (2 nm SiO_2 gate oxide thickness; $V_{DS} = 0$ V; $T = 300$ K). The corner effect analysis was done from subthreshold to strong accumulation, considering various channel doping levels (1×10^{18}–1×10^{19} cm^{-3}) and channel cross-sectional dimensions (5–15 nm Si NW width).

To make a clear corner effect study in GAA Si NW JL MOSFETs with minimized short channel effects on the device characteristics, 40 nm long channel architectures were used for the simulations (>6 times longer than the natural length of the widest NW; see, e.g., [10]). This is a first step to make a precise device and transport analysis in multi-gate JL architectures with short channel lengths including corners (see e.g., [11]). Note that various Si NW cross-sections can be experimentally achievable using bottom-up [12], [13] or Si NW sidewall engineering by anisotropic Si etching in top-down [6], [14] platforms. In this paper, we only concentrate on the equilateral triangular cross-sections, due to having the narrowest corner angle among the symmetrical architectures.

In this paper and as a first step, we investigate the corner effect through the local and total electron densities in the channel cross-section (with and without channel quantization) using a 15 nm wide Si NW MOSFET at various channel doping levels. Afterward, the effect of channel dimension shrinkage in a JL MOSFET at a fixed channel doping level will be studied in details.

II. Numerical Simulation

TCAD Sentaurus Device (G-2012.06) was used for the quasi-stationary numerical simulation of GAA Si NW MOSFETs. Considering electrostatic and quasi-Fermi potential equations, the local carrier densities in a 3-D structure can be extracted at each bias voltage. The electrostatic potential for the classic case is the solution of the nonlinear Poisson equation

$$\nabla \cdot (\epsilon \nabla \psi) = -q(-n + p + N_D^+) \quad (1)$$

where q, n, p, and N_D^+ are electron charge, electron density, hole density, and ionized donor concentration, respectively

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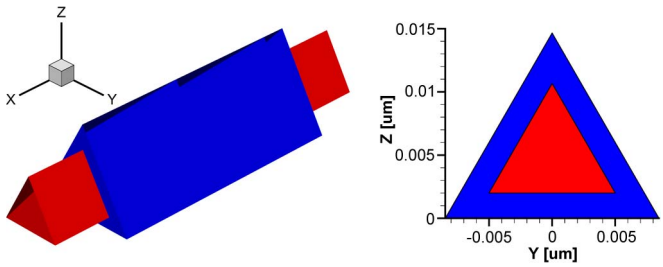

Fig. 1. Equilateral triangular GAA Si NW MOSFET and its cross-section.

(ionized acceptor concentration is neglected in our case). To include the 3-D quantization effects in nanoscale, the density gradient quantization model is coupled to the Poisson equation [15], [16]. The quantum correction procedure includes modification of the density of states [16]. The semi-classical Slotboom bandgap narrowing model was used for the highly and heavily doped Si channels [16], [17]. The local carrier densities can be computed from the electron and hole quasi-Fermi potentials, considering Fermi-Dirac statistics covering both degenerate and nondegenerate regimes [16].

Fig. 1 shows the 3-D GAA Si NW architecture, used for the device simulations (gate length: 40 nm; SiO_2 gate oxide thickness: 2 nm). The Si NW width is set to 15 nm (equilateral triangle), and three channel doping levels were investigated. The gate workfunction was set to 4.5 eV (a midgap workfunction). In all the simulations, $V_{\rm DS}$ was fixed at 0 V, to eliminate the effect of longitudinal electric field from source–drain potential difference on the local electron density distribution along the channel.

III. From Subthreshold to Strong Accumulation in a 15 nm Wide Si NW MOSFET

Quasi-stationary TCAD device simulation was done on a 15 nm wide Si NW MOSFET at three channel doping levels $(1 \times 10^{19}, 5 \times 10^{18},$ and 1×10^{18} cm$^{-3})$. The device characteristics can be studied using local electron density distribution in the channel at each gate voltage as well as charge on the gate versus gate voltage characteristics (Q_G–$V_{\rm GS}$, can be obtained directly from the simulations).

A. Operation of AM/JL MOSFETs

The JL and AM MOSFETs, unlike the typical inversion-mode (IM) MOSFETs, do not have any p-n junction, and the channel doping level is nominally determining the device type (heavily doped devices, $> 1 \times 10^{19}$ cm^{-3}, called JL) [1]. Both devices have the same operation mechanism, while here, we provide a brief explanation on this mechanism for a simple planar single-gate AM/JL nMOSFET.

Below the threshold voltage, the channel is fully depleted, while the majority of the subthreshold current is passing through the channel volume (the closer to the channel–dielectric interface, the more depletion). There can be different definitions of threshold voltage. Whereas a simple extrapolation was proposed in [18], in this paper, we will adopt a slightly different condition. Assuming a full depletion approximation, our threshold voltage condition can be approximated when creating a neutral region at the middle of the fully depleted channel (the corresponding local electron density almost equals the channel doping). The current passing through the neutral region is called bulk current. Applying a higher gate voltage extends the neutral region causing an increase in the bulk current.

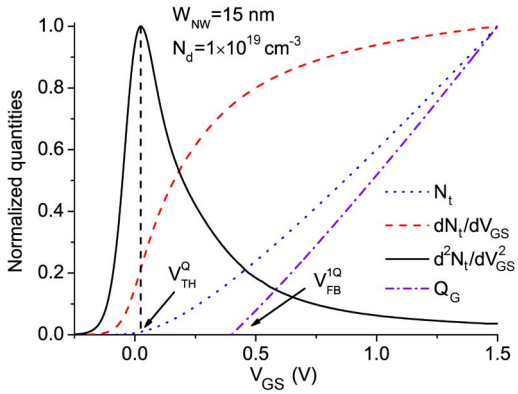

Fig. 2. Normalized quantities of N_t, $dN_t/dV_{\rm GS}$, $d^2N_t/dV_{\rm GS}^2$, and Q_G with respect to the maximum values versus $V_{\rm GS}$ for the GAA 15 nm wide Si NW MOSFET at 1×10^{19} cm^{-3} channel doping including quantum confinement. The maximum values for each parameter are 5.46×10^7 cm^{-1}, 4.48×10^7 cm$^{-1} \cdot$ V^{-1}, 1.29×10^8 cm$^{-1} \cdot$ V^{-2}, and 7.35×10^{-12} C $\cdot$ cm^{-1}, respectively.

The flat-band condition will be reached when the entire channel cross-section is neutral, implying that the bulk current will saturate at this point. Applying a higher gate voltage leads to the creation of an accumulation layer close to the channel-dielectric interface. Therefore, the drain current includes one fixed (saturated bulk current) and one variable (accumulation current) component. Note that the $V_{\rm FB}$–$V_{\rm TH}$ can be engineered by channel doping, gate oxide thickness, channel cross-sectional geometry, and dimension.

B. Threshold Voltage Extraction Method

The threshold voltage can be extracted from the peak of the second derivative of the total electron density per unit length (N_t) versus gate voltage [19] (similar to the transconductance change method [20]), while N_t can be calculated by integrating the electron density over the channel cross-section and at the middle of the channel ($x = L_G/2$; L_G equals gate length)

$$N_t = \int \int n(y, z)\, dy\, dz. \tag{2}$$

Fig. 2 shows the total electron density per unit length and the corresponding derivatives (normalized to the corresponding maximum values) for a GAA 15 nm wide Si NW MOSFET doped at 1×10^{19} cm^{-3}, including quantum confinement.

C. Flat-band Voltage Extraction Method

In a standard planar MOSFET, the flat-band voltage is the gate voltage for which the electrostatic potential is being constant in the entire channel cross-section. However, due to the quantum confinement, the flat-band condition cannot be reached in the entire channel cross-section for a certain gate

TABLE I
KEY DEVICE PARAMETER EXTRACTION FROM THE QUASI-STATIC DEVICE SIMULATIONS OF THE GAA 15 nm WIDE Si NW MOSFETs AT DIFFERENT CHANNEL DOPING LEVELS

N_d (cm^{-3})	V_{TH}^{C} (V)	V_{TH}^{Q} (V)	V_{FB}^{1C} (V)	V_{FB}^{1Q} (V)	V_{FB}^{C} (V)	V_{FB}^{Q} (V)	CW_{eff}^{Cmax} (F/cm)	CW_{eff}^{Qmax} (F/cm)
1×10^{18}	0.306	0.316	0.332	0.351	0.319	0.338	7.62×10^{-12}	7.11×10^{-12}
5×10^{18}	0.181	0.183	0.349	0.379	0.345	0.375	7.63×10^{-12}	7.14×10^{-12}
1×10^{19}	0.025	0.027	0.360	0.399	0.360	0.399	7.65×10^{-12}	7.16×10^{-12}

voltage when including corners. Nevertheless, we can still define an effective flat-band voltage for the entire channel cross-section (or *quantum flat-band voltage*) as a key device operation parameter which can be approximated from the x-intercept of the Q_G–V_{GS} curve as a first step (called V_{FB}^{1Q}), a direct output result from the presented gate charge–V_{GS} quasi-static simulations.

While the flat-band condition can be reached in the entire channel cross-section when discarding quantization, even in the corners, the observed slight difference between the actual flat-band voltage (V_{FB}^{C}) and the extracted one from the Q_G–V_{GS} curve for the classic case, $V_{FB}^{1C} - V_{FB}^{C}$, can be used to justify the flat-band voltage extraction method mismatch when quantum effects cannot be neglected. This slight inaccuracy, observed to be below a 13 mV range in Table I, is mainly due to the higher electron density in the channel parts close to the source and drain, as well as to the parameter extraction methodology. Based on this remark, we can estimate the effective flat-band voltage for the entire device (V_{FB}^{Q} or V_{FB}^{C}).

Note that the flat-band condition may not be reached in the entire channel cross-section even for the classic case. This could be due to some local effective bulk doping concentrations in the corners, as reported previously in the subthreshold regime of the IM devices to describe the local threshold voltage downshift in the corners [19], [21]. However, perhaps a much narrower corner angle is needed to significantly affect the local flat-band voltage variation between the corner and the side.

D. Gate–Channel Capacitance and Effective Channel Width

Due to the quantization-based gate–channel capacitance [22] and effective channel width shrinkages in GAA NWs, instead of extracting each parameter separately, the CW_{eff} parameter, the product of the gate-channel capacitance and the channel width, is introduced. This parameter can be extracted from the first derivative of the total electron density per unit length (N_t) versus the gate voltage in strong accumulation regime

$$CW_{eff}(V_{GS}) = (dN_t/dV_{GS}) \cdot q. \tag{3}$$

The CW_{eff}^{max} values, reported in Table I, are extracted at $V_{GS} = 1.500$ V for all structures.

E. Key MOSFET Parameters at Different Channel Doping Levels

Fig. 3 shows the second derivative of the total electron density per unit length (d^2N_t/dV_{GS}^2) versus V_{GS} for the GAA

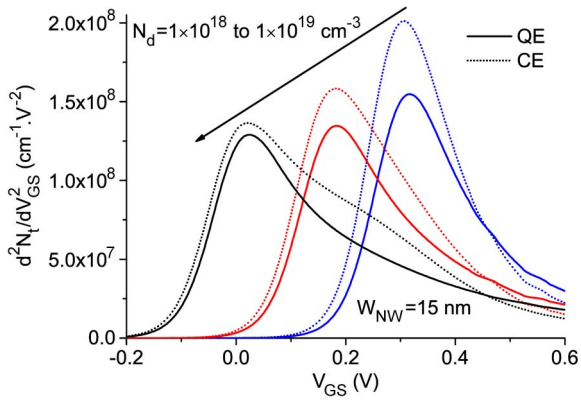

Fig. 3. d^2N_t/dV_{GS}^2 versus gate voltage for the GAA Si NW MOSFETs at various doping levels with or without quantization (QE or CE, respectively).

15 nm wide Si NW MOSFETs for three channel doping concentrations, considering classical and quantum effects. The results reported in Table I show that the quantization is upshifting both the threshold and the flat-band voltages, due to the higher quantized subband energies [9], [23], [24]. Note that, even for the heavily doped structure and on the contrary to the IM devices [19], there is no hump effect below the gate voltage corresponding to the main peak in the d^2N_t/dV_{GS}^2 versus V_{GS} curve, thus representing a unique threshold voltage in the system. The hump appearing above the threshold voltage of the heavily doped device in the classical simulation is due to the nonlinear operation of bulk regime between the threshold and the flat-band voltages as well as creation of accumulation conduction paths in the channel, reported before for the planar AM devices [2].

IV. LOCAL ELECTRON DENSITY DISTRIBUTION ACROSS THE CHANNEL FROM SUBTHRESHOLD TO STRONG ACCUMULATION

Figs. 4 and 5 show the quantum electron density (QED) and classical electron density (CED) in the cross-section of a GAA 15 nm wide Si NW JL MOSFET (channel doping: 1×10^{19} cm^{-3}) in subthreshold, above threshold, and strong accumulation regimes. According to the figures, the majority of electrons are accommodated in the corner regions only in strong accumulation. To study better the bias-dependent charge distribution mechanism in the channel cross-section, local QED and CED profiles as functions of gate voltage are plotted along $y = 0$ (see e.g., Fig. 4) in Fig. 6. This provides a wide range of information on the local electron density variation in the corner, side, and volume.

The maximum and minimum of the local CEDs in accumulation and depletion regimes are both occurring on the Si NW–dielectric interface, respectively. Therefore, a simple way to study the effect of corners on the local electron density variation can be the local CED corner to side ratio at different channel doping and gate voltages. Note that, due to the quantization effects, the peak of QED occurs inside the channel volume. Fig. 6 inset shows this classical ratio as a function of V_{GS}–V_{FB}. According to this figure (as well as from the local CEDs at different channel doping levels in Fig. 7),

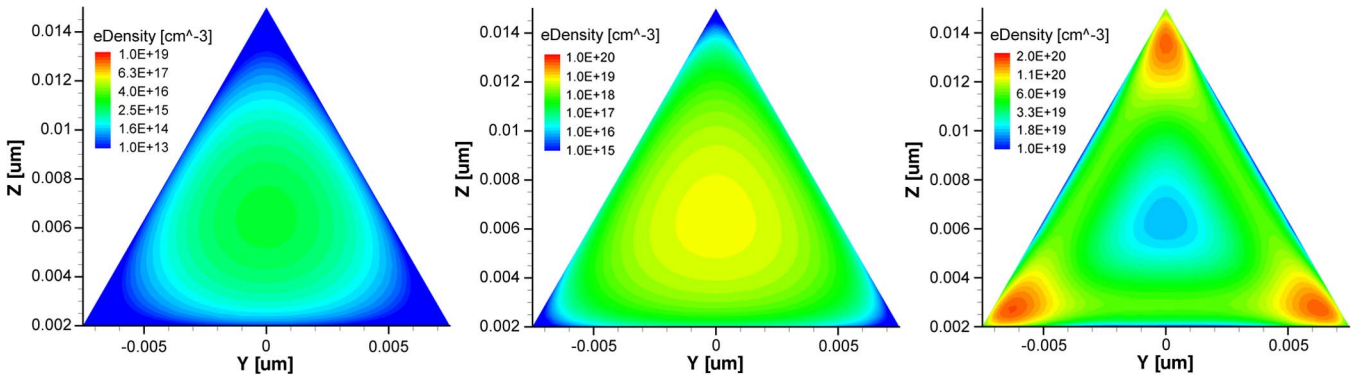

Fig. 4. Cross-sectional QED at the middle of a GAA 15 nm wide Si NW JL MOSFET for three operation regimes (oxide is not shown; channel doping: 1×10^{19} cm^{-3}). (Left) Subthreshold ($V_{\rm GS} = -0.200$ V). (Center) Above threshold ($V_{\rm GS} = 0.100$ V). (Right) Strong accumulation ($V_{\rm GS} = 1.500$ V). Note that $V_{\rm TH}^{Q} = 0.027$ V and $V_{\rm FB}^{Q} = 0.399$ V.

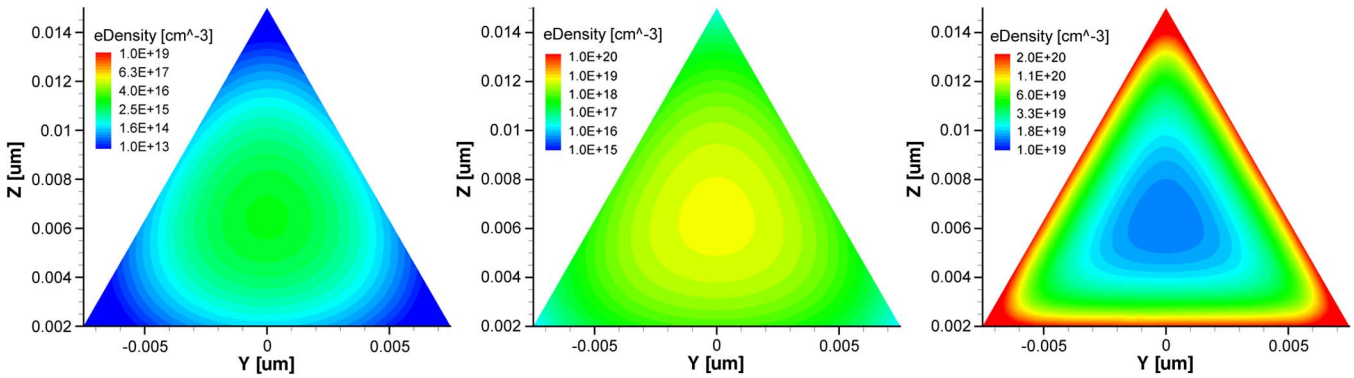

Fig. 5. Cross-sectional CED at the middle of a GAA 15 nm wide Si NW JL MOSFET for three operation regimes (oxide is not shown; channel doping: 1×10^{19} cm^{-3}). (Left) Subthreshold ($V_{\rm GS} = -0.200$ V). (Center) Above threshold ($V_{\rm GS} = 0.100$ V). (Right) Strong accumulation ($V_{\rm GS} = 1.500$ V). Note that $V_{\rm TH}^{C} = 0.025$ V and $V_{\rm FB}^{C} = 0.360$ V.

corners accumulate more electrons in comparison to the side in accumulation regime ($> V_{\rm FB}$), while they deplete also further below the flat-band voltage.

A. *Origin of Local Depletion/Local Accumulation in AM/JL MOSFETs*

The different corner effects and device behavior in the IM and the AM/JL MOSFETs come from a distinct conduction mechanism, surface versus volume conduction in different regimes, as well as conduction of minority versus majority carriers. Analyzing the effect of corners on the carrier density distribution in the channel cross-section is not simple. According to the simulations, it strongly depends on the channel geometry, doping level, and dielectric thickness (see e.g., [19], [25]–[27]). There is no clear geometrical definition of the corner region, while the analysis becomes even more complex including quantization.

The surface conduction by minority carriers is the only conduction mechanism in the IM devices, while the AM/JL MOSFETs exhibit surface conduction above $V_{\rm FB}$ and volume conduction below $V_{\rm FB}$, both involving majority carriers. Due to having a maximized surface to volume ratio in the corner region in comparison to the side region, the surface conduction mechanisms (above $V_{\rm FB}$ for the AM/JL, all operation regimes for the IM devices) should provide a higher local mobile charge density in the corner region (local volume inversion or local volume accumulation in the IM and the AM/JL devices, respectively). On the other hand, reduction of the local effective channel doping in the corners because of side gates and the effective body thickness reduction in the corners were suggested previously to describe the local threshold voltage downshift and the local volume inversion in the corners of the IM devices in subthreshold regime as well [21].

Due to having a smaller effective channel body thickness in the corner region in comparison to the side, the volume conduction mechanism in the corner region is expected to be minimized with respect to the side region below the flat-band voltage, since the volume of corner is negligible. Therefore, no subthreshold conduction path in the corner regions of the AM/JL MOSFETs is expected to emerge from I_D–$V_{\rm GS}$ characteristics, as already observed in Fig. 3 (no hump below the main peak of the $d^2N_t/dV_{\rm GS}^2$ versus $V_{\rm GS}$ curves).

B. *Corner Effects on Global Accumulation Electron Densities in Accumulation Regime*

To assess corner effects on the global device characteristics, the normalized total accumulation electron density per unit length in the entire channel cross-section is defined as ($V_{\rm GS} > V_{\rm FB}$)

$$N_t^{\rm acc}(V_{\rm GS}) = N_t(V_{\rm GS}) - N_t(V_{\rm FB}). \tag{4}$$

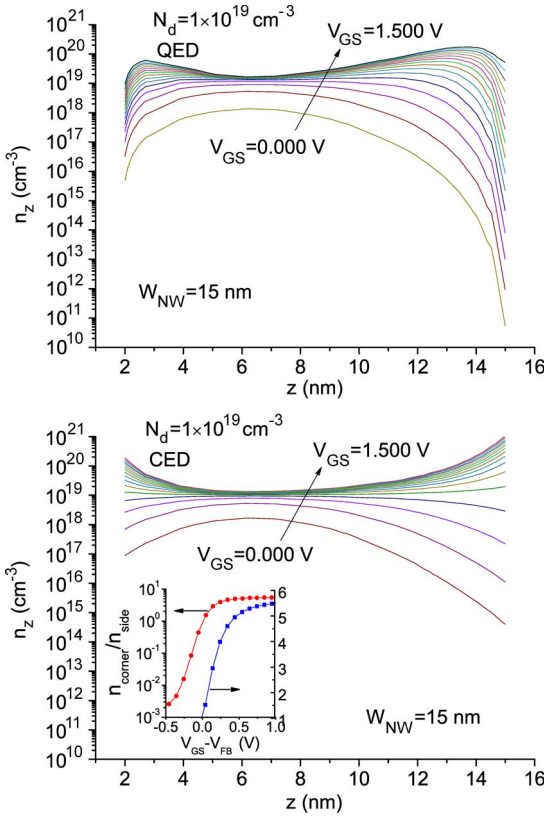

Fig. 6. Local (top) QED and (bottom) CED profiles across the 15 nm wide NW channel volume at different $V_{\rm GS}$ values (from subthreshold to strong accumulation; step: 0.100 V) at $N_d = 1 \times 10^{19}$ cm^{-3} (cut at $y = 0$; see e.g., Fig. 4). The inset shows local CED corner to side ratio from subthreshold to strong accumulation.

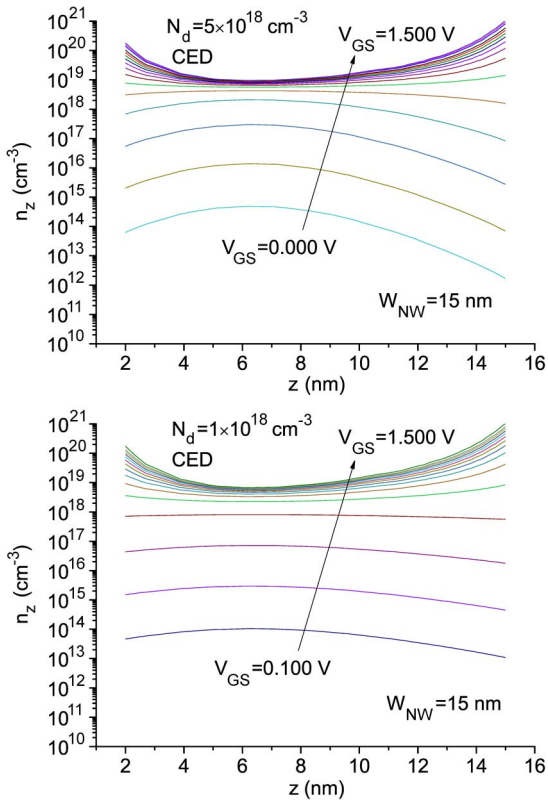

Fig. 7. Local CED profiles across the 15 nm wide Si NW channel volume at different gate voltages (from subthreshold to strong accumulation; step: 0.100 V) for (top) $N_d = 5 \times 10^{18}$ cm^{-3} and (bottom) 1×10^{18} cm^{-3}. The plots correspond to the cut at $y = 0$.

Fig. 8 shows how this normalized accumulation electron density varies with respect to the gate voltage for the 15 nm wide Si NW MOSFETs, with three different channel doping levels at $V_{\rm GS} > V_{\rm FB}$. In order to study the effect of quantization and channel cross-sectional variation for various devices, accumulation electron densities are normalized to $\mathrm{CW}_{\rm eff}(V_{\rm GS})$ at each bias voltage (see also Section V-A). According to Fig. 8, the normalized total accumulation electron density above the flat-band voltage is increasing with the channel doping, while all the normalized values are slightly below the ideal limit that can be calculated as follows:

$$N_t^{\rm acc}(V_{\rm GS})/\left[\mathrm{CW}_{\rm eff}(V_{\rm GS})\right] = (V_{\rm GS} - V_{\rm FB})/q. \qquad (5)$$

Therefore, corners clearly cannot be considered as CMOS boosters. Note that the local CED corner to side ratio is increasing by channel doping reduction in accumulation regime (Fig. 8 inset). On the other hand and from Fig. 8, heavily doped structures represent a higher normalized total accumulation electron density per unit length and reveal characteristics closer to the ideal case, reflecting a more uniform distribution of the local electrons in the cross-section. This could be explained by electrostatic screening increase at higher doping levels in accumulation regime. In all cases, the normalized total accumulation electron density per unit length is slightly degraded by quantum confinement as well.

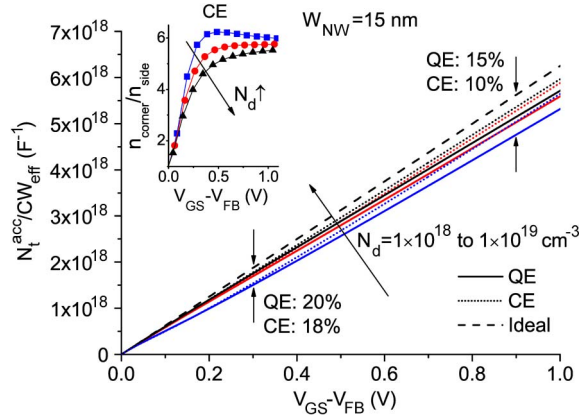

Fig. 8. Normalized total accumulation electron density per unit length versus $V_{\rm GS}$–$V_{\rm FB}$ at various channel doping levels including both quantum and classical electrons. The normalization factor is $\mathrm{CW}_{\rm eff}(V_{\rm GS})$. The inset shows local CED corner to side ratios in accumulation regime.

V. Cross-Sectional Shrinkage and Corner Effect

In this section, GAA equilateral triangular Si NW MOSFETs with 5 and 10 nm NW widths were simulated at a 1×10^{19} cm^{-3} channel doping level (2 nm SiO_2 gate oxide thickness). The second derivative of N_t ($d^2N_t/dV_{\rm GS}^2$) versus gate voltage curves are plotted in Fig. 9, and the extracted device parameters are reported in Table II (the

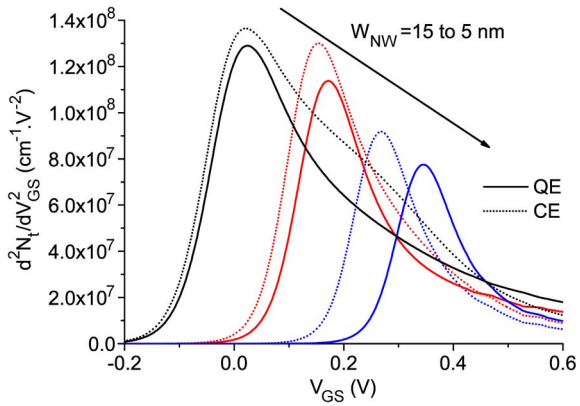

Fig. 9. $d^2N_t/dV_{\rm GS}^2$ versus gate voltage for the GAA Si NW MOSFETs for various NW widths doped at $N_d = 1 \times 10^{19}$ cm^{-3}, including both (QE) quantum and (CE) classical electrons.

TABLE II
KEY DEVICE PARAMETER EXTRACTION FROM THE QUASI-STATIONARY DEVICE SIMULATIONS OF THE GAA Si NW MOSFETs WITH VARIOUS NW WIDTHS, ALL AT $N_d = 1 \times 10^{19}$ cm^{-3}

W_{NW} (nm)	V_{TH}^{C} (V)	V_{TH}^{Q} (V)	V_{FB}^{1C} (V)	V_{FB}^{1Q} (V)	V_{FB}^{C} (V)	V_{FB}^{Q} (V)	CW_{eff}^{Cmax} (F/cm)	CW_{eff}^{Qmax} (F/cm)
5	0.267	0.344	0.360	0.447	0.360	0.447	2.86×10^{-12}	2.66×10^{-12}
10	0.153	0.171	0.360	0.408	0.360	0.408	5.25×10^{-12}	4.94×10^{-12}
15	0.025	0.027	0.360	0.399	0.360	0.399	7.65×10^{-12}	7.16×10^{-12}

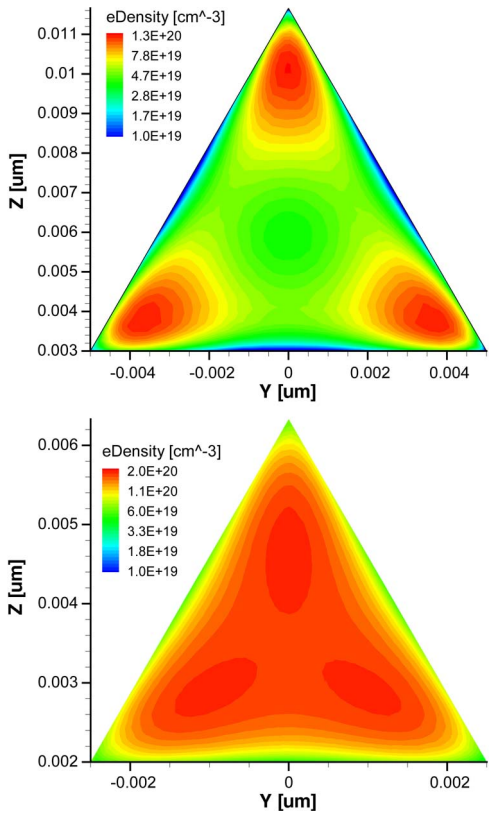

Fig. 10. Cross-sectional QED at the middle of a GAA Si NW JL MOSFET in strong accumulation regime ($V_{\rm GS} = 1.500$ V) for (top) 10 and (bottom) 5 nm wide Si NW MOSFETs at $N_d = 1 \times 10^{19}$ cm^{-3}.

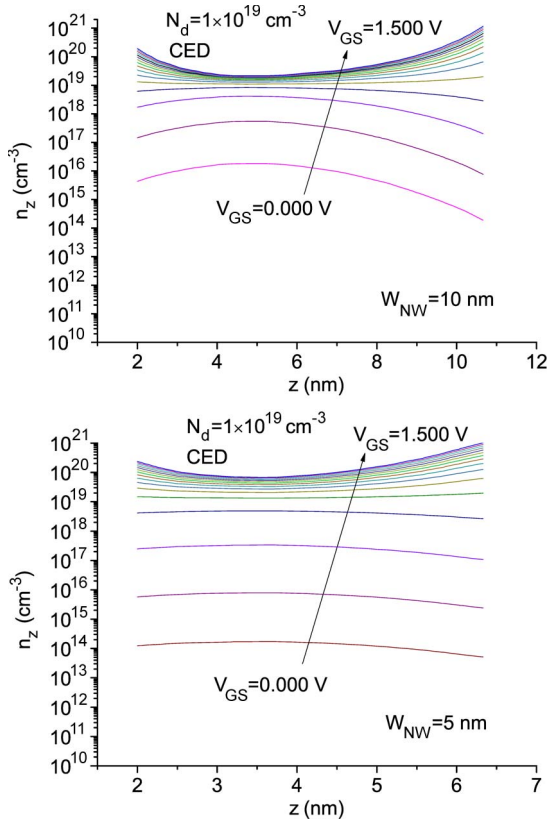

Fig. 11. Local CED profile across the Si NW channel volume at different gate voltages (from subthreshold to strong accumulation; step: 0.100 V) for (top) 10 and (bottom) 5 nm wide Si NW MOSFETs at $N_d = 1 \times 10^{19}$ cm^{-3}. Plots correspond to the cut at $y = 0$.

15 nm wide NW with a similar doping is added from Table I for comparison). No hump exists below the threshold voltage, while the one above the threshold voltage for the classical simulation disappears by cross-sectional shrinkage as well, mainly due to the reduction of bulk conduction regime ($V_{\rm FB}$–$V_{\rm TH}$).

A. Local Electron Density for Various Cross-Sectional Dimensions

Fig. 10 shows the cross-sectional local electron density distribution in the channel with quantization for 10 and 5 nm wide Si NW JL MOSFETs in strong accumulation ($V_{\rm GS} = 1.500$ V). Significant charge redistribution in the 5 nm wide NW cross-section, which can be called *volume accumulation*, in comparison to the wider ones together with 77 and 87 mV upshifts in the threshold and the flat-band voltages, respectively, are the typical quantization effects in such scaled 1DEG architectures. The local CED profiles along $y = 0$ are plotted in Fig. 11 for both devices at different $V_{\rm GS}$ values. According to Fig. 12, the normalized total accumulation electron density per unit length becomes closer to the ideal limit for the wider structures. This corner effect is pretty close to the one occurring in the IM devices, simply due to less contribution of the corner regions on the electrostatics in the entire channel cross-section and less quantization effects for wider structures.

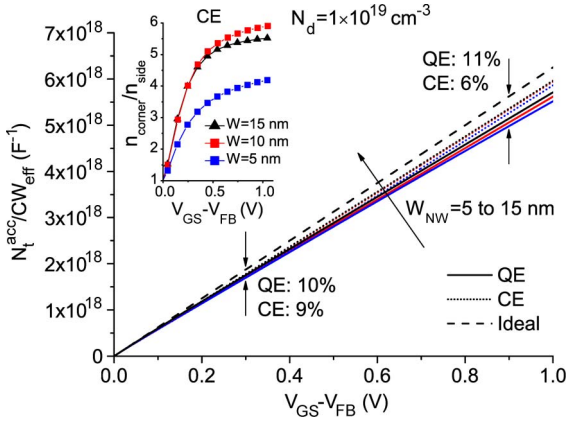

Fig. 12. Normalized total accumulation electron density per unit length versus $V_{\rm GS}$–$V_{\rm FB}$ at various NW cross-sectional dimensions including both quantum and classical electrons. The normalization factor is $\mathrm{CW_{eff}}(V_{\rm GS})$. The inset shows local CED corner to side ratios in accumulation regime.

VI. Conclusion

In this paper, we have reported corner effect study in the single-type doped (AM and JL) GAA equilateral triangular Si NW nMOSFETs for the first time. In the IM MOSFETs, the corners slightly degrade the subthreshold behavior due to the parasitic corner conductions below the threshold voltage. Therefore, the typical well-known corner effect (local threshold voltage downshift in the corners and, therefore, increased OFF current) is suppressed completely using AM and JL architectures by having a unique threshold voltage in the system. On the other hand, the corners cannot be classified as CMOS boosters (e.g., stressors), due to having a normalized total accumulation electron density per unit length [normalization factor: $\mathrm{CW_{eff}}(V_{\rm GS})$] slightly below the ideal MOSFET limit, even having a higher local charge accumulation in the corner regions in comparison to the side regions above flat-band.

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