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Ambipolar silicon nanowire FETs with stenciled-deposited metal gate

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ABSTRACT

We report on a fully CMOS compatible fabrication method for ambipolar silicon nanowire FinFETs. The low thermal budget processing, compatible with monolithic 3D device integration, makes use of low pressure chemical vapor deposition (LPCVD) of amorphous Si (a-Si) and SiO_2 layers as well as metal gate patterning using stencil lithography, demonstrated for the first time. FinFETs with stenciled Al gates are successfully co-fabricated with polycrystalline silicon Ω-gated devices. Stencil lithography is envisaged as a key enabler for gate patterning on 3D structures, such as vertically stacked nanowire transistors.

1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures or different state variables other than charge [1]. All these approaches will lead to significant modifications of the traditional planar transistor design. Considering novel device structures, the nanowire (NW) channel transistor with FinFET construction has been demonstrated to be one of the best in terms of electrostatic control, thus enabling further device scaling [2]. Another example can be the monolithic 3D integration, a process integration scheme that achieves higher device density by stacking p-type FETs on top of n-type FETs [3]. In terms of state variables, one example is given by device ambipolarity. The ambipolar property can be described by the presence of two high conductance states for the same FET, each of these related to carriers of opposite charge values [4]. Preliminary works on device ambipolarity show how it can be used to compute more complex logic functions per chip [5]. However, in terms of process integration, a few technologies have the flexibility to be implemented within 3D integration schemes and, at the same time, offer the ambipolar property with good CMOS compatibility and electrical performance.

We report on a fully CMOS compatible fabrication of ambipolar SiNW FinFETs by means of amorphous Si (a-Si) and low temperature oxide (LTO) deposited with low pressure chemical vapor deposition (LPCVD) technique. FinFETs with stenciled Al gates are successfully co-fabricated with polycrystalline Si (pc-Si) gated devices achieving excellent performance. The difficulty of achieving high resolution gate patterning on non-planar devices is addressed for the first time by means of stencil metal deposition [6]. We envisage the use of this technique also for metal patterning on high aspect ratio FETs, such as vertically stacked nanowire transistors [7]. It is worth noting that this process can be repeated several times, eventually being used for monolithic 3D integration.

In Section 2 we present the fabrication steps to build the devices. Then in Section 3 the fabricated structures are shown and described. In Section 4 we describe the electrical behavior of the two types of FinFETs fabricated and on the pseudo-inverter operation of pc-Si FinFETs. Finally, in Section 5 we draw the conclusions.

2. Process flow

The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500 nm thick wet oxide and a 100 nm LTO layer. Then a 100 nm a-Si film is deposited as the active layer. A 70 nm thick dilution of hydrogen silsesquioxane (HSQ) is spin coated and patterned with e-beam lithography. Lines having widths ranging from 70 nm to 250 nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip buffered hydrofluoridric acid (BHF) step. The obtained a-Si nanowires are then covered by a 40 nm dry oxide and a 50 nm LPCVD pc-Si layers. Large 100 μm × 100 μm pc-Si pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, pc-Si Ω-gated FinFETs with gate lengths between 1 μm and 10 μm are obtained.

Then a bi-layer of 20 nm Ti/55 nm Ni is patterned with lift-off to form electrical contacts between the Si nanowires and the pads. A 400 °C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been

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chosen for its mid-gap work function and for its use in a-Si metal induced recrystallization process [8]. The fabrication flow is completed by the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100 nm thick SiN membranes with apertures having widths between 100 nm and 1 μm [9]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2 μm [9] accuracy using a customized SUSS MA/BA 6 mask aligner [10]. The clamped substrate–stencil setup is placed in an evaporator where 100 nm thick Al gates are deposited.

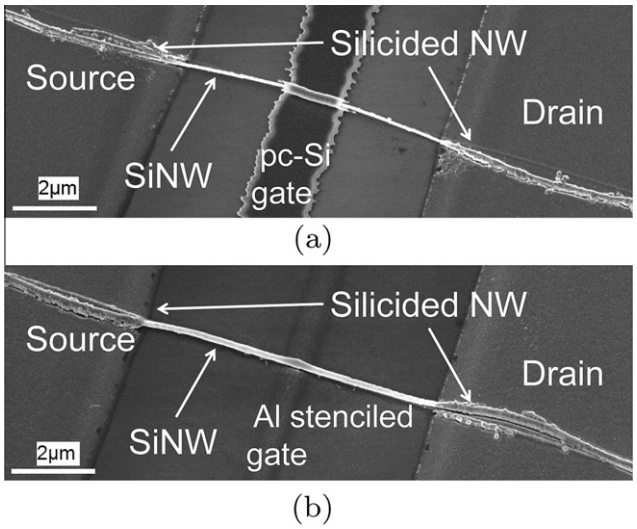

Fig. 1. FinFETs with silicide nanowire portions at source/drain contacts: (a) pc-Si FinFET having 2 μm long gate and 60 nm × 65 nm channel cross-section. (b) Al stenciled FinFET having 700 nm gate length and 60 nm × 140 nm channel cross-section.

3. Fabricated structures

FinFETs and inverters with up to 62 μm nanowire length were fabricated. An example of a 2 μm long pc-Si gate FinFET having 100 nm × 65 nm Si nanowire channel is shown in the SEM tilted view of Fig. 1(a). In Fig. 1(b), a Si nanowire transistor with 130 nm × 65 nm channel (see Fig. 2(d)) cross-section and 700 nm large stenciled Al gate is shown. Focused ion beam (FIB) cross-sections (see Fig. 2(a)–(c)) demonstrate nanowire channels sections having widths between 65 nm and 130 nm. The total Si thickness is reduced from the initial value of 100 nm to 65 nm due to processing. Narrower nanowires (the expected nanowire size was around 35 nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

4. Electrical measurements and discussion

The I_{ds}—V_{gs} curve of a pc-Si Ω-gate FinFET has a typical ambipolar behavior, with a higher conductance for holes (at negative V_{gs} voltages) than for electrons (Fig. 3(a)). In the holes-conductance regime, a subthreshold slope SS ≈ 420 mV/dec is observed, while a larger SS is observed for the electron-dominated current. The gate misalignment error is source of variation for the channel series

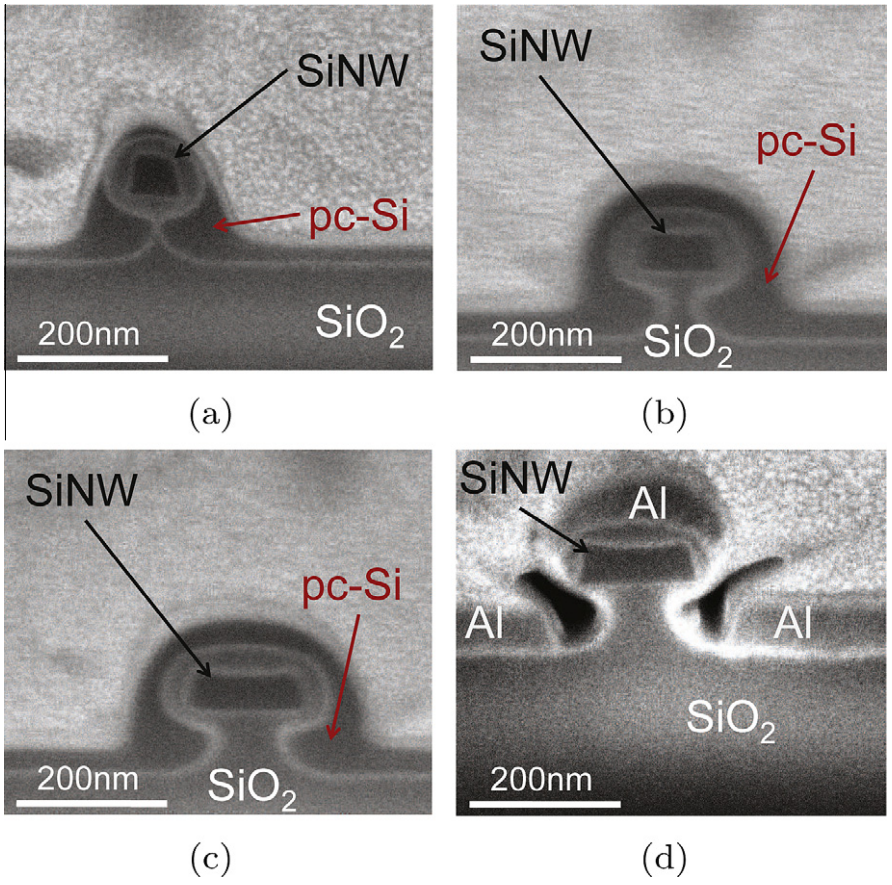

Fig. 2. FIB cross-sections showing the nanowire channels embedded in 40 nm oxide and gate materials: (a) pc-Si Ω-gate FinFET with 60 nm × 65 nm section. (b) pc-Si Ω-gate FinFET with 60 nm × 110 nm section. (c) pc-Si Ω-gate FinFET with 60 nm × 140 nm section. (d) Al stenciled-gate FinFET with 60 nm × 140 nm section.

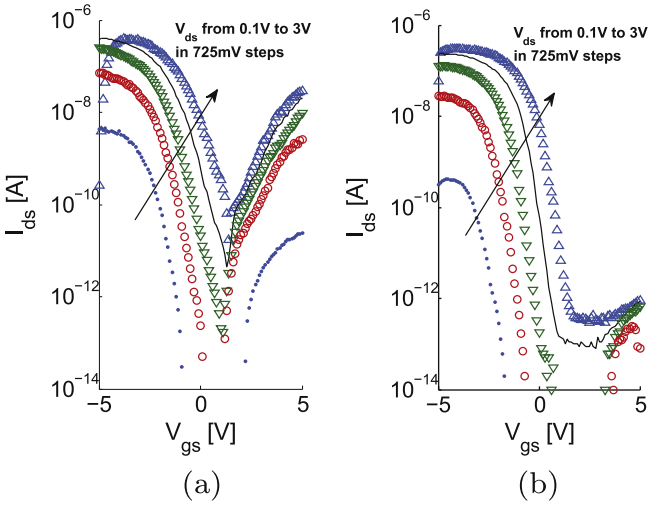

Fig. 3. (a) Ambipolar I_d–V_g curve of a pc-Si Ω-gated FinFET having 1 μm gate length and 60 nm × 110 nm nanowire section. (b) Ambipolar I_d–V_g curve of a stenciled Al-gate FinFET having 1 μm gate length and 60 nm × 110 nm nanowire section.

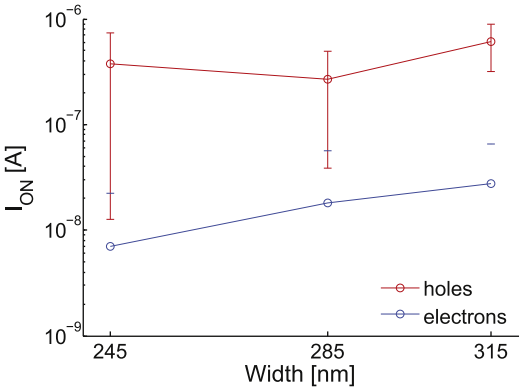

Fig. 4. Average I_{ON} for holes and electrons of pc-Si Ω-gated FinFETs of different widths. The error bar represents the standard deviation over a sample of eight devices.

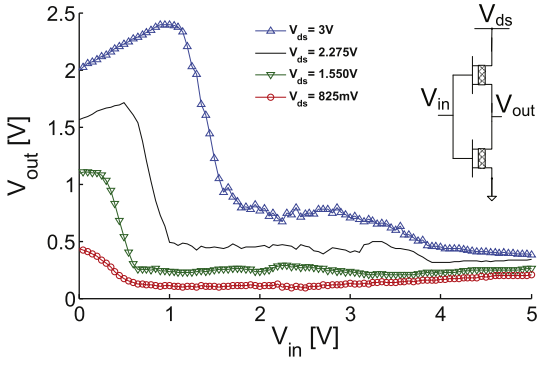

Fig. 5. Voltage transfer characteristic of a 2 in series connected pc-Si Ω-gate FinFETs on-a-wire and biased as for inverter operation. The insets represent the inverter bias scheme. Two ambipolar pc-Si FinFETs are connected in series.

resistance which in turn impacts the overall current conductance. Nevertheless, the main limiting factor for the current conductance is the injection of carriers over the Schottky barrier, and the series resistance is considered to play a minor role. This aspect is

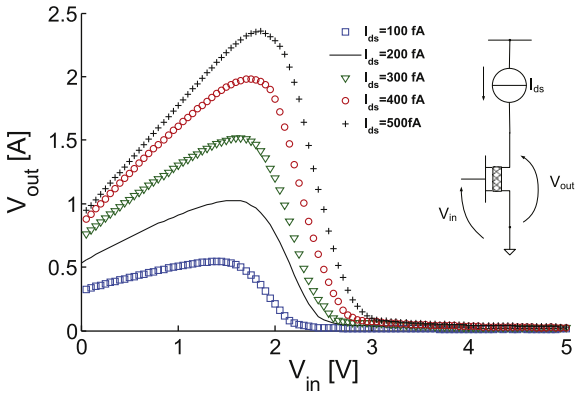

Fig. 6. pc-Si FinFET biased for pseudo-inverter operation having 2 μm gate lengths and 60 nm × 110 nm channel cross-section. The insets show the pseudo-inverter bias scheme using a single pc-Si FinFET and a current source.

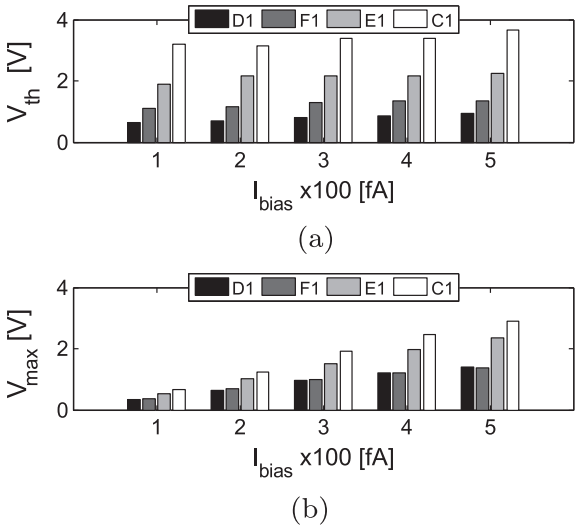

Fig. 7. (a) Threshold voltage (V_{th}) values for the pc-Si gated pseudo-inverters. The inversion voltages are stable under different current bias. (b) Maximum output voltages values for the pc-Si gated pseudo-inverters. The V_{max} values tend to increase linearly with I_{bias}.

confirmed by the observation of a lower I_{ON} for electrons than holes over a large number of samples. In Fig. 4, the average I_{ON} for holes and electrons is shown. The I_{ON} increase linearly with the channel width, which is calculated as the perimeter of the SiNW, since volume inversion effect are negligible for SiNW-channel diameters larger than 10 nm.

Conversely, Al-gated devices show a p-type conductance mainly (see Fig. 3(b)), which can be explained with Al contamination at pad regions due to the stencil process. This is also reflected in a SS ≈ 200 mV/dec, indicating that doping can effectively be used to improve SS by suppressing the ambipolar conductance. In both devices, I_{ON}/I_{OFF} ratios of more than six orders of magnitude are observed. The lower current for the *n*-branch in the Al gated devices might be due to metal gate-induced doping. The transfer characteristic of pc-Si Ω-gate inverters show (Fig. 5) an output voltage range V_{out} compatible with the input voltage range and a gain of $\Delta V_{out}/\Delta V_{in} \approx 4$. Thus, pc-Si gated inverters are suitable elements for cascading additional devices, enabling the construction of more complex circuits. Similarly, a current bias scheme for FinFETs can be used to obtain pseudo-inverter operation, which consist in using a current bias scheme as depicted in Fig. 6. For pseudo-inverter operation a triangular voltage transfer

characteristic is obtained, with very low power consumption ($\leqslant$1.2 pW). Data from different dies on the wafer show stability of the V_{in} value for which inversion occurs (V_{th}) under different current bias (see Fig. 7(a)). Moreover, as it is shown in Fig. 7(b), the maximum of V_{out} increases linearly with the current bias. Al gated inverters and pseudo-inverters are currently under investigation.

5. Conclusions

A fully CMOS compatible fabrication flow using low temperature a-Si LPCVD and stencil lithography has been developed and proved suitable for SiNW FinFETs having ambipolar conductance. Nanowires with up to 62 μm length with two separate gates have been successfully fabricated, giving space for complex circuit design. Moreover, the stencil lithography has been demonstrated for the first time as a suitable technique for metal gate patterning on 3D nanowire structures. The excellent performance of individual FinFETs and preliminary data of inverter functionality pave the way for the fabrication of more complex Si nanowire FinFET circuits. Further characterization of Al stenciled inverters and fabrication on high aspect ratio structures is envisaged as natural continuation of this work.

Acknowledgments

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