Process/Design Co-optimization of Regular Logic Tiles for Double-Gate Silicon Nanowire Transistors

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***Abstract*—**
Ambipolar transistors with on-line configurability to n-type and p-type polarity are desirable for future integrated circuits. Regular logic tiles have been recognized as an efficient layout fabric for ambipolar devices. In this work, we present a process/design co-optimization approach for designing logic tiles for *double-gate silicon nanowire field effect transistors* (DG-SiNWFET) technology. A compact Verilog-A model of the device is extracted from TCAD simulations. Cell libraries with different tile configurations are mapped to study the performance of DG-SiNWFET technology at various technology nodes. With an optimal tile size comprising of 6 vertically-stacked nanowires, we observe 1.6x improvement in area, 2x decrease in the leakage power and 1.8x improvement in delay when compared to Si-CMOS.

I. Introduction

As we advance into the era of nanotechnology, the semiconductor devices are scaled down to their physical and economic limits. In this nanometer regime, most of the devices exhibit ambipolar behavior. While technologists target to suppress the ambipolar behavior of the devices, new design methodologies are proposed by designers for exploiting the phenomenon of controllable ambipolarity [11].

An ambipolar device exhibits simultaneously n- and p-type characteristics. By engineering the source and drain contacts and by constructing independent double-gate structures, the device polarity can be electrostatically forced to either n- or p-type by polarizing one of the two gates. The in-field polarizability of a device enables the development of new logic architectures, which are intrinsically not implementable in CMOS in a compact form [5][11].

While such devices were demonstrated using carbon electronics [6], they suffer from the lack of maturity of the bottom-up fabrication processes. In this work, we propose the use of vertically-stacked *silicon nanowire field effect transistors* (SiNWFETs) as they are a promising extension to the tri-gate FinFETs. The ambipolar behavior of the SiNWFET can be controlled by realizing an independent second gate, forming a *double-gate* SiNWFET (DG-SiNWFET). The presence of an extra gate, called the *polarity Gate* (PG), for each and every transistor, adds to the routing complexity of the basic standard gates. Hence, specific device organization is required to enable the design of novel nano-architectures based on ambipolar logic gates.

Regularity is one of the key features required to increase the yield of integrated circuits at advanced technology nodes [21], while keeping the routing complexity under control. Hence, design styles based on regular layout fabrics have the advantage of higher yield as they maximize the layout manufacturability. Various regular fabrics have been proposed throughout the evolution of semiconductor industry, where some recent approaches are discussed in [7][17][20]. On the other hand, strict design rules, at 22nm technology node and beyond, have led to cell layouts with arrays of gates with a constant gate pitch, which resemble a sea-of-gates layout style.

A regular logic tile, that has an array of prefabricated transistor-pairs grouped together, was presented as an optimal layout fabric for ambipolar SiNWFET [1]. A desired logic function can be mapped onto an array of logic tiles, called *Sea-of-Tiles* (SoT). Bobba *et al.* proposed SoT design methodology for finding efficient logic tiles for DG-SiNWFET technology. Ambipolar circuits designed with regular logic tiles improves the overall yield, and forms a fundamental building block for novel architectures based on ambipolar logic [22][5]. However, since a unique tile is replicated in the SoT approach, correct tile sizing is crucial for the overall circuit performances.

As a main contribution of this work, we present a process/design co-optimization approach for sizing the tiles with respect to the number of vertically-stacked *Silicon Nanowires* (SiNWs) and study the performance at the architectural level. Prospective performance of the SiNWFET with varying SiNW stacks is extracted by TCAD model of the devices and used to characterize various cell libraries. Benchmark circuits are mapped onto SoT to compare the performance (*timing*, *leakage power* and *area*) of logic tiles with varying SiNWs (vertically stacked) to traditional CMOS at various technology nodes. When compared to Si-CMOS, averaged across various benchmark circuits, we observe 1.6x improvement in area, 2x decrease in the leakage power and 1.8x improvement in delay.

The remainder of this paper is organized as follows. In Section 2, we present our DG-SiNWFET technology for realizing ambipolar logic gates. We characterize its expected performances by TCAD simulations and build a basic compact model. In Section 3, we introduce regular logic tiles for SiNWFETs and present the optimal tile for our architectural study. Section 4 explains our design flow and the experimental setup. Architectural study is explained in Section 5 followed by conclusion in Section 6.

II. COMPACT MODEL OF AN AMBIPOLAR DG-SINWFET

In this section, we showcase the viability of ambipolar logic circuits realized with DG-SiNWFETs. In order to obtain an efficient DG-SiNWFET, device optimization is done using *technological computed aided design* (TCAD) simulation. A compact *Verilog-A* model of the device is derived for studying the circuit level implications of ambipolar circuits.

A. Technology Background

FinFET transistors are successfully replacing planar CMOS transistors beyond 22nm technology node [4]. Following the trend to *one-dimensional* (1-D) structures, SiNWFETs are a promising extension to the tri-gate FinFETs [19]. The superior performance of these 1-D channel devices comes from a high *Ion*/*Ioff* ratio, due to the gate-all-around structure, which improves the electrostatic control of the channel, thereby reducing the leakage current of the device. The advantage of SiNWFETs over other one-dimensional devices such as carbon nanotube transistors is that SiNWs can be fabricated with a top-down silicon process [10]. Moreover, SiNWs can be built in vertical stacks, thereby giving highly dense array of nanowire transistors [18]. Figure 1(a, b) illustrates a possible extension of a FinFET to SiNWFET device structure with SiNWs suspended between source and drain pillars.

In addition, SiNWFET exhibit enhanced electrostatics properties, such as polarity control, which are electrically impossible for planar- and FinFETs. Figure 1c illustrates a *double gate* (DG) SiNWFET device structure with *control gate* (CG) and *polarity gate* (PG). DG-SiNWFET can be built to be ambipolar, thereby exhibiting both n- and p- type characteristics. This SiNW is divided into three sections, which are in turn polarized by two gate-all-around gate regions. The center gate region works as in a conventional MOSFET, switching conduction in the device channel by means of a potential barrier. The side regions are instead polarized by a polarity gate, which controls Schottky barrier thicknesses at the S/D junctions and selects the majority carrier type, thus forcing the device to be either n- or p-type. The circuit symbol of the device along with the dumbbell-stick diagram is shown in Fig. 1(d, e).

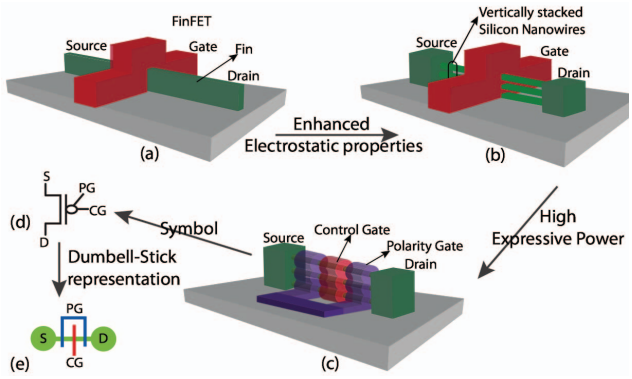

Figure 1. (a) FinFET providing increase in controllable channel area between the source and drain regions (b) Vertically-stacked SiNWFET with multiple parallel nanowire channels, each with Gate-All-Around (GAA) control (c) Double-Gate SiNWFET with control and polarity gates (d) Circuit symbol of DG-SiNWFET (e) Dumbell-stick representation of the device.

B. TCAD model of the Device

A single silicon nanowire with 45nm gate length is simulated using Synopsys Sentaurus. Metal gates with mid-gap work function are used on the HfO_2 high-k dielectric layer as shown in Fig 2. The Schottky barrier height for electron is set to around 0.36eV (i.e. 0.74eV for holes) in the simulation, which is achievable in actual process by using barrier height modulation technology, such as selective phase modulation of NiSi [8] or interfacial dielectric dipole [2]. The symmetric characteristics obtained from TCAD simulation are demonstrated in Fig 3. The device is simulated based on hydrodynamic transport and density gradient quantization models. Both barrier-tunneling and barrier-lowering models are activated at source and drain terminals. V_{CG} and V_{PG} are swept from 0 to +2V with fixed V_{DS} at +2V. The voltage level can be further reduced by band gap engineering.

For symmetric NMOS and PMOS characteristics, Schottky barrier height for holes is higher than the height for electrons due to the barrier narrowing for holes induced by drain voltage. Meanwhile, the lower barrier for electrons and the narrower barrier for holes can also provide larger on-state current. In order to further improve the performance, the silicide contacts should locate close enough to the gate-controlled region, and spaces between central gate and polarity gates are helpful for reducing the off-state leakage.

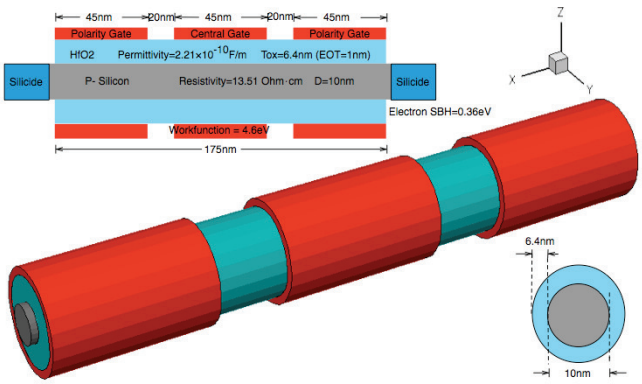

Figure 2. The schematic of the ambipolar silicon nanowire used in TCAD simulation.

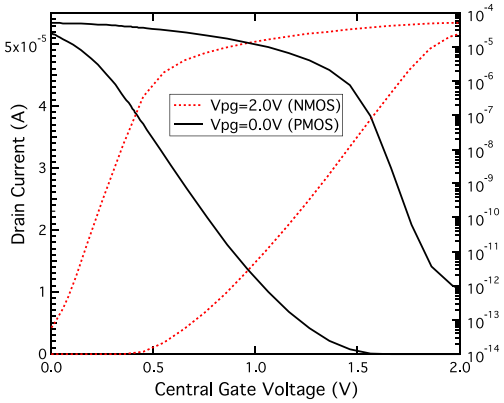

Figure 3. TCAD simulation: Symmetric characteristics of ambipolar SiNWFET.

C. *Verilog-A Compact Model*

To enable a first-order evaluation at the circuit level, a simple compact model has been written in Verilog-A. The equivalent circuit of a single wire *nanowire FET* (NWFET) is described in Fig. 4. The core of the model is based on a table model describing the channel resistance as a function of the polarity gate and the control gate. The table model has been extracted from TCAD simulations for V_{CG} and V_{PG} sweeping between 0V and +2V with a step of 0.1V and 0.25V respectively. Parasitic capacitances and resistances have been extracted from the device geometry presented in Fig. 4. The access resistance corresponds to the pillar at drain and source contacts. Capacitances extraction has been done assuming ideal cylindrical capacitors between the respective gates and the channel. Polarity gate impact is equally split to source and drain regions.

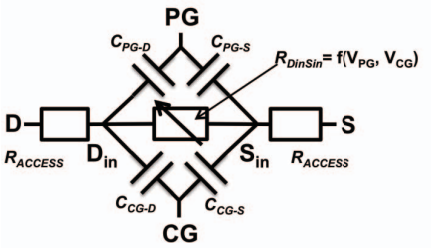

Figure 4. Single NWFET equivalent circuit

This model is able to capture the basic behavior of a single wire transistor. In a first order, a stack of several wires might be seen as the parallel interconnection of several NWFETs. Then, a stack of wires is modeled by the parallel arrangement of single transistor model.

III. Regular Layout Fabric for Ambipolar Circuits: Sea-of-Tiles

Regular layout fabrics maximize the layout manufacturability thereby improving the overall yield of the chip. Logic tiles have been proposed as a basic building block for future ambipolar circuits [1]. The layout of each tile is engineered to minimize the routing overhead caused by the extra polarity gate for ambipolar-FETs. Moreover, each tile can be configured to various basic logic gates. With *Sea-of-Tiles* (SoT) design methodology [1], a complex Boolean logic function can be mapped onto an array of logic tiles, which are uniformly spread across the chip.

A. *Logic Tiles*

A logic tile is defined as an array of transistor pairs, which are grouped together. Figure 5a illustrates the concept of transistor pairing and grouping. Transistor pairing helps in aligning the control gates of the complementary transistors in the pull-up and pull-down networks, whereas with transistor grouping polarity gates of adjacent transistors are connected together. By grouping the polarity gates of the adjacent transistors we can reduce the number of *input* pins to the connected fabric, tile. A $Tile_{Gn}$ (shown in Fig. 5b) is an array of *n* transistor-pairs grouped together. All the polarity gates of the top/bottom transistor array are connected together. This is the first step towards minimizing the intra-cell routing congestion.

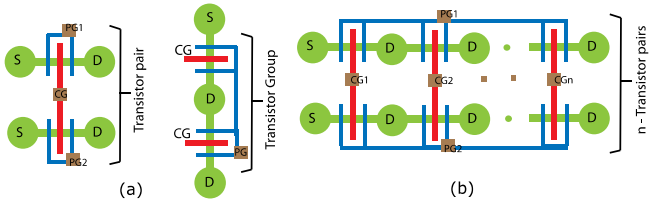

Figure 5. (a) Transistor pairing and transistor grouping (b) $Tile_{Gn}$.

B. *Mapping of Logic gates onto Sea-of-Tiles (SoT)*

Figure 6a shows an un-mapped (not configured) $Tile_{G2}$. Various logic functions can be realized by connecting the nodes (*n1-n6*) and gates (*g1*, *g2*, *G1* and *G2*) to appropriate inputs. By connecting the nodes and gates to appropriate signals (A, B are input signals; V is Vdd; G is Gnd; O is the final output signal) various basic logic gates can be realized. Figure 6(b,c) illustrates $Tile_{G2}$ configured to a 2-input NAND and XOR gates. Moreover, complex logic functions can be obtained by considering a SoT of $Tile_{G2}$.

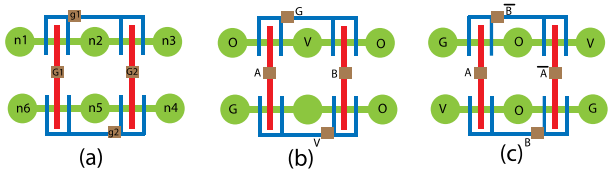

Figure 6. (a) Unconfigured $Tile_{G2}$ (b) NAND2 gate realized with $Tile_{G2}$ (c) XOR2 gate realized with $Tile_{G2}$.

C. *Optimal Tiles*

Performance of various logic tiles, $Tile_{G1}$, $Tile_{G2}$, $Tile_{G3}$ and $Tile_{G1h2}$, have been studied for DG-SiNWFET technology [1]. $Tile_{G1}$ is the simplest tile with only one pair of transistors. Any Boolean function can be mapped on to an array of $Tile_{G1}$. The flexibility of building generic logic gates comes at a cost of area. Moreover, providing access to each and every polarity gate adds to

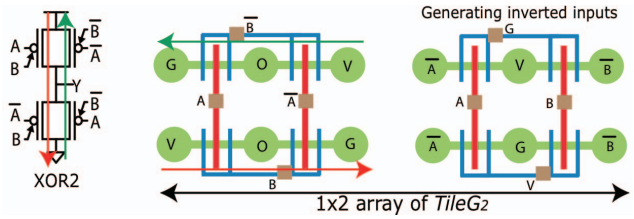

Figure 7. Schematic and dumbell-stick representation of a 2-input XOR gate mapped onto two adjacent tiles ($TileG_2$).

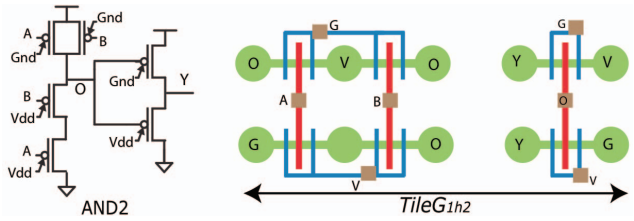

Figure 8. Schematic and dumbell-stick representation of a 2-input AND gate mapped onto a $Tile_{G1h2}$.

the intra-cell routing (Metal1 and Metal2 routing) complexity. $Tile_{G2}$ and $Tile_{G3}$ include two and three transistor pairs, respectively, grouped together. A hybrid tile $Tile_{G1h2}$ is a combination of $Tile_{G1}$ and $Tile_{G2}$, which are not connected (see Fig. 8). This gives the flexibility of utilizing a part of a tile, when remained un-mapped, by functions with low utilization factor.

Figure 7 demonstrates a 2-input XOR gate mapped onto two adjacent tiles of $Tile_{G2}$. An extra tile is needed to generate the inverted input signals for the XOR operation. Similar demonstration of a 2-input AND gate mapped onto a $Tile_{G1h2}$ is shown in the Fig. 8. From the layouts of XOR2 and AND2 (Fig.7 and Fig. 8), we can observe that the power and ground signals are spread all over the tiles. In order to achieve regularity in the power and ground signals, as in the case of regular CMOS design with power and ground rails, we have optimized the power distribution network for tiles. Fig.9 illustrates the power distribution network for SoT of $Tile_{G2}$, with 2-input NAND and XOR gates mapped onto two adjacent tiles.

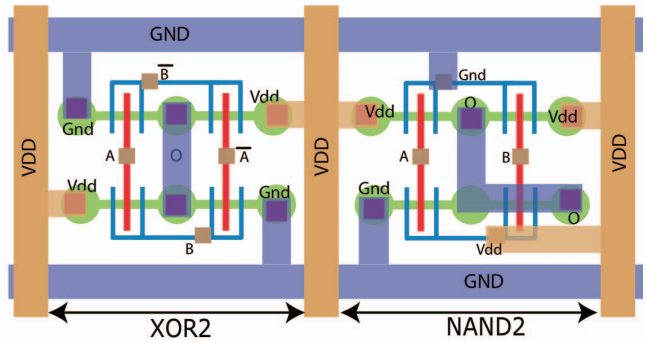

Figure 9. Layout of the power distribution network for SoT with $Tile_{G2}$.

In the previous work, with the help of technology mapping onto various benchmarks, we find $Tile_{G2}$ and $Tile_{G1h2}$ as an efficient choice when optimized for area [1]. In this work, we find the optimal number of vertical silicon nanowire stacks for the tiles $Tile_{G2}$ and $Tile_{G1h2}$.

IV. Design Flow and Experimental Setup

Our design flow for finding the optimal tile size for $Tile_{G2}$ and $Tile_{G1h2}$ is shown in the Fig. 10. Various cell libraries for $Tile_{G2}$ and $Tile_{G1h2}$ were generated with a varying set of vertically stacked silicon nanowires (from 1 to 16). With the help of the TCAD model of the NWFET, we characterized the electrical performances of the DG-SiNWFET transistors. Based on the TCAD evaluation, a basic compact Verilog-A model is derived (see Section 2c), which is employed to characterize various cell libraries. Different flavors of the library were generated based on the number of vertically stacked nanowires to form the channel (from one to 6 nanowires). A set of logic cells consists of 16 combinational logic cells such as NAND2, NAND3, NOR2, AOI21, … and one D flip-flop with asynchronous reset and preset. Characterization was performed with Encounter Library Characterizer tool [16].

With the generated *lib* file, we synthesize various benchmark circuits [13] using Synopsys Design Compiler [15]. We consider

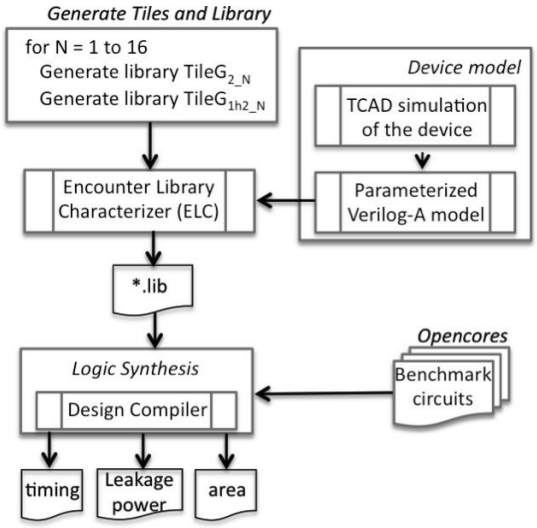

Figure 9. Design flow

timing, *leakage power* and *area* reports to compare the performance of logic tiles ($Tile_{G2}$ and $Tile_{G1h2}$ with varying stacked SiNWs) to traditional CMOS at various technology nodes. CMOS counterpart libraries have been generated using PTM models [14]. The nominal voltages for the different technologies have been used, such as 1.0V for CMOS at 45nm node and 2.0V for NWFETs. The nominal voltage for NWFET can be scaled down to 1.0V by band-gap engineering of the device. The gate sizing respects the Nangate library [9] sizing and ideal scaling have been applied between the different technology nodes. In addition to the gate characterization, a simple ideally scaled model for the wire load is added to the libraries.

V. Simulation Results

In this section, we first study the sizing of the tile for DG-SiNWFET technology. Once the optimal size of the tile is determined, we look at the architectural evaluation of ambipolar DG-SiNWFET technology when compared to Si-CMOS.

A. Optimal Tile Sizing

We determine the optimal size of the tile by studying the performance of various benchmark circuits when mapped to DG-SiNWFET and Si-CMOS technologies. Optimal tile size corresponds to best tradeoff with respect to area and delay when compared to Si-CMOS implementation. Various cell libraries are designed by varying the number of stacked silicon nanowires, which form the channel region of the SiNWFET. Figure 11 shows the normalized delay and area of a *memory controller* (mc) circuit mapped onto SoT with $Tile_{G2}$ with varying number of nanowires. *Ni* (forming the x-axis) corresponds to a tile with *i* silicon nanowires forming the channel region. We limit the maximum number of vertically stacked nanowires to 6, in order to maintain an acceptable form factor of the pillars (Source/Drain contacts in Fig. 1). Hence, for tiles with *N1* to *N6*, we consider only one stack of nanowires. Tiles with *N8*, *N12* and *N16* are implemented with multiple stacks. For example, *N12* corresponds to an array of *(4 X*

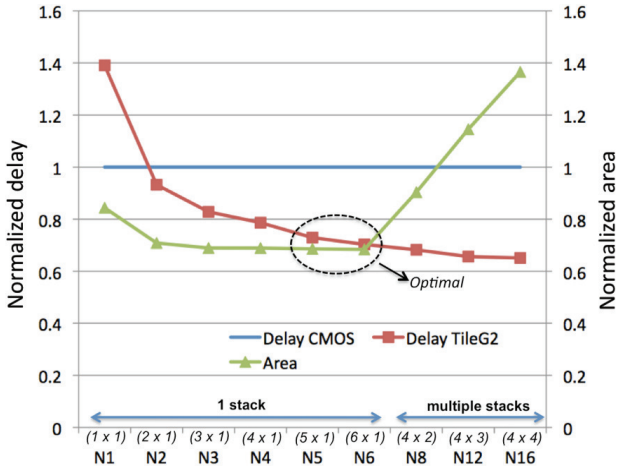

Figure 11. Optimal tile sizing for an memory controller benchmark mapped onto SOT with $Tile_{G2}$

3) nanowires, which refers to 3 stacks of 4 vertically stacked nanowires. Figure 11 uses this convention, array of nanowires, for different sizes of the tile. For tiles with only one nanowire (*N1*), we observe that the circuits mapped onto $Tile_{G2}$ has 1.4x more delay when compared to Si-CMOS implementation. The drive current increases with the increase in the number of nanowires, thereby reducing the delay of the circuit. However, the improvement in delay starts to saturate from *N5*. An improvement of only 6% is observed from *N5* to *N16*. With *N16*, we achieve 35% improvement in delay compared to Si-CMOS.

For a single stack of nanowires, the area of the design decreases with the increase in the number of stacked nanowires. From Figure 10, we can observe 15% improvement in area from *N1* to *N3*. High drive strength of the tile with size *N3*, results in utilizing fewer gates (especially buffers and inverters), thereby decreasing the area of the circuit. However, beyond *N3*, for tiles with 1 stack, the area of the design remains constant. We observe increase in area when mapped onto tiles with multiple stacks, i.e. *N8*, *N12* and *N16*. This can be accounted to the increase in the transistor size (doubled for *N8* when compared to the transistor size in *N4*), which increases the size of the basic tile thereby increasing the overall area of the design.

Considering both the delay and area of the benchmark mapped onto a SoT of $Tile_{G2}$, we obtain the best performance with a tile size of *N6* followed by *N5*. Similar trend has been observed for $Tile_{G1h2}$.

B. Comparision with CMOS

We study area, leakage power and delay of various benchmarks circuits when mapped with DG-SiNWFET and CMOS technologies. We choose optimal tile ($Tile_{G2}$ and $Tile_{G1h2}$) with 6-stacked nanowires (*N6* size) for DG-SiNWFET technology. Table I reports all the performance metrics after mapping with CMOS, $Tile_{G2}$ and $Tile_{G1h2}$ libraries. Though we observe similar delay characteristics for both the tiles, with an exception of wb_conmax benchmark, $Tile_{G1h2}$ outperforms $Tile_{G2}$ in leakage power and area. Figure 13 illustrates the performance improvement of various benchmarks when mapped onto an array of tile $Tile_{G1h2}$. Averaged across all the benchmarks we observe 1.6x improvement in area, 2x decrease in the leakage power and 1.8x improvement in delay.

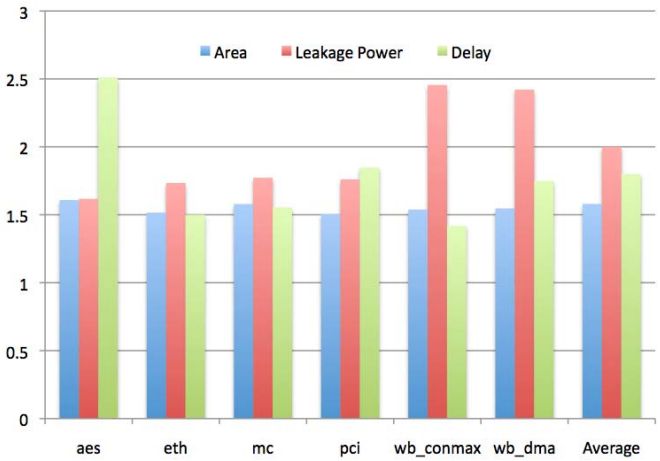

Figure 13. Performance improvement of ambipolar DG-SiNWFETs with respect to CMOS.

VI. OPPORTUNITIES

In this section we highlight the future opportunities for technology, design, and CAD community.

Technology:

Fabrication of vertically-stacked SiNWFET has many challenges. Technologists have to take into account the variations in the diameter of nanowires placed on top of each other. Increasing the number of stacked nanowires increases variations, hence there is an interest to keep the number of stacked nanowires to a minimal number. On the other hand, increasing the number of

TABLE I. AREA, LEAKAGE POWER, AND DELAY OF VARIOUS BENCHMARK CIRCUITS WHEN REALIZED WITH CMOS, AND OPTIMIZED $TILE_{G2}$ AND $TILE_{G1H2}$

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nanowires, improves the drive current of the SiNWFET. In this study, the device is optimized for performance (delay and area) by varying the number of stacked silicon nanowires as well as the transistor width. Benchmarking at the design level we show best performance for a vertical stack of 5 to 6 nanowires. Beyond which we observe minimal improvement in performance. The optimal tile size of 5 to 6 nanowires for the DG-SiNWFET provides a good starting point for technologists to realize the SiNWFET and also in studying the diameter variations.

CAD tools:

In this study, we employed commercial logic synthesis tools during the technology-mapping phase with DG-SiNWFET technology. It has to be noted that ambipolar logic gates are efficient in implementing XOR dominated circuits. State-of-the-art logic synthesis tools are effective for unate logic functions, as the Boolean function is decomposed into *and-inverter-graphs* (AIG). Hence, we envisage better performance with novel logic synthesis tools specifically designed for XOR dominated circuits. This opens up new promising venue for logic synthesis tools targeted for ambipolar logic gates.

Architecture:

In this paper, logic tiles have been employed to realize semi-custom circuits over a sea-of-tiles approach. However, it is noteworthy that the logic tiles are inherently reconfigurable. The in-field configurability opens novel opportunities to build reconfigurable logic operators with a very limited amount of transistors [12]. Hence, we can envisage using the SoT fabric to efficiently build reconfigurable circuits such as Field Programmable Gate Arrays (FPGAs). However, specific architectural organization should be used in order to keep the wiring complexity minimal, such as in [3] where a matrix arrangement with fixed interconnection pattern was proposed. Such organization can also be extended to semi-custom circuits, with matrices of logic tiles with a reduced wiring complexity between the building gates.

VII. CONCLUSIONS

The SoT design approach, with regular layout fabric, is promising for efficient implementation of ambipolar circuits [1]. In this work, we evaluate the performance of regular logic tiles for DG-SiNWFETs. Starting from a TCAD model of DG-SiNWFET, which exhibits p-type and n-type characteristics by controlling the polarity of the second gate, we perform process/design co-optimization to enhance the device performance for achieving a balanced p- and n-type behavior. We show that tiles $Tile_{G1h2}$ and $Tile_{G2}$, with 6 vertically stacked nanowires are optimal for achieving the best performance for a minimal area. SoT with optimal $Tile_{G1h2}$, outperform Si-CMOS, averaged across various benchmark circuits, with 1.6x improvement in area, 2x decrease in the leakage power and 1.8x improvement in delay.

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