Multigate Buckled Self-Aligned Dual Si Nanowire MOSFETs on Bulk Si for High Electron Mobility

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***Abstract*—In this paper, we report for the first time making multi-gate buckled self-aligned dual Si nanowires including two sub-100 nm cross-sectional cores on bulk Si substrate using optical lithography, hard mask/spacer technology, and local oxidation. ≈0.8 GPa uniaxial tensile stress was measured on the buckled dual nanowires using micro-Raman spectroscopy. The buckled multigate dual Si nanowires show excellent electrical characteristics, e.g., 62 mV/decade and 42% low-field electron mobility enhancement due to uniaxial tensile stress in comparison to the non-strained device, all at $V_{DS} = 50$ mV and 293 K.**

***Index Terms*—Local oxidation, local stressor, micro-Raman spectroscopy, MOSFET, multi-gate, Si nanowire, strain engineering, uniaxial tensile stress.**

I. Introduction

MULTI-GATE devices such as gate-all-around Si nanowires are promising candidates during aggressive CMOS downscaling, due to having optimized subthreshold slope, immunity against short-channel effect and optimized power consumption. For further performance enhancement while downscaling especially for the 90-nm technology nodes and beyond, CMOS boosters, e.g., stressors have been integrated in the CMOS process flows. According to [1]–[3], Si nanowires show excellent mechanical properties versus bulk Si in terms of yield and fracture strengths. On the other hand, due to the freedom on buckling in the suspended Si nanowires, a significant level of stress in the Si channel can be obtained [4], [5]. Therefore, the Si nanowires can be counted as the best innovation platforms for various strain engineering-based CMOS booster applications, e.g., significant stress level modulation in the channel [5] to boost the carrier mobility in the classical MOSFETs and stress profile engineering along the channel [6], [7] for band-to-band tunneling current boost in tunnel FETs. Including stress in the suspended channels is also a technology challenge and until now only a few methods are reported: strained substrate [8], metal gate strain [4], local oxidation [9], SiGe S/D [10], diamond-like carbon (DLC) [11], and local oxidation and metal gate strain [5], [12]–[14].

Parallel to the CMOS boosters, making a 3-D stack of multigate devices using various techniques, e.g., dual SOI wafer [15], epitaxial Si–SiGe stacks [16], [17], and stress-limited oxidation [18] can enhance further the current density. Among the 3-D integration techniques, stress-limited oxidation is the simplest way used previously to make dual Si nanowires based on a vertical fin on silicon on insulator (SOI) [18], and vertical stack of Si nanowires from a preshaped vertical fin using scalloping on bulk Si [19]. A well-controlled stress-limited oxidation can even cause keeping a thin Si bridge between the vertical Si nanowire cores, leading to a significant improve in drive current [20], while keeping the nanowires in a more self-aligned manner and helping to suppress the sticking issue of the dense array of parallel nanowires due to the possible buckling in the case of, e.g., using local stressors and, therefore, providing more freedom to make a more dense array structure from the top-down Si nanowire platforms.

In this paper, we are reporting the fabrication and characterization of strained self-aligned dual Si nanowires on bulk Si substrate using 0.8-μm optical lithography and hard mask/spacer technology for the first time. The stress value is measured in the buckled Si nanowires by micro-Raman spectroscopy and finally, the low-field electron mobility boost due to stress is reported.

II. Fabrication Process

The process flow to fabricate self-aligned dual Si nanowires from bulk Si substrate is demonstrated in Fig. 1. As the first step, the 100 mm (1 0 0) p-type (0.1–0.5 Ω·cm) bulk prime Si wafers were oxidized using wet oxidation at 1050 °C to grow 500 nm of SiO_2 including −310 MPa residual thin-film biaxial compressive stress. Afterward, DWL200 was used to write the active resist pattern (S/D and wires) directly on the wafer using 0.8-μm resolution optical lithography. The length and the width of the wire masks were varying from 2.0 to 20.0 μm and 0.8 to 1.8 μm, respectively. To transfer the active layer to the wafer, the SiO_2 hard mask and Si were etched anisotropically using fluorine-based chemistry to make ≈1.1 μm high ribs. A 5 hour sacrificial wet oxidation at 850 °C was done to narrow the Si ribs from the two sides, smooth the Si side walls, and simultaneously grow an oxide spacer layer. A short fluorine-based dry anisotropic SiO_2 etching step was performed to remove the grown SiO_2 on the substrate. The higher oxidation rate for the Si side walls in comparison to the (1 0 0) Si surface leading to grow a thicker oxide on the side walls while due to the slightly

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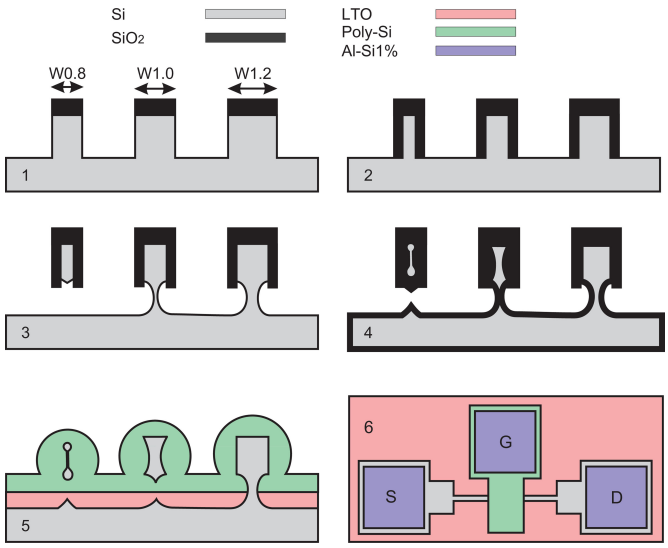

Fig. 1. Process flow to obtain multigate Si nanowire MOSFETs on bulk. W0.8 corresponds to the initial 0.8 μm mask nanowire width.

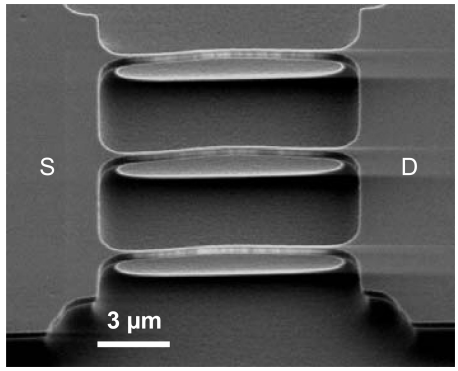

Fig. 2. Tilted-view SEM micrograph of an array of 10 μm long buckled dual Si nanowires on bulk Si right after the SiO_2 stripping step, representing the reproducibility of the process flow from strain engineering and dual Si nanowire formation aspects. The two sub-100 nm cross-sectional nanowire cores are connected to each other using a thin-Si bridge. The out-of-plane buckling is the signature of uniaxial tensile stress in the nanowire.

slanted side walls, the final SiO_2 spacer thickness right after the SiO_2 etching step is estimated to be $\leq$50 nm. Afterward, a fluorine-based isotropic Si etching was done to suspend the narrowest ribs (0.8 μm initial mask NW width, called W0.8 in this paper) from the substrate, while the rest of the Si ribs were still connected to the substrate.

A 4 hour wet oxidation at 850 °C (8.3 L/min O_2, 16.0 L/min H_2) was done to nominally consume 120 nm of (1 0 0) Si to reduce the nanowire dimensions, consume the remained Si between the wider nanowires (W1.0) and substrate to suspend the structures. The oxidation temperature was chosen to be below the glass transition temperature of SiO_2, 960 °C, to avoid relaxation of stress in the SiO_2 thin films to be able to accumulate mechanical potential energy in the nanowires during oxidation [21], [22]. The higher oxidation rate for the Si side walls in comparison to the top (1 0 0) Si surface as well as built-in stress in the growing oxide layer during the oxidation step yields to obtain two Si cores with rounded corners connected with a sub-10 nm thick Si bridge after oxidation of the narrowest Si ribs (W0.8).

Stripping the SiO_2 hard mask/spacer and the grown oxide was done using wet buffered hydrofluoric (BHF) etching (volume ratio of 7:1 of NH_4F 40% and HF 50%). Fig. 2 represents an array of Si nanowires including two sub-100 nm cross-sectional self-aligned Si cores connected with a thin Si bridge right after the stripping step. The buckling in the nanowires after the stripping step is due to releasing the stored mechanical potential energy in the nanowires during the oxidation step [21], [22], a clear sign of uniaxial tensile stress in the nanowire.

An isolation step including low-temperature oxide (LTO) deposition, CMP, and isotropic LTO etching using BHF was done to isolate the suspended nanowires from bulk. The gate stack step includes RCA, dry oxidation to grow 15 nm of gate oxide at 850 °C and finally 230 nm of LPCVD in-situ doped N^+ poly-Si (phosphorous: 2×10^{20} cm^{-3}) at 480 °C. The thin Si bridge during the gate stack step is being consumed and finally two separated self-aligned sub-100 nm cross-sectional Si cores can be obtained (see Fig. 3).

To activate the dopants in the poly-Si thin film, a 5 min furnace annealing at 900 °C was done. The gate pattern was transferred to the wafer using optical lithography and fluorine-based isotropic poly-Si etching. Stripping the resist layer, S/D phosphorous ion implantation (2×10^{15} cm^{-2}, 30 keV) and annealing to activate the dopants, metallization, and sintering (450 °C, 30 min) were the further steps.

III. Strain Analysis in the Buckled Si Nanowires

A. Stress Measurement on the Buckled Dual Si Nanowires by Micro-Raman Spectroscopy

Micro-Raman spectroscopy was employed for measuring stress on a finalized dual Si nanowire MOSFET at 293 K. A Renishaw inVia spectrometer setup is used with a green laser of 532 nm in wavelength. As the penetration depth of the laser in Si ($\approx$1 μm) is longer than the thickness of the Si nanowire ($<$500 nm), both Raman spectra of the strained Si nanowire and the relaxed Si underneath are observed, while the laser beam is focused on the nanowire. The line scan with the step of 0.5 μm was done across the naked part of the Si nanowire between S/D pad and gate pattern (see Fig. 4) as the measurement on the Si channel via the poly-Si gate stack is challenging due to the broad spectra of poly-Si around the crystalline Si spectra.

A spectrum shown in Fig. 5 was taken at the 10th from the top out of 16 points along the scan axis. A considerable satellite peak is only observed at this point while just a single peak originated from relaxed bulk Si at 520.6 cm^{-3} is observed in the others except for a very subtle shoulder at the 9th and 11th points. The result suggests that the buckled nanowire was spotted on in the measurement at the 10th point. As shown in Fig. 5, the corresponding two peaks are deconvoluted from the spectrum by using Lorentzian peak fitting [23]. 0.465%/0.785 GPa uniaxial tensile strain/stress in the buckled Si nanowire are estimated by assuming Young's modulus of 169 GPa in Si.

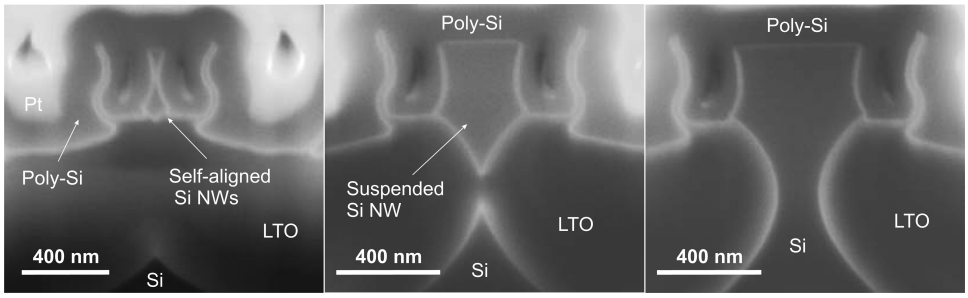

Fig. 3. SEM nanograph from the cross-section of multi-gate MOSFETs on bulk Si: multi-gate suspended dual self-aligned Si nanowires (W0.8, left), multi-gate suspended Si nanowire (W1.0, center) and omega-gate MOSFET (W1.2, right).

B. Process-Based Stress Optimization in the Top-Down Si Nanowire Platform

Previously in [21] and [22], we reported in-depth stress analysis of local oxidation of the Si nanowires with a Si_3N_4/SiO_2 tensile hard mask on the top. In this paper, due to using a SiO_2 hard mask, grown by wet oxidation, the sign of the stress in the hard mask is reverse because of volume expansion during oxidation. Less restrictions on out-of-plane buckling during the oxidation step due to having a compressive hard mask on top leads to a smaller accumulation of mechanical potential energy during oxidation, and finally a smaller amount of stress in the Si nanowires is expected in comparison to the Si nanowires with a tensile hard mask on the top. On the other hand, using a SiO_2 hard mask and spacer has the advantage of further rounding the sharp corners of the Si nanowire channel. To improve further the level of uniaxial tensile stress in the Si nanowires, a high-k/metal-gate stack including an intrinsic compressive thin-film stress in the metal-gate layer can be used [4], [5]. As a consequence, to even significantly relax the level of stress to make the Si nanowire platform suitable for the pMOS devices without hole mobility degradation, the thermal oxidation can be performed at temperatures higher than the glass transition temperature of SiO_2, 960 °C, for viscoelastic stress relaxation in the SiO_2 thin films on the wafer and further compressive stress can be induced to the suspended nanowire channel using a high-k/metal-gate stack including an intrinsic biaxial tensile stress in the metal-gate layer.

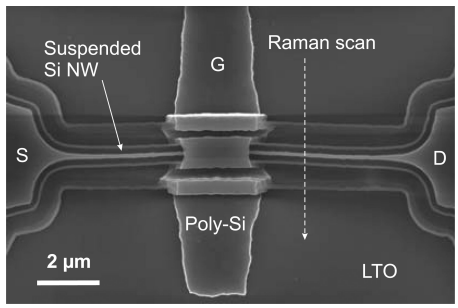

Fig. 4. Top-view SEM micrograph of a multi-gate dual Si nanowire MOSFET on bulk Si. The in-plane nanowire buckling is a sign of uniaxial tensile stress in the channel. The arrow indicates the scan axis and direction of the laser spot in the micro-Raman measurement.

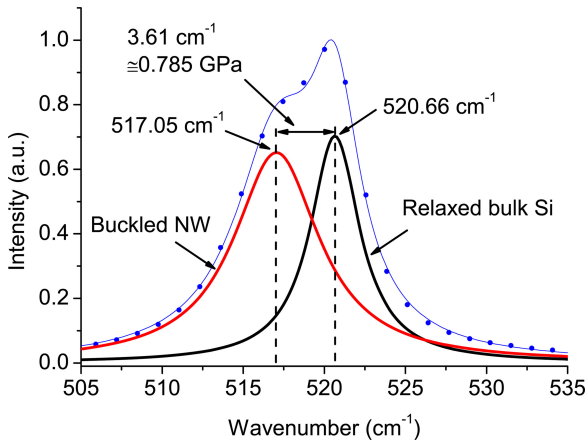

Fig. 5. Micro-Raman spectrum taken on a 12 μm long buckled dual Si nanowire on bulk Si (SEM top-view in Fig. 4). The spectrum is well fitted with two Lorentzian peaks corresponding to the relaxed bulk Si at 520.66 cm^{-1} and the strained Si nanowire at 517.05 cm^{-1}.

IV. Electrical Characterization and Extraction of Parameters

Electrical characterization was done at 293 K using a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer. Figs. 6 and 7 show output and input characteristics of the multi-gate dual Si nanowire MOSFET with the shown SEM micrographs in Figs. 3 (left) and 4. The threshold voltage and low-field mobility values were extracted using the $I_D/\sqrt{g_m}$ method [24], [25], quasi-independent of series resistance and mobility attenuation factor reporting $V_{TH} = -0.061$ V and $\mu_0 = 468\ cm^2/V{\cdot}s$ at $V_{DS} = 50$ mV. According to Fig. 7, the I_{on}/I_{off} ratio at $V = 2.000$ V can be as high as $\approx 10^8$ in the case of tuning the threshold voltage using a metal gate with a mid-gap work function or channel doping modulation. During the extraction of parameters, only the covered faces of the nanowires with the poly-Si/SiO_2 gate stack in Fig. 3 were considered as the W_{eff} of the MOSFETs. Note that the bottom part of the suspended nanowires not covered with the gate stack, mainly due to its challenging isolation step, acts as an independent transistor with a thick gate-oxide layer (>200 nm LTO) and using bulk Si as the back gate. Due to its fairly thick oxide thickness and since V_{BS} is fixed to 0 V during all the measurements, this independent transistor cannot involve significantly in the conduction.

To compare the results, the wider MOSFETs with the SEM cross-sections in Fig. 3 and with the same gate length in Fig. 4 were also characterized (see Figs. 8 and 9). The omega-gate

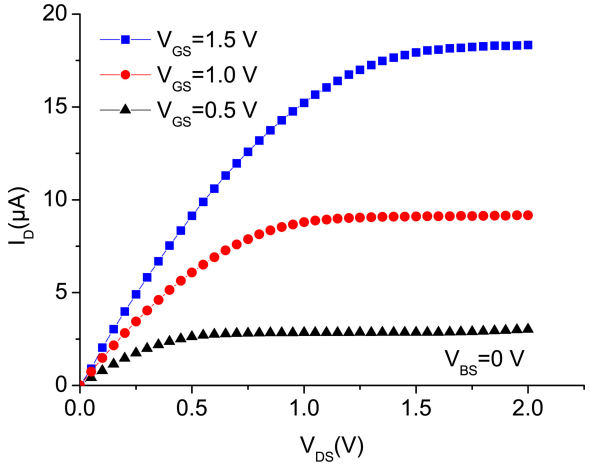

Fig. 6. Output characteristics of the multi-gate dual Si nanowire MOSFET [W0.8, SEM cross-section in Fig. 3 (left)].

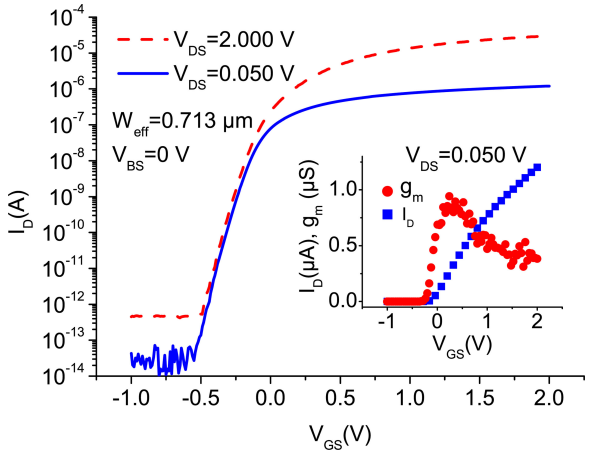

Fig. 7. Input characteristics of the multi-gate dual Si nanowire MOSFET [W0.8; SEM cross-section in Fig. 3, left; W_{eff} = 0.713 μm (top NW: 0.273 μm; bottom NW: 0.440 μm)]. SS = 62 mV/decade, V_{TH} = −0.061 V, μ_0 = 468 cm^2/V·s, and R_{SD} = 18.7 kΩ, all at V_{DS} = 50 mV.

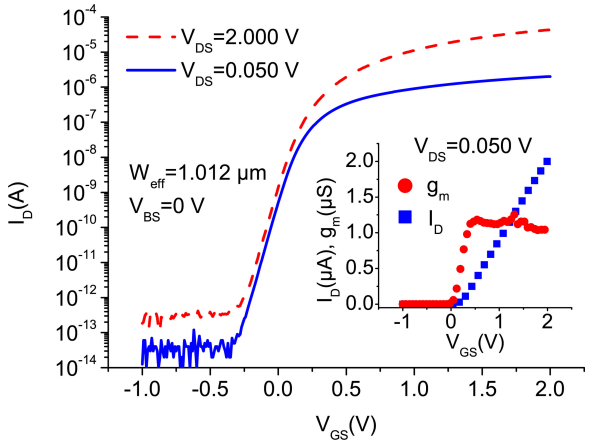

Fig. 8. Input characteristics of the multi-gate Si nanowire MOSFET (W1.0; SEM cross-section in Fig. 3 (center); W_{eff} = 1.012 μm). SS = 64 mV/decade, V_{TH} = 0.213 V, μ_0 = 353 cm^2/V·s, and R_{SD} = 3.7 kΩ, all at V_{DS} = 50 mV.

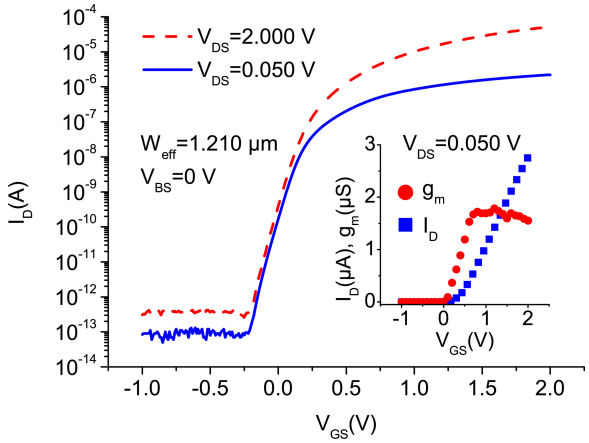

Fig. 9. Input characteristics of the omega-gate MOSFET (W1.2, SEM cross-section in Fig. 3 (right), W_{eff} = 1.210 μm). SS = 68 mV/decade, V_{TH} = 0.255 V, μ_0 = 329 cm^2/V·s, and R_{SD} = 0.8 kΩ, all at V_{DS} = 50 mV.

MOSFET shows V_{TH} = +0.255 V and μ_0 = 329 cm^2/V·s at V_{DS} = 50 mV. The observed downshift in the threshold voltage of the dual Si nanowire is mainly due to the local volume inversion, corner effect, and uniaxial tensile stress in the channel [26], [27]. The optimum values of the subthreshold slope as well as very low leakage current values are reflecting an excellent gate stack while the narrower channels represent a better value due to a better electrostatic control on the channel. A 42% low-field electron mobility improvement in the buckled dual Si nanowire in comparison to the omega-gate MOSFET is due to uniaxial tensile stress in the channel. The higher transconductance drop in Fig. 7 in strong inversion regime in comparison to the wider devices is mainly due to the higher series resistance in the scaled Si nanowire MOSFETs.

The series resistance values reported in the caption of Figs. 7–9 are extracted and estimated using the *y*-intercept of total resistance ($R_{tot} = V_{DS}/I_D$) versus $1/(V_{GS} - V_{TH} - V_{DS}/2)$ at V_{DS} = 50 mV [28], assuming series resistance as the major transconductance drop mechanism in strong inversion regime. Note that the contribution of intrinsic mobility attenuation factor (θ_0, see [24], can be influenced mainly by channel-dielectric interface quality [29]) on the transconductance drop in strong inversion should be negligible due to having an excellent gate stack (optimum subthreshold slope and pretty low leakage drain current in a sub-100 fA range for all the multi-gate devices at V_{DS} = 50 mV).

V. Conclusion

We demonstrated multi-gate buckled self-aligned dual Si nanowires including two sub-100 nanometer cross-sectional cores on bulk Si substrate using optical lithography, hard mask/spacer technology and local oxidation for the first time. Uniaxial tensile stress was measured in the buckled dual Si nanowires using micro-Raman spectroscopy and the stress-based low-field electron mobility enhancement was reported.

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