Standard-Cell Based Memories (SCMs): from Sub-VT to Error-Resilient Systems

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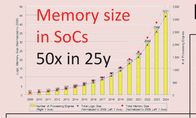
Motivation & Research Overview

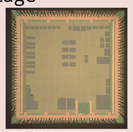


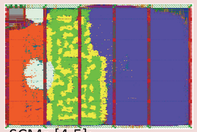
Increasing Need for **Embedded Memories** [ITRS'09] in …

	Biomedical Implants, Remote Sensors, …	**Near-VT Processor [Intel'11: Claremont], Handheld devices, …**	**Error-Resilient Computing [Intel], Transceivers, …**
Robustness	Robust		Unreliable
Area priority	Secondary		High
Supply Voltage	Sub-VT	Near-VT	Nominal
Power	Very Low		High
Speed	Very Slow		Fast
State of the art	SRAM with 10T bitcells [1], or 8T bitcells [2]	6T SRAM eDRAM: special technology, extra cost Gain-cells: logic-compatible	
Contribution	**Standard-cell based memories (SCMs)** [3,4]		
	Low-leakage latch	Commercial library	**Dynamic latches**

SCMs guarantee functionality in any system from **reliable sub-VT** to **error-resilient high-performance**, at any supply voltage

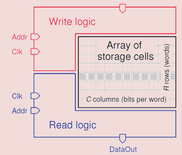
Simplified design flow compared to SRAM
- Fine-granular organizations
- Generic description, any desired size
- Modifications at design time
- Portability (unless custom cells)
- Automatic placement, no power routing

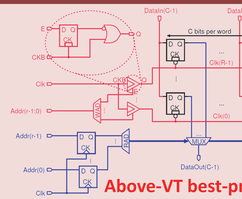

SRAM macros: Complicated floorplan


SCMs [4,5]: Merged with logic Simplified design flow

Best-Practice SCM Implementations

SCM building blocks





Above-VT best-practice

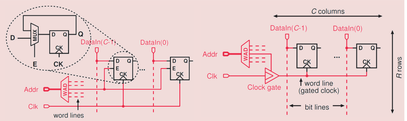
Architectural comparison results true for different
- technology nodes,
- fabs, and
- library providers [4]

Write logic

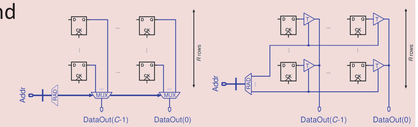
Clock gates (b): smaller and less power than enable flip-flops (a)

Read logic

- Above-VT
  - **Multiplexers** (c): smaller, faster, and less power than tri-state buffers
- Sub-VT
  - **Tri-state buffers** (d): less leakage (energy) than multiplexers



(a) Enable flip-flops (b) Clock gates



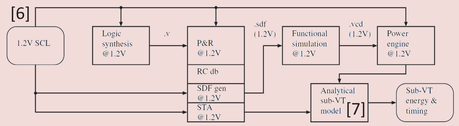
(c) Multiplexers (d) Tri-state buffers

Array of storage cells

- **Latch** arrays smaller than FF arrays, but longer write-address setup time

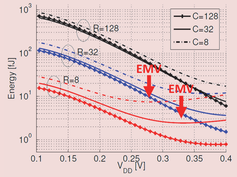
Reliable Sub-VT SCMs

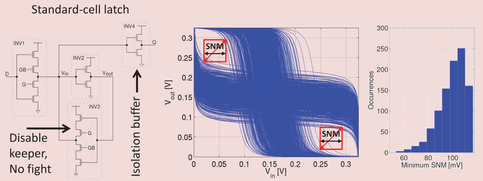
Sub-VT compilation and characterization flow [6]
- Above-VT synthesis, STA, and power analysis
- Analytical sub-VT model [7]
- ✓ Ideal for quick **design-space exploration**



SCMs are immediately **robust in sub-VT** domain [3]
- Write & read failures encountered in 6T SRAM are avoided by standard-cell latch
- Still good hold-SNM at V_{DD}=300mV

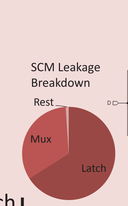
Leakage is dominant, active energy negligible
- Only smallest SCMs reach EMV in sub-VT domain

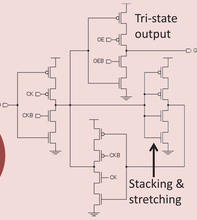


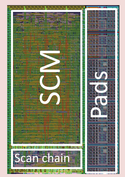


Cell customization for low leakage
- Transistor stacking & stretching
- Integrated tri-state output

All dominant leakage contributers are addressed by designing only 1 custom standard-cell







65nm tape-out

Low-leakage latch
Commercial library

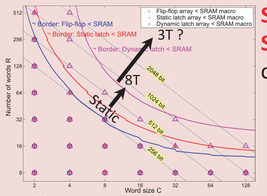
Publication	**[1]**	**[2]**	**[3]**	**This**
Memory Type	SRAM macro		SCM	
V_{DDmin} [mV]	380	350	300	300
f_{max} [kHz]	475	25	1'000	1'000
Energy [fJ/bit]	65.6	884.4	**32.7**	**15.0**
Area [um^2/bit]	2.9	4.0	12.5	12.5

SCM w.r.t. SRAM (all work in 65nm)
- Similar V_{DDmin}
- **Faster** → Lower energy
- Larger

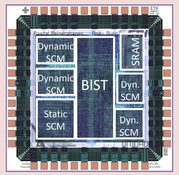
Designing only **1 custom cell**
- **Energy cut into half**

SCMs for Error-Resilient Systems

System tolerates a few errors in memory
- **Dynamic latches** w.r.t. static latches
  - Smaller
  - Less reliable

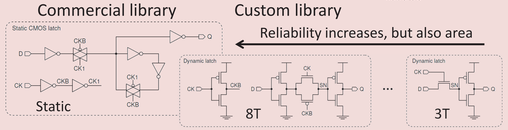


SCMs are smaller than SRAM for storage capacities up to 2kb



Measurement & reliability analysis in progress

Commercial library
Custom library
Reliability increases, but also area



Key Points

- **Functional in any system, at any voltage**
- **Synthesizable, any size, no power routing**
- **Faster than sub-VT SRAM, smaller than 6T SRAM**

[1] Calhoun *et al.*, JSSC'07; [2] Verma, Chandrakasan, ISSCC'07; [3] Meinerzhagen *et al.*, JETCAS'11; [4] Meinerzhagen *et al.*, MWSCAS'10, **nomination student paper contest**; [5] Roth, Meinerzhagen *et al.*, A-SSCC'10; [6] Meinerzhagen *et al.*, ECCTD'11, **invited paper**; [7] Akgun *et al.*, TBCAS'11

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