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Modeling Techniques and Verification Methodologies for Substrate Coupling Effects in Mixed-Signal System-on-Chip Designs

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***Abstract*—The substrate noise coupling problems in today's complex mixed-signal system-on-chip (MS-SOC) brings a new set of challenges for designers. In this paper, we propose a global methodology that includes an early verification in the design flow as well as a postlayout iterative optimization to deal with substrate noise, and helps designers to achieve a first silicon-success of their chips. An improved semi-analytical modeling technique exploiting the basic behaviors of this noise is developed. This method significantly accelerates the substrate modeling, avoids the dense matrix storage, and, hence, enables the implementation of an iterative noise-immunity optimization loop working at full-chip level. The integration of the methodology in a typical mixed-signal design flow is illustrated and its successful application to achieve a single-chip integration of a transceiver is demonstrated.**

***Index Terms*—Mixed-signal ICs, RF designs, substrate noise, system-on-chip, transceiver design, verification.**

I. Introduction

TODAY'S mixed-signal system-on-chip (MS-SOC) can include, on a single chip, such heterogeneous designs as embedded DRAM, digital, analog, RF front-ends, complex mixed-signal, microprocessor, DSP, etc. This situation leads to two seemingly contradictory requirements on design methodology: on one hand, higher levels of abstraction is needed to cope with the added complexity in design, while at the same time, the shrinking process technologies and the single-chip integration requires inclusion of lower level details. The unprecedented impact of lower level physical effects such as interconnect parasitics, cross talk, as well as substrate bounce, IR drops, and inductance effects represent enormous challenges for electronics design automation (EDA) tool developers [1]. Currently, designers are often forced to drift away from the transistor-level physical phenomena to higher levels in the design hierarchy, to be able to manage the increasing complexity of their designs. In this context, the potential of computer simulation in aiding the design decisions is becoming evident.

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For instance, the relentless drive toward a single chip integration of digital and analog circuits has opened the door to a host of challenging noise coupling effects which should be controlled [2]. The switching activity of digital subcircuits injects spurious signals into the substrate through the reverse-junction capacitances or by impact ionization (hot carriers). Moreover, the transient current consumed, generates fluctuations in the internal supply voltage ($\Delta V = Ldi/dt$). These transient voltages couple through metal lines and through the substrate to the sensitive parts of the chip corrupting their functionality by body effect or capacitive coupling. The problem becomes more acute if RF sections are added to the chip. In fact, many side effects that corrupt the RF signal such as: local oscillator (LO) leakage, self mixing, dc offset, and oscillator pulling and pushing, are partially due to the substrate coupling and supply noise. Moreover, side-band spurs, jitter and phase noise [3]–[6], which leads to dramatic change in the frequency spectrum and timing properties are also enhanced by the switching noise that gets coupled to the voltage-controlled oscillator (VCO) through the substrate from the high speed divider/counter circuit of phase-locked loop (PLL) or from digital subcircuits. Currently, only RF front-ends with frequency synthesizers are sometimes integrated for such demanding applications as wireless phones. Efforts are underway, however, to integrate the entire transceiver for relatively undemanding applications such as RF identification systems and wireless local-area networks.

The principal strategies to limit substrate noise coupling are [5], [6]: using multiple pins/wires assignment for on-chip power supply/ground, in order to reduce the value of the corresponding parasitic inductance; splitting supply lines and terminals of noisy and sensitive blocks; installing guard ring with dedicated on-chip ground; increasing the distances between noisy and sensitive circuits; using on-chip decoupling capacitance; using special package like ball-grid array package or flipchip; adopting differential topology for analog design; using silicon-on-insulator or triple-well technology etc. However, without the ability to analyze the true effects of substrate noise, many of these techniques are often over deployed, resulting in longer design cycles and increased manufacturing costs. Thus it is highly desirable to select the correct noise avoidance strategy to save valuable silicon area and avoid the use of costly process or packaging solutions. Many authors [8]–[15] have proposed useful techniques to the EDA tool developers, to improve the substrate modeling methods. The most precise solution for substrate modeling certainly comes from the use of solver based on finite-difference method (FDM)

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or boundary-element method (BEM). However, despite the improvements realized in this domain, the computational effort involved in computing by field solvers is still considerable to enable full-chip MS-SOC analysis. In addition, even if the size of the circuits enables the substrate extraction, the storage and the manipulation of the enormous resulting $N \times N$ matrix of coupling resistances, is impractical [16]. In fact, in practical MS-SOCs, the number of coupling resistances can reach several millions. Some approaches were proposed to deal with the complexity encountered when simulating large and dense coupling networks [15]–[17]. Recently [17], an approach inspired by wavelets to sparsify the dense conductance matrix, was proposed. However, even though the multilevel representation presented offers greater flexibility, the method is less mature and has difficulty in handling problems with multiple geometric scales [16]. Other approaches, which are worthy of further investigation, are presented in [16]. The BEM has been successfully adapted to the substrate modeling problem [9], [10]. This method reduces the complexity of the problem, as it requires only a 2-D discretization, matching the layout of the circuit, and uses the fast Fourier transform algorithm to compute the impedance matrix. Storage and inversion of the resulting impedance matrix, however, make the required computational effort often prohibitive, even for relatively small circuits. As a result, noise coupling analysis at full-chip level can quickly become intractable. All these prior studies try to resolve the problem from a numerical point of view and without taking into account neither the physical phenomena that govern the noise coupling nor the characteristics of the analyzed circuits. The substrate coupling depends strongly on the kind of the circuit, the technology used, the layout, the substrate doping profiles, and package parasitics. A successful extraction/sparsification method is thus only possible by taking all these aspects into consideration. On the other hand, without a design-oriented methodology that efficiently uses these tools in the design flow, the substrate coupling problems will continue to lead to prolonged design cycles, and missed market opportunities. We have recently proposed a methodology based on this analysis, for a successful single-chip integration of RF transceivers [8], [18].

In this paper, we propose a global methodology as well as a suite of tools to deal with substrate noise problems and enables designers to achieve an optimal integration and first silicon-success of their chips. The first ultimate objective is to verify early in design flow if the noise coupling will corrupt the functions of the system. This verification process enables us to make necessary design changes before physical implementation of the system, resulting in a significant reduction of the delay and the cost of the operation. However, the verifications at these stages are highly domain/circuit specific and can not be easily generalized or automated. Nevertheless, a general strategy to guide designers in the early analysis can be formulated. On the other hand, the substrate coupling is essentially a global problem that depends on the full-chip layout, the technology used, and the package parasitics. Therefore, a strategy considering all these aspects in an iterative noise-immunity optimization loop, at full-chip level, is proposed. A successful application of this iterative strategy is only possible if a high-speed substrate modeling extractor is available. A new approach, which combines a thorough physical comprehension of the noise coupling fundamentals and an improved version of the BEM, to build such high-speed extractor, will be illustrated. We have chosen to improve BEM, because it is a semi-analytical method and thus lends itself to an adaptation to the physics of specific problems much more readily than do pure numerical methods such as the FDM. The low computational efforts required as well as speed and accuracy reached by the proposed method, make it one of the most promising alternatives, able to verify complex MS-SOCs even with multimillion transistors. To enable a comparison with FDM and classical BEM, a relatively simple test chips with 1700 to 5000 transistors will be used in our study.

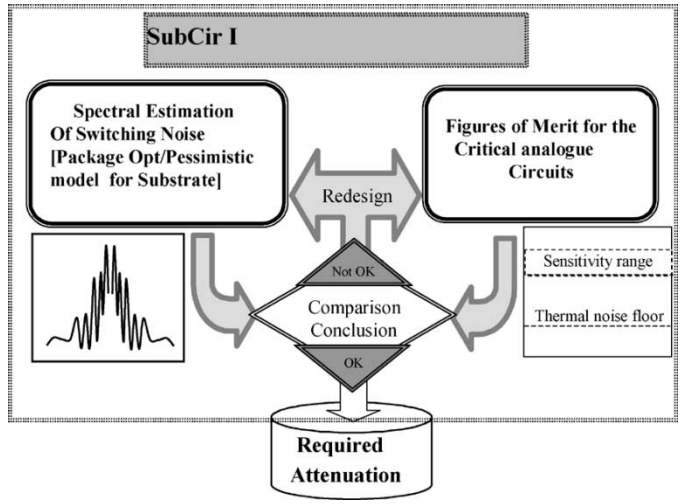

Fig. 1. Flow diagram of SubCirl methodology.

This paper is organized as follows. In Section II, a methodology for noise verifications early in the design stage is described. Section III outlines a hierarchical strategy for post-layout substrate modeling and the improvements introduced in the BEM. In Section IV, an iterative verification/optimization procedure is presented. An application of our methodologies and tools to achieve a single-chip integration of a transceiver dedicated to ISM applications is illustrated in Section V.

II. Early Verifications in the Design Flow

The cost of design corrections grows exponentially as we go deeper in the design flow, and waiting until the full-system implementation to verify noise-coupling problems generates an unsupportable additive delay and cost. To deal with this problem, we have developed the methodology entitled **SubCirI** and illustrated in Fig. 1. The high-level role of this methodology is to verify the analogue components and/or RF front-end early in the design flow, and to make sure that they will continue to meet the desired specifications even in their future noisy environment. This methodology will enable us to make decisions during the circuit-level design, and to focus on the analog and RF parts which do not meet the desired specifications in the presence of the digital switching noise. The possibility of redesigning sensitive sections to be more robust as well as redesigning perturbing sections to generate less noise is then

considered. Eventually, the noise attenuation required to save the basic functionality of the system will be estimated. This information is very helpful to estimate the failure risk as a function of the technology and the package expected to be used. The blocks which meet specification with larger margin than required can also be relaxed, saving cost and power [19].

As shown in Fig. 1, the successful construction of such methodology is only possible through a well-considered approach of three different aspects: 1) the model of substrate and supply noise produced by perturbing circuits; 2) the sensitivity to noise for analog and RF blocks; and 3) the estimation of the noise-transfer functions from noisy blocks to sensitive parts. In our study, a worst case where the substrate is modeled as a single node, causing no attenuation of the noise between different placements of the chip, is used in a first stage. Therefore, we can verify if the analog and RF circuits meet the figures of merit defined by the designers, even in presence of substrate noise and eventually determine which attenuation is necessary for this.

A. Spectral Estimation of Switching Noise

Several kinds of circuits can generate supply/substrate noise. In general, digital circuits are the noisiest parts of the chip. However, some analog cells, especially those with voltage/current transients or large signals such as power amplifiers, can be noise generators as well. For large circuits, the simulation at transistor-level makes the exact switching noise evaluation very demanding in terms of memory and extraction time and even infeasible in several cases. To deal with this complexity, useful techniques have been proposed in the literature [20], [21]. The methodology of [21], for instance, uses a macromodel library of digital cells that includes package parasitics, in combination with VHDL switching events simulation, to generate the transient noise of digital circuits. Because of the high-level nature of the method, it seems to be the more compatible approach for our SubCirI methodology. In the case of small and medium size perturbing circuits, SPICE-like simulator is sufficient to simulate the power spectral density of their noise, as will be seen in Section V.

B. Noise Effects on Analogue Circuits

The principal impact of the noise on analog circuits is to limit the minimum signal that can be processed with acceptable quality and, therefore, to limit their sensitivity. The key metric, characterizing the circuit performances in a noisy environment, is the signal-to-noise ratio (SNR). However, the variety and complexity of analog cells makes a unified physical explanation of how the noise affects their performances almost impossible. Our requirement of evaluating whether the analog/RF functionalities are corrupted is only possible with an accurate transistor-level analysis of each potentially sensitive circuit separately. The analog circuits of mixed-signal systems are often designed with a differential topology. Therefore, the supply and substrate noise appears as common-mode (CM) perturbations and should be rejected by the balanced operation. In reality, however, neither are the circuits fully symmetric nor does their current sources exhibit an infinite output impedance. For instance, nominally identical devices suffer from a finite mismatch due to uncertainties in each step of the manufacturing process. As a result, the analogue operations, even differential, can be seriously affected by the CM supply and substrate signals. The key metric that characterize the CM to differential conversion is the CM rejection ratio (CMRR). The CMRR is defined as the undesirable differential component produced by CM variations, normalized to the wanted differential output. Therefore, the CMRR is very good optimization parameters for SubCirI, enabling to evaluate the failure risk of analog operations in a noisy environment. On the other hand, many studies of noise impact on specific blocks such as Mixers, VCO, LNA have been published [4], [26], [27]. These works provide a very useful background for a successful application of our methodology.

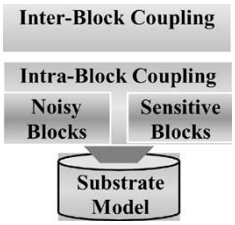

Fig. 2. Substrate modeling flow.

III. Postlayout Substrate Modeling

In this section, we will show how a good physical analysis of the noise coupling in MS-IC will enable us to build an efficient hierarchical postlayout modeling strategy. The substrate coupling verification flow will be broken into a set of independent modeling stages as shown in Fig. 2.

The crucial result we demonstrate here, is that the accuracy parameters governing the global substrate coupling, that is the interblock coupling, are different from those governing the local transistor level coupling (i.e., intrablock coupling). As a result, we can accurately analyze the interblock substrate coupling with a coarse local intrablock coupling representation. At the same time we can accurately analyze the transistor level substrate coupling with a coarse global interblock substrate coupling representation. The BEM will be adapted to our substrate modeling strategy and improvements will be introduced to accelerate the parasitic extraction and avoid the dense matrix storage.

A. BEM Approach

We will briefly describe the application of the BEM to the substrate noise problem. The more common formulation applied to the solution of Laplace's equation is using the Green's function. The Green's function in a medium with prescribed boundary conditions is defined as the potential at any point in the medium due to a unit current injected somewhere in the medium. For the substrate problem, the boundary conditions are Dirichlet boundary for voltage ($\Phi = 0$) at the backplane and Neumann boundaries ($\partial\Phi/\partial \mathrm{n} = 0$) at the remaining faces. The substrate without a grounded backside can be simulated after inserting artificial layer with high resistivity between the actual substrate and the backplane. Based on this formulation, we will consider a system of P planar contacts on the top of a substrate. The substrate is composed in L homogeneous layers,

and each layer is characterized by its conductivity. Each contact is then subdivided into a set of panels so that we can consider the current as constant at each panel. This results in a system with N panels. For such a system, the relation between the N total panels potentials ($\Phi\mathrm{p} \in \Re^{\mathrm{N}}$) and N total currents through each panel ($\mathrm{Ip} \in \Re^{\mathrm{N}}$) is given by $\Phi\mathrm{p} = \mathrm{Zp} \cdot \mathrm{Ip}$. Where Zp ($\in \Re^{\mathrm{N}\times\mathrm{N}}$) is the impedance matrix. Obtaining each entry in this impedance matrix requires computing an integral involving the Green's function over the appropriate contact surfaces.

The impedance matrix elements $\mathrm{z_{ij}}$ and the substrate Green's function G has been previously computed in analytical form [9] and shown to be

$$\mathrm{z_{ij}} = \frac{\overline{\phi_i}}{\mathrm{I_j}} = \frac{1}{\mathrm{s_i s_j}} \int_{\mathrm{s_i}} \int_{\mathrm{s_i}} \mathrm{G(x, y, x', y')ds_j ds_i}$$

and

$$\mathrm{G(x, y, x', y')} = \sum_{\mathrm{n=0}}^{\infty} \sum_{\mathrm{m=0}}^{\infty} \left\{ \begin{array}{l} \mathrm{f_{mn}} \cos\left(\frac{\mathrm{m\pi x}}{\mathrm{a}}\right) \cos\left(\frac{\mathrm{m\pi x'}}{\mathrm{a}}\right) \\ \cos\left(\frac{\mathrm{n\pi y}}{\mathrm{b}}\right) \cos\left(\frac{\mathrm{n\pi y'}}{\mathrm{b}}\right) \end{array} \right\} \quad (1)$$

where a and b are the substrate lateral dimensions, $\mathrm{s_i}$ and $\mathrm{s_j}$ the surfaces of the panels i and j, and $\mathrm{f_{mn}}$ is a function representing the effects of the conductivity and the thickness of the substrate layers, and computed using a recursion formulas as shown in [19]. According to the boundary conditions of the substrate and the positions of the panels on the substrate, $\mathrm{z_{ij}}$ can be expressed as a function of 64 2–D discrete cosine transform (DCT) coefficients ($\mathrm{K(p, q)}$), with

$$\mathrm{K(p, q)} = \sum_{\mathrm{m=0}}^{\mathrm{P-1}} \sum_{\mathrm{n=0}}^{\mathrm{Q-1}} \mathrm{k_{mn}} \cos\left(\mathrm{m}\pi\frac{\mathrm{p}}{\mathrm{P}}\right) \cos\left(\mathrm{n}\pi\frac{\mathrm{q}}{\mathrm{Q}}\right) \quad (2)$$

$\mathrm{k_{mn}}$ is a function of $\mathrm{f_{mn}}$, and the $64(\mathrm{p, q})$ terms are determined from the ratio of contacts coordinates and substrate dimensions. For more details, see [9] and [10]. A high-speed computation of those coefficients can be made using the fast Fourier transform. Once the impedance matrix Zp is computed, one needs to invert it, to generate the admittance matrix Yp. The time and memory hungriest step in BEM is the storage and inversion of the impedance matrix. In general, the matrix Zp is very dense and its inversion involves such a considerable effort that it is difficult to handle problems with a large number of contacts [16].

B. Interblock Coupling

1) Fundamentals: Several investigations of the substrate noise coupling process were performed in order to capture their fundamental characteristics. As most CMOS logic elements can be reduced or decomposed into CMOS inverters, the designed substrate noise evaluation chips (Fig. 3) include N inverters with N varying from 12 to 1200.

For lightly doped substrate (the standard technology in RF ICs), it is obvious that the metal connecting the ground/V_{cc} substrate contacts provides the lower impedance path to spurious signals. In addition, the power supply noise is generally several orders of magnitude higher than spurious currents injected through the Sources/Drains into the substrate [6], [7]. As a consequence, our analysis will target the parasitic coupling between V_{cc}/ground contacts of the various blocks. On the other hand,

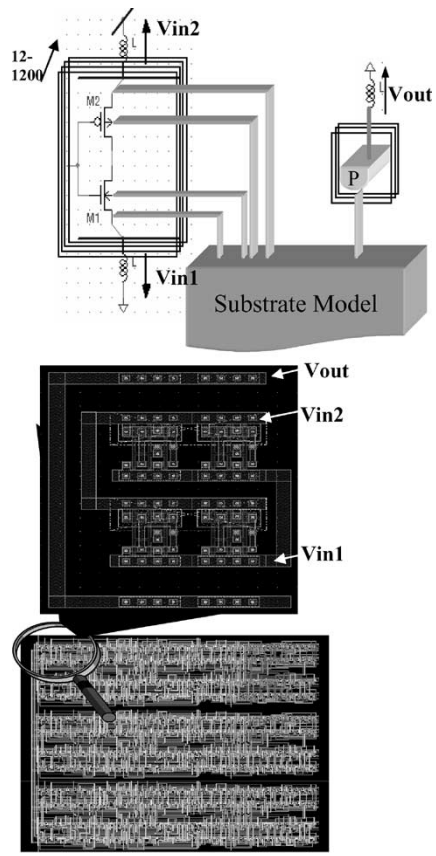

Fig. 3. Schematic and layout of substrate-coupling evaluation chip.

the FET and bipolar transistors have a capacitance to the substrate in the range of few fF and $Z(1\ \mathrm{fF}) \sim 1\ \mathrm{M\Omega}$ (at 0.15 GHz), which can be considered as infinite compared to typical substrate resistances. Consequently, we can predict that their presence around on-chip ground/V_{cc} contacts have no effects on the isolation between the ground/V_{cc} contacts. However, at the same time, the impedance of the transistors to substrate decreases at high frequency and for large circuits. Therefore, the first questions that emerge are: according to these considerations can we consider only ground/V_{cc} contacts of the chip while formulating the substrate model, and what the limit of that model is in terms of frequency and number of transistors? To answer these questions, simulations are performed on several chips with 12 inverters for the smaller and 1200 inverters for the larger. A typical tested chip schematic and layout are illustrated in Fig. 3. During this study, we will extract an accurate 3-D model for the substrate of each chip, using the FDM-based extractor SubstrateStorm [13] with very fine meshes, we will add the netlist of the circuits (i.e., inverters) and a typical package model (wires inductances $= 5$ nH), and afterward we perform the simulation of the transfer function $\mathrm{V_{out}/V_{in1}}$. As shown in Fig. 3 the transfer function $\mathrm{V_{out}/V_{in1}}$ represents the isolation between the noisy inverters on-chip ground contacts and the sensitive on-chip ground contacts. Two models will be compared. The first model is the *Full-SubMode,l* where the substrate model of the full layout considering PMOS, NMOS, Wells, V_{cc}, and ground contacts was extracted, the typical resulting network for one inverter is illustrated in Fig. 4(a). The second model is *the Simplified-Sub Model*, where the capacitors (i.e., nMOS

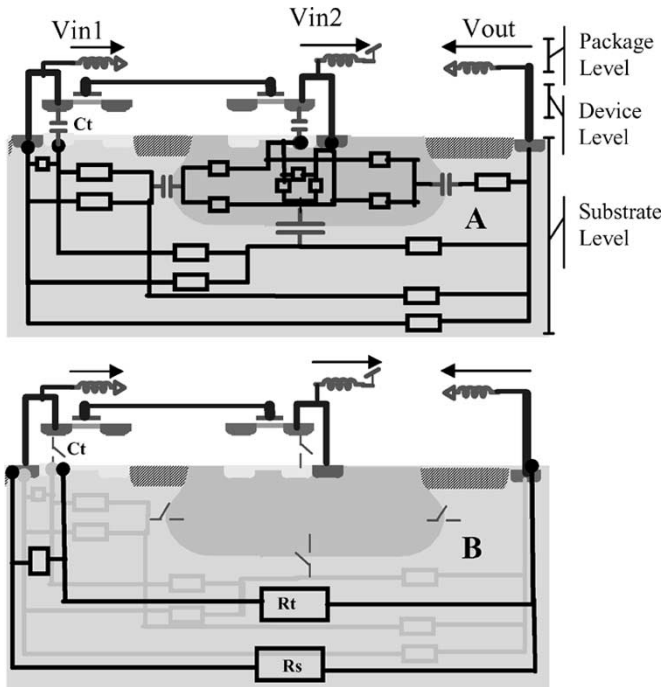

Fig. 4. Typical extracted network for one inverter: (A) with full SubModel; and (B) with simplified SubModel.

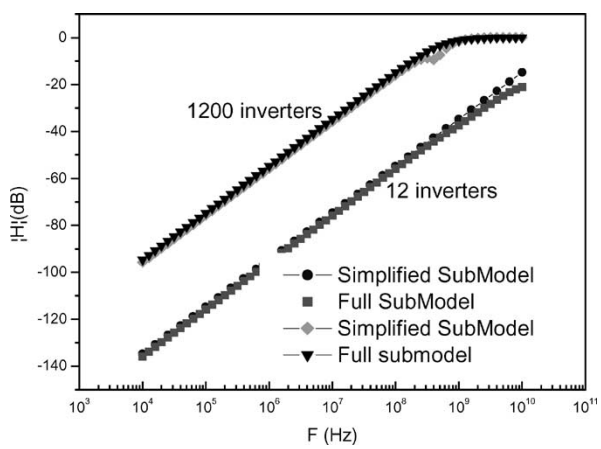

Fig. 5. On-chip ground-to-ground isolation ($\mathrm{H} = \mathrm{V_{out}}/\mathrm{V_{in1}}$) for 12 and 1200 inverters as a function of frequency using simplified and full substrate models.

to substrate capacitance and nwell to substrate capacitance) are considered as open circuits and so only ground contacts of the layout were considered for substrate modeling. The typical resulting network with *the Simplified-Sub Model* for one inverter is illustrated in Fig. 4(b).

As shown in Fig. 5, the simplified and full substrate models show an excellent agreement for all frequencies and numbers of inverters considered. The reason is as follows: the coupling path from V_{in1} to V_{out} can be decomposed into N parallel paths, and each path decomposed into tow principal coupling path [Fig. 4(b)] an indirect paths through the NMOS ($R_t + 1/j\omega C_t$) in parallel with a direct path through the substrate (R_{s}). The term $\ddagger 1/j\omega C_t + R_t \ddagger$ is much larger than R_{s} for two reasons: the low value of $C_t(\sim \mathrm{fF})$ and high value of R_t (indirect path). In addition, even if the equivalent impedance of the N indirect path ($R_t + 1/j\omega C_t$) decreases for large circuits (i.e., large N) the equivalent impedance of the N direct path (R_{s}) also decreases proportionally, and thus, remain the dominant coupling paths. Note that the package substrate system ($V_{\mathrm{out}} \approx jL\omega/(R_{\mathrm{s}} + jL\omega)$) becomes a high-pass filter, with a corner frequency of R/L.

For a final validation of the simplified model and a more realistic accuracy comparison, measurements on a real design (Fig. 6) that is representative of mixed signal design style and complexity are achieved. The tested circuit (Fig. 6) is a transceiver dedicated to ISM applications (see Section V for more details). In this circuit the power amplifier (block I) is the strongest noisy blocks and we would like to evaluate the isolation between their on-chip ground contacts and those dedicated to the other subcircuits of the chip (block II). The on-chip contacts of the chip are, however, physically inaccessible due the package, and the on-chip ac ground to ground transfer function considering the substrate, the package and the devices of the chip, such as those extracted by simulation and shown in Fig. 5, are impossible to achieve experimentally. To overcome this limitation, we have achieved dc measurements of the resistance equivalent to the distributed network linking the substrate ground contacts of the PA to the substrate ground contacts the other blocks. In fact, the package parasitics has only a negligible effect on dc measurements and hence the on-chip ground to ground substrate model can be measured from the outside that is through the package corresponding nodes. Afterwards, we have added to the measured substrate model the package model and the schematics of the circuits and we have used a SPICE-like simulator to achieve the ac simulation of the ground to ground isolation. The results are illustrated by curve (1) in Fig. 6. For comparison the same simulation is achieved, but instead of the measured network, an extracted network using FDM and considering only ground contacts of the layout [i.e., Simplified SubModel of Fig. 4(b)] is used. The results are illustrated by curve (2) in Fig. 6 and as expected the simplified substrate models shows a good agreement with the measured one for all the considered frequencies.

The second question now is, according to the fact that V_{cc} contacts are isolated using n-well in CMOS technology, can we neglect V_{cc}-to-V_{cc} and V_{cc}-to-ground coupling and consider only ground contacts of the layout when we perform the substrate model? To answer this question, simulations of the noisy-V_{cc} to sensitive-ground isolation [$V_{\mathrm{out}}/V_{\mathrm{in2}}$ Fig. 4(a)] were performed for the chips with 12 to 1200 inverters of Fig. 3 and compared with $V_{\mathrm{out}}/V_{\mathrm{in1}}$. The results are shown in Fig. 7. The values of ground-to-ground isolation ($V_{\mathrm{out}}/V_{\mathrm{in1}}$) are very low compared to V_{cc}-to-ground isolation ($V_{\mathrm{out}}/V_{\mathrm{in2}}$) values in low-frequency range and within the same order of magnitude in the high-frequency range. Therefore, the low-frequency components of the power supply noise at V_{cc} are effectively filtered by well-junction capacitances and the high-frequency components is only attenuated. Hence, neglecting the V_{cc} and wells in the substrate model can lead to an underestimation of the high-frequency noise effects.

In conclusion, by considering only a layout with V_{cc}, ground contacts and wells for substrate model we can analyze and compare the isolation between various blocks of the circuits without any significant loss of accuracy and with a considerable gain in

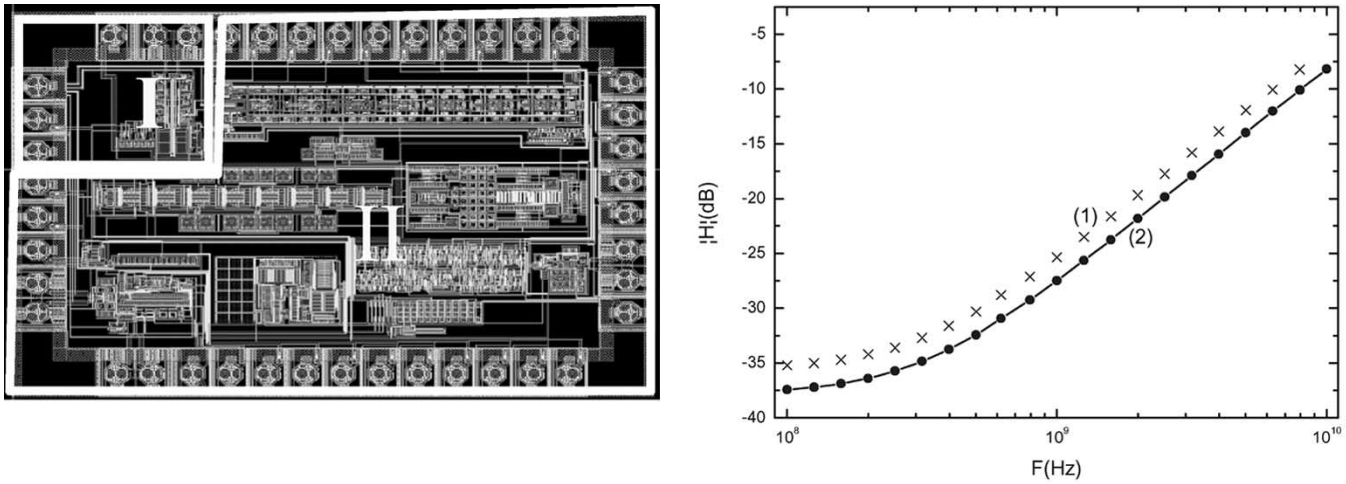

Fig. 6. Transceiver chip and the simulated ground-to-ground isolation between the PA (block I) and the other subcircuits of the chip (block II): (1) using the measured substrate model and (2) using the substrate model extracted by FDM.

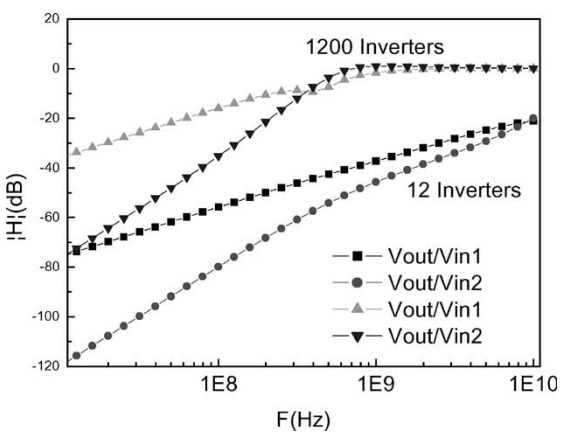

Fig. 7. On-chip V_{cc}-to-ground isolation ($V_{\mathrm{out}}/V_{\mathrm{in2}}$) and ground-to-ground isolation ($V\mathrm{out}/V\mathrm{in1}$).

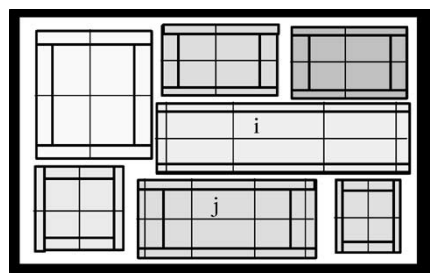

Fig. 8. MS-SOC Partitioning example for fast interblock coupling analysis.

terms of execution time and memory used. Note that all these simulations were repeated for various positions of the inverters and sensitive contacts on the chip, and exactly the same conclusions were made.

2) Numerical Analysis: FastBEM: As demonstrated in the previous section, a layout with wells, V_{cc}, and ground contacts, is sufficient to have an accurate representation of the interblock substrate coupling. Despite these simplifications of the layout, the resulting network remains too dense to enable the targeted full-chip analysis. Therefore, further modification in numerical methods has been made in order to reduce computational efforts. The crucial observation we make here is that the ground substrate contacts (or V_{cc} contacts) of each block of the chip are linked by metal lines. Hence, all substrate coupling paths between them are shorted. We can, therefore, consider the ground contacts (or V_{cc} contacts) of each block (supposed to have its own on-chip ground) as a single contact, while performing interblock substrate coupling. Consequently, the discretization explained in Fig. 8 is sufficient for an accurate interblock coupling representation.

In fact, since we focus on the coupling path between the various blocks of the chip, we can consider that the currents at the contacts positioned near the edges of each block are very high, compared to the currents at the contacts situated in its center. Therefore, the edge contacts are the most dominant coupling paths between blocks. This is the reason why a fine partition should be used in the edge regions. As we move toward the center of the block, the role of the contacts in the interblock coupling becomes progressively weaker, and hence, we can use increasingly coarser partitions. The currents at the ground contacts (respectively, V_{cc} contacts) of each partition are considered to be constant.

The question that emerges now is: how to exploit this partition to speed up the numerical computation? Let us consider two partitions of the chip i and j, having L and M number of contacts respectively (Fig. 8).

Since we assume that the currents (Ii) of the L contacts, the currents (Ij) of the M contacts are constant, the impedance $\mathrm{z_{ij}}$ representing the substrate coupling between the two partitions can be defined as

$$\mathrm{z_{ij}} = \frac{\overline{\phi_{\mathrm{i}}}}{\mathrm{I_j}} = \frac{\overline{\phi_{\mathrm{j}}}}{\mathrm{I_i}} = \frac{1}{\sum\limits_{\mathrm{l=1}}^{\mathrm{L}} \mathrm{s_l} \sum\limits_{\mathrm{m=1}}^{\mathrm{M}} \mathrm{s_m}} \int_{\sum\limits_{\mathrm{l=1}}^{\mathrm{L}} \mathrm{s_l}} \int_{\sum\limits_{\mathrm{m=1}}^{\mathrm{M}} \mathrm{s_m}} \mathrm{G(s,s')dsds'} \tag{3}$$

$\mathrm{s_l}$ and $\mathrm{s_m}$ are the surfaces of each contact in the partitions i and j ($\mathrm{l} \in [1, \mathrm{L}]$ and $\mathrm{m} \in [1, \mathrm{M}]$), G is the Green's function of the substrate, $\mathrm{I_{i,j}}$ and $\phi_{\mathrm{i,j}}$ are the current and the potential of the contacts in partitions (i and j) respectively. From a decomposition

of the integrals on each contact within the partitions i and j, we obtain

$$z_{ij} = \frac{1}{\sum_{l=1}^{L} s_l \sum_{m=1}^{M} s_m} \sum_{l=1}^{L} \sum_{m=1}^{M} \int_{s_l} \int_{s_m} G(s, s') ds ds'. \quad (4)$$

The double integrals in this equation represent the impedance between the contact l of partition i, and contact m of partition j. Thus z_{ij} can be represented by a sum of impedances (z_{lm}) between the contacts of each partition as

$$z_{ij} = \frac{\sum_{l=1}^{L} \sum_{m=1}^{M} z_{lm} s_l s_m}{\sum_{l=1}^{L} \sum_{m=1}^{M} s_l s_m}. \quad (5)$$

Using the same procedure with some algebra, we can relate z_{ii} to the impedance between the contacts of the partition i. Thus, we obtain

$$z_{ii} = \frac{\left(2 \times \sum_{l=1}^{L} \sum_{j=l+1}^{L} z_{lj} s_l s_j + \sum_{l=1}^{L} z_{ll} s_l^2\right)}{\left(\sum_{l=1}^{L} s_l\right)^2}. \quad (6)$$

As mentioned earlier, the time hungriest step in BEM is the storage and inversion of the impedance matrix. Our algorithm transforms this impedance from a matrix of M^2 elements, with M the number of contacts, to an impedance matrix of P^2 elements, with P is the number of partitions. Therefore, the gain in computational cost is evident. Suppose that the chip of Fig. 8 is composed of one million of contacts. The memory required to store the impedance matrix entries is $O(10^{12})$. If each block is decomposed into 1000 partitions, with a chip of 7 blocks, the memory requirement is $O(5.10^7)$. The memory gain is, thus, considerable (10^5). The inversion requirement by LU factorization, for example, is $O(10^{18})$, and the gain in execution time by our procedure is more important.

We would like to point out that the inversion of the matrix, without partitioning simplification, is problematic for another extremely important reason. The admittance matrix elements that we would compute are very heterogeneous. The yij corresponding to the geometrically distant panels are very small, especially for high-resistivity substrate and when the number of panels between the i and j is significant. At the same time, the yij elements corresponding to neighboring panels are very large. The system matrix that results, may be ill-conditioned. In this context, the unavoidable physical and numerical errors, although small, can lead to wrong results and even nonphysical values for a number of low yij elements. The meshing strategy resolves the problem due to the following three effects. First, the number of matrix entries is significantly reduced, which decreases the numerical inversion errors. Second, by choosing the edge partition to be smaller center then center one (Fig. 8), the large elements of the current density vector near the edges are compensated by smaller area, so that more uniform total current vector is obtained. Third, by decreasing the number of effective contacts that can exist between geometrically distant ones, we reduce the probability of having very weak y_{ij} elements. The algorithm of the method is represented below:

```
FastBEM for interblock model (Algorithm 1)
Compute the K1(p,q) coefficients;
Discretize The chip of M blocks into L
partitions; /* L is an accuracy control
parameter see Fig. 8*/
Discretize M ensemble of ground/Vcc con-
tacts into X ensemble; /* each ensemble
in each partition is considered as inde-
pendent*/
Compute the [Z] matrix;
For j from 1 to X
 For i from 1 to X
   for k from 1 to Aj /* Aj nbr of con-
tacts in the ensemble j*/
    for r from 1 to Ai /* Ai nbr of con-
tacts in the ensemble i*/
     Compute zkr;
   Compute zij; /* from (5) if i  =  j else
from (6)*/
 Compute the [Y] = [Z]^-1 matrix; /* By LU
fact. (cost = O(n^3)) or GMRES (cost = O(n^2)) */
Compute the [R] matrix;
For i from 1 to X
 j from 1 to X
  Rij= -1/Yij; /* for i ≠ j */
  Rii= 1/[Yii+(∑Yim)i≠ m]; /* for i = j */
```

C. Intrablock Transistor-Level Coupling

Once the block-to-block substrate coupling is well represented, we are interesting on the intrablock coupling. For this, we will distinguish between the noisy block modeling and the sensitive block modeling.

1) Sensitive Analog Block: The sensitive analog blocks can require a more accurate substrate model. In fact, for some analog circuits, the substrate resistances can have a direct effect on their performances, independently of the noise coupling. For instance, the noise figure of an LNA can be affected by the substrate resistance thermal noise. The substrate resistances can also result in a change in the input/output matching of LNA, reducing its gain and its reverse isolation [26]. Moreover, The standard process technologies, produces substrate with three-dimensional (3-D) contacts (wells, collectors), vertical and lateral doping profiles (channel stop, well, triple-well, buried layer, heavily doped bulk substrate, etc.), and complex 3-D structures (trench oxide, thick metal, integrated inductor, bonding path…). Using a multilayer substrate representation, the BEM handles vertical conductivity variation with high accuracy, but ignore totally its lateral variation. This situation can leads to severe errors in the substrate models of the 3-D structures. For this reason, in all modern analog and RF process technologies, an accurate scalable substrate model deduced from measurements is added the SPICE models of all critical components such as passive elements (varactors and inductors) as well as active elements such as bipolar transistors. The substrate of those elements is

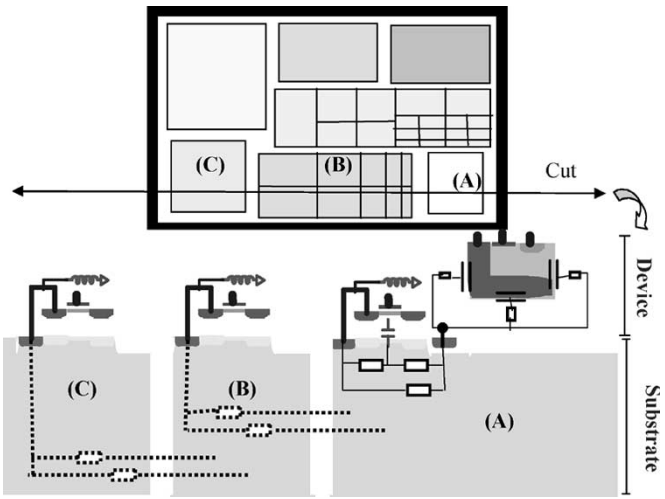

Fig. 9. MS-SOC partitioning example for fast intrablock coupling analysis of the targeted sensitive block and 2-D representation of the corresponding substrate with the resulting network.

thus handled at device-level as illustrated in Fig. 9, and the intrablock model will be used only to link their ground contacts to the other elements of the layout. Windowing strategy, considering only this part of the chip (block A) can be used to extract this interblock substrate network. However, the substrate resistance between the ports at the edge of the considered block can be influenced by the interblock coupling of this block to its neighbors.

To consider the effects of the interblock coupling on the intrablock substrate model without a significant increase in the computational cost the methodology based on the partitioning of Fig. 9 is proposed. The partitioning process used for transistor-level coupling analysis is the inverse of the one used for interblock coupling. We use very fine partitions inside the sensitive block of interest. The partitions increase in size as we go far from the analyzed block. The partition around the analog block of interest, are only used for modeling the effects of distant contacts on the intrablock resistances values, and since this effect becomes negligible as we go far from the analyzed block the partitions become coarser.

It is worth noting that only the part of the resulting block-to-block network concerning the substrate coupling of the block (A) to their neighbors is accurately represented when we use the partition of Fig. 9. Therefore, once the intrablock coupling is finished, we eliminate the block-to-block network (elements represented by dotted lines in Fig. 9) and we replace it the network extracted by the interblock methodology of Section III-B2. As for interblock strategy, the currents in the partitions around the handled circuit will be supposed constant, and the same analytical formula [(5) and (6)] will be used to speedup the computation and avoid a large ill-conditioned matrix. The algorithm of the method is represented below.

```
FastBEM for intrablock model (Algorithm 2)
Discretize The chip of M' blocks into L'
partitions; /* L' is an accuracy control
parameter see Fig. 8*/
Discretize M ensemble contacts into X'
ensemble; /* each ensemble in each parti-
tion is considered as independent*/
Compute the [Z'] matrix;
For j from 1 to X'
 For i from 1 to X'
   for k from 1 to Aj' /* Aj nbr of con-
tacts in the ensemble j*/
    for r from 1 to Ai' /* Ai nbr of con-
tacts in the ensemble i*/
     Compute z'_kr;
   Compute z'_ij; /* from (5) if i = j else
from (6)*/
 Compute the [Y'] = [Z']^-1 matrix; /* By LU
fact. (cost = O(n^3)) or GMRES (cost = O(n^2)) */
Compute the [R'] matrix;
For i from 1 to X'
 j from 1 to X'
  R'_ij = -1/Y'_ij; /* for i ≠ j */
  R'_ii = 1/[Y'_ii + (∑ Y'_im)_i ≠ m]; /* for i = j */
```

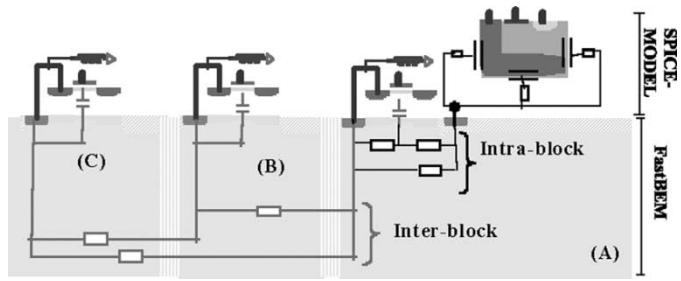

Fig. 10. MS-SOC substrate model example with interblock and intrablock resulting network.

2) Noisy Blocks: In addition to power-supply noise, the switching activity of digital blocks injects spurious signals in the substrate through the reverse junction capacitances of transistors or by impact ionization (hot carriers). Transistor neighboring substrate contacts pick up the most of these signals. We can expect that the substrate model at transistor level will have an effect on this kind of noise. We can also predict that connecting the bulk of each transistor directly to ground will represent the worst coupling case. The circuits optimized with this configuration will work, but with a larger margin than necessary. On the other hand, each transistor is linked to substrate ground by impedance equal to $(\mathrm{Rs} + 1/\mathrm{jCw})$. As C is of about few fF, the substrate resistances play only a negligible role in this coupling. In conclusion, for all noisy blocks, we can connect the bulk of NMOS transistors directly to ground (respectively, PMOS to V_{cc}) without a significant loss of accuracy.

Finally, the full resulting network after inter and intrablock methodology application is illustrated in Fig. 10

D. Computational Results

In this section, we present examples that show the accuracy and the efficiency of the proposed methodology. We focus on the interblock substrate modeling, since it is the crucial process,

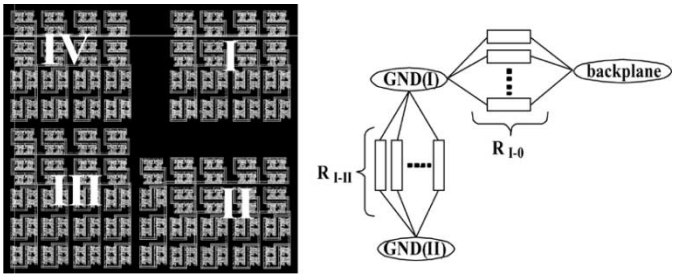

Fig. 11. Overview of substrate coupling evaluation chip. Test structure [4 blocks (I-III, and IV) – 864 Inverters – 600 × 600 μm] and an example of the extracted substrate model.

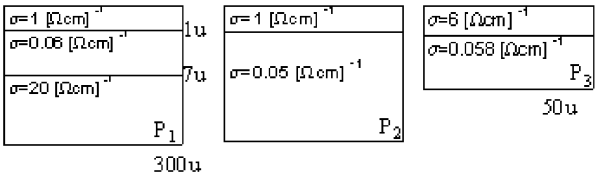

Fig. 12. Substrate profiles used for extraction: P_1 low-resistivity substrate; P_2 high-resistivity substrate; P_3 high_resistivity and low substrate thickness.

enabling us to evaluate the efficiency of the isolation strategy adopted, such as the block placement, the guard ring distribution, the multiple bond-path assignment, etc.

A real design, that is representative of mixed-signal design style and complexity, will always give the most realistic accuracy benchmark results. At the same time, most CMOS logic elements can be reduced or decomposed into CMOS inverters. Therefore, the test layout used for preliminary verifications is presented in Fig. 11. It is composed on 4 blocks (I-IV) representing 864 inverters.

Several experiments, using three substrate doping profiles (see Fig. 12), will be performed. The first two profiles are the low-resistivity and the high-resistivity profiles used in typical CMOS and BiCMOS technology. The third one is the high-resistivity substrate, but with only 50 μm as thickness. The weak thickness will enable a fine meshes discretization, for an accurate FDM analyzes. The FDM and classical BEM will be used for the comparisons. For most design teams, accuracy is the most important aspect of an extraction benchmark. For each of the substrate profiles indicated, extraction was performed between the ground and the V_{cc} contacts of the blocks.

Table I(a) and (b) shows the interblock computed resistances with BEM and the proposed method (Fast BEM), of respectively Substrate P1 and P2 of Fig. 12. As shown in Fig. 11, R I-0, for instance, is the computed resistance between the ground contacts of block I and the backplane of the substrate and R I-II is the resistances between the ground contacts of block I and those of block II. Table II shows a comparaison between the results of BEM, FastBEM, and FDM in the case of P3 profile (Fig. 12). The agreement between the results of BEM, FDM, and FastBEM (Algorithm 1) is evident for all profiles considered.

Table III summarizes the computational cost of the three methods. "Runtime line" represents both User (the time to execute the command run_extraction_job) System (the additional system time to complete the job) time of the extraction including postprocessing. "MaxMem line" represent the peak memory usage over the total runtime, including input data processing, parasitic extraction, and writing outputs. For runtime, as for peak memory usage, the supremacy of the FastBEM is evident. It should be noted also that this supremacy is increasingly important as the test cases will include a larger and more complex designs.

TABLE I
INTERBLOCK SUBSTRATE RESISTANCES OF THE TEST-CHIP: LOW-RESISTIVITY PROFILE P_1 (ON THE LEFT); HIGH-RESISTIVIY PROFILE P_2 (ON THE RIGHT)

R	BEM	FastBEM
I-0	95	95
II-0	76	76
III-0	75	75
VI-0	94	94
I-II	9119	9180
I-III	10642	10694
I-VI	12325	12743
II-III	6829	6930
II-IV	10670	10740
III-IV	7932	7919

(a)

R	BEM	FastBEM
I-0	791	801
II-0	721	717
III-0	746	746
VI-0	835	836
I-II	1587	1712
I-III	7412	8113
I-VI	1763	1822
II-III	825	856
II-IV	7330	7836
III-IV	956	1133

(b)

TABLE II
INTERBLOCK SUBSTRATE RESISTANCES OF THE TEST-CHIP USING LOW-RES, PROFILE P_3

R	FDM	BEM	FastBEM
I-0	117	115	115
II-0	104	104	104
III-0	105	107	108
VI-0	121	121	121
I-II	1172	1036	1067
I-III	-	17069	20050
I-VI	1183	1123	1204
II-III	352	328	349
II-IV	-	14087	1561
III-IV	430	407	412

TABLE III
PERFORMANCES COMPARISON BETWEEN THE EXTRACTION METHODS IN THE CASE OF P3 PROFILE

Profil(P_3)	K(p,q)	BEM	FastBEM	FDM
Runtime user+sys	1mn 14s	4mn 30s 3mn 16s (*)	1mn 18s 4s (*)	1h 3mn
MaxMem	9328K	17M	9328K	1200M

(*) i.e., without $K(p, q)$ computation time

IV. METHODOLOGY FOR A FINAL OPTIMIZATION

The final stage of our methodology is named **SubCirII,** and its flowchart described in Fig. 13. In this approach, we use the full package and substrate model in an iterative verification procedure of large varieties of isolation strategies. The visited strategies are those mentioned in Section I, that is: floorplanning, guard ring placement, pinning strategy, etc. This methodology will enable us to achieve the best noise rejection, by choosing the best isolation techniques for a given technology, circuit and package. We can also verify if we can meet the attenuation specified in SubCirI without changing the package or splitting the digital and the analog parts of the circuits.

The attenuation between sensitive and perturbing parts of the circuits depends essentially on substrate, package, and wire par-

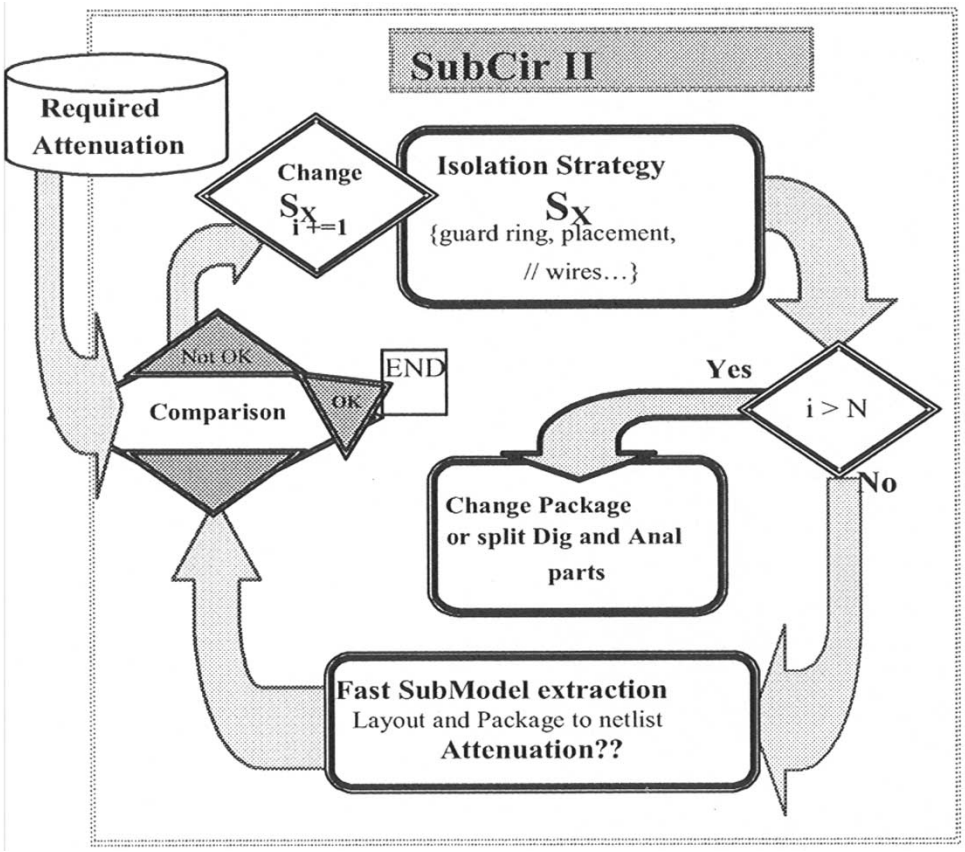

Fig. 13. Flow diagram of SubCirll methodology.

asitics. The algorithm developed in Section III-B2 fits very well the low computational efforts and accuracy requirements of this iterative method. In fact, the verification and comparison of large variety of isolation strategies are necessary to achieve the best noise rejection. For this purpose, we can also use a suite of tools based on numerical FDM. The base feature of the numerical method (FDM) is the high accuracy of the generated 3-D substrate model, since it can handle lateral and vertical resistivity variations and also arbitrary substrate geometry. The full chip simulation, however, makes the exact substrate coupling evaluation cumbersome. This problem is particularly critical for lightly doped substrate where the single-bulk-node model is not valid and a mesh over the entire substrate is necessary. Although sparse nonuniform grids can be used to speed up the extraction, an enormous amount of the surface mesh is necessary to match the full layout.

V. Case Study

The first purpose of this study is to show how to use the methodology, SubCirI, to help a single-chip integration of a BiCMOS super-regenerative transceiver dedicated to ISM applications [22], [23]. The substrate used is lightly doped with a resistivity of 20 Ω-cm. The basic block diagram of a super-regenerative receiver is very simple [22]: the RF input is connected to an isolation amplifier, followed by a gain stage connected in closed loop with a selective network. This stage represents an oscillator whose startup time depends on the RF signal at the input. The gain of the amplifier is periodically modified

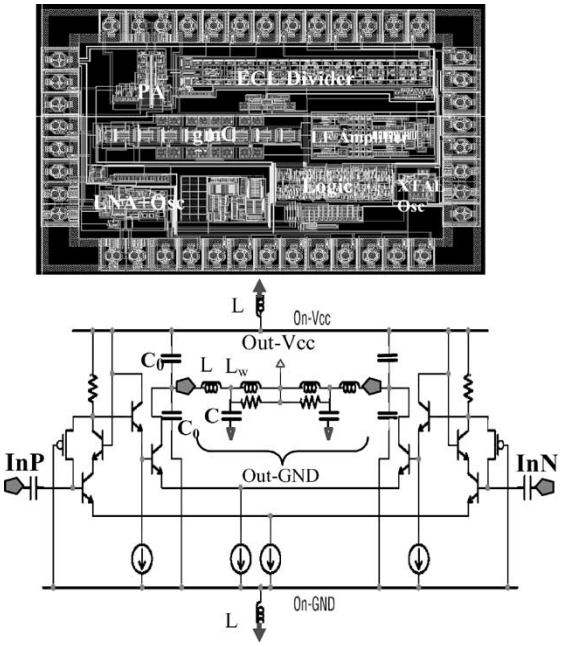

Fig. 14. Transceiver chip and PA schematic. Version l(load 1 with only off-chip C): $C = 5.5$ pF; $L = 5$ nH; $R = 300\ \Omega$; Version 2(load 2 with only on-chip C_0):$C_0 = 2$ pF;$L = 5$ nH; $R = 300\ \Omega$.

below and above the critical oscillating conditions by the quench signal and the demodulation is achieved through detection of the envelope of the output signal of the oscillator. The transmitter is based on the oscillator of the receiver. This oscillator,

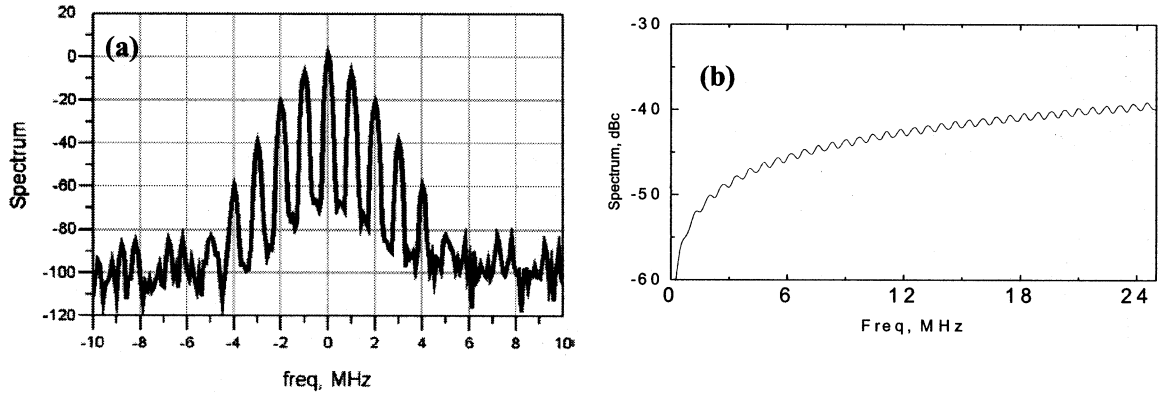

Fig. 15. (a) Spectrum of spurious tones generated by a 0.01 V/1 MHz signal at the control path of the oscillator. (b) The maximum tolerated noise PSD by the oscillator to have an out-of-channel spurs lower than -70 dBc.

which is followed by a power amplifier (PA), is able to deliver a minimum of 0 dBm to a differential load. In this design the power amplifier, with its associated bond-path and wires are the strongest transmitters of cross-talk.

In the first designed version, an off-chip load-resonant (without the on-chip capacitors C_0: version1 Fig. 14) is designed to restore a 916 MHz sinusoidal voltage at the antenna and suppress their higher harmonics. A fully differential design is used to minimize the substrate noise injection and the transient currents in the power supply. However, the oscillator is the best receiver of cross-talk and even a low noise coupling from the PA can result in its malfunction and, therefore, the instability of the system.

According to our methodology (Fig. 1), we focus on the oscillator as the potential "listener" and the PA as the possible "talker." The oscillator is designed to have less than -100 dBc/Hz of phase noise at 500 kHz offset. Generally, to meet the Federal Communication Commission (FCC) regulation, the 902–928-MHz ISM band is partitioned into 54 channels, requiring a frequency resolution of 482 kHz in the synthesizer [25]. In our design, to preserve the required SNR in the adjacent channels, we specify a certain spectral purity with spurious tones below -70 dBc at 482 kHz offset from the carrier. In the oscillators, the environmental noise translates to spurs by frequency modulation FM phenomena. In fact, the noise corrupts the dc voltage applied across the varactors, and varies the tank capacitance and hence the resonance frequency. Viewed as analog FM, this effect translates low-frequency noise components in the control path to region around the carrier [4]. The example of spurious tones generated by a 0.01-V/1 MHz signal at the control path of our oscillator is shown in Fig. 15(a). Therefore, by applying sinusoidal signals with various amplitudes and frequencies at the control path, we can determine the maximum amplitude that the oscillator can tolerate without generation of FM spurs higher than -70 dBc beyond 482 vHz offset from the carrier. To compare these signals to power spectral density (PSD) of the PA noise, their amplitudes will be translated to a power spectrum. The results are represented in Fig. 15(b). The PA noise generated at its on-chip ground and its PSD is represented in Fig. 16. The peak-to-peak noise reaches its maximum (0.14 V) when the PA switches from off-mode to on-mode. The PSD of the noise indicates that most of the

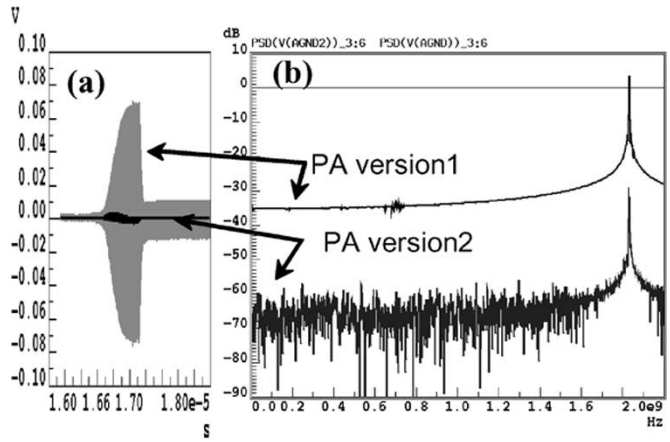

Fig. 16. (a) PA noise waveform and (b) its PSD at the off–on transition.

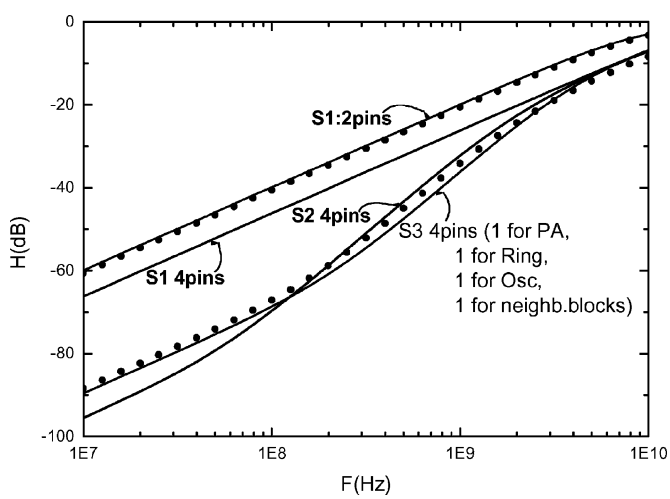

Fig. 17. Comparison between the results of S1, S2, and those of the adopted strategy for the final design, S3. The extractions are performed both by FastBEM (dotted lines) and by the FDM (continuous lines).

TABLE IV
RUNTIME COMPARISON BETWEEN THE EXTRACTION METHODS (FDM AND FASTBEM) FOR EACH ITERATION OF SUBCIRLL

	K(p,q)	Fast BEM	FDM
Runtime User+Sys.	1mn 14 s	4mn 24s	1h 30mn 40s

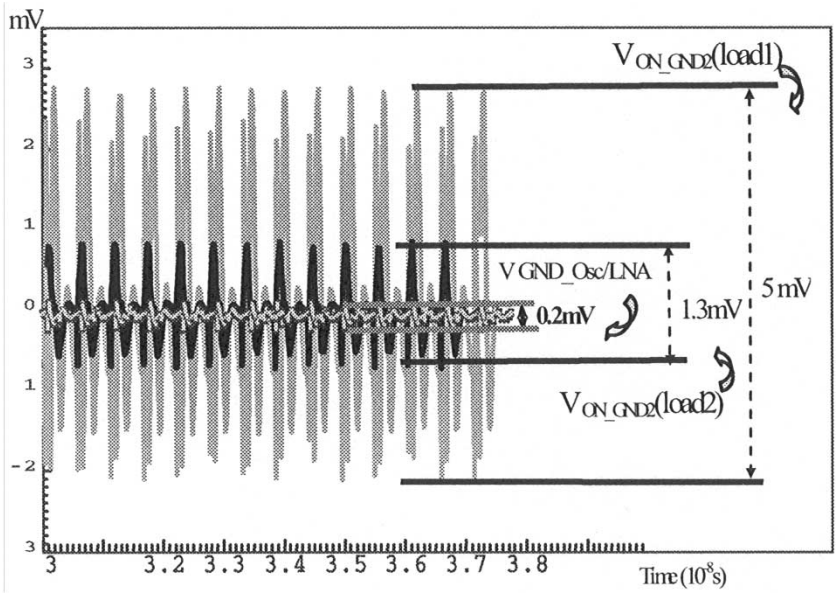

Fig. 18. Noise waveform at the on-chip ground used to bias exclusively the substrate for the two versions of the PA ($\mathrm{V_{ON_GND2}}$(Loadl/2)), and the noise waveform detected at the GND of the oscillator ($\mathrm{VGND_Osc/LNA}$).

spectrum is located around 1.8 GHz (twice the input/output frequency). This is due to the differential topology of the PA. In low-frequency (LF) range, the PSD of the noise is around -37 dB. The maximum tolerated noise in the control path of the oscillator is, however, in the range of -60 to -40 dB as shown in Fig. 15(b). Therefore, the PA generates a supply noise PSD of 3 to 23 dB higher than the maximum tolerated by the oscillator.

To preserve the functionality of our system we have the choice between two solutions: redesign the PA to generate less noise or add a voltage regulator circuit to the oscillator with bandgap reference to decouple the VCO and its control path from on-chip power supply. It is obvious that the first solution is the best, since it provides a quiet environment and therefore avoids the corruption of other circuits by the PA noise.

The method proposed to avoid the generation of the high frequency noise at the bond wires is based on the exploitation of the filtering properties of the load-resonant. In fact, coupling the on-chip ground and V_{cc} to the outputs of the PA using the on-chip capacitances C_0 (Fig. 14) instead of the use of the off-chip C, results in a significant decrease in the on-chip ground and V_{cc} impedances. The schematic of the redesigned PA according to this technique is shown in Fig. 14 (PA version 2). The peak to peak noise at on-chip ground, which is proportional to this impedance ($\Delta V \approx Z_{dL} di/dt$) is, therefore, strongly reduced. To avoid the generation of low-frequency noise, an on-chip ground different from that of the circuit, is used to bias the substrate. The low transistor junction capacitances between the noisy ground of the circuit and the substrate contacts strongly attenuate the low frequency noise.

The noise PSD generated by the PA at LF range is reduced from -37 dB for PA version 1 to -70 dB for PA version 2 as shown in Fig. 16, and thus becomes lower than the maximum noise tolerated by the oscillator.

Finally, during the physical implementation of the various blocks, we can start the application of methodology SubCirII. As mentioned in the introduction, several noise-transfer reduction techniques are reported in the literature. Usually, the efficiency of these techniques depends on the design parameters, such as the resistivity of the substrate, the bond-wires inductance values, the frequency of the noise etc.

In this paragraph, we show how the methodology SubCirII allows us to verify and compare the efficiency of the various strategies and to achieve the optimal quiet noise environment for our circuit. To speed up the substrate model extraction, and therefore to enable an iterative verification of these strategies, the simplified model (outlined in Section III-A) that takes into account only the coupling between ground taps is used. Note that, since the technology used is BiCMOS, the amount of V_{cc} substrate contacts is very low and have negligible effects on substrate coupling. The layout of the transceiver is represented in Fig. 14. Both the FDM and the improved BEM (FastBEM) were used for the substrate modeling in each iteration. Similar results between the FDM and the FastBEM techniques were found as shown in Fig. 17 (continuous lines for FDM and dotted lines for BEM). However, the time and memory gain is considerable when we use the improved BEM as illustrated in Table IV.

The first visited strategy by the loop (named S1) consists of the increase of the number of the package pins and wires. The second strategy (S2) consists of the use of separate on-chip grounds for the Oscillator-LNA and the rest of the circuit. The effect of S1 is illustrated by solid lines (Fig. 17): top curve for 2 pin-wires (One for the PA and one common pin for the Oscillator-LNA and neighboring blocks-peripheral to the circuit), and bottom curve for four pin-wires (one for the PA and three common pins for the Oscillator-LNA and neighboring blocks-peripheral to the circuit). The isolation is improved by about 16 dB when the number of package pins is increased from 2 to 5. This is mainly due to the reduction of the bond-wire inductance value, which results in an on-chip GND close to the external reference (off-chip GND). Beyond five package pins, the improvement of the isolation becomes negligible. In addition, this

improvement is practically independent of the frequency. The effect of S2 is illustrated by the dotted line. For the same number of package pins (that is, four), the separation of the GND improves the isolation by 25 dB at 100 MHz and 10 dB at 1 GHz in comparison to S1. In addition, it is verified that the improvement due to the increase in the number of pins is negligible when the on-chip grounds are separated.

The strategy adopted for the final iteration is S3. It consists of placing and biasing guard rings. Compared to S2, for the same number of pins (that is, four); the placement of a guard ring, with dedicated pins, around the amplifier allows a significant improvement at high frequency (10 dB at 1 GHz) as shown in Fig. 17. It should also be noted that this result is practically independent of the size of the guard ring. The improved design of the PA (Fig. 14) is combined with the isolation strategies S3, to ensure a quiet environment for the oscillator. The results are illustrated in Fig. 18.

The waveform of the noise detected at the ground of the oscillator after applying strategy S3 is also represented by the curve $V_{\mathrm{GND_Osc/LNA}}$ in the same figure. It is evident that the combinations of the PA low noise-supply technique and the optimal isolation strategy S3 lead practically to the elimination of substrate noise coupling in our circuit. The performances of the final version of the transceiver were found to be in agreement with the initial specifications. The measured transmitter current with an output power of 0 dBm on a 300 Ω resonant load is 6 mA. The maximum operating frequency measured with a chip-on-board technology is 1.5 GHz.

VI. Conclusion

In this paper, we have focused on the development of methodologies for the analysis and optimization of substrate noise effects in mixed-signal circuits. Two methodologies were elaborated: one for an early design verification, and another for a final verification/optimization of the noise immunity of the circuits. A new approach, which combines a thorough physical comprehension of the noise coupling effects and an improved version of the BEM, to accelerate the substrate model extraction and enable the use of the iterative optimization procedure is proposed. These methodologies have been successfully employed to verify the functionality of the components of an RF system, and to make sure that they meet the specified figures of merit before being assembled together. The redesign of the PA results in a reduction of low frequency spurs around the carrier by about 30 dB. The iterative optimization procedure enables us to increase the isolation between the noisy PA and the sensitive oscillator, by about 40 dB in medium frequency range and 30 dB around 1 GHz.

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