Modeling Stressed MOS Oxides Using a Multiphonon-Assisted Quantum Approach—Part II: Transient Effects

Davide Garetto, Yoann Mamy Randriamihaja, Denis Rideau, Alban Zaka, Alexandre Schmid, Yusuf Leblebici, and Hervé Jaouen

***Abstract*—Multifrequency charge pumping analysis has been performed using a multiphonon-assisted charge trapping model in the view of analyzing the oxide region in energy and position that can be characterized using charge pumping (CP) characterization. Transient phenomena observed during CP and ac characterization (hysteresis loops) have been modeled, and the role of out-of-equilibrium quasi-Fermi levels in proximity of the Si/SiO$_2$ interface has been studied in detail.**

***Index Terms*—Charge pumping (CP), charge trapping, multiphonon-assisted model, oxide degradation.**

I. INTRODUCTION

THE CHARACTERIZATION and extraction of defect concentrations in CMOS oxides are challenging device reliability tasks due to the complexity of the trapping mechanisms in oxide and interface defects. For this reason, several techniques are employed to extract the defect concentration in electrically stressed oxide layers, including capacitance/conductance voltage (CGV) methods [1]–[3], charge pumping (CP) characterization [4]–[6], random telegraph noise measurements [7], [8], scanning tunneling spectroscopy (STS), and time-dependent defect spectroscopy (TDDS) analyses [9]. Multifrequency charge pumping (MFCP) techniques are increasingly adopted to determine the defect distribution $N_T(x, E_T)$ in particular regions of the oxide. Although multistate [8], [9] and multiphonon-assisted models [10]–[14] have been proposed for the analysis of trapping dynamics, the interpretation of the electrical characteristics generally relies on simplified compact analytical approaches [1], [3], [6], [15], [16]. In particular, the sensitivity and dependence of the MFCP current on the pulse characteristics as well as on the nature of the defects has been demonstrated significantly more intricate for traps located within the dielectrics than for interface traps [6]. This aspect reinforces the need for a rigorous approach in modeling the transient dynamics of charge trapping.

In part I [17], a multiphonon-assisted impedance model has been described and validated on ac measurements. This study has been performed considering equilibrium conditions for dc and small-signal ac analysis [17], and the region of the dielectric layer characterized with capacitance measurements has been determined.

In this paper, the multiphonon-assisted model presented in [17] is applied to the analysis of transient effects on ac characteristics and to the assessment of MFCP measurements for trap dynamics analysis. The proposed model can be adopted to evaluate the accuracy of trap extraction techniques and for the determination of the spatial and energetic distribution of defects. This paper is organized as follows. In Section II, the validity of trap equilibrium conditions is investigated. Out-of-equilibrium conditions and transient effects in MFCP characteristics are investigated in Section III. The dependence of the CP current and of the extension of the probed region on CP pulse parameters is also discussed. Section IV details the role of capture/emission (C/E) dynamics of oxide traps on hysteresis loops in ac characteristics.

II. EQUILIBRIUM CONDITIONS AND TRAPPING DYNAMICS

Let us consider a cross-sectional plane in the dielectric at a given oxide depth x. During a transient pulse, we can assume that each individual trap at depth x exchanges carriers only with the channel and the gate. In the present 1-D model, transverse directions (y, z) are not explicitly accounted for. The large number and variety of defects that can be present in the cross-sectional plane at x have been associated to an energy distribution. Moreover, carrier exchange by trap-to-trap tunneling has been neglected.

The rate equation needs to be solved for each energetic level, calculating the quasi-Fermi level E_F in the oxide stack for all the possible trap energies E_T. Thus

$$N_T(x, E_T) g \frac{\partial f_T}{\partial t} = \Big[\Phi_c(x, E_T, t) + \tilde{\Phi}_e(x, E_T, t) - \Phi_e(x, E_T, t) - \tilde{\Phi}_c(x, E_T, t)\Big]. \quad (1)$$

Traps follow a spatial and energetic distribution $N_T(x, E_T)$ in the oxide layer, $f_T(x, E_T, E_F, t) = 1/(1 + \exp((E_T - E_F)/k_B T))$ is the electron trap occupation, the holes (electron,

Manuscript received July 1, 2011; revised December 6, 2011 and December 13, 2011; accepted December 14, 2011. Date of publication January 26, 2012; date of current version February 23, 2012. The review of this paper was arranged by Editor B. Kaczer.

D. Garetto is with IBM STG, 38926 Crolles, France, and also with the École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland (e-mail: david.gigabyte@gmail.com).

Y. M. Randriamihaja, D. Rideau, A. Zaka, and H. Jaouen are with STMicroelectronics, 38921 Crolles, France.

A. Schmid and Y. Leblebici are with the École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2181389

0018-9383/$31.00 © 2012 IEEE

respectively) C/E fluxes $\tilde{\Phi}_C/\tilde{\Phi}_E$ (Φ_C/Φ_E, respectively) have been calculated as in [17] and [18], and g is a charge factor introduced to take into account the defect charging model. The general approach of (1) is required to accurately take into account the out-of-equilibrium conditions of the system.

It should be pointed out that the attribution of a quasi-Fermi level to a single defect has been only performed in the view of better illustrating the *equilibrium* steady state condition. Indeed, in part I [17], the dc operating point for the ac analysis has been calculated in quasi-static conditions, neglecting all the large-signal transient effects. After a sufficiently long time, the defects establish a common equilibrium condition with the substrate/gate, and their quasi-Fermi levels equal the one in the carrier reservoirs. Under this equilibrium condition, a uniform quasi-Fermi level is eventually established for all the defects located on an entire device cross section x. In practice, since $E_F(x)$ is the same for the totality of defects at depth x, the rate equations describing the dynamics of the different traps can be summed term-to-term, and a single rate equation controlling the trapping dynamics is obtained. Thus

$$\int_{E_T} N_T(x, E_T) g \frac{\partial f_T(x, E_T, E_F(x,t), t)}{\partial t}\, dE_T = \int_{E_T} \left[\Phi_c(x, E_T, t) + \tilde{\Phi}_e(x, E_T, t) - \Phi_e(x, E_T, t) - \tilde{\Phi}_c(x, E_T, t)\right] dE_T. \quad (2)$$

Equation (2) differs from (1) as it includes the integration over trap energy E_T. In the following, this approach will be referred to as "quasi-equilibrium" (QE) approximation. In such an approach, nonequilibrium effects on f_T are neglected. As pointed out in this part II, the QE approximation can lead to unphysical interpretations when large signals are applied. Moreover, since the approximation still remains applicable to small-signal ac analysis (part I) and this solution is sensibly more efficient compared with the general approach, it is important to discuss the range of validity of this solution and its consequences on the misleading interpretations of transient results.

III. MFCP

A. Calibration Methodology

In this section, MFCP and ac results have been analyzed to investigate the importance of transient out-of-equilibrium effects on CP characteristics and the relevance of the methodology applied for the extraction of trap concentration profiles.

In a first step, ac characteristics, measured on electrically stressed multifingered nMOS devices integrated in a 65-nm technology, have been compared with simulation results by solving (2) in dc equilibrium conditions. The extracted spatial/energetic defect profile follows a bivariate Gaussian distribution, whose validity has been discussed in part I [17].

In a second step, for the same stress conditions, CP measurements have been performed applying periodic pulses on the gate of the CMOS device. Channel inversion occurs in the

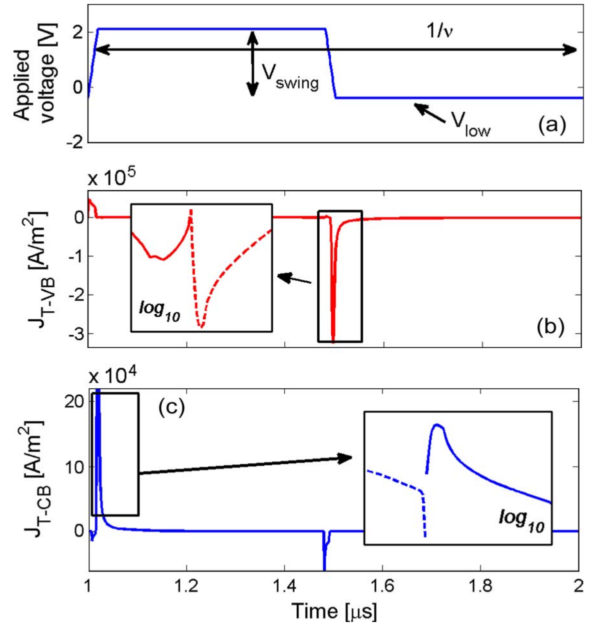

Fig. 1. (a) Pulse applied for CP analysis. Both the amplitude of the pulse, the voltage swing $V_{\rm sw}$, and the frequency have been varied. (b) Simulated current density generated by the capture emission of holes from the valence band of the substrate. Similar results are also shown for the C/E flow of electrons on the conduction band of the Si substrate in (c). Insets indicate the current components in log scale during the transition phases: (solid red) h^+ emission dominating, (solid blue) e^- capture dominating, (dashed red) h^+ capture dominating, and (dashed blue) e^- emission dominating.

high phase of each pulse, and the oxide and interface defects capture electrons from the conduction band. When the voltage decreases to the low-level region, trapped electrons recombine with holes captured from the valence band [6]. Carrier emission toward the gate can also occur. This contribution becomes dominant in ultrascaled oxide layers [19]. All the aforementioned effects have been considered in the model.

As reported in [20] from large-signal voltage sweep characteristics indicated (not shown here), trap recovery can occur during the application of typical CP pulses, and the CP current has been shown decreasing with time. Therefore, since trap recovery phenomena are not considered in the proposed implementation of the model, the results illustrated in this paper could be considered as an effective averaged response of the defects for the totality of the applied CP pulses.

Fig. 1(a) shows a single simulated CP pulse applied to the device. The analysis has been performed varying the low base voltage bias $V_{\rm low}$ from -2 to 0.5 V, whereas the amplitude of the applied pulse, i.e., the swing voltage $V_{\rm sw} = V_{\rm high} - V_{\rm low}$, ranges from 0.8 to 2.5 V. The signal frequency ν is varied from 1 kHz to 1 MHz. Three square pulses have been simulated to avoid the presence of undesired transient effects originated from the initial equilibrium condition.

The transient trapping currents are shown in Fig. 1(b) and (c) and can be expressed by the net e^-/h^+ fluxes

$$J_{T_{\rm VB}}(t) = \int_x \int_{E_T} \left[\tilde{\Phi}_C(x, E_T, t) - \tilde{\Phi}_E(x, E_T, t)\right] dE_T\, dx$$

$$J_{T_{\rm CB}}(t) = \int_x \int_{E_T} \left[\Phi_C(x, E_T, t) - \Phi_E(x, E_T, t)\right] dE_T\, dx.$$

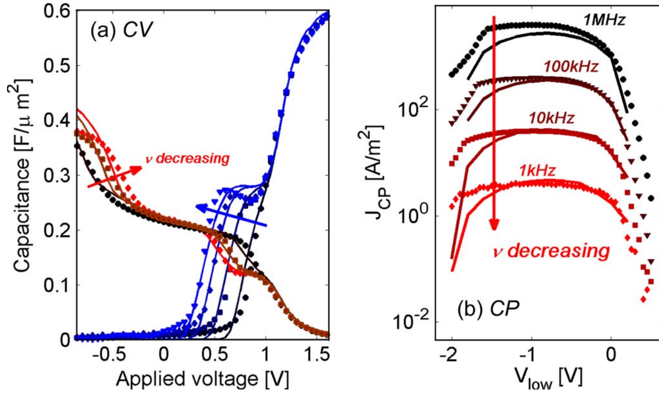

Fig. 2. (a) Gate-channel (in blue) and bulk (in red) capacitance values as a function of the bias voltage for different small-signal frequencies and after a positive constant voltage stress of 1000 s at 5.5 V. Symbols indicate measurement results, whereas simulations are shown in a solid line. Both the threshold voltage shift and the parasitic capacitive component of the traps are accurately reproduced for a frequency range from 1 kHz to 1 MHz. (b) CP current versus $V_{\rm low}$ voltage for different CP pulse frequencies and using $V_{\rm swing} = 2.5$ V. The same spatial/energetic trap distribution profile (similar to the one described for results in part I of this paper) has been adopted to reproduce all the results.

Fig. 1(b) shows that, for the CP pulses where the MOS operates both in accumulation and inversion ($V_{\rm sw} = 2.5$ V, $V_{\rm low} = -0.4$ V), the HIGH → LOW transition generates a hole capture current (dashed red curve), which exponentially decreases when the voltage is maintained at $V_{\rm low}$. Electron emission can be also noticed in this phase. On the other hand, during the LOW → HIGH transition shown in the inset in Fig. 1(c), electron capture (solid blue) dominates in weak/strong inversion, whereas hole emission occurs when the device is in depletion. The current contributions during the transitions must be carefully taken into account due to their important role in the estimation of the CP current.

The total CP current $J_{\rm cp}$, depicted in Fig. 2(b) as a function of $V_{\rm low}$, has been calculated integrating the net transient currents $J_{T_{\rm VB}}(t)$ and $J_{T_{\rm CB}}(t)$ over an entire square pulse. Thus

$$J_{\rm cp} = \int_T J_{T_{\rm VB}}(t)\, dt = -\int_T J_{T_{\rm CB}}(t)\, dt \qquad (3)$$

where T corresponds to a full period of the CP pulse $T = 1/\nu$.

Fig. 2(a) indicates the ac characteristics of the MOS device for various small-signal frequencies from 1 kHz to 1 MHz. AC simulations are performed using (2) as in [17]. In (b), MFCP measurements and simulations performed using the same defect distribution as for ac characteristics [17]. For each $V_{\rm low}$ in Fig. 2(b), a full transient simulation has been performed with the general transient model of (1), and the CP current has been calculated. Good correlation with transient results for different frequencies has been found.

B. On the Validity of QE Approximation

Fig. 3 shows the calculated E_F and f_T as a function of energy and position in the dielectric for two timesteps of a CP simulation. At the beginning of the pulse [plots (a,b)], the trap distribution is in equilibrium with one of the reservoirs (dc conditions; $V = V_{\rm low} = -1.2$ V), following the quasi-Fermi level in proximity of the Si/SiO_2 interface regions. In the middle of

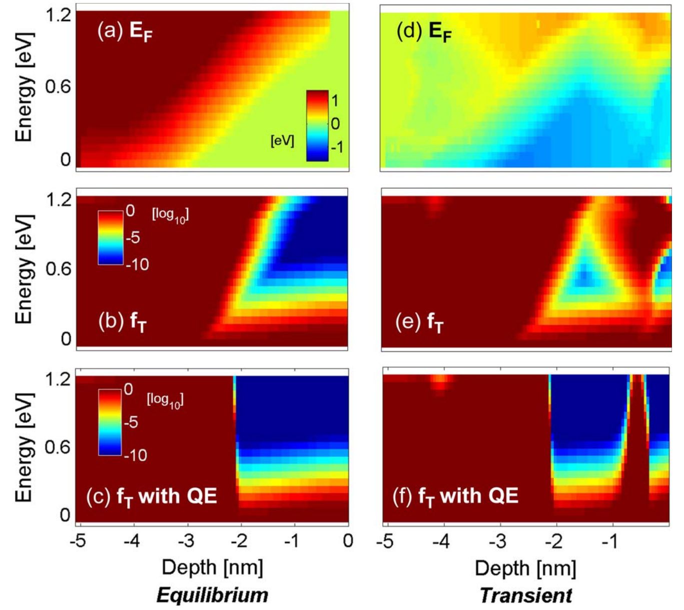

Fig. 3. Calculated quasi-Fermi level (a,d) and trap occupation (b,e) distributions in energy and oxide depth for different bias conditions during a CP pulse using the transient model of (1). The Si/SiO_2 interface is placed at position $x = 0$ with the substrate conduction and valence band edges at 0 and 1.2 eV. Initial dc equilibrium conditions at $V_{\rm low} = -1.2$ V are shown in (a) and (b). Transient conditions after two CP cycles are represented in (d) and (e). Drastical differences are noticed when the QE approximation is considered. In transient conditions, only the dependence of C/E rates in depth is considered [plots (c,f)], causing border/oxide defects to remain filled almost independently from their energetic level.

the oxide, when taking into account the gate C/E contributions, different equilibrium conditions dependent on the energetic positions of the defects are created, and as a consequence, both E_F and f_T vary with energy. If one considers the QE approximation [see Fig. 3(c)], a similar equilibrium condition on f_T is found in proximity of the two interfaces, e.g., within 1 nm–depth, but differences are found in the transition region, i.e., for a depth between 1 and 3 nm.

On the rising edge of the voltage pulse, defects in proximity of $E_C^{\rm Si}$ are progressively filled by e^-, whereas traps near $E_V^{\rm Si}$ are emptied of holes. The equilibrium front propagates from the two Si band edges as charge exchange driven by the C/E time constants continues [21]. When decreasing the applied voltage, e^- are emitted toward the Si conduction band and traps at the midgap capture h^+ from the valence band.

After an entire CP pulse, deep defects do not reach equilibrium [see Fig. 3(d)] and remain filled of e^- following a spatial and energetic f_T distribution [see Fig. 3(e)]. If one chooses to apply the QE approximation to transient simulations, the C/E fronts only propagate along the direction of oxide depth while the propagation along the direction of the energy level is not present. As a consequence, the charge distribution in out-of-equilibrium conditions after a CP pulse is uniform in energy and forms a peak at a given depth. A supplementary color MPEG file showing the trap occupation for a complete CP pulse is available at http://ieeexplore.ieee.org[1].

[1]The MPEG file is available to reviewers as supplementary file and shows the evolution of the electron trap occupation distribution plotted as a function of trap position and energy in the oxide layer during a typical charge pumping experiment. Out-of-equilibrium conditions can be clearly identified.

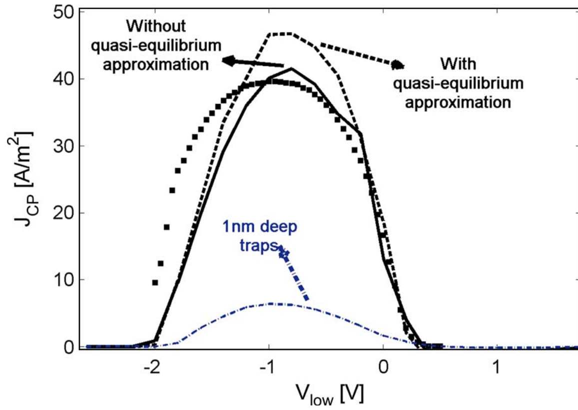

Fig. 4. (Symbols) Measured and (lines) simulated CP current as a function of V_{low}. Simulation results for the same trap distribution but shifted 1 nm away from Si/SiO_2 are also shown in dot-dashed line.

Fig. 4 shows the differences on the maximum CP current obtained with the QE approximation, illustrating the effects of neglecting the energy dependence of the trapping time constants during the extraction and confirming its importance in a general transient analysis. In the following, the general transient approach is used without considering the QE approximation.

C. Pumped and Probed CP Regions

Two representative metrics are used to assess the limitations of the MFCP technique in the extraction of the defects distribution, namely, the pumped and effectively probed oxide regions. The pumped region represents the spatial and energetic portion of the oxide where traps are exchanging carriers with the substrate during a single CP pulse. This quantity has been calculated using an analytical approach similar to the one adopted in [6], [15], and [22] from the maximum electron and hole occupations using

$$g_{\mathrm{CP}}(x, E_T) = (1 - f_T(x, E_T, t_A))\, f_T(x, E_T, t_B) \quad (4)$$

where t_A and t_B represent the timestep, which occur after the low-level voltage plateau (corresponding to the maximum capture of h^+) and after the high-level voltage plateau (corresponding to the maximum capture of e^-), respectively.

Fig. 5 shows the pumped zone for different V_{low} voltages and for a 1-kHz CP signal and indicates the regions exchanging carriers with the substrate during the voltage pulse. Charge exchange is higher (bright color) in proximity of both the substrate conduction and valence band edges located at 0 and 1.2 eV at position $x = 0$. Additionally, midgap traps are able to capture electrons and emit holes contributing as well to the pumped region.

We believe that the probed region offers a better estimation of the degraded oxide regions contributing to carrier recombination and to the CP current calculated with (3). This quantity can be interpreted as the impulse response of the CP current due to a single trap placed at (x, E_T) and is determined as

$$f_{\mathrm{CP}}(x, E_T) = \frac{\int_t \left(\tilde{\Phi}_C(x, E_T, t) - \tilde{\Phi}_E(x, E_T, t)\right) dt}{N_T(x, E_T)}. \quad (5)$$

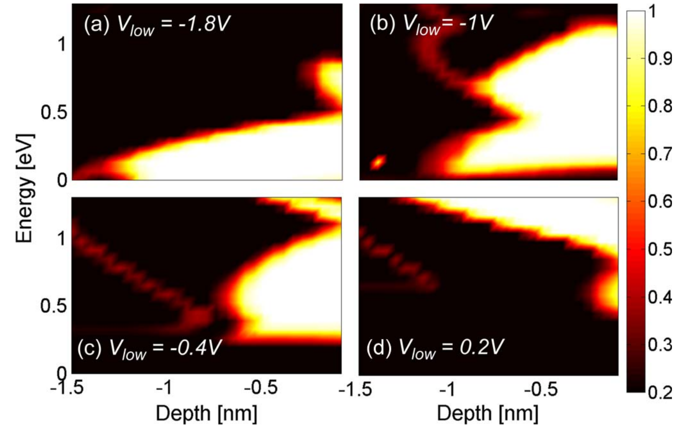

Fig. 5. Pumped region calculated using (4) for various V_{low} voltages and using a 1-kHz pulse. The Si/SiO_2 interface is placed at position $x = 0$, whereas the Si conduction and valence bands are respectively at 0 and 1.2 eV. The bright regions at the interface and near E_C^{Si} and E_V^{Si} are able to communicate with the substrate during the CP pulse. The value has been normalized between 0, corresponding to no carrier exchange, and 1, indicating maximum C/E.

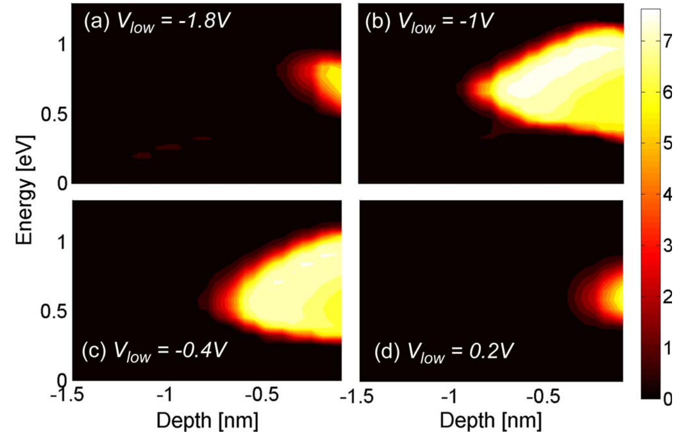

Fig. 6. Probed CP region versus trap energy and position in the oxide layer, calculated with (5) at $\nu = 1$ kHz, $V_{\mathrm{sw}} = 2.5$ V, and $T = 300$ K. The current peak in Fig. 4 corresponds to the condition where the probed region is maximum in extension and the operating regime varies from accumulation to inversion as in (b). The Si/SiO_2 interface is placed at position $x = 0$, whereas the Si conduction and valence bands are at 0 and 1.2 eV, respectively.

Fig. 6 shows the calculated $f_{\mathrm{CP}}(x, E_T)$ for a signal frequency of 1 kHz and for different V_{low} conditions. Only midgap defects placed at the Si/SiO_2 interface are probed, as carrier recombination occurs in these energetic positions at the Si/SiO_2 interface with the substrate. This is observed in Fig. 6 by the presence of a bright area at midgap representing the probed region versus energy and oxide depth. Defects placed near the conduction and valence bands have too high C/E rates to contribute to the CP current: Electrons in the conduction band captured into the defects during the rising edge are immediately emitted toward the same band during the falling edge, and thus, do not contribute to the CP current. Deeper defects have long time constants and are not probed, as they are not able to exchange carriers with the channel at the considered pulse frequency. Fig. 4 shows CP simulations for the same defect distribution profile but shifted 1.2 nm away from the interface. Different V_{low} voltage conditions are shown and indicate that

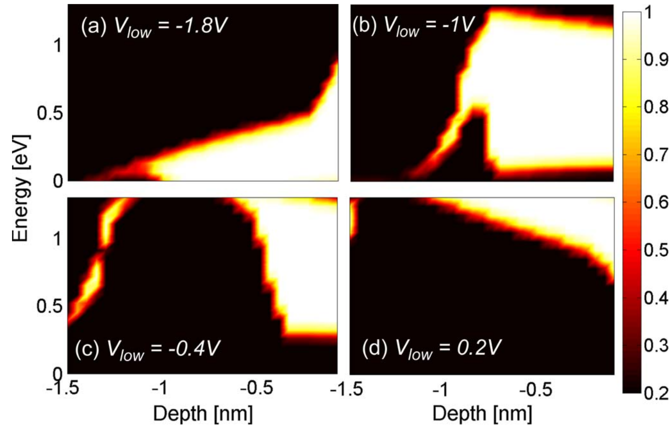

Fig. 7. Pumped CP region versus trap depth and energy, calculated using (4) for different $V_{\rm low}$ conditions and using the SFL approximation ($\nu = 1$ kHz, $V_{\rm sw} = 2.5$ V, and $T = 300$ K). The reference energy is the Si valence band, whereas Si/SiO_2 is at depth $x = 0$ nm. A trapezoidal region is found in (b), which relates to the $V_{\rm low}$ condition where the peak in $J_{\rm cp}$ is maximum. This result is in accordance with calculations performed in [6]. The extension of the region in energy is larger due to the fact that traps are in equilibrium with the substrate. The extension in depth remains comparable to the results shown in Fig. 6.

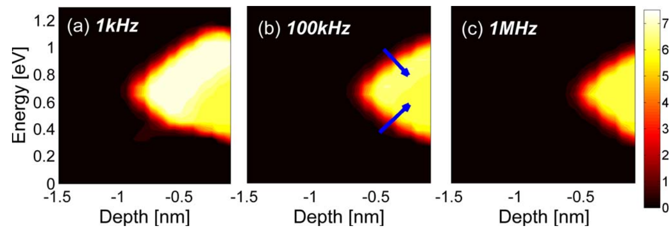

Fig. 8. Probed CP region versus trap depth and energy, calculated using CP pulses with $V_{\rm low} = -1.4$ V and different frequencies. Deeper defects having reduced time constants are scanned using low-frequency pulses.

only specific midgap regions and at the Si/SiO$_2$ interface can be probed.

Comparing the pumped region $g_{\rm CP}$ and the probed region $f_{\rm CP}$ in Figs. 5 and 6, respectively, one evidences that the pumped zone includes the probed region. Indeed, $g_{\rm CP}$ includes two parasitic *wings* near $E_C^{\rm Si}$ and $E_V^{\rm Si}$, corresponding to the regions where both capture and emission of electrons or holes occur, which should not be taken into account in the determination of the probed region and $J_{\rm cp}$ current calculation.

Even larger discrepancies are observed in the pumped region when the SFL approximation is introduced (see Fig. 7): The energy dependence of the pumped region on the trap energy is reduced, and thus, a large portion of the energy gap is pumped. However, in this case, the probed regions cannot be derived from the flux contributions using (5), since this would conduct to the incorrect interpretation concluding that fluxes near $E_C^{\rm Si}$ and $E_V^{\rm Si}$ dominate over the fluxes at midgap [14].

The extension of $f_{\rm CP}$ in oxide depth and energy strongly varies with the pulse characteristics (swing, frequency, low-base bias, ...). For this reason, MFCP techniques are adopted to scan particular regions of the oxide layer by comparing the measured CP currents in response to diverse pulse conditions. Fig. 8 illustrates the simulated $f_{\rm CP}$ for three frequencies (1 kHz, 10 kHz, and 1 MHz) at $T = 300$ K and $V_{\rm sw} = 2.5$ V. The maximum probed regions achievable are illustrated at $V_{\rm low}$ corresponding to the maximum CP current. The trap concentration in specific areas of the oxide (in energy and depth) can be extracted by comparing the current contribution of the additional probed regions scanned with lower frequency signals. Similar considerations can be applied considering the variation of $J_{\rm CP}$ with $V_{\rm sw}$, shown in Fig. 9 from $V_{\rm sw} = 1$ to 2.5 V. Defects (1-nm deep) at the midgap can be probed at approximately $\nu = 1$ kHz and using $V_{\rm sw} = 2.5$ V, whereas the defects closer to the Si band edges require much lower frequencies.

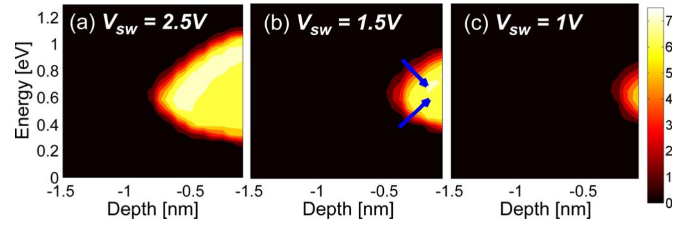

Fig. 9. $V_{\rm sw}$ dependence of the probed region at $\nu = 10$ kHz, $V_{\rm low} = -1.2$ V, and $T = 300$ K. The reference energy is the Si valence band, whereas Si/SiO_2 is at depth $x = 0$ nm. Higher $V_{\rm sw}$ permits scanning deeper in the oxide depth and at energies closer to the Si band edges.

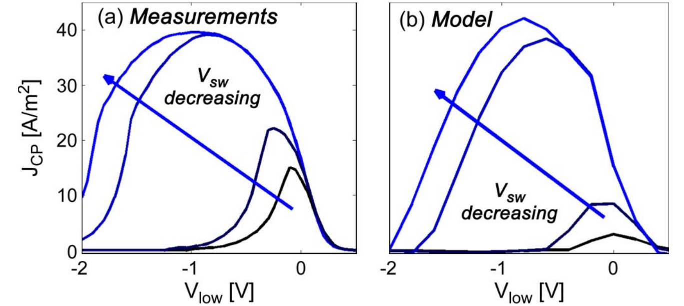

Fig. 10. CP current as a function of the low-level $V_{\rm low}$ voltage and for different pulse swings $V_{\rm sw}$. The reference energy is the Si valence band, whereas Si/SiO_2 is at depth $x = 0$ nm. Measurement results in (a) are in agreement with simulations in (b) and with literature [5], [15], [16], [23].

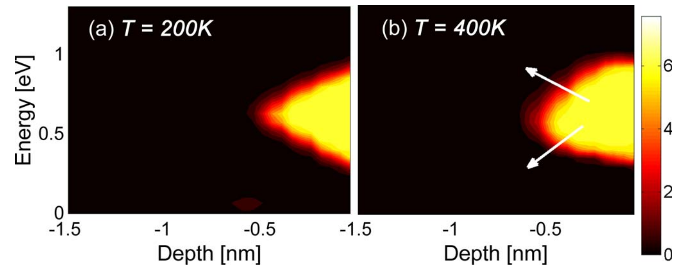

Fig. 11. Temperature dependence of the probed CP region at $\nu = 1$ MHz, $V_{\rm low} = -1.2$ V, and $V_{\rm sw} = 2.5$ V. The reference energy is the Si valence band, whereas Si/SiO$_2$ is at depth $x = 0$ nm. Higher temperatures scan deeper in the oxide depth.

Fig. 10 shows the dependence of the CP current with $V_{\rm sw}$ for a 10-kHz CP signal frequency. The CP current is analyzed as a function of $V_{\rm low}$ and for different voltage swings $V_{\rm sw}$. Increasing the magnitude of the swing allows scanning of deeper traps, and consequently, the peak increases since carrier capture increases.

Temperature also plays an important role in multiphonon-assisted transitions. Fig. 11 shows the variation of the probed region extension at (a) $T = 200$ K and (b) $T = 400$ K, indicating the increase in the probed region extension when temperature is

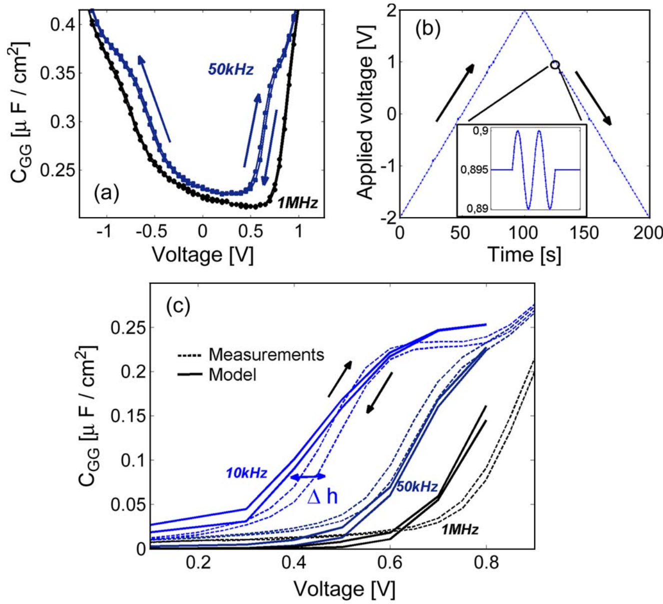

Fig. 12. (a) Gate capacitance measurements performed after 1000 s of positive constant voltage stress, ramping-up and subsequently ramping down the large-signal voltage for two frequencies. (b) Applied voltage versus time used for the simulation and the analysis of hysteresis effects. A slowly varying dc voltage is applied to the device, whereas an ac small-signal pulse (inset) is used to calculate the ac response of the device from the trap displacement currents. The ac small-signal pulse is considered on both the rise and the fall of the dc voltage. (c) Detail of the hysteresis loops of the C_{GC} capacitance in the frequency range from 10 kHz to 1 MHz. The width of the hysteresis loops Δh increases due to the fact that the total measurement time increases at lower frequencies and more time is granted to deep traps to capture/emit carriers, increasing the magnitude of the phenomenon. (Solid lines) Simulation results; (dashed lines) measurements. The arrows indicate the sense of the applied dc voltage.

raised. Arrows in Fig. 11 indicate the widening of the region for increasing temperatures. The rise/fall times and the duty cycle of the pulse have been found to play a minor role on the CP current and on the simulated probed region.

Finally, since the C/E rates are exponentially dependent on trap defect parameters (S, $\hbar\omega$, and F_C), their variation would affect the spatial and energetic extension of the probed regions and the magnitude of the currents. In our studies, we mainly focused on considering nominal properties with defect parameters extracted from the studies in [24]. The consequence of varying defect parameters is the subject of a separate publication [25].

IV. Hysteresis Effects

Hysteresis loops are observed in measured ac characteristics; the interpretation provided by the multiphonon model indicates that they are due to the long time constants of border and oxide traps, which are filled during the dc voltage sweep. Fig. 12(a) shows the C_{GG} capacitance measurement results after 1000 s of constant voltage stress, where the ac measurements have been performed ramping the applied voltage up and down. A hysteresis loop of magnitude Δh is observed in weak inversion and accumulation. The full pulse applied by the ac analyzer and simulated with the model is shown in Fig. 12(b). During the voltage ramp-up, deep traps having time constants in the order of seconds/minutes (the time elapsed during the ramp-up) are progressively filled, and the electrostatics of the system changes with a positive increasing stretch-out. During ramping down, the system is in a different condition with respect to the ramp-up as deep traps are filled and require a certain amount of time to emit carriers. Consequently, the dynamics of charge trapping is altered, causing the hysteresis loop. As shown in Fig. 12(c), the magnitude of the loop is found to be slightly dependent on the frequency of the small-signal pulse. It should be pointed out that the hysteresis loops in Fig. 12(a) cross each other in depletion, revealing electron filling in inversion (V_{th} increase) and hole capture in accumulation (V_{fb} decrease).

The hysteresis effect is observed in a full transient simulation using the multiphonon model and the pulse characteristics depicted in Fig. 12(b). A low-frequency large-signal sawtooth pulse is applied. When reaching a certain voltage, the response of the system to a small-signal sinusoidal pulse is then calculated. The calculated transient current flows permit the determination of the admittances of the system as in part I [17]. This operation is performed on the ramping up and down of the large-signal pulse, for a limited set of dc voltages and frequencies. The simulated capacitance values shown in Fig. 12(c) indicate the fairly good agreement with measurements of the hysteresis loops on the C_{GC} capacitance.

The observation of hysteresis loops on the capacitance values further confirms the presence of a widespread distribution of C/E rates for deeper traps in energy and depth, in accordance with multiphonon model results and recent TDDS measurements of the trap relaxation constants [9], [26]. Additionally, the stretch-out shown for all the CGV curves of part I [17] and in Fig. 2(a) is affected by the measurement time, and thus, the history of the system affects the accurate determination of the threshold voltage shift.

The magnitude of the hysteresis loops strongly depends on the total rise time of the dc pulse (not shown here), i.e., a rapid increase in the dc voltage gives deeper traps less time to reach equilibrium with the substrate, and thus, hysteresis decreases.

V. Conclusion

Transient and hysteresis effects impacting MFCP and CV characteristics of CMOS oxides have been analyzed by means of a multiphonon-assisted charge trapping model, which has been presented in detail in part I. In particular, the effects of the approximation introduced when considering traps in equilibrium with the carrier reservoirs have been analyzed. The SFL approach can be used in dc conditions or for ac analysis around an equilibrium point. It can be applied to the extraction and investigation of P_b centers, as these interface defects respond with high C/E rates, and thus, the energy dependence of their time constants is reduced. The general transient approach is suitable for analyzing bulk or border traps as in this model the traps communicate with the gate or channel reservoirs with their own C/E rates, and thus, they may not reach equilibrium conditions due to their low C/E rates.

The multiphonon approach has been used for extracting relevant trap distributions of interfacial defects using both CV and CP techniques. The dependence of the probed region in CP with pulse configuration, swing voltage, temperature, and

equilibrium model has been investigated. In part I [17], similar regions have been extracted from ac measurements. However, whereas MFCP techniques permit scanning of midgap defects, probing this region with CVG techniques requires frequencies that are excessively small. On the other hand, CV methods appear suitable for the extraction of defect concentrations in proximity of $E_C^{\rm Si}$ and $E_V^{\rm Si}$.

Hysteresis loops present in CV characteristics have been analyzed and justified by the presence of border/oxide defects, which are filled with the low time constants of the large-signal dc pulse.

The proposed ac and transient model can be also applied to evaluate the accuracy of extraction techniques based on compact or analytical models and to a physical-based investigation of the trapping phenomena. The analysis could be performed also on complex oxide stacks and heterostructures, including HighK Metal Gate (HKMG) and Silicon On Insulator (SOI) devices.

APPENDIX
C/E MULTIPHONON TRANSITIONS

A. C/E Probability

The theory of multiphonon-assisted interaction [11], [12], [27] predicts capture probabilities W_c given by

$$W_c(x,\mathcal{E}_j,E_T)=\frac{2\pi}{\hbar}R(\Delta E)|V|^2\exp\left(\frac{F^2}{F_C^2}\right)\times\left[rS\left(1-\frac{\Delta E}{\hbar\omega S}\right)^2+(1-r)\sqrt{\left(\frac{\Delta E}{\hbar\omega S}\right)^2+4\overline{n}(\overline{n}+1)}\right] \quad (6)$$

where $\Delta E = \mathcal{E}_j - E_T$ and $\overline{n} = (\exp(\hbar\omega/(k_BT)) - 1)^{-1}$ the average number of phonons of pulsation ω given by Bose–Einstein statistics, r and the Huang–Rhys factor S are model parameters [10]. The discrete energy levels $\mathcal{E}_j$ in the carrier reservoir have been calculated with the Schröedinger solver [28].

The term $R(\Delta E)$ is expressed as

$$\frac{1}{\hbar\omega}\exp\left[-(2\overline{n}+1)S+\frac{\Delta E}{2k_BT}\right]\sum_m I_m(z)\delta(m\hbar\omega-\Delta E) \quad (7)$$

being $I_m(z)$ the reduced Bessel function of order m and T the device temperature.

The factor $\exp(F^2/F_C^2)$ has been included to take into account the exponential dependence of the capture probability with respect to the electric field F in the oxide. The critical field F_C is an empirical model parameter, whose value has been extracted from TDDS and STS measurements [9], [26], [29]. It has been introduced to model the exponential dependence of the trapping rates with the stress voltage. A value of $F_C =$ 2.6 MV/cm has been used throughout this study. This result is in good accordance with the measurements performed in [9] and [26].

The calculation of the emission probability W_e assumes that the trap is in thermal equilibrium with the gate/channel. From this hypothesis and applying the detailed balance principle [30], one has

$$W_e(x,\mathcal{E}_j,E_T)=e^{\frac{E_T-\mathcal{E}_j}{k_BT}}W_c(x,\mathcal{E}_j,E_T). \quad (8)$$

B. Defect Wave Function Model

In order to calculate the wave function overlap $|V|^2$ and the microscopic model parameters S and r, a model for the defect wave function is needed. In this paper, the billiard-ball (BB) model at the trapping center proposed by Ridley and Amato [31] is used. Thus

$$|\Phi_b\rangle=\begin{cases}1/\sqrt{z_T^3}, & \text{for } |z-z_0|\le\frac{z_0}{2}\\ 0, & \text{for } |z-z_0|>\frac{z_0}{2}\end{cases} \quad (9)$$

where z_0 is the position of the trap center, and z_T is the edge of the cube, which is isovolumetric to the sphere of the defect [10]. Thus, $z_T = a_T(4\pi/3)^{1/3}$ and $a_T = (\hbar/\sqrt{2m^*(E_c(x) - E_T)})$ and $E_c(x)$ is the conduction band level at position x. The influence of the trapped charge and state on the trap potential and wave function has been neglected.

C. Microscopic Parameters Calculation

The transition matrix element between a trapped state $\langle\Phi_b|$ and a state in the channel $|\Phi_i\rangle$ [18] has been expressed as

$$|V|^2=|\langle\Phi_b|U|\Phi_i\rangle|^2 = 5\pi S(\hbar\omega^2)^2a_T^2\int_{x-r_T/2}^{x+r_T/2}|\zeta(z,\mathcal{E}_j)|^2\,dz \quad (10)$$

where $\zeta(z, \mathcal{E}_j)$ is the wave function calculated using the Schröedinger solver, and U is the Hamiltonian describing the carrier-phonon interaction.

The Huang–Rhys factor S in the BB model can be calculated using

$$S=\frac{27}{4(\hbar\omega)^2(q_Dr_T)^3}\cdot\frac{D_{\rm ph}^2}{M_r\omega/\hbar} \quad (11)$$

where $M_r\omega/\hbar = 1/(\rho_m\omega)$ and $D_{\rm ph}$ is the phonon-deformation potential and ρ_m the material density. A single defect phonon frequency ω has been assumed in this work considering an average value determined in the studies of Berthe *et al.* [32]. The Debye cutoff wave vector q_D is defined as $q_D = (6\pi^2/a_0)^{1/3}$, with a_0 equal to $(0.25^{1/3})$ of the lattice constant in zinc-blend lattice.

The properties of the defects in the Si/SiO_2 interface and in the SiO_2 remain difficult to be estimated and probably vary from defect to defect; in this paper, we used the set of parameters determined by STS studies in [32] and [33] ($S =$ 9.6 and $\hbar\omega = 32.5$ meV). The phonon-deformation potential $D_{\rm ph} = 6\cdot10^8$ eV/cm is a parameter that has been extracted from the measured values of the Huang–Rhys factor using (11).

These values have been used throughout this study, but the dependence of the ac characteristics on the Huang–Rhys

factor S has been also investigated, varying its value from 0.1 to 50 and noticing a significant variation of the intrinsic trap frequency [21]. The calculation and measurement of this parameter and of its field dependence is still under debate; literature studies performed on bulk materials reported a wide range of values from several decades down to 1 [12], [27].

D. C/E Rates

The C/E rates of e^- are defined as

$$\tau_c^{-1}(x, E_T) = \sum_j W_c(x, \mathcal{E}_j, E_T) g_{2D} D^-(\mathcal{E}_j)$$
$$\tau_e^{-1}(x, E_T) = \sum_j W_e(x, \mathcal{E}_j, E_T) g_{2D} D^0(\mathcal{E}_j) \qquad (12)$$

where $g_{2D} = (m^*_{\mathrm{Si}}/\pi\hbar^2)$ represents the 2-D density of states in the semiconductor carrier reservoir, and m^*_{Si} is the effective mass of the carriers in Si ($0.19m_0$ and $0.514m_0$ for e^- and h^+, respectively, compared with the free e^- mass m_0). The quantized energetic levels in the reservoir are indicated with $\mathcal{E}_j$ and determined using the Poisson–Schroedinger (PS) solver [34]. The coefficients D are expressed as

$$D^-(\mathcal{E}_j) = k_B T \ln\left[1 + \exp\left(\frac{-(\mathcal{E}_j - E_F)}{k_B T}\right)\right]$$
$$D^0(\mathcal{E}_j) = k_B T \ln\left[1 + \exp\left(\frac{-(\mathcal{E}_j - E_F)}{k_B T}\right)\right] \times \exp\left(\frac{\mathcal{E}_j - E_F}{k_B T}\right). \qquad (13)$$

Similar considerations are applied for the calculation of the C/E rates of holes $\tilde{\tau}_c^{-1}/\tilde{\tau}_e^{-1}$. Considering the system in thermal equilibrium, a Fermi–Dirac distribution can be used to describe the carrier distribution function $f(x, \mathcal{E}_j, E_F, t)$ in the semiconductor.

ACKNOWLEDGMENT

The authors would like to thank Dr. V. Huard, Prof. W. F. Clark, Dr. E. Dornel, C. Tavernier, and Dr. M. Kerbaugh for their precious technical advice and support.

REFERENCES

[1] E. Nicollian and J. Brews, *MOS/Metal Oxide Semiconductor/Physics and Technology*. Hoboken, NJ: Wiley, 1982.

[2] M. Satter and M. A. Haque, “Modeling effects of interface traps on the gate CV characteristics of MOS devices on alternative high-mobility substrates,” *Solid State Electron.*, vol. 54, no. 6, pp. 621–627, Jun. 2010.

[3] P. Masson, J. Autran, M. Houssa, X. Garros, and C. Leroux, “Frequency characterization and modeling of interface traps in $HFSi_xO_y/HFO_2$ gate dielectric stack from a capacitance point-of-view,” *Appl. Phys. Lett.*, vol. 81, no. 18, pp. 3392–3394, Oct. 2002.

[4] D. Bauza, “Near interface oxide trap capture kinetics in metal–oxide–semiconductor transistors: Modeling and measurements,” *J. Appl. Phys.*, vol. 84, no. 11, pp. 6178–6186, Dec. 1998.

[5] D. Bauza, “Rigorous analysis of two-level charge pumping: Application to the extraction of interface trap concentration versus energy profiles in metal–oxide–semiconductor transistors,” *J. Appl. Phys.*, vol. 94, no. 5, pp. 3239–3248, Sep. 2003.

[6] M. Masuduzzaman, A. Islam, and M. Alam, “Exploring the capability of multifrequency charge pumping in resolving location and energy levels of traps within dielectric,” *IEEE Trans. Electron Devices*, vol. 55, no. 12, pp. 3421–3431, Dec. 2008.

[7] A. van der Wel, E. Klumperink, E. Hoekstra, and B. Nauta, “Relating random telegraph signal noise in metal–oxide–semiconductor transistors to interface trap energy distribution,” *Appl. Phys. Lett.*, vol. 87, no. 18, pp. 183 507–183 507-3, Oct. 2005.

[8] T. Grasser, H. Reisinger, W. Goes, T. Aichinger, P. Hehenberger, P. Wagner, M. Nelhiebel, J. Franco, and B. Kaczer, “Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise,” in *IEDM Tech. Dig.*, 2010, pp. 1–4.

[9] T. Grasser, H. Reisinger, P. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, “The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability,” in *Proc. IRPS*, 2010, pp. 16–25.

[10] B. Ridley, “The photoionisation cross section of deep-level impurities in semiconductors,” *J. Phys. C, Solid State Phys.*, vol. 13, no. 10, p. 2015, Apr. 1980.

[11] D. Goguenheim and M. Lannoo, “Theoretical and experimental aspects of the thermal dependence of electron capture coefficients,” *J. Appl. Phys.*, vol. 68, no. 3, pp. 1059–1069, Aug. 1990.

[12] J. Zheng, H. Tan, and S. Ng, “Theory of non-radiative capture of carriers by multiphonon processes for deep centres in semiconductors,” *J. Phys., Condens. Matter*, vol. 6, no. 9, p. 1695, Feb. 1994.

[13] A. Palma, A. Godoy, J. Jimenez-Tejada, J. Carceller, and J. López-Villanueva, “Quantum two-dimensional calculation of time constants of random telegraph signals in metal–oxide–semiconductor structures,” *Phys. Rev. B*, vol. 56, no. 15, pp. 9565–9574, Oct. 1997.

[14] D. Garetto, Y. M. Randriamihaja, A. Zaka, D. Rideau, A. Schmid, H. Jaouen, and Y. Leblebici, “AC analysis of defect cross sections using non-radiative MPA quantum model,” in *Proc. 11th IEEE Int. Conf. ULIS*, 2011, pp. 1–4.

[15] D. Bauza, “A general and reliable model for charge pumping Part I: Model and basic charge-pumping mechanisms,” *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 70–77, Jan. 2009.

[16] D. Bauza, “A general and reliable model for charge pumping Part II: Application to the study of traps in SiO_2 or in high-k gate stacks,” *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 78–84, Jan. 2009.

[17] D. Garetto, Y. Mamy-Randriamihaja, A. Zaka, D. Rideau, A. Schmid, H. Jaouen, and Y. Leblebici, “Modeling of stressed MOS oxides using a multiphonon-assisted quantum approach—Part I: Impedance analysis,” *IEEE Trans. Electron Devices*, 2011, Submitted for publication.

[18] F. Jiménez-Molinos, A. Palma, F. Gamiz, J. Banqueri, and J. Lopez-Villanueva, “Physical model for trap-assisted inelastic tunneling in metal–oxide–semiconductor structures,” *J. Appl. Phys.*, vol. 90, no. 7, pp. 3396–3404, Oct. 2001.

[19] P. Masson, J.-L. Autran, and J. Brini, “On the tunneling component of charge pumping current in ultrathin gate oxide MOSFETS,” *IEEE Electron Device Lett.*, vol. 20, no. 2, pp. 92–94, Feb. 1999.

[20] T. Grasser, T. Aichinger, G. Pobegen, H. Reisinger, P. Wagner, J. Franco, M. Nelhiebel, and B. Kaczer, “The permanent component of NBTI: Composition and annealing,” in *Proc. IEEE IRPS*, 2011, pp. 6A–2.1–6A–2.9.

[21] D. Garetto, Y. M. Randriamihaja, A. Zaka, D. Rideau, A. Schmid, H. Jaouem, and Y. Leblebici, “Analysis of defect cross sections using non-radiative MPA quantum model,” *Solid State Electron.*, 2011, to be published.

[22] M. Masuduzzaman, A. Islam, and M. Alam, “Physics and mechanisms of dielectric trap profiling by Multi-frequency Charge Pumping (MFCP) method,” in *Proc. IEEE Int. Reliab. Phys. Symp.*, 2009, pp. 13–20.

[23] D. Bauza, O. Ghobar, N. Guénifi, and S. Bayon, “Advanced analysis of silicon insulator interface traps in MOSFETs with SiO_2 and HfO_2 as gate dielectrics,” *ECS Trans.*, vol. 19, no. 2, pp. 19–54, 2009.

[24] T. Nguyen, G. Mahieu, M. Berthe, B. Grandidier, C. Delerue, D. Stiévenard, and P. Ebert, “Coulomb energy determination of a single Si dangling bond,” *Phys. Rev. Lett.*, vol. 105, no. 22, p. 226 404, Nov. 2010.

[25] D. Garetto, Y. Mamy-Randriamihaja, D. Rideau, A. Schmid, H. Jaouen, and Y. Leblebici, “Comparing defect characterization techniques with non-radiative multiphonon charge trapping model,” *J. Comput. Electron.*, 2011, Submitted for publication.

[26] V. Huard, “Two independent components modeling for negative bias temperature instability,” in *Proc. IEEE IRPS*, 2010, pp. 33–42.

[27] B. Ridley, “Multiphonon, non-radiative transition rate for electrons in semiconductors and insulators,” *J. Phys. C, Solid State Phys.*, vol. 11, no. 11, p. 2323, Jun. 1978.

[28] D. Garetto, D. Rideau, E. Dornel, W. F. Clark, C. Tavernier, Y. Leblebici, A. Schmid, and H. Jaouen, “Modeling study of capacitance and gate current in strained high k–metal gate technology,” in *Proc. 13th Int. Nanotech. Conf.*, 2010, pp. 605–608.
[29] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P. Wagner, F. Schanovsky, J. Franco, M. T. Luque, and M. Nelhiebel, “The paradigm shift in understanding the bias temperature instability: From reaction–diffusion to switching oxide traps,” *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3652–3666, Nov. 2011.
[30] W. Shockley and W. Read, Jr., “Statistics of the recombinations of holes and electrons,” *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.
[31] B. Ridley and M. Amato, “A model for the interpretation of measurements of photoionisation and capture cross sections associated with deep-level impurities,” *J. Phys. C, Solid State Phys.*, vol. 14, no. 9, p. 1255, Mar. 1981.
[32] M. Berthe, R. Stiufiuc, B. Grandidier, D. Deresmes, C. Delerue, and D. Stievenard, “Probing the carrier capture rate of a single quantum level,” *Science*, vol. 319, no. 5862, pp. 436–438, Jan. 2008.
[33] M. Berthe, A. Urbieta, L. Perdigão, B. Grandidier, D. Deresmes, C. Delerue, D. Stiévenard, R. Rurali, N. Lorente, L. Magaud, and P. Ordejón, “Electron transport via local polarons at interface atoms,” *Phys. Rev. Lett.*, vol. 97, no. 20, p. 206 801, Nov. 2006.
[34] D. Garetto, Y. M. Randriamihaja, D. Rideau, E. Dornel, W. Clark, A. Schmid, V. Huard, H. Jaouen, and Y. Leblebici, “Small signal analysis of electrically-stressed oxides with Poisson–Schroedinger based multiphonon capture model,” in *Proc. IEEE Int. Workshop Comput. Electron.*, 2010, pp. 1–4.

Davide Garetto was born in Turin, Italy, in 1984. He received the B.Sc. degree in computer engineering from Politecnico di Torino, Turin, in 2006, and the jointed M.Sc. degree in micro- and nanotechnologies for integrated systems from the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland; from the Institut National Polytechnique de Grenoble, Grenoble, France; and Politecnico di Torino in 2008. He is currently working toward the Ph.D. degree with Microelectronic System Laboratory, EPFL, IBM Systems & Technology Group, ST Microelectronics, Crolles, France.

His project involves analytical and optimized modeling of flash cells, numerical simulations of device degradation, and electrical characterization. His current research interests include the modeling and integrated circuit design of advanced metal–oxide–semiconductor devices in embedded nonvolatile memory technologies, with emphasis on floating-gate transistors.

Mr. Garetto was the recipient of the IBM Ph.D. fellowship for 2010 and 2011.

Yoann Mamy Randriamihaja was born in Grenoble, France, in 1985. He received the M.S. degree in micro- and nanoelectronics from Joseph Fourier University, Grenoble, and the Engineering degree in microelectronics from the Ecole Nationale Supérieure d’Electronique et de radioélectricité de Grenoble, Grenoble, in 2009. He is currently working toward the Ph.D. degree in micro- and nanoelectronics in the frame of a collaboration between the Institut Matériaux Microélectronique Nanosciences de Provence, Toulon, and the Department of Electrical Characterization and Reliability, STMicroelectronics, Crolles, France.

His Ph.D. work focuses on the improvement of electrical characterization techniques of oxide defects and the understanding of physical phenomenas observed when a transistor is under stress.

Denis Rideau received the Engineering degree from ESIEE, Paris, France, in 1996, and the Ph.D. degree in physics from the University of Orsay, Orsay, France in 2001.

He is currently performing research and development in solid-state physics with STMicroelectronics, Crolles, France. His research interests include radio-frequency modeling and simulation of Si nanodevices, with emphasis on quantum effects, strain effects, and wafer orientations in FDSOI and FinFETs.

Alban Zaka was born in Tirana, Albania, in 1985. He received the M.Sc. degree in materials science and engineering from the National Institute of Applied Sciences, Lyon, France, in 2008. He is currently working toward the Ph.D. degree from the the Institut National Polytechnique de Grenoble, Grenoble, France, and the University of Udine, Udine, Italy.

His current thesis work is supported by STMicroelectronics, Crolles, France. His research topic includes the characterization and the simulation of hot-carrier injection phenomena in advanced nonvolatile-memory devices.

Alexandre Schmid (S’98–M’04) received the M.Sc. degree in microengineering and the Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Belgium, in 1994 and 2000, respectively.

Since 1994, he has been with the EPFL, working with the Integrated Systems Laboratory as a Research and Teaching Assistant, and with the Electronics Laboratories as a Postdoctoral Fellow. In 2002, he joined the Microelectronic Systems Laboratory, EPFL, as a Senior Research Associate, where he has been conducting research in the fields of bioelectronic interfaces, nonconventional signal processing and neuromorphic hardware, and reliability of nanoelectronic devices, and has also been teaching with the Department of Microengineering and the Department of Electrical Engineering, EPFL. Since 2011, he has been a “Maître d’Enseignement et de Recherche” faculty member with EPFL. He is a coauthor and a coeditor of two books and over 90 articles published in journals and conferences.

Dr. Schmid served as the General Chair of the Fourth International Conference on Nano-Networks in 2009 and has served as an Associate Editor of the *IEICE Electronics Express* since 2009.

Yusuf Leblebici (M’90–SM’98–F’09) received the B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 1984 and in 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign (UIUC), Urbana–Champaign, in 1990.

From 1991 to 2001, he worked as a faculty member with UIUC, with Istanbul Technical University, and with Worcester Polytechnic Institute (WPI), Worcester, MA. From 2000 to 2001, he also served as the Microelectronics Program Coordinator with Sabanci University, Istanbul. Since 2002, Dr. Leblebici has been a Chair Professor with the Swiss Federal Institute of Technology (EPFL), Lausanne, Belgium, and the Director of Microelectronic Systems Laboratory (EPFL). He is the coauthor of four textbooks, namely, *Hot-Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers, 1993), *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications* (Springer, 2007) and *Fundamentals of High Frequency CMOS Analog Integrated Circuits* (Cambridge University Press, 2009), as well as more than 200 articles published in various journals and conferences. His research interests include the design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of very large scale integrated (VLSI) systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis.

Dr. Leblebici has served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (II) and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS. He has also served as the general Cochair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference. He has been elected as a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.

Hervé Jaouen (SM'01) received the M.S. degree in engineering and the Ph.D. degree from the Institut National Polytechnique de Grenoble, France, in 1979 and 1984, respectively.

From 1981 to 1989, he was an Associate Professor with the Institut National Polytechnique de Grenoble, where he developed for his Ph.D. work a novel microwave annealing technique of semiconductors. He then worked on electronic-transport properties of disordered matter. In 1989, he joined the Technology Computer-Aided Design (TCAD) Group, SGS Thomson Microelectronics, where he was involved in the STORM EEC program with the goal of developing a 2-D process simulation tool. Then, he became the Manager of the TCAD Group of the Crolles' Plant, STMicroelectronics. Since 2004, he has been the Head of the ST Modeling Department, Crolles, France. The scope covered by his department includes TCAD, compact modeling, and ESD modeling. He is the author of 80 papers in the area of microelectronics. He is the holder of 18 granted U.S. patents.

Dr. Jaouen currently holds positions on the technical program committees of 2006 European Solid State Device Research Conference, SISPAD, and ESREF conferences. He was a member of the IEDM technical program committee. He serves as a European representative for the International Roadmap for Semiconductors in the Modeling and Simulation ITWG. He was involved in the coordination of the activity of STMicroelectronics in the technical management committees of IST European Community programs. He held positions in the management committees of some French national research programs such as ANR-PNANO on nanotechnology, ANR-Blanc on nanoscience, and ANR-CIS on high-performance computing. He is currently holding a position on the editorial board of IEEE TRANSACTIONS ON ELECTRON DEVICES. He was a recipient of the ST's Exceptional Patent Award in 2003.