View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by Infoscience - École polytechnique fédérale de Lausanne

Modeling Stressed MOS Oxides Using a Multiphonon-Assisted Quantum Approach—Part I: Impedance Analysis

Davide Garetto, Yoann Mamy Randriamihaja, Denis Rideau, Alban Zaka, Alexandre Schmid, *Member, IEEE*, Yusuf Leblebici, *Fellow, IEEE*, and Hervé Jaouen, *Senior Member, IEEE*

***Abstract*—Complementary MOS device electrical performances are considerably affected by the degradation of the oxide layers and Si/SiO$_2$ interfaces. A general expression for electrically stressed MOS impedance has been derived and applied within the nonradiative multiphonon theory of carrier capture/emission at oxide defects. The capacitance and the conductance of aged MOS field-effect transistor oxides, and their dependences on bias voltage, temperature, and stress conditions have been investigated.**

***Index Terms*—Charge trapping, impedance characterization, multiphonon-assisted (MPA) capture, oxide degradation.**

I. Introduction

THE INFLUENCE of oxide defects in advanced CMOS technologies is becoming more prominent as aggressive low-power requirements and high-endurance performances are targeted. The degradation of both oxide layers and Si/SiO$_2$ interfaces in MOS devices is responsible for uncontrolled threshold voltage $V_{\rm th}$ shifts [1], gate transconductance g_m reduction [2], gate leakage [3], Flicker noise [4], and general device lifetime reduction by oxide breakdown [5]. Moreover, both defect states and fixed oxide charges affect dc and ac performances; program/erase dynamics; memory retention; and endurance [3], [6], [7] of Flash, silicon–oxide–nitride–oxide–silicon, and nanocrystal memory devices [3], [6], [8], [9].

A standard method in Si/SiO$_2$ defect characterization uses the well-known capacitance/conductance-voltage (CGV) characterization methods [10]–[12]. The energy distribution of interface defects in the band gap can be extracted from quasi-static (QS) and high-frequency (HF) CV curves. Although, in the past 30 years, CGV methods have been considered reliable approaches [11], [13]–[15], they had to also face critics by a part of the scientific community due to the limitations of their empirical extraction models [10], [16]. Since the formulation of pioneering models investigating the impact of defect states that reside on the semiconductor surface in MOS capacitors [11], a considerable amount of effort has been devoted to obtaining a wider understanding of the behavior of deeper traps in dielectric layers [17], [18]. Most of these latter approaches rely on the extension of the Shockley–Read–Hall (SRH) recombination theory [19] considering elastic tunneling through the oxide barrier. Multifrequency CV [14], [15], [18], deep-level transient spectroscopy [20], [21], trap-assisted tunneling (TAT) [3], [22], and multifrequency charge pumping [23]–[25] experiences have been analyzed to extract the spatial and energetic distribution of defects. However, the models adopted in the aforementioned extractions can lead to major approximations in the estimation of the total trap density and incorrect temperature dependence [26]. Indeed, as pointed out in [27], the standard extension of the SRH recombination theory essentially predicts a correlation between the time constants and the depthwise position, which is not experimentally verified.

Carrier capture/emission (C/E) by means of multiphonon-assisted (MPA) processes [28], [29] have been studied in its application to TAT in SiO$_2$ [22], [30]–[33] and HfO$_2$ [34] dielectrics. However, an approach consisting of coupling an accurate MPA model to physical MOS impedance models to reproduce trapping effects has not been developed yet. A general small-signal model for the effects of traps on ac MOS characteristics has been derived and coupled with an MPA model integrated in a Poisson–Schroedinger (PS) solver (see Section II). In Section III, the model is verified on ac measurements on an advanced CMOS technology, and the energetic and spatial trap distribution profile is discussed in Section IV.

II. MPA Trapping Model

A. Rate Equation

Defects are distributed in the oxide layer in all spatial directions, and as highlighted in [35], they can have different energy levels. At a given cut at position x across the oxide stack, the spatial distribution of traps in the transversal plane can be related to a wide energy distribution. In this paper, a time-independent spatial and energy distribution of the defects $N_T(x, E_T)$ in the oxide layer stack has been adopted. We did not consider the possible change of the distribution versus time, as it is the case in multistate models linking the carrier C/E mechanisms with the generation/annealing dynamics, which

Manuscript received July 1, 2011; revised December 6, 2011 and December 9, 2011; accepted December 14, 2011. Date of publication January 23, 2012; date of current version February 23, 2012. The review of this paper was arranged by Editor B. Kaczer.

D. Garetto is with the IBM Systems & Technology Group-850, 38926 Crolles, France, and also with the Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland.

Y. M. Randriamihaja, D. Rideau, A. Zaka, and H. Jaouen are with the STMicroelectronics, 38926 Crolles, France.

A. Schmid and Y. Leblebici are with the Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2181388

0018-9383/$31.00 © 2012 IEEE

have been developed within the negative-bias temperature instability and random telegraph noise context [36]–[41]. Performing subsequent impedance measurements, we verified that, once the device has been stressed, no significant degradation or recovery is added during ac measurements.

The dynamics of trap occupation are controlled by the rate equation [30], i.e.,

$$\frac{\partial \rho_T(x,E_T,t)}{\partial t} = \Phi_c(x,t,E_T) - \Phi_e(x,t,E_T) - \tilde{\Phi}_c(x,t,E_T) + \tilde{\Phi}_e(x,t,E_T) \quad (1)$$

relating the variation in time of ρ_T (x, E_T, t) with electrons e^- (holes h^+, respectively) capture and emission flows $\Phi_c(x,E_T,t)$ and $\Phi_e(x,E_T,t)$ [$\tilde{\Phi}_c(x,E_T,t)$ and $\tilde{\Phi}_e(x,E_T,t)$, respectively]. The trap is assumed to be placed at position x in the oxide and at energy E_T.

In the steady state, the defect occupancy functions are at equilibrium with the carrier reservoirs (channel/gate). Thus, the concept of a quasi-Fermi level $E_F(x)$ valid in the substrate can be extended to the trap site at position x. Therefore, summing left- and right-hand sides of the set of equations expressed by (1) for each energy level, the rate equation reduces to

$$\int_{E_T} gN_T(x,E_T)\frac{\partial f_T(x,E_T,E_F(x,t),t)}{\partial t}dE_T = \int_{E_T}\Big[\Phi_c(x,E_T,t) + \tilde{\Phi}_e(x,E_T,t) + - \Phi_e(x,E_T,t) - \tilde{\Phi}_c(x,E_T,t)\Big]\,dE_T \quad (2)$$

where $f_T(x, E_T, E_F(x,t), t)$ expresses the occupation function of the trap, i.e., the probability a trap placed at energy E_T and position x is occupied by an electron at time t. In practice, the rate equation includes all the charge trapping fluxes of the defects located at a given cross section x and at different energies. The expression of ρ_T in the left-hand side of (1) depends on the defect type and has been replaced by one of the expressions in (20) and (21) of Annex A, with a different defect charge factor $g = \{-1, -2\}$, resulting from the derivative of ρ_T (acceptor/donor and amphoteric, respectively).

Typical defects at the interfaces are due to the breaking of Si–H bonds at Si/SiO_2 interfaces (P_b centers). Bulk oxide E'_γ and E'_δ defects generated by oxide vacancy have been also detected in amorphous SiO_2 [42]. *Ab initio* density functional theory simulations indicate that the Si/SiO_2 interface should be considered as a gradual transition from bulk Si to bulk SiO_2 more likely formed of a $Si_XO_{2(1-x)}$ material [43]. The extension of this region has been suggested to be ranging from 2 to 10 Å [43], [44] and to present a large number of unpassivated dangling bonds after electrical stress [45], [46]. Consequently, a clear distinction between P_b and E' defects is difficult to be established in such a region. However, as discussed later, amphoteric defects often associated to Si dangling bonds have been found to dominate the dc stretch-out and ac response in the electrical characteristics.

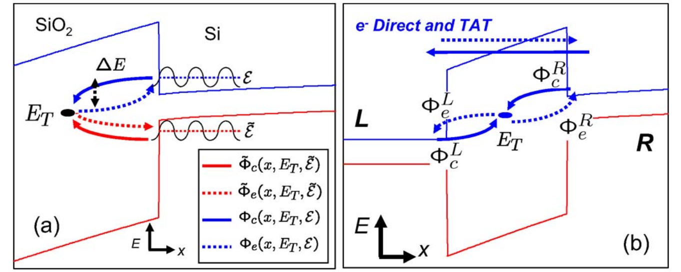

Fig. 1. MPA trapping mechanisms considered in the proposed model. (a) An e^- (h^+, respectively) from the channel at energy $\mathcal{E}$ ($\tilde{\mathcal{E}}$, respectively) is captured by an inelastic tunneling event through the energy barrier at the Si/SiO_2 interface losing energy ΔE (four C/E fluxes for both e^- Φ_c/Φ_e and h^+ $\tilde{\Phi}_c/\tilde{\Phi}_e$ are considered). (b) The electron fluxes cross the oxide with direct and TAT. Similar considerations apply to h^+.

B. C/E Flows

The C/E flows Φ_c/Φ_e in (1) and (2) and have been obtained using the theory of nonradiative trapping of carriers by MPA processes [47], [48]. For amphoteric defects, the e^- trapping flows are expressed using

$$\begin{aligned}\Phi_c(x,E_T,t) &= N_T(x,E_T)\left(1 - f_T(x,E_T,E_F,t)\right) \times \tau_c^{-1}\left(x,E_T,V(t)\right)\\ \Phi_e(x,E_T,t) &= N_T(x,E_T)f_T(x,E_T,E_F,t) \times \tau_e^{-1}\left(x,E_T,V(t)\right)\end{aligned} \quad (3)$$

where τ_c^{-1}/τ_e^{-1} are the e^- C/E rates as detailed in the Annex of part II (for h^+ fluxes, similar expressions hold).

Fig. 1(a) illustrates the MPA tunneling mechanisms involved and the C/E trapping flows considered at the interface with the channel (see Annex A when the interface with the gate is also considered). In the considered model, an e^- (h^+, respectively) can be captured (emitted) from (to) the energy level $\mathcal{E}$ ($\tilde{\mathcal{E}}$, respectively) in a carrier reservoir (gate or channel) to an unoccupied trap site at energy E_T. This transition is assisted by phonon emission/absorption associated to a structural lattice energy relaxation ΔE. In the multiphonon theory (see Annex of part II), the capture rate exponentially depends on ΔE. Once the carrier is captured, any further structural relaxation or defect annealing modifying the trap wave function, its potential, or energy E_T, e.g., through metastable states as described in [35]–[41], is neglected in our model. Consequently, since the emission occurs from the same trap energy value E_T, it is reasonable to apply the detailed balance principle for the calculation of the emission rate [see (8) in the Annex in part II].

C. Steady-State DC Regime

In steady-state conditions, i.e., for $(\partial\rho_t(x,t)/\partial t) = 0$, the solution of (2) provides the value of the quasi-Fermi level at the trap position. In equilibrium conditions, the calculated quasi-Fermi level is piecewise constant in the dielectric. In the proximity of the oxide interface with the gate (channel, respectively), it remains equal to the quasi-Fermi level in the gate (channel, respectively). This is consistent with the commonly adopted detailed balance hypothesis [19]. In the middle

of the dielectric, the result of the calculation leads to out-of-equilibrium conditions with respect to both gate and channel carrier reservoirs, and therefore, E_F varies from the gate value to the channel one. The role of out-of-equilibrium conditions on E_F is detailed in Part II. The trap occupation $f_T(x)$ and the trapped charges $\rho_T(x)$ can be calculated supposing a Fermi–Dirac distribution at the trap position.

Steady-state TAT current calculation requires the fluxes calculation to be performed for the two interfaces and for both the gate and the channel [L and R in Fig. 1(b)], which are present in MOS structures and from which tunneling can occur. The fluxes at the two interfaces (left, L; right, R) are indicated in Fig. 1(b) as Φ^L and Φ^R. Both the e^- and h^+ contributions have been included in (1). In addition to TAT tunneling mechanisms, for thin oxides, direct quantum tunneling can occur. The net current density flowing at one interface is given by

$$J_{\mathrm{TAT}}^{j}(x) = \int_{E_T} \left(\Phi_c^j + \tilde{\Phi}_e^j - \tilde{\Phi}_c^j - \Phi_e^j\right) dE_T \tag{4}$$

where index $j = \{R, L\}$ has been added and refers to the left or right oxide interface. The total net steady-state current density is expressed as

$$J_{\mathrm{TAT}}^{\mathrm{SS}} = \int_x J_{\mathrm{TAT}}^{R}(x) dx = -\int_x J_{\mathrm{TAT}}^{L}(x) dx. \tag{5}$$

The direct tunneling current component J_{WKB} has been considered as well using a Tsu–Esaki model and adopting a WKB approximation for the determination of the barrier transparency [49], [50]. The total tunneling current is thus expressed as $J_{\mathrm{TOT}} = J_{\mathrm{TAT}}^{\mathrm{SS}} + J_{\mathrm{WKB}}$.

D. Transient and AC Analysis

The transient TAT current at time t is represented by the left-hand side of (1) and is defined as

$$J_{\mathrm{TAT}}^{T}(t) = \int_x \int_{E_T} N_T(x, E_T) g \frac{\delta f_T}{\delta t} dE_T dx. \tag{6}$$

The transient rate equation is solved using a finite-difference approach for the trap occupation.

From a practical point of view, it is possible to obtain the gate impedance of the device from a transient simulation, applying a small sinusoidal signal on the gate. However, such an approach requires a large computational effort, and thus, an alternate small-signal model is preferred. Equations for such a model are described and validated in the following sections.

The total system admittances Y are calculated with

$$Y(V, \omega) = Y^V(V, \omega) + Y^T(\omega) \tag{7}$$

where ω is the angular frequency of the applied sinusoidal signal $V(t) = V_0 + v(t)$. The first contribution $Y^T(\omega)$ represents the intrinsic response of the defects at a given ω due to local quasi-Fermi level variation. The second contribution $Y^V(V, \omega)$ corresponding to the influence of the defects on the MOS charges should be also taken into account. In the calculation that follows, all references to position x have been intentionally omitted.

1) Intrinsic-Trap AC Response: A general frequency-dependent model suitable for multiphonon C/E is formulated, performing a small-signal analysis of the rate equation in the Fourier domain. Applying a gate voltage signal $V(t)$, a Taylor expansion is adopted around the dc point V_0, yielding

$$\begin{aligned} f_T(x, E_T, V(t)) &\approx f_{T0} + \delta f_T \\ E_F(x, V(t)) &\approx E_{F0} + \delta E_F \\ \tau^{-1}(x, E_T, V(t)) &\approx \tau_0^{-1} + \delta\tau^{-1} \end{aligned} \tag{8}$$

where f_{T0}, E_{F0}, and τ_0^{-1} are the steady-state values of the trap distribution, quasi-Fermi level, and C/E times.

Considering (2), we replace $(\partial/\partial t)$ with $j\omega = j2\pi\nu$ and the expressions of the C/E fluxes in (3) for both holes and electrons. Adding the flux contributions and removing the steady-state flux contributions, it can be seen that, after mathematical derivation, (2) reduces to

$$\begin{aligned} j\omega \int_{E_T} g\delta f_T N_T(x, E_T) dE_T &= \int_{E_T} N_T(x, E_T) \\ &\times \left[(1 - f_{T0})\left(\delta\tau_c^{-1} - \delta\tau_e^{-1}\right)\right. \\ &\quad \left. + f_{T0}\left(\delta\tilde{\tau}_c^{-1} - \delta\tilde{\tau}_e^{-1}\right) - \delta f_T \tau_t^{-1}\right] dE_T. \end{aligned} \tag{9}$$

In such an expression, we expressed the sum of all the trapping as a characteristic trap frequency τ_t^{-1}, i.e.,

$$\begin{aligned} \tau_t^{-1} = &\ \tau_{c0}^{-1} + \delta\tau_c^{-1} + \tau_{e0}^{-1} + \delta\tau_e^{-1} \\ &- \left(\tilde{\tau}_{c0}^{-1} + \delta\tilde{\tau}_c^{-1} + \tilde{\tau}_{e0}^{-1} + \delta\tilde{\tau}_e^{-1}\right). \end{aligned} \tag{10}$$

The importance of this quantity relies on its direct relation with the cutoff frequency of the MOS admittances, as clearly shown in Section III-A and [26].

Expressing $f_T(x, E_T, V(t))$ using Taylor series expansion around the dc operating point yields to

$$\delta f_T = -\delta E_F \frac{(1 - f_{T0}) f_{T0}}{k_B T} \tag{11}$$

and thus

$$\begin{aligned} \delta E_F = &\ \frac{k_B T \int_{E_T} N_T \left(\delta\tau_c^{-1} - \delta\tau_e^{-1}\right)(1 - f_{T0}) dE_T}{\int_{E_T} N_T \left(gj\omega + \tau_t^{-1}\right)(1 - f_{T0}) f_{T0} dE_T} \\ &+ \frac{k_B T \int_{E_T} N_T \left(\delta\tilde{\tau}_c^{-1} - \delta\tilde{\tau}_e^{-1}\right) f_{T0} dE_T}{\int_{E_T} N_T \left(gj\omega + \tau_t^{-1}\right)(1 - f_{T0}) f_{T0} dE_T}. \end{aligned} \tag{12}$$

The admittance component is calculated using the trapped charge expression in the left-hand side of (2), i.e.,

$$\begin{aligned} y^T(x, \omega) &= j\omega \frac{\partial \rho_T}{\partial V} = j\omega g \int_{E_T} \frac{N_T(x, E_T)\delta f_T}{v_{ac}} dE_T \\ Y^T(\omega) &= \int_x y^T(x, \omega) dx \end{aligned} \tag{13}$$

where v_{ac} is the amplitude of the small-signal pulse.

Equations (12) and (13) are key equations that have been derived to compute the total intrinsic trap conductance $G^T = \mathrm{Re}(Y^T(\omega))$ and capacitance $C^T = \mathrm{Im}(Y^T(\omega))/\omega$. In the derivation of (12) and (13), we have only considered the charge-trapping fluxes exchanged with substrate R. Extending the method including the C/E with the gate reservoir L and separating each contribution between holes and electron components (see Annex A), leads to consider four admittances $y_T^R(x,\omega)$, $y_T^L(x,\omega)$, $\tilde{y}_T^R(x,\omega)$, and $\tilde{y}_T^L(x,\omega)$.

Upon the application of a low-frequency sinusoidal signal to the gate, all traps are expected to respond to the bias voltage [10]. In such a case, the transient fluxes are considered null, with the traps reaching the equilibrium with the carrier reservoirs whenever the bias voltage changes. Consequently, G^T is null, and the intrinsic QS trap capacitance C^T can be defined as

$$C_{\mathrm{DC}}^T \equiv C^T(\omega \to 0) = \frac{\partial Q_{T0}}{\partial V} = \frac{\partial \int\int \rho_{T0} dE_T dx}{\partial V}. \quad (14)$$

As ω increases, the trap C/E rates become comparable with the frequency of the small-signal component and filling of defects, and trap response is reduced [10]. When driving the device at HF, traps do not follow the small-signal voltage applied to the gate and can be out of equilibrium with the reservoirs. Consequently, for a given dc bias, the charge density due to filled traps is a distribution of fixed charges, and only their influence on device electrostatics is considered.

2) Complete MOS Admittance Model: Trap filling induces a modification of the electrostatics of the system, affecting the MOS field-effect transistor bulk and inversion charges Q_B and Q_I. This corresponds to two admittance components Y_{GB}^V and Y_{GC}^V, respectively. These quantities do not only depend on the applied voltage V but also on the total trapped charge $Q_T = Q_{T0} + \delta Q_T(t)$ and, consequently, on the frequency. The charges can be linearized using Taylor expansion around the dc point O (V_0, Q_{T0}), where the device and the defects are in equilibrium conditions. For simplicity, the calculation is shown for Q_B, the same considerations of which applying to Q_I (see Annex A for details on charge partitioning), i.e.,

$$Q_B(V,Q_T,t) = Q_B(V_0,Q_{T0}) + \left.\frac{\partial Q_B(V,Q_T)}{\partial Q_T}\right|_O \delta Q_T(t) + \left.\frac{\partial Q_B(V,Q_T)}{\partial V}\right|_O v(t) \quad (15)$$

and the related admittances as

$$Y_{\mathrm{GB}}^V(V,Q_T) = j\omega\frac{\partial Q_B(V,Q_T)}{\partial V} = \left.\frac{\partial Q_B(V,Q_T)}{\partial Q_T}\right|_O Y^T(\omega) + j\omega \left.\frac{\partial Q_B(V,Q_T)}{\partial V}\right|_O. \quad (16)$$

Two contributions enter in (16). Indeed, recalling (13), we can notice that the first contribution depends on $j\omega(\partial Q_T/\partial V) = Y^T(\omega)$ with the corrective term $(\partial Q_B(V,Q_T)/\partial Q_T)|_O$. This can be determined by expressing the charge variation as

$$\left.\frac{\partial Q_B(V,Q_T)}{\partial Q_T}\right|_O = \frac{Q_B^{\mathrm{HF}} - Q_B^{\mathrm{LF}}}{Q_T^{\mathrm{HF}} - Q_T^{\mathrm{LF}}} = \frac{C_{\mathrm{GB}}(\omega\to\infty) - C_{\mathrm{GB}}(\omega\to 0)}{C^T(\omega\to\infty) - C^T(\omega\to 0)} \quad (17)$$

with $Q_B^{\mathrm{HF}} = Q_B(V,\omega\to\infty)$ and $Q_B^{\mathrm{LF}} = Q_B(V,\omega\to 0)$.

The gate-to-bulk $C_{\mathrm{GB}}(\omega\to\infty) = Q_B^{\mathrm{HF}} - Q_{B0}/v_{\mathrm{ac}}$ is calculated from the device electrostatics simulated at $V = V_0 + v_{\mathrm{ac}}$ with the self-consistent PS solver, when all the traps are not supposed to respond to the frequency and are considered as fixed charges. In such a case, they do not follow the small-signal bias voltage, and their charge distribution remains the same as the one calculated in dc (modulated through f_{T0}), as at infinite frequency, the defects do not have the time to respond to a small-signal voltage variation applied to the gate. Capacitance $C_{\mathrm{GB}}(\omega\to 0) = Q_B^{\mathrm{LF}} - Q_{B0}/v_{\mathrm{ac}}$, on the other hand, is obtained from a PS simulation applying the same dc voltage $V = V_0 + v_{\mathrm{ac}}$, with f_T calculated from the new bias conditions. Similar considerations apply for the gate-to-channel capacitances $C_{\mathrm{GC}}(\omega\to\infty)$ and $C_{\mathrm{GC}}(\omega\to 0)$ using Q_I.

Knowing that the trap response is null at HF ($\omega\to\infty \Rightarrow \delta Q_T \to 0$), the second contribution in (16) is

$$j\omega \left.\frac{\partial Q_B(V,Q_T)}{\partial V}\right|_O = Y_{\mathrm{GB}}^V(\omega\to\infty) = G_{\mathrm{GB}}(\omega\to\infty) - j\omega C_{\mathrm{GB}}(\omega\to\infty). \quad (18)$$

Conductance $G_{\mathrm{GB}} = \Delta(J_{\mathrm{WKB}} + J_{\mathrm{TAT}}^{\mathrm{SS}})/v_{\mathrm{ac}}$ is determined from the steady-state trap-assisted $J_{\mathrm{TAT}}^{\mathrm{SS}}$ and the direct tunneling J_{WKB} current components.

We replace the two contributions with the expressions obtained in (17) and (18). Therefore, (16) can be rewritten as

$$Y_{\mathrm{GB}}^V(V,Q_T) = -Y^T(\omega)\frac{C_{\mathrm{GB}}(\omega\to\infty) - C_{\mathrm{GB}}(\omega\to 0)}{C^T(\omega\to 0)} + Y_{\mathrm{GB}}^V(\omega\to\infty). \quad (19)$$

In other words, the total admittances can be expressed from the HF term and a correction term proportional to the intrinsic total trap admittance.

3) AC Model Validation: The proposed ac signal model has been compared with the transient approach, simulating the response upon the application of a sinusoidal voltage pulse and extracting all the displacement currents in the system. The structure taken into account is a 50-Å-thick SiO_2 NMOS device, where a uniform trap distribution in energy is placed from the Si conduction and valence-band edges at 2 Å from the Si/SiO_2 interface. Fig. 2 compares the trap response obtained with the two approaches for an *amphoteric*-like trap distribution. The displacement currents determined from transient simulations are used for extracting the admittance components of the system. In particular, Y_{GB}^V, Y_{GB}^T, Y_{GC}^V, and Y_{GC}^T have been extracted from the amplitudes of the current

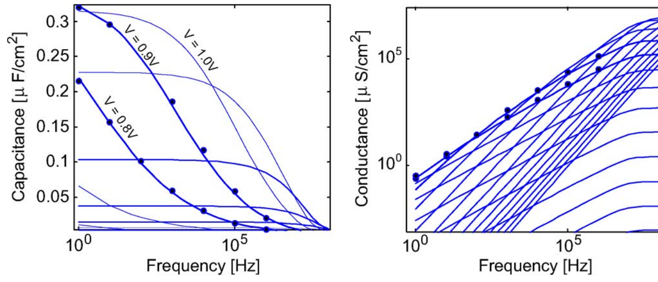

Fig. 2. Trap (left) capacitance $C_{\rm CB}^{T} = {\rm Im}(Y_{\rm CB}^{T})/\omega$ and (right) conductance $G_{\rm CB}^{T} = {\rm Re}(Y_{\rm CB}^{T})$ calculated with (lines) the ac small-signal model and (symbols) the transient extraction as a function of the ac frequency and for voltages ranging from 0 to 2.0 V with steps of 0.1 V. The cut frequency is related to the characteristic trap frequency τ_t^{-1} determined with (10). The admittances $Y_{\rm CB}^{T}$ and $Y_{\rm CB}^{T}$ are computed with (13) and partitioning the holes and electrons following the considerations in Annex A.

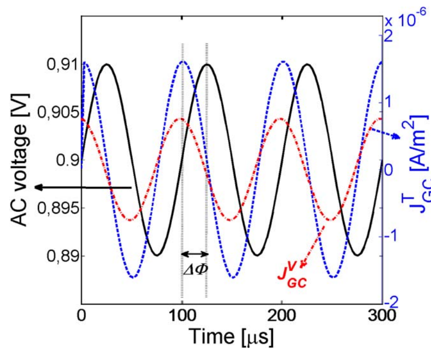

Fig. 3. (Black solid line) Applied ac pulse, (red dot-dashed line) channel displacement current $J_{\rm GC}^{V}$, and (blue dashed line) trap displacement current $J_{\rm GC}^{T}$ as a function of time simulated in the transient regime. The calculation of the admittance component is performed determining a phase shift $\Delta\Phi$ and the ratio of the amplitudes between the curves and the applied pulse.

densities $J_{\rm GB}^{V} = \partial Q_B/\partial t$, $J_{\rm GB}^{T} = \partial \tilde{Q}_T/\partial t$, $J_{\rm GC}^{V} = \partial Q_I/\partial t$, and $J_{\rm GC}^{T} = \partial Q_T/\partial t$, using $Y = |J|/v_{\rm ac} \exp(j\Delta\Phi)$; $\Delta\Phi$ is the phase shift between J and $v(t)$. In Fig. 3, the applied ac sinusoidal pulse and the transient current flowing toward the conduction band upon the application of a small-signal voltage are shown as a function of time. The admittances are then extracted from the phase shift $\Delta\Phi$ and the amplitude of the response signal with respect to the applied sinusoidal pulse.

III. AC Analysis

AC characteristics of multifingered NMOS devices integrated in a 65-nm technology have been measured using a HP4284A LCR meter. The transistors have been subject to electrical stress by applying a positive constant gate voltage stress through the $\rm SiO_2$ gate dielectric, keeping the other nodes grounded and varying the duration of pulse $t_{\rm str}$ and the applied stress voltage $V_{\rm str}$. This also corresponds to the positive-bias temperature instability stress condition that NMOS devices are commonly subject to.

A. CV Characteristics

Figs. 4 and 5 compare the split CV characteristics $C_{\rm GC}$ and $C_{\rm GB}$ of fresh and degraded devices, after different stress conditions and at temperature $T = 25\ ^\circ$C. In Fig. 4(a), the characteristics of an unstressed device having an oxide thickness of $T_{\rm ox} = 65$ Å have been fitted without traps in the $\rm SiO_2$ stack. Different stress conditions have been applied, i.e., $t_{\rm str} = 1000s$ at $V_{\rm str} = 6$ V, $t_{\rm str} = 100s$ at $V_{\rm str} = 6.7$ V, and $t_{\rm str} = 1000s$ at $V_{\rm str} = 6.7$ V [see Fig. 4(b)–(d)]. The spatial and energy distributions are a result of the reverse modeling extraction methodology. They have been extracted from measurement results and taking into account physical considerations. They have been found to be compatible with both measurement results and extracted profiles using conventional CGV extraction methods [10], [12]. The adopted spatial/energetic defect profile has been modeled with two uncorrelated Gaussian distributions in which the spatial mean value is placed at 2 Å from the Si/$\rm SiO_2$,

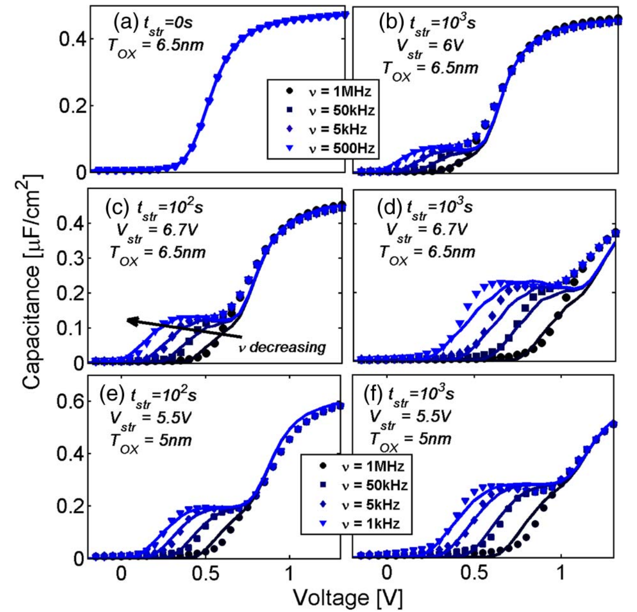

Fig. 4. Gate-channel capacitance $C_{\rm GC}$ as a function of the bias voltage for different small-signal frequencies and stress durations. (a) The characteristic of a fresh MOS device is shown. [(b)–(d)] The device has been stressed for different conditions using positive constant voltage stress. (Symbols) Measured results match capacitance values calculated with (lines) the MPA ac model well. Plots in (e)–(f) indicate results obtained with devices having $T_{\rm OX} = 5$ nm.

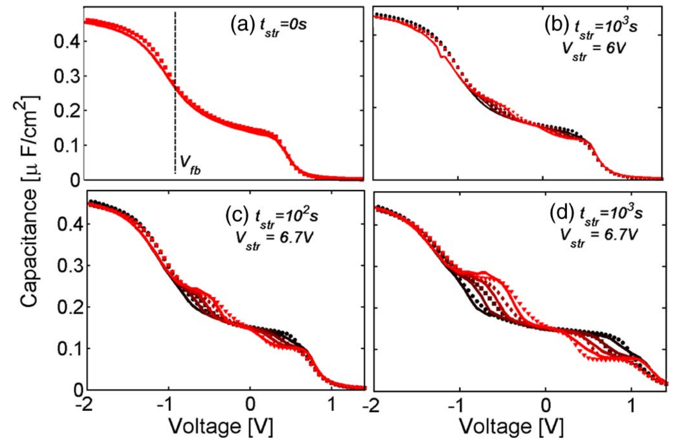

Fig. 5. Identical measurement conditions as in Fig. 4(b)–(d) but showing the gate-bulk capacitance $C_{\rm GB}$. Moreover, in this case, the effects are reproduced, including the frequency dependence of bulk charges in weak inversion.

the energy mean is in correspondence of the Si midgap, the spatial variance σ_x is 2 Å, and the energetic variance σ_E is 0.6 eV (almost uniform energetic profile in the midgap). The same profile has been adopted for all the cases. Only the peak of the Gaussian defect concentration is varied, i.e., $N_T = 1.25 \cdot 10^{19}$ cm^{-3}eV^{-1}, $N_T = 2.45 \cdot 10^{19}$ cm^{-3}eV^{-1}, and $N_T = 5.72 \cdot 10^{19}$ cm^{-3}eV^{-1} [see Fig. 4(b)–(d)]. In addition, fixed charges are expected to be stuck in the oxide during degradation by, e.g., Fowler–Nordheim tunneling [51], causing a slight rigid voltage shift of the characteristics. The positive voltage shift varies with the stress condition and remains relatively small compared with the 600- to 700-mV stretch-out $V_{\rm th}$ shift due to trap filling, i.e., $\Delta V = 50$ mV, corresponding to a surface concentration of $1.56 \cdot 10^{11}$ cm^{-2}; $\Delta V = 100$ mV, corresponding to $3.12 \cdot 10^{11}$ cm^{-2}; and $\Delta V = 250$ mV, corresponding to $7.8 \cdot 10^{11}$ cm^{-2}. Both the threshold voltage shift and the parasitic capacitive component of the traps are reproduced for a frequency range from 500 Hz to 1 MHz. A similar extraction has been performed in Fig. 4(e) and (f) on a device with $T_{\rm ox} = 50$ Å, stressed for 100 and 1000 s at $V_{\rm str} = 5.5$ V. Minimal variations in the defect concentration energy profile have been applied. The extracted total trap concentration is $4.09 \cdot 10^{19}$ and $6.45 \cdot 10^{19}$ cm^{-3}eV^{-1}, respectively.

As evidenced by CV curves, the following effects attributed to charge trapping emerge: 1) Inversion/accumulation are delayed to higher/lower voltages, i.e., $C_{\rm GC}/C_{\rm GB}$ are subject to a shift and a stretch-out [10]. 2) The $C_{\rm GC}$ ($C_{\rm GB}$, respectively) capacitance presents a frequency-dependent increase in the proximity of the weak-inversion (depletion, respectively) regions whose amplitude depends on $t_{\rm str}$ and $V_{\rm str}$. 3) The $C_{\rm GB}$ capacitance presents a frequency-dependent reduction in the weak-inversion region in correspondence of effect 2. The stretch-out of the capacitance in both inversion and accumulation is attributed to defect charging [1] and is correlated to the amplitude of the peaks in weak inversion and depletion. Since the CV stretch-out is only caused by a change in the electrostatics of the system in *equilibrium* conditions, effect 1 is not dependent on the frequency of the applied pulse.

The C/E rates of the traps have to be considered to explain the frequency dependence of both $C_{\rm GC}$ and $C_{\rm GB}$ (effect 2). At a given frequency, only traps with C/E rates higher than the measurement frequency are able to follow the ac small-signal voltage. The strong dependence of the rates with respect to trap depth results from the exponential decrease in the evanescent carrier wave function in the oxide depth [18]. Wide distributions of C/E rates in energy have been also obtained. This is highlighted in Fig. 6, where the characteristic trap frequency τ_t^{-1}, calculated with (10), is plotted as a function of trap depth but also energy. The wide exponential distribution of C/E rates in energy could be at the origin of an apparent lack of correlation between the capture rate and the defect depth, as reported in [27] and [52]. The large exponential decrease in τ_t^{-1} in energy and position also explains the strong frequency dependence of the intrinsic trap capacitance, i.e., in weak/strong inversion, traps near the Si conduction band easily exchange carriers with the channel and their capacitance response is maximum and saturating. In depletion, both the carrier concentrations and the cutoff frequency are reduced, with lower frequencies required

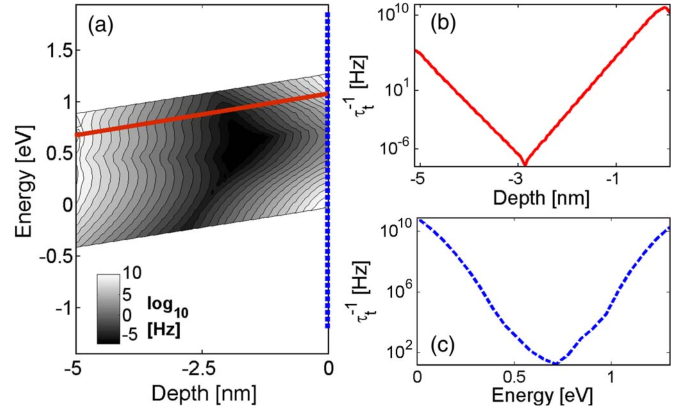

Fig. 6. Simulated trap characteristic frequency in depletion. (a) The energetic and spatial profile is shown. C/E of charges with the substrate increases when approaching the conduction or valence bands of the channel/gate reservoirs. The decrease in oxide depth shown in (b) in a cut at $E = E_C^{\rm Si}$ is due to the exponential carrier wave-function penetration, whereas inelastic multi-phonon events determine the behavior in energy shown in (c) at the Si/SiO$_2$ interface ($x = 0$ nm). The energy reference adopted is the valence band of the Si substrate.

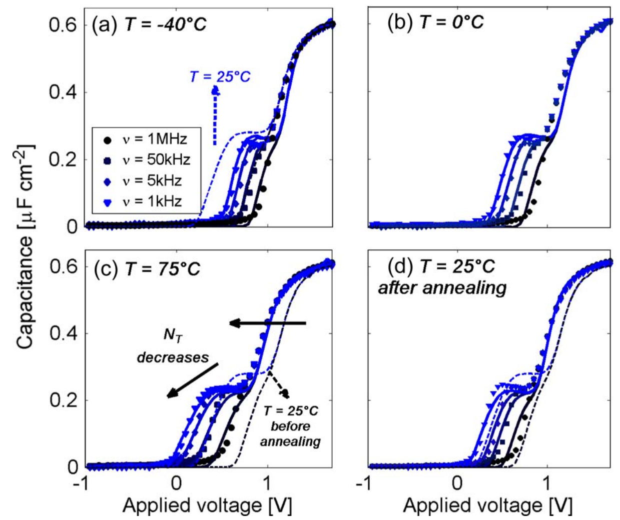

Fig. 7. (Symbols) Measured and (lines) simulated $C_{\rm GC}$ capacitance as a function of applied bias, for different frequencies and temperatures. The measurements are performed in a specific order. Low-temperature measurements at (a) -40 °C and (b) 0 °C show a decrease in the trap frequency response and the narrowing of the capacitive parasitic response. (c) At 75 °C, a part of the defects relaxes due to the long bench stabilization time (10 min), performed before the measurement. (d) Measured and simulated capacitances at 75 °C with the distribution in (c), highlighting trap recovery.

to scan the traps; consequently, for a given frequency, the capacitive response decreases. At flat band and in accumulation, the h^+ trapping probability increases, and defects near the Si valence band having a cutoff frequency higher than the ac signal frequency can be characterized [53].

B. Temperature Dependence

MPA transitions generally exhibit a strong temperature dependence. CV curves of the stressed device in Fig. 4(f) have been measured at lower temperatures [see Fig. 7(a) and (b)], where multiphonon transitions are slower due to the decrease in the phonon occupation factor. Consequently, the trap cutoff

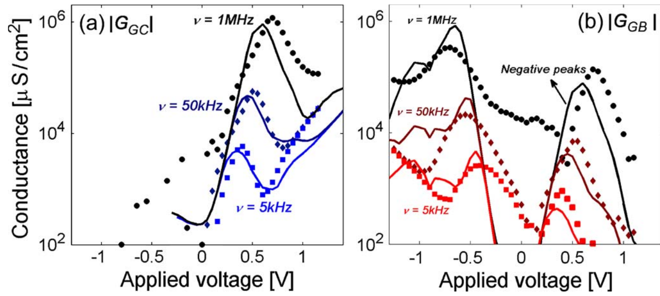

Fig. 8. (Symbols) Measured and (lines) simulated conductances as a function of applied voltage and frequency (from 5 kHz to 1 MHz) for a device with $T_{\rm ox} = 18$ Å and after 1000 s of constant current stress at $I_{\rm str} = 10^{-8}$ A. Good agreement is found for both (a) $|G_{\rm GC}|$ and (b) $|G_{\rm GB}|$. In particular, the negative peak on $G_{\rm GB}$ in weak inversion is also well reproduced.

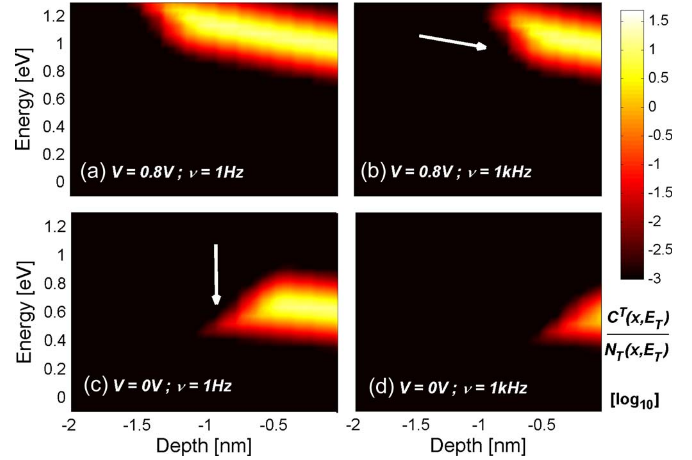

Fig. 9. Simulated and normalized capacitive response of traps in oxide depth and trap energy, for two frequencies (1 Hz and 1 kHz) and two dc voltages in depletion and accumulation. Lower frequencies scan deeper in the oxide. The energy reference adopted is the valence band of the Si substrate.

frequency decreases, and thus, the trap capacitance measured at a given frequency is reduced [53]. The magnitude of the parasitic capacitance contribution and the quantity of stretch-out remain constant, i.e., the total defect concentration does not vary for low temperatures.

The CV measurement has been also performed at higher temperatures. In such a case, the parasitic trap capacitance is enhanced at intermediate frequencies (i.e., larger spreading of the curves in frequency). In addition, the evidence of trap recovery is found in the reduction of both capacitance peaks and stretch-out effects with temperature increase. This phenomenon has been taken into account in the model by decreasing the trap concentration to $N_T = 5.72 \cdot 10^{19}$ cm^{-3}eV^{-1}. Good agreement with measurements has been found both in terms of stretch-out and magnitude of parasitic peaks. In addition, the spreading in frequency is well aligned with the increase in C/E rates and of the capacitive response at lower frequencies.

C. GV Characteristics

Fig. 8 presents conductance measurements as a function of applied voltage performed after 1000 s of positive constant current stress at $I_{\rm str} = 10^{-8}$ A using a device with $T_{\rm ox} = 18$ Å. Simulations obtained using $N_T = 2.8 \cdot 10^{12}$ cm^{-2} are also shown in Fig. 8(b), with a distribution similar to the one adopted for Fig. 4. Both channel $|G_{\rm GC}|$ in Fig. 8(a) and bulk $|G_{\rm GB}|$ conductances in Fig. 8(b) are matching well with measurements and show the exponential decrease in the peaks in frequency.

Parasitic peaks can be seen on both $|G_{\rm GC}|$ and $|G_{\rm GB}|$ conductances after 1000 s of electrical stress. In addition to the positive parasitic peak near the flat band voltage, the bulk conductance shows a negative parasitic contribution in correspondence of the peak on $G_{\rm GC}$ in weak inversion. This indicates the response of the bulk charges to the filling of traps by electrons and corresponds to the frequency dependence of $C_{\rm GB}$ in inversion. The magnitude of all the peaks increases at HF. It should be pointed out that the negative peak on $G_{\rm GB}$ is generally masked by the rise of $G_{\rm GC}$ in inversion and it cannot be thus identified only by measuring the total conductance $G_{\rm GG}$. Additionally, both the steady-state TAT and the direct tunneling currents calculated with (5) have been taken into account. This is particularly evident at higher bias voltages, where the conductance increase due to oxide leakage current is present in both simulation and measurement results.

IV. Discussion

A first relevant question relates to whether trap parameters such as the Huang–Rhys factor and the spatial/energetic trap distribution can be experimentally determined. Inversely, could the presented model be used in the interpretation of measurements, such as CV versus frequency, and capture cross sections results associated with deep-level oxide defects? Some authors claim it is possible and interesting to do so [15], [47], [54], although as pointed out by Stoneham, fitting the defect parameters with a simplified model would certainly cause a false illusion of accuracy [55]. This results from the fact that one tries to describe a complex system using models including coarse approximations. The parameters should be regarded as effective values rather than microscopic ones, and the fit may not be unique.

Nevertheless, some interesting qualitative features can be investigated concerning the trap charging model, as well as their energetic and spatial distribution. Using the device analyzed in Fig. 4(f), the oxide regions contributing to the CV response have been calculated and shown in Fig. 9, where the capacitive response normalized over $N_T(x, E_T)$ is plotted as a function of the oxide depth and energy for two different frequencies and dc voltages.[1] This quantity, representing the probed region at a given dc bias and frequency, should be compared with the probed region determined in charge pumping (CP) simulations shown in Part II of this paper.

Fig. 10 shows the effects of the energy variance of amphoteric defects localized at the midgap. In Fig. 10(a), for $\sigma_E = 0.1$ eV, the intrinsic trap response is small due to the high cutoff frequency of midgap traps. When σ_E increases, interface and border traps localized near the Si conduction- and valence-band edges communicate with the channel, and the trap capacitance

[1] A supplementary color MPEG file showing the probed region for a sweep on the dc bias is available at http://ieeexplore.ieee.org.

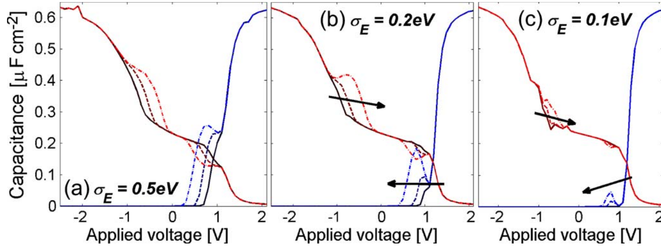

Fig. 10. Capacitance versus applied voltage curves for different distributions of defects centered at midgap, where the variance in energy has been applied from 0.5 to 0.1 eV. The simulated temperature is $T = 300$ K, and the total concentration has been kept constant.

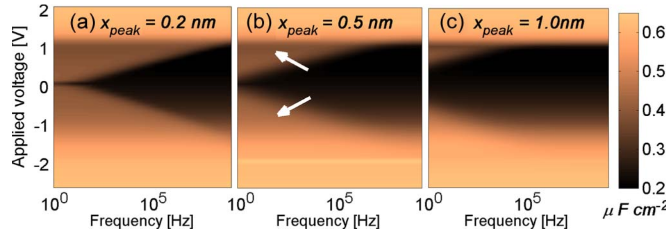

Fig. 11. Color plots showing the simulated gate capacitance versus the applied voltage and the small-signal frequency for three different mean positions of the spatial trap distribution, from 0.2 to 1 nm. Deeper traps have longer time constants causing trap C/E with the Si conduction and valence bands of the gate and channel to decrease.

significantly increases. The same amount of stretch-out can be observed since the dc electrostatics is only impacted by the total trap concentration, maintained constant for all the simulations.

The response of deeper defects has been also investigated. In Fig. 11, the depth of defects in the oxide layer is progressively increased. Traps located in the middle of the oxide indeed have a lower frequency response, but they can be characterized with TAT measurements as they communicate with both the substrate (high carrier capture probability) and gate reservoirs (high carrier emission probability) [30].

V. Conclusion

Multiphonon models are promising approaches for the investigation of charge-trapping effects in dielectrics. A general model for the calculation of MOS impedances and supporting multiphonon trapping theory has been derived. It includes TAT and direct tunneling effects across the oxide and intrinsically accounts for capacitance stretch-out, trap frequency response, and temperature dependence. Additionally, the frequency-dependent peaks and the effects of direct tunneling on conductance curves have been reproduced.

The widespread distribution of trapping rates is responsible of the strong frequency dependence of the capacitances and conductances of stressed devices. Correlation between the trapping constants with the ac response in frequency and stretch-out has been found. This result confirms the measured trap C/E constants recently reported in literature [40], whose values range from nanoseconds to months or years.

The proposed model can be used for the physical analysis of charge-trapping effects, the extraction of trap concentration from ac characteristics, and for evaluating the quality of dielectrics in modern nanoscale technologies.

In the previous simulations, the dc operating point for the ac analysis has been calculated in *equilibrium* conditions, thus neglecting all the transient effects present in the real system when ramping the dc voltage rapidly. However, the model results indicate that some traps have time constants much higher than the measurement time between two voltages. Single defect studies [56], [57] and transient characteristics also indicated the presence of nonequilibrium conditions. This second extreme situation is analyzed in the second part of this paper, focused in particular on out-of-equilibrium transient effects in CP analyses and hysteresis effects in ac curves.

Appendix A
Trap Charge Models and Partitioning

As electron spin resonance and scanning tunneling spectroscopy experiments [58], [59] extensively demonstrated, P_b centers exhibit an *amphoteric* charge nature, being neutral when unoccupied and have the possibility to capture an h^+ or an e^- $(+ \rightarrow 0 \rightarrow -)$. In addition, depending on their nature (E'_γ, E'_δ centers, ... [35]), oxide/border defects can be *acceptor*-like traps, i.e., neutral defects becoming negatively charged $(0 \rightarrow -)$ when an e^- is captured or an h^+ is emitted, or *donor*like traps, which are positively charged defects becoming neutralized $(+ \rightarrow 0)$ when an e^- is captured or an h^+ is emitted.

The total trapped charge $\rho_T(x,t)$ for acceptor and donor, respectively, can be calculated using

$$\rho_T(x,t) = -\int_{E_T} f_T(x, E_T, E_F, t) N_T dE_T$$

$$\rho_T(x,t) = \int_{E_T} \left(1 - f_T(x, E_T, E_F, t)\right) N_T dE_T \qquad (20)$$

where $f_T(x, E_T, E_F(x,t), t)$ expresses the occupation function of the trap, i.e., the probability a trap placed at energy E_T and position x is occupied by an electron at time t.

Rigorous modeling of amphoteric states with doubled occupancy would require to account for the Coulombic energy shift between the $(0/-)$ and $(+/0)$ energy transitions. For Si dangling bonds, such energy shift can be quite large (e.g., approximately 0.75 eV for defects on (111) Si surfaces [60]) and a rigorous calculation would require to determine two occupation functions f_T^0 and f_T^- for each occupancy state [61]. However, in order to extend the formalism developed in this paper to amphoteric-like defects, we neglected the Coulombic energy and approximate the total charge with

$$\rho_T(x,t) = \int_{E_T} \left(1 - 2f_T(x, E_T, E_F, t)\right) N_T dE_T. \qquad (21)$$

In Fig. 12, calculations of the gate capacitance have been performed using donor-, acceptor-, and amphoteric-like defects. The trap capacitive response is observed similar for *donor* and *acceptor* traps, whereas the amplitude is doubled for *amphoteric* ones. The main difference between the three models originates from the rigid voltage shift and stretch-out

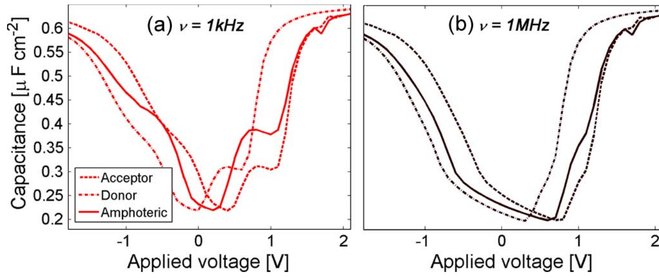

Fig. 12. (a) Low-frequency and (b) HF gate capacitance as a function of applied voltage for the three charge models, i.e., amphoteric, acceptor, and donor traps. While acceptor traps and donor traps are stretching out the capacitance curve in inversion and accumulation, respectively, amphoteric traps are altering the curves in both inversion and accumulation regions.

that is positive for *acceptors* in inversion, negative for *donors* in accumulation, and positive and negative for *amphoteric* in both accumulation and inversion. This latter behavior confirmed by experiment indicates that trapping mechanisms involving P_b centers dominate the effects on impedances [1], [12].

Partitioning is required to attribute the trapped charge to its correct energy band and interface in the calculation of the ac response. The criteria adopted in this paper consider the net tunneling fluxes $\Phi_n = \Phi_c - \Phi_e$ between the different bands and interfaces as weighting factors. Considering the net flux currents at the two interfaces, the trapped charge ρ_T can be partitioned in two components ρ_T^L and ρ_T^R, associated to the contribution of gate L and of channel R, respectively. The four net fluxes $\Phi_n^L = \Phi_c^L - \Phi_e^L$, $\Phi_n^R = \Phi_c^R - \Phi_e^R$, $\tilde{\Phi}_n^L = \tilde{\Phi}_c^L - \tilde{\Phi}_e^L$, and $\tilde{\Phi}_n^R = \tilde{\Phi}_c^R - \tilde{\Phi}_e^R$ with respect to the e^- and h^+ flows at the left and right oxide interfaces are determined using the notations in Fig. 1(b). The charge partitioning is obtained using

$$\rho_T^R = -\frac{\Phi_n^R}{\Phi_n^L - \tilde{\Phi}_n^L - \left(\Phi_n^R - \tilde{\Phi}_n^R\right)}\rho_T$$

$$\rho_T^L = \frac{\Phi_n^L}{\Phi_n^L - \tilde{\Phi}_n^L - \left(\Phi_n^R - \tilde{\Phi}_n^R\right)}\rho_T. \quad (22)$$

A similar approach is applied for holes and for weighting the TAT currents.

References

[1] D. Fleetwood, P. Winokur, R. Reber, T. Meisenheimer, J. Schwank, M. Shaneyfelt, and L. Riewe, “Effects of oxide traps, interface traps, and border traps on metal-oxide-semiconductor devices,” *J. Appl. Phys.*, vol. 73, no. 10, pp. 5058–5074, 2009.

[2] H. Wong, M. White, T. Krutsick, and R. Booth, “Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFETs,” *Solid State Electron.*, vol. 30, no. 9, pp. 953–968, 1987.

[3] D. Ielmini, A. Spinelli, M. Rigamonti, and A. Lacaita, “Modeling of SILC based on electron and hole tunneling. I. Transient effects,” *IEEE Trans. Electron Devices*, vol. 47, no. 6, pp. 1258–1265, Jun. 2000.

[4] A. van der Wel, E. Klumperink, E. Hoekstra, and B. Nauta, “Relating random telegraph signal noise in metal-oxide-semiconductor transistors to interface trap energy distribution,” *Appl. Phys. Lett.*, vol. 87, no. 18, p. 183 507, Oct. 2005.

[5] I. Chen, S. Holland, and C. Hu, “Electrical breakdown in thin gate and tunneling oxides,” *IEEE J. Solid-State Circuits*, vol. SSC-20, no. 1, pp. 333–342, Feb. 1985.

[6] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, “Introduction to Flash memory,” *Proc. IEEE*, vol. 91, no. 4, pp. 489–502, Apr. 2003.

[7] D. Garetto, Y. M. Randriamihaja, D. Rideau, E. Dornel, W. Clark, A. Schmid, V. Huard, H. Jaouen, and Y. Leblebici, “Small signal analysis of electrically-stressed oxides with Poisson–Schroedinger based multi-phonon capture model,” in *Proc. IEEE Int. Workshop Comput. Electron.*, 2010, pp. 1–4.

[8] S. Lombardo, B. De Salvo, C. Gerardi, and T. Baron, “Silicon nanocrystal memories,” *Microelectron. Eng.*, vol. 72, no. 1–4, pp. 388–394, 2004.

[9] D. Ielmini, A. Spinelli, M. Rigamonti, and A. Lacaita, “Modeling of SILC based on electron and hole tunneling. II. Steady-state,” *IEEE Trans. Electron Devices*, vol. 47, no. 6, pp. 1266–1272, Jun. 2000.

[10] E. Nicollian and J. Brews, *MOS/Metal Oxide Semiconductor/Physics and Technology*. Hoboken, NJ: Wiley, 1982.

[11] L. Terman, “An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes,” *Solid State Electron.*, vol. 5, no. 5, pp. 285–299, Sep./Oct. 1962.

[12] M. Fischetti, “Generation of positive charge in silicon dioxide during avalanche and tunnel electron injection,” *J. Appl. Phys.*, vol. 57, no. 8, pp. 2860–2879, Apr. 1985.

[13] R. Castagne and A. Vapaille, “Description of the SiO_2—Si interface properties by means of very low frequency MOS capacitance measurements,” *Surf. Sci.*, vol. 28, no. 1, pp. 157–193, Nov. 1971.

[14] P. Masson, J. Autran, M. Houssa, X. Garros, and C. Leroux, “Frequency characterization and modeling of interface traps in $HFSi_xO_y/HFO_2$ gate dielectric stack from a capacitance point-of-view,” *Appl. Phys. Lett.*, vol. 81, no. 18, pp. 3392–3394, Oct. 2002.

[15] M. Satter and A. Haque, “Modeling effects of interface traps on the gate CV characteristics of MOS devices on alternative high-mobility substrates,” *Solid State Electron.*, vol. 54, no. 6, pp. 621–627, Jun. 2010.

[16] K. Zaininger and G. Warfield, “Limitations of the MOS capacitance method for the determination of semiconductor surface properties,” *IEEE Trans. Electron Devices*, vol. ED-12, no. 4, pp. 179–193, Apr. 1965.

[17] F. Heiman and G. Warfield, “The effects of oxide traps on the MOS capacitance,” *IEEE Trans. Electron Devices*, vol. ED-12, no. 4, pp. 167–178, Apr. 1965.

[18] L. Freeman and W. Dahlke, “Theory of tunneling into interface states,” *Solid State Electron.*, vol. 13, no. 11, pp. 1483–1503, Nov. 1970.

[19] W. Shockley and W. Read, Jr, “Statistics of the recombinations of holes and electrons,” *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.

[20] H. Lakhdari, D. Vuillaume, and J. Bourgoin, “Spatial and energetic distribution of Si-SiO_2 near-interface states,” *Phys. Rev. B, Condens. Matter*, vol. 38, no. 18, pp. 13 124–13 132, Dec. 1988.

[21] D. Bauza and G. Ghibaudo, “New model for the characterization of bulk traps by current deep level transient spectroscopy in metal-oxide-semiconductor transistors,” *J. Appl. Phys.*, vol. 70, no. 6, pp. 3333–3337, Sep. 1991.

[22] A. Palma, A. Godoy, J. Jimenez-Tejada, J. Carceller, and J. Lopez-Villanueva, “Quantum two-dimensional calculation of time constants of random telegraph signals in metal-oxide–semiconductor structures,” *Phys. Rev. B, Condens. Matter Mater. Phys.*, vol. 56, no. 15, pp. 9565–9574, Oct. 1997.

[23] D. Bauza and Y. Maneglia, “In-depth exploration of Si-SiO_2 interface traps in MOS transistors using the charge pumping technique,” *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2262–2266, Dec. 1997.

[24] P. Masson, J.-L. Autran, and J. Brini, “On the tunneling component of charge pumping current in ultrathin gate oxide MOSFETs,” *IEEE Electron Device Lett.*, vol. 20, no. 2, pp. 92–94, Feb. 1999.

[25] X. Garros, M. Casse, G. Reimbold, F. Martin, L. Brunet, F. Andrieu, and F. Boulanger, “Reliability concerns in high-k/metal gate technologies,” in *Proc. IEEE ICICDT*, 2010, pp. 90–93.

[26] D. Garetto, Y. M. Randriamihaja, A. Zaka, D. Rideau, A. Schmid, H. Jaouen, and Y. Leblebici, “Analysis of defect cross sections using non-radiative MPA quantum model,” *Solid State Electron.*, 2011, to be published. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S003811011100387X.

[27] T. Nagumo, K. Takeuchi, T. Hase, and Y. Hayashi, “Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps,” in *IEDM Tech. Dig.*, 2010, pp. 28.3.1–28.3.4.

[28] B. Ridley, “The photoionisation cross section of deep-level impurities in semiconductors,” *J. Phys. C, Solid State Phys.*, vol. 13, no. 10, p. 2015, Apr. 1980.

[29] D. Goguenheim and M. Lannoo, “Theoretical and experimental aspects of the thermal dependence of electron capture coefficients,” *J. Appl. Phys.*, vol. 68, no. 3, pp. 1059–1069, Aug. 1990.

[30] F. Jiménez-Molinos, A. Palma, F. Gamiz, J. Banqueri, and J. Lopez-Villanueva, “Physical model for trap-assisted inelastic tunneling in

metal-oxide-semiconductor structures," *J. Appl. Phys.*, vol. 90, no. 7, pp. 3396–3404, Oct. 2001.

[31] F. Jiménez-Molinos, A. Palma, A. Gehring, F. Gámiz, H. Kosina, and S. Selberherr, "Static and transient simulation of inelastic trap-assisted tunneling," in *Proc. 14th Workshop Model. Simul. Electron Devices*, 2003, pp. 65–68.

[32] F. Jiménez-Molinos, F. Gámiz, A. Palma, P. Cartujo, and J. López-Villanueva, "Direct and trap-assisted elastic tunneling through ultrathin gate oxides," *J. Appl. Phys.*, vol. 91, no. 8, pp. 5116–5124, Apr. 2009.

[33] L. Larcher, "Statistical simulation of leakage currents in MOS and Flash memory devices with a new multiphonon trap-assisted tunneling model," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1246–1253, May 2003.

[34] L. Vandelli, A. Padovani, L. Larcher, R. Southwick, W. Knowlton, and G. Bersuker, "A physical model of the temperature dependence of the current through SiO_2/HfO_2 stacks," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2878–2887, Sep. 2011.

[35] W. Goes, M. Karner, V. Sverdlov, and T. Grasser, "Charging and discharging of oxide defects in reliability issues," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 3, pp. 491–500, Sep. 2008.

[36] T. Grasser, W. Gos, and B. Kaczer, "Dispersive transport and negative bias temperature instability: Boundary conditions, initial conditions, and transport models," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 1, pp. 79–97, Mar. 2008.

[37] T. Grasser and B. Kaczer, "Evidence that two tightly coupled mechanisms are responsible for negative bias temperature instability in oxynitride MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1056–1062, May 2009.

[38] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "Understanding negative bias temperature instability in the context of hole trapping (Invited Paper)," *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1876–1882, Jul. 2009.

[39] T. Grasser and B. Kaczer, "Critical modeling issues in negative bias temperature instability," in *Proc. Eur. Symp. Reliab. Electron Devices*, 2009, p. 265.

[40] T. Grasser, H. Reisinger, W. Goes, T. Aichinger, P. Hehenberger, P. Wagner, M. Nelhiebel, J. Franco, and B. Kaczer, "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," in *IEDM Tech. Dig.*, 2010, pp. 1–4.

[41] T. Grasser, H. Reisinger, P. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *Proc. IRPS*, 2010, pp. 16–25.

[42] R. Weeks, "The many varieties of E' centers: A review," *J. Non-Cryst. Solids*, vol. 179, pp. 1–9, Nov. 1994.

[43] S. Markov, "Gate leakage variability in nano-CMOS transistors," Ph.D. dissertation, Univ. Glasgow, Glasgow, U.K., 2009.

[44] P. Carrier, L. Lewis, and M. D. Wardana, "Optical properties of structurally relaxed Si/SiO_2 superlattices: The role of bonding at interfaces," *Phys. Rev. B, Condens. Matter Mater. Phys.*, vol. 65, no. 16, p. 165 339, Apr. 2002.

[45] F. Grunthaner, P. Grunthaner, R. Vasquez, B. Lewis, J. Maserjian, and A. Madhukar, "High-resolution X-ray photoelectron spectroscopy as a probe of local atomic structure: Application to amorphous SiO_2 and the Si- SiO_2 interface," *Phys. Rev. Lett.*, vol. 43, no. 22, pp. 1683–1686, Nov. 1979.

[46] A. Demkov and O. Sankey, "Growth study and theoretical investigation of the ultrathin oxide SiO_2-Si heterojunction," *Phys. Rev. Lett.*, vol. 83, no. 10, pp. 2038–2041, Sep. 1999.

[47] J. Zheng, H. Tan, and S. Ng, "Theory of non-radiative capture of carriers by multiphonon processes for deep centres in semiconductors," *J. Phys., Condens. Matter*, vol. 6, no. 9, p. 1695, Feb. 1994.

[48] B. Ridley, "Multiphonon, non-radiative transition rate for electrons in semiconductors and insulators," *J. Phys. C, Solid State Phys.*, vol. 11, no. 11, p. 2323, Jun. 1978.

[49] R. Tsu and L. Esaki, "Tunneling in a finite superlattice," *Appl. Phys. Lett.*, vol. 22, no. 11, pp. 562–564, Jun. 1973.

[50] R. Clerc, A. Spinelli, G. Ghibaudo, and G. Pananakakis, "Theory of direct tunneling current in metal–oxide–semiconductor structures," *J. Appl. Phys.*, vol. 91, no. 3, p. 1400, Feb. 2002.

[51] N. Klein and P. Solomon, "Current runaway in insulators affected by impact ionization and recombination," *J. Appl. Phys.*, vol. 47, no. 10, pp. 4364–4372, Oct. 1976.

[52] D. Goguenheim, D. Vuillaume, G. Vincent, and N. Johnson, "Accurate measurements of capture cross sections of semiconductor insulator interface states by a trap-filling experiment," *J. Appl. Phys.*, vol. 68, no. 3, pp. 1104–1113, Aug. 1990.

[53] D. Garetto, Y. Mamy-Randriamihaja, A. Zaka, D. Rideau, A. Schmid, H. Jaouen, and Y. Leblebici, "AC analysis of defect cross sections using non-radiative MPA quantum model," in *Proc. 11th IEEE Int. Conf. ULIS*, 2011, pp. 1–4.

[54] T. Kang, M. Chen, C. Liu, Y. Chang, and S. Fan, "Numerical confirmation of inelastic trap-assisted tunneling (ITAT) as SILC mechanism," *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 2317–2322, Oct. 2001.

[55] A. Stoneham, "Non-radiative transitions in semiconductors," *Rep. Progr. Phys.*, vol. 44, no. 12, p. 1251, Dec. 1981.

[56] M. Berthe, A. Urbieta, L. Perdigão, B. Grandidier, D. Deresmes, C. Delerue, D. Stiévenard, R. Rurali, N. Lorente, L. Magaud, and P. Ordejón, "Electron transport via local polarons at interface atoms," *Phys. Rev. Lett.*, vol. 97, no. 20, p. 206 801, Nov. 2006.

[57] M. Berthe, R. Stiufiuc, B. Grandidier, D. Deresmes, C. Delerue, and D. Stievenard, "Probing the carrier capture rate of a single quantum level," *Science*, vol. 319, no. 5862, pp. 436–438, Dec. 2008.

[58] W. Futako, N. Mizuochi, and S. Yamasaki, "In situ ESR Observation of interface dangling bond formation processes during ultrathin SiO_2 growth on Si(111)," *Phys. Rev. Lett.*, vol. 92, no. 10, p. 105 505, Mar. 2004.

[59] B. Tuttle, "Hydrogen and Pb defects at the (111) Si-SiO_2 interface: An ab-initio cluster study," *Phys. Rev. B, Condens. Matter Mater. Phys.*, vol. 60, no. 4, pp. 2631–2637, Jul. 1999.

[60] T. Nguyen, G. Mahieu, M. Berthe, B. Grandidier, C. Delerue, D. Stiévenard, and P. Ebert, "Coulomb energy determination of a single Si dangling bond," *Phys. Rev. Lett.*, vol. 105, no. 22, p. 226 404, Nov. 2010.

[61] M. White and C. Chao, "Statistics of deep-level amphoteric traps in insulators and at interfaces," *J. Appl. Phys.*, vol. 57, no. 6, pp. 2318–2321, Mar. 1985.

Davide Garetto was born in Torino, Italy, in 1984. He received the B.Sc. degree in computer engineering from Politecnico di Torino, Torino, in 2006, and the jointed M.Sc. degree in micro and nano technologies for integrated systems from the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland; the Institut National Polytechnique de Grenoble, Grenoble, France; and the Politecnico di Torino in 2008. Since November 2008, he has been working toward the Ph.D. degree in the Microelectronic System Laboratory (LSM), EPFL, in the IBM Systems and Technology group at the STMicroelectronics facility in Crolles, France.

His current research activity involves the modeling and integrated-circuit design of advanced metal–oxide–semiconductor devices in embedded non-volatile memory technologies, with emphasis on floating-gate transistors. His project involves analytical and optimized modeling of Flash cells, numerical simulations of device degradation, and electrical characterization.

Mr. Garetto was a recipient of the IBM Ph.D. fellowship for the years 2010 and 2011.

Yoann Mamy Randriamihaja was born in Grenoble, France, in 1985. He received the M.S. degree in micro- and nanoelectronics from Joseph Fourier University and the Engineering degree in microelectronics from the Institut National Polytechnique de Grenoble, Grenoble, in 2009. Since October 2009, he has been working toward the Ph.D. degree in micro- and nanoelectronics in the frame of a collaboration between the Institut Matériaux Microélectronique Nanosciences de Provence (IM2NP), Toulon, France, and the Department of Electrical Characterization and Reliability, STMicroelectronics, Crolles, France. His Ph.D. work focuses on the improvement of electrical characterization techniques of oxide defects and the understanding of physical phenomena observed when a transistor is under stress.

Denis Rideau received a Ph.D. degree in physics from the University of Orsay, Orsay, France, in 2001, and the Engineering degree from ESIEE, Paris, France, in 1996.

He is currently performing research and development in solid-state physics with STMicroelectronics, Crolles, France. He is involved in radio-frequency modeling and simulation of Si nanodevices, with emphasis on quantum effects, strain effects, and wafer orientations in FDSOI and fin-type metal–oxide–semiconductor field-effect transistors.

Alban Zaka was born in Tirana, Albania, in 1985. He received the M.Sc. degree in materials science and engineering from the National Institute of Applied Sciences (INSA), Lyon, France, in 2008. He is currently working toward the Ph.D. degree from the Institut National Polytechnique de Grenoble, Grenoble, France, and the University of Udine, Udine, Italy.

His current thesis work is supported by STMicroelectronics, Crolles, France. His research topics include the characterization and the simulation of hot-carrier injection phenomena in advanced nonvolatile memory devices.

Alexandre Schmid (S'98–M'04) received the M.Sc. degree in microengineering and the Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1994 and 2000, respectively.

Since 1994, he has been with the EPFL, working with the Integrated Systems Laboratory as a Research and Teaching Assistant, and with the Electronics Laboratories as a Postdoctoral Fellow. In 2002, he was a Senior Research Associate with the Microelectronic Systems Laboratory, where he has been conducting research in the fields of bioelectronic interfaces, nonconventional signal processing and neuromorphic hardware, and reliability of nanoelectronic devices, and also teaches with the Microengineering and Electrical Engineering Departments of EPFL. Since 2011, he is a "Maître d'Enseignement et de Recherche" Faculty Member with EPFL. He is a coauthor and a coeditor of two books and over 90 articles published in journals and conferences.

Dr. Schmid has served as the General Chair of the Fourth International Conference on Nano-Networks in 2009 and has been serving as an Associate Editor of the Institute of Electrical, Information, and Communication Engineers Electronics Express since 2009.

Yusuf Leblebici (M'90–SM'98–F'09) received the B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign (UIUC), Urbana-Champaign, in 1990.

Between 1991 and 2001, he was a Faculty Member with UIUC, Istanbul Technical University, and Worcester Polytechnic Institute. From 2000 to 2001, he was the Microelectronics Program Coordinator with Sabanci University. Since 2002, he has been a Chair Professor with the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, and the Director of the Microelectronic Systems Laboratory. He is the coauthor of four textbooks, namely, *Hot-Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers, 1993), *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications* (Springer, 2007), and *Fundamentals of High Frequency CMOS Analog Integrated Circuits* (Cambridge University Press, 2009), as well as more than 200 articles published in various journals and conferences. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of very large scale integrated (VLSI) systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis.

Dr. Leblebici has served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II and the IEEE TRANSACTIONS ON VLSI SYSTEMS. He has also served as the General Cochair of the 2006 European Solid-State Circuits Conference and the 2006 European Solid State Device Research Conference. He has been elected as a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.

Hervé Jaouen (SM'01) received the degree in engineering and the Ph.D. degree from the Institut National Polytechnique de Grenoble, Grenoble, France, in 1979 and 1984, respectively.

From 1981 to 1989, he was an Associate Professor with the Institut National Polytechnique de Grenoble, where he developed for his Ph.D. a novel microwave annealing technique of semiconductors. He then worked on electronic-transport properties of disordered matter. In 1989, he was with the Technology Computer-Aided Design (TCAD) Group of SGS Thomson Microelectronics, with the goal of developing a 2-D process simulation tool. Next, he was the Manager of the TCAD Group of Crolles' Plant for STMicroelectronics. Since 2004, he has been the Head of the ST Modeling Department, Crolles, France. The scope covered by his department includes TCAD, compact modeling, and electrostatic discharge (ESD) modeling. He has published over 80 papers in the area of microelectronics and is the holder of 18 granted U.S. patents in the field.

Dr. Jaouen was a recipient of the ST's Exceptional Patent Award in 2003. He holds positions on the technical program committees of ESSDERC, International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), and European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) conferences and was a member of the International Electron Devices Meeting (IEDM) technical program committee. He serves as the European representative for the International Roadmap for Semiconductors in the Modeling and Simulation ITWG. He was involved in coordination of the activity of STMicroelectronics in the technical management committees of IST European Community programs. He held positions in the management committees of some French national research programs such as ANR–PNANO on nanotechnology, ANR-Blanc on nanoscience, and ANR–CIS on high-performance computing. He is currently holding position on the Editorial Board of IEEE TRANSACTIONS ON ELECTRON DEVICES.