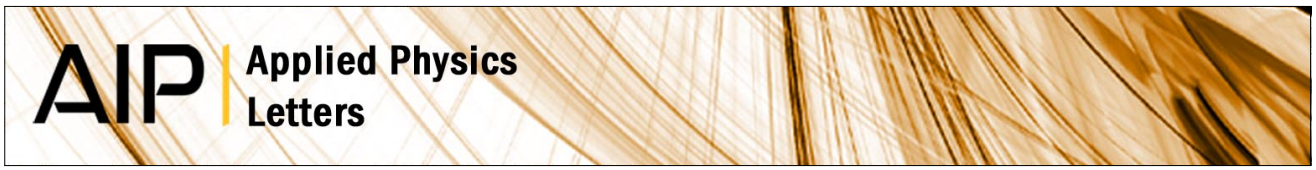

Long-term retention in organic ferroelectric-graphene memories

Santosh Raghavan, Igor Stolichnov, Nava Setter, Jean-Savin Heron, Mahmut Tosun et al.

Citation: Appl. Phys. Lett. **100**, 023507 (2012); doi: 10.1063/1.3676055

View online: http://dx.doi.org/10.1063/1.3676055

View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v100/i2

Published by the American Institute of Physics.

Long-term retention in organic ferroelectric-graphene memories

Santosh Raghavan,[1,a)] Igor Stolichnov,[1] Nava Setter,[1] Jean-Savin Heron,[2] Mahmut Tosun,[2] and Andras Kis[2]
[1]*Ceramics Laboratory, EPFL—Swiss Federal Institute of Technology, Lausanne 1015, Switzerland*
[2]*Laboratory of Nanoscale Electronics and Structures, EPFL—Swiss Federal Institute of Technology, Lausanne 1015, Switzerland*

(Received 19 September 2011; accepted 17 December 2011; published online 11 January 2012)

Long-term stability of high- and low-resistance states in full-organic ferroelectrically gated graphene transistors is an essential prerequisite for memory applications. Here, we demonstrate high retention performance for both memory states with fully saturated time-dependence of the graphene channel resistance. This behavior is in contrast with ferroelectric-polymer-gated silicon field-effect-transistors, where the gap between the two memory states continuously decreases with time. Before reaching saturation, the current decays exponentially as predicted by the retention model based on the charge injection into the interface-adjacent layer. The drain current saturation attests to a high quality of the graphene/ferroelectric interface with low density of charge traps. © *2012 American Institute of Physics*. [doi:10.1063/1.3676055]

The entry of graphene in the field of thin film electronics has substantially changed the game of miniaturization of devices. Its unique properties like its two dimensional monolayer form with ultra-high carrier mobilities[1] have led to the development of several graphene-based device prototypes[2–5] and prompted quest for graphene-based memory devices. Simultaneous development of resistive random access memory (RAM) technology using transition metal oxides,[6] with its simple structure, easy processing, higher density due to smaller size and faster switching capabilities, maybe offer a viable alternative to the existing dynamic-RAMs and flash array memories.[7] The non-destructive read and write process in resistive RAMs also gives it an advantage over conventional ferroelectric-RAMs.[8] Thus arose the possibility of graphene-based memory devices that can function as resistive memories. Integration of graphene with ferroelectrics offers a possible way to overcome graphene's lack of a band-gap and utilize its ambivalent conduction while introducing non-volatile functionality. Organic ferroelectric polymers, with their low processing temperatures and high polarization values allow for such easy integration.[9] Zheng *et al.*[10] were first to fabricate non-volatile ferroelectric graphene devices. They subsequently proposed an effective mechanism of dual gates to control this memory functionality.[11] Similar attempts have been made by depositing graphene using exfoliation[12] and chemical vapour deposition[13] on top of lead zirconium titanate (PZT) thin films for memory applications. For all these device concepts, the non-volatile control of properties of the graphene layer via the ferroelectric gate effect implies a very high stability of spontaneous polarization in the ferroelectric layer. However, the polarization retention behavior in graphene-based devices and stability of the memory states over time in such devices have not yet been addressed in literature.

We report here, a high-retention-performance non-volatile graphene memory device with saturated time dependence of two alternate memory states. The retention characteristics of these devices were studied using time-dependent transport measurements.

The structure of our device has been illustrated in Fig. 1(a). We deposited monolayer flakes of graphene using standard exfoliation technique on 270 nm of SiO_2/doped-Si wafer. Raman spectroscopy was used to confirm that our graphene is monolayer. The electrodes were patterned using electron-beam lithography, followed by the evaporation of Ti/Au (10/50 nm). Transport measurements were done using four-probe technique, where a Keithley system sourcemeter was used as a constant current source to maintain I_{s-d} of 1 μA and a voltmeter was used to measure the change in potential V_{s-d} with time (thus gives the resistance R). Standard methods were used to characterize our graphene-FETs.[14] Our graphene had a Dirac point value of +20 V due to p-doping from the underlying SiO_2 layer, and the mobility of charge carriers in the graphene channel was found to be $\sim$5000 $cm^2\ V^{-1}\ s^{-1}$. Subsequently, a 200 nm thin film of poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] copolymer with molar ratio of 77%/23% was deposited on top of the graphene-FET using spin-coating technique, followed by thermal evaporation of gold as the top-gate. A photolithography step and gold etching step were done to pattern the gold top-gate right on top of the graphene channel. The switching of the ferroelectric on top of the graphene surface was studied using piezo-response scanning probe microscopy. The piezoelectric hysteresis loop obtained for this surface using the technique described elsewhere[15] is shown in the Fig. 1(b). Loop shapes and coercive field values of 500 kV/cm are similar to P(VDF-TrFE) on Au.[16]

Similar to earlier observations,[11] most samples retained their high mobility in the graphene ferroelectric FET after the deposition of ferroelectric. Using the values of mobility and conductivity, we calculate the initial number of charge carriers n in the graphene channel before depositing the polymer. According to the classic model, $\sigma = ne\mu$, where σ is the conductivity, e is the electronic charge, and μ is the mobility of charge carriers. We perform the same calculation after depositing and poling the ferroelectric polymer. The

a)Electronic mail: santosh.raghavan@epfl.ch.

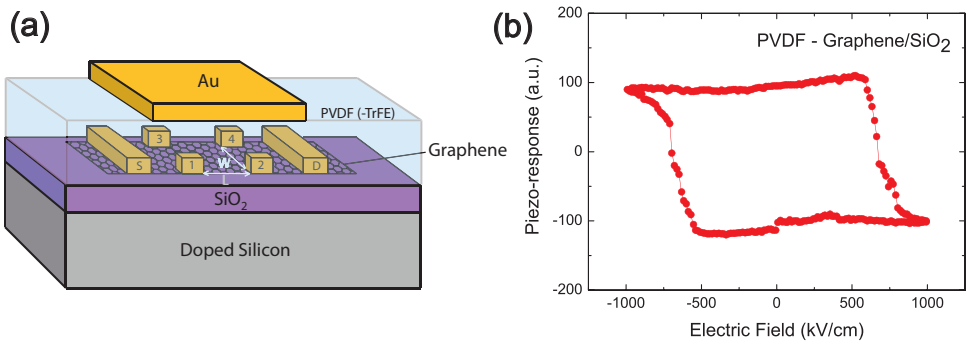

FIG. 1. (Color online) (a) Geometry of the organic ferroelectric-graphene memory device, where W is the width and L is the length of the graphene channel. (b) Piezoelectric hysteresis loop of P(VDF-TrFE) on graphene surface, obtained using piezo-response scanning probe microscopy.

difference in the two values yields the amount of doping in the channel resulting from the ferroelectric. This doping amount is equivalent to 2.4 μC/cm^2, which is around 40% of the maximal value that corresponds to the charge density of P(VDF-TrFE) spontaneous polarization.[17] This degree of field-effect control of the channel is significantly higher than previously obtained 10% for devices with P(VDF-TrFE) on GaMnAs (Ref. 17) and 20% on silicon FETs.[18] Such enhancement of the gate effect suggests a relatively weak compensation of the polarization at the graphene-ferroelectric interface.

Our devices show reproducible and consistent resistance hysteresis behavior as illustrated in the Fig. 2(a), where asymmetry occurs due to some extraneous doping during processing and the continuous presence of background reference doping from the silicon wafer. The peaks of resistance vs. gate voltage observed when the graphene channel reaches the charge neutrality (Dirac point) are associated with the coercive field of the ferroelectric, consistent with previous observations.[10] These peaks occur when the negative charge of the poled gate equals the charge of unintentional p-doping of the channel. Further increase/decrease of the polarization results in a positive/negative carrier concentration increase; therefore, the channel resistance decreases. Within the voltage regions where the spontaneous polarization P does not switch, the resistance shows a relatively weak gradual change, which follows the electric displacement of the gate $D = \epsilon\epsilon_o E + P$, where ϵ, ϵ_o, E are dielectric constant, dielectric permittivity of vacuum, and electric field, respectively. Fig. 2(b) illustrates the time-dependent behavior of the two alternate resistive memory states (retention) at zero gate bias. Throughout the retention measurements, the doped-silicon back-gate is kept grounded. Whilst comparing the two memory states, we see at the initial stage a rapid surge for the high resistance state, which causes its separation from the low resistance state, followed by a gradual increase leading to saturation.

Generally, the retention performance of ferroelectric FETs is determined by the phenomena of charge injection and screening in the interface-adjacent layer.[17,18] These phenomena occur due to the thin dielectric (non-ferroelectric) layer at the ferroelectric interface, which separates the polarization charge in the gate and the channel. When the gate polarization switches, this thin layer is exposed to a very high electric field of the range of MV/cm (Ref. 18) resulting in a significant charge transfer (injection) through the interfacial dielectric layer. The charge injected and subsequently trapped at the interface screens the polarization and, hence, reduces the net polarization that controls the channel resistance. Since there is an inherent p-doping in our graphene channel, there is asymmetric injection of charges due to an increased availability of holes to the interfacial layer. Thus, the screening of charges is more efficient for one poled-state (low-resistance state R_0) compared to the other (high-resistance state R_1). This insufficient screening for the high-resistance state results in a polarization instability and provokes a loss of polarization in the ferroelectric, causing the surge. This can be visualized in the resistance-hysteresis loop as the device moves from the unstable state R_1 to a more stable state at point B, as indicated by the dashed arrow in Figs. 2(a) and 2(b). After 25 h, both resistance states reach saturation and then remain unchanged. We report a factor of difference of 2.5 between the saturated values of high and low resistance states in our devices.

Fig. 3 shows the exponential behavior of the low and high resistance states, respectively. The time-dependence of the graphene channel resistance exhibits three distinct steps occurring consequently after the gate is poled and gate

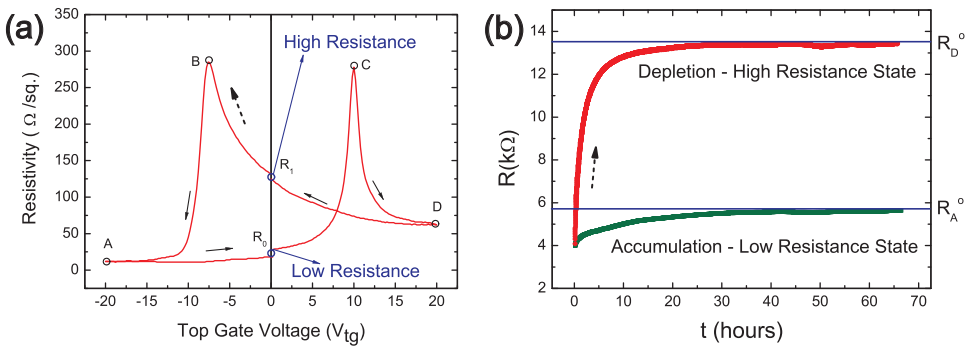

FIG. 2. (Color online) (a) Resistance hysteresis loops for resistivity of the graphene channel vs. top-gate voltage V_{tg}. The two memory states (high and low resistance) at zero-bias are shown, with small black arrows indicating the direction of V_{tg} sweep. (b) Behavior of resistance of the two memory states as a function of time is shown, as achieving saturation.

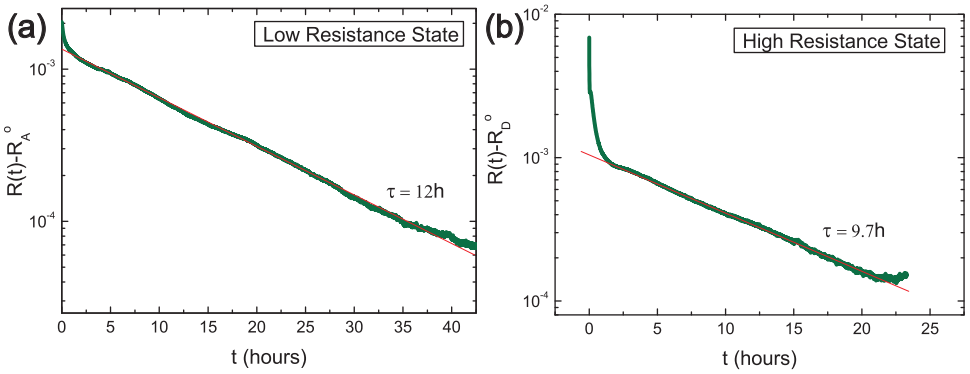

FIG. 3. (Color online) Exponential relation between resistance (in kΩ) and time is observed indicating time-dependent charge injection in (a) low-resistance state and (b) high-resistance state. (τ indicated is the time constant of the exponential behavior.)

voltage reset to zero. The initial quick non-linear drop of resistance is followed by a slow exponential decay, and finally, a steady-state saturation regime observed after 20–25 h for the high resistance state. This time dependence agrees with the model of charge injection into the passive layer earlier evoked for analysis of retention of silicon-based ferroelectric FET.[18] The charge injection into the passive layer originating from the gradual decrease of polarization at the interface-adjacent region of the ferroelectric gate results in a partial screening and reduction of the net polarization influencing the transport in the channel. The initial non-linear injection associated with very strong electric field in the passive layer occurring within the subsecond time range is followed by the linear injection regime as discussed in detail in Ref. 18. In this regime, the injection current J is a linear function of the electric field in the passive layer E_d,

$$J(E_d) = \alpha E_d, \tag{1}$$

which results in an exponential decay of E_d vs. time,

$$E_d = \frac{V_g}{d} = C\exp\left[\frac{-\alpha t}{\epsilon_o \epsilon_d}\right]. \tag{2}$$

The conductivity of graphene shows linear behavior with respect to the back-gate voltage V_g, for V_g values near the Dirac point of graphene.[1] Thus, we obtain a linear relation between log R and t, as shown in Fig. 3. The low resistance state (accumulation mode) shows a gradual increase in resistance over time. The change in resistance follows exponential behavior as shown in Fig. 3(a). The high-resistance state, subsequent to the initial surge, also observes time-dependent charge injection as shown in Fig. 3(b).

In conclusion, we report long-term retention in organic ferroelectric-graphene memory devices, with saturated gap between the low and high resistance memory states. And the time dependence of resistance for both memory states is consistent with the charge injection model.

E.U. is acknowledged for financial support through the project ERC- 268058 MOBILE-W.

[1]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[2]Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris *et al.*, Science **332**(6035), 1294 (2011).
[3]Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, Science **327**(5966), 662 (2010).
[4]X. Wang, L. Zhi, and K. Mullen, Nano Lett. **8**(1), 323 (2008).
[5]K. Y. Shin, J. Y. Hong, and J. Jang, Chem. Commun. (Cambridge) **47**, 8527 (2011).
[6]A. Beck, J. G. Bednorz, C. Gerber, C. Rossel, and D. Widmer. Appl. Phys. Lett. **77**(1), 139 (2000).
[7]K. Prall, in *22nd IEEE Non-Volatile Semiconductor Memory Workshop, 2007* (IEEE, New York, 2007), pp. 510, DOI: 10.1109/NVSMW.2007.4290561.
[8]R. E. Jones, P. D. Maniar, R. Moazzami, P. Zurcher, J. Z. Witowski, Y. T. Lii, P. Chu, and S. J. Gillespie, Thin Solid Films **270**(1–2), 584 (1995).
[9]P. Sharma, T. Reece, D. Wu, V. M. Fridkin, S. Ducharme, and A. Gruverman, J. Phys.:Condens. Matter **21**, 485902 (2009).
[10]Y. Zheng, G. X. Ni, C. T. Toh, M. G. Zeng, S. T. Chen, K. Yao, and B. Özyilmaz, Appl. Phys. Lett. **94**, 163505 (2009).
[11]Y. Zheng, G. X. Ni, C. T. Toh, C. Y. Tan, K. Yao, and B. Özyilmaz. Phys. Rev. Lett. **105**, 166602 (2010).
[12]E. B. Song, B. Lian, S. M. Kim, S. Lee, T. K. Chung, M. Wang, C. Zeng, G. Xu, K. Wong, Y. Zhou *et al.*, Appl. Phys. Lett. **99**, 042109 (2011).
[13]Y. Zheng, G. X. Ni, S. Bae, C. X. Cong, O. Kahya, C. T. Toh, H. R. Kim, D. Im, T. Yu, J. H. Ahn *et al.*, EPL **93**(1), 17002 (2011).
[14]J. L. Xia, F. Chen, P. Wiktor, D. K. Ferry, and N. J. Tao, Nano Lett. **10**, 5060 (2010).
[15]L. Malin, I. Stolichnov, and N. Setter, J. Appl. Phys. **102**, 114101 (2007).
[16]R. Gysel, I. Stolichnov, A. K. Tagantsev, N. Setter, and P. Mokrỳ, J. Appl. Phys. **103**, 084120 (2008).
[17]I. Stolichnov, S. W. E. Riester, E. Mikheev, N. Setter, A. W. Rushforth, K. W. Edmonds, R. P. Campion, C. T. Foxon, B. L. Gallagher, T. Jungwirth *et al.*, Nanotechnology **22**, 254004 (2011).
[18]R. Gysel, I. Stolichnov, A. K. Tagantsev, S. W. E. Riester, N. Setter, G. A. Salvatore, D. Bouvet, and A. M. Ionescu, Appl. Phys. Lett. **94**, 263507 (2009).