Student Paper

Local Stressors to Accommodate 1.2 to 5.6 GPa Uniaxial Tensile Stress in Suspended Gate-All-Around Si Nanowire nMOSFETs by Elastic Local Buckling

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Multi-gate architectures such as gate-all-around (GAA) Si nanowires are the promising candidates for aggressive CMOS downscaling due to the immunity to the issues regarding short channel effect, improved subthreshold slope and optimized power consumption. On the other hand, Si nanowires represent excellent mechanical properties e.g. yield strength of 10±2% [1] in comparison to 3.7% for bulk Si [2], a strong motivation to be used as interesting exclusive platforms for innovative nanoelectronic applications e.g. novel strain engineering techniques for carrier transport enhancement in multi-gate 3D suspended channels [3]-[5] or local band-gap modulation using >4 GPa uniaxial tensile stress in suspended Si channels to enhance band-to-band tunneling current in multi-gate Tunnel-FETs [6], all without plastic deformation and therefore, no carrier mobility degradation in deeply scaled channels.

In this paper, we demonstrate the integration of local oxidation [3] and metal-gate strain [4] technologies to induce 3.3%/5.6 GPa uniaxial tensile strain/stress in 2 µm long suspended Si nanowire MOSFETs, *the highest process-based stress record in MOSFETs until now*, by elastic local buckling. Fig. 1 represents the fabrication process to make GAA uniaxially tensile strained Si nanowire MOSFETs from a 100 mm (100) Unibond SOI substrate with 1×10^{18} cm^{-3} phosphorous channel doping. Highly doped accumulation-mode was chosen as the operation regime to mainly simplify the process in nanoscale [7]. Dry oxidation of the Si nanowires with a tensile Si_3N_4 hard mask on top at 925 °C helps to accumulate mechanical potential energy in the nanowires due to in-plane/out-of-plane elongation/bending restrictions during the oxidation process [3]. This stored mechanical potential energy will be released in the form of mechanical buckling after stripping the hard mask, the grown oxide and the nanowire detachment from the BOX layer. The high-k/metal-gate stack step includes 5 nm ALD HfO_2, RTA (600 °C, 15 min) and finally, 50 nm TiN by sputtering at 25 °C including -2.0 GPa biaxial compressive intrinsic thin film stress. The thin film stress in the metal-gate layer can be engineered by sputtering power, thickness and deposition temperature [4]. The metal-gate thin film with an intrinsic compressive stress tends to stretch, causing further elongation/buckling of the suspended Si nanowires. Gate pattern, S/D implantation, metallization and sintering are the further process steps.

Employing micro-Raman spectroscopy to measure stress in GAA deeply scaled SOI Si NWs with a high-k/metal-gate stack is pretty challenging due to the non-transparency of the metal-gate and on the other hand, low level of Raman signal from deeply scaled NWs in comparison to the strong background Raman signal from the Si carrier wafer. Therefore, top and tilted-view SEM micrographs were used to estimate the stress level in the NWs, instead of micro-Raman spectroscopy. Fig. 1 represents the top-view SEM micrograph of a buckled array of 2 µm long Si NWs with the represented TEM cross-section. The actual maximum NW deflection is calculated based on the observed maximum in-plane and out-of-plane deflections. Afterward, by considering a symmetric Gaussian buckling profile along the NWs (η=1 µm, σ=0.5 µm, see Fig. 2) and assuming a uniform strain profile along the NWs, the expected elongation is calculated from the arc-length of the buckled NWs and afterward, the stress values vs. NW widths are reported in Fig. 3 (assuming Si Young's modulus of 169 GPa). It is worth mentioning that the local stress can be even higher in the case of a non-uniform stress profile along the NWs [3], can be detected only by micro-Raman spectroscopy. As Fig. 3 represents, the narrower NWs have a higher buckling, mainly due to a smaller critical-load-for-buckling value. Therefore, the NW width modulation, from 44 to 4 nm, leads to a significant uniaxial tensile stress modulation in NWs, from 1.2 to 5.6 GPa, respectively, on a single wafer, providing room for further potential applications while impossible by global stressors e.g. [5].

Electrical characterization was done using a Cascade prober and a HP 4155B Semiconductor Parameter Analyser at room temperature. Fig. 4 represents transfer and transconductance characteristics of a GAA MOSFET with the TEM cross-section in Fig. 1, including 10 triangular <110> Si NWs with W_{top}~4 nm, under 5.6 GPa uniaxial tensile stress at different V_{DS}. The threshold voltage and low-field electron mobility in the accumulation-regime were extracted using transconductance change [8] and

$I_D/g_m^{0.5}$ [9] methods, respectively, yielding low-field electron mobility of 332 $cm^2/V{\cdot}s$ at V_{DS}=100 mV. This corresponds to 32% electron mobility enhancement in comparison to non-strained bulk Si at the same doping level [10], due to the uniaxial tensile stress in the channel. The electron mobility enhancement can be even higher up to ~100% at >~2 GPa uniaxial tensile stress [11] using excellent channel-dielectric interface. I_{on}/I_{off} ratio is also ~10^5 at V_{DS}=1.500 V.

In conclusion, *the highest process-based stress record in MOSFETs* is represented by elastic local buckling using top-down Si NWs. Significant stress level modulation in the channel from 1.2 to 5.6 GPa on a single wafer is demonstrated for the first time by varying the NW width. The GAA Si NW MOSFET with 5.6 GPa uniaxial tensile stress is characterized and the electron mobility enhancement is reported.

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References

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- (100) Unibond SOI
- SOI doping (P:1e18 cm^{-3})
- SiO_2/Si_3N_4 hard mask dep.
- HSQ-NW pattern by EBL
- Dry hard mask and Si etch
- Dry oxidation, 925°C, 7 h
- Suspend naked Si NWs by wet Si_3N_4 and SiO_2 etch
- HfO_2/TiN gate stack dep.
- Gate pattern
- S/D doping (P: 2e20 cm^{-3})
- Metallization (AlSi-1%)
- Sintering

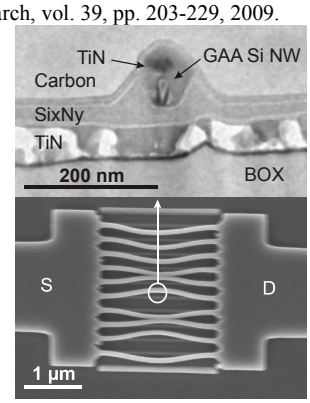

Fig. 1: Process flow (left), a dense array of elastically buckled GAA Si NWs with 5.6 GPa uniaxial tensile stress in the channel and a triangular cross-section (W_{top}~4 nm) (right).

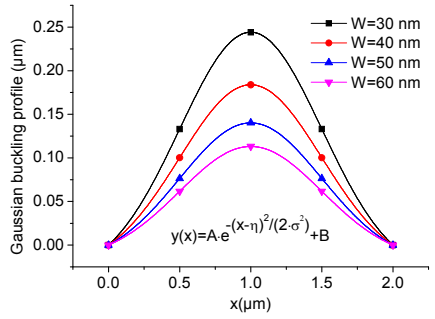

Fig. 2: Symmetric Gaussian buckling profiles along 2 µm long GAA Si nanowires with different initial mask nanowire widths.

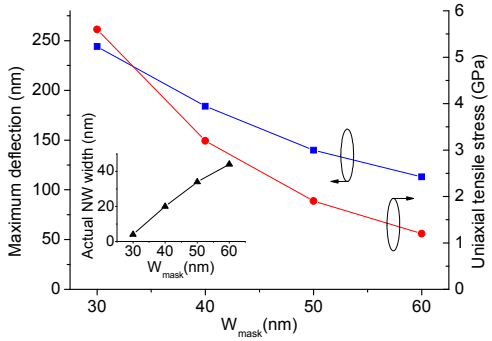

Fig. 3: Maximum deflection and uniaxial tensile stress level in the buckled Si NW vs. NW width on the mask. The inset shows actual NW width vs. mask NW width.

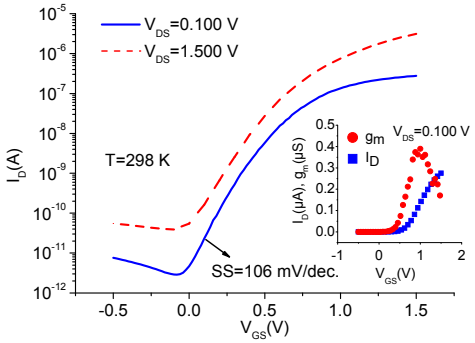

Fig. 4: Transfer and transconductance characteristics of a GAA nMOSFET with 5.6 GPa uniaxial tensile stress in the NWs (V_{TH}=0.70 V at V_{DS}=100 mV).