Uniaxially Tensile Strained Accumulation-Mode Gate-All-Around Si Nanowire nMOSFETs

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In this work we report an experimental study on accumulation-mode (AM) gate-all-around (GAA) nMOSFETs based on silicon nanowires with uniaxial tensile strain. Their electrical characteristics are studied from room temperature up to ~400 K and carrier mobility, flat-band and threshold voltages are extracted and investigated.

Recently, highly single-type doped devices such as accumulation-mode (AM) and junctionless (JL) FETs have been proposed as straightforward switch architectures able to eliminate some of the limitations of nano-scale FETs such as the ultra-abrupt junctions and related processing challenges, allowing to fabricate even shorter channel devices [1-3]. Achieving a high I_{on} in a heavily doped channel is an engineering challenge since the carrier mobility in heavily doped devices is limited by ionized impurity scattering. In this paper we evaluate the impact of a local uniaxial tensile strain engineering method by local bending of nanowires to improve the mobility in highly doped AMOSFETs, without affecting their I_{on}/I_{off}.

Figure 1 represents the process flow to make dense array (~8 NW/µm) of deeply scaled sub-50 nm wide/thick Si nanowires on a Silicon-On-Insulator substrate. A sacrificial oxidation was formed in the presence of silicon nitride hard mask to shrink further the width of the Si nanowires, round the possible sharp corners as well as accumulate uniaxial tensile stress in the channel after stripping the hard mask and suspending the channel [4]. The gate stack includes 5 nm HfO_2 ALD deposition, RTA and afterward, 20 nm TiN deposition by sputtering to accumulate further uniaxial tensile stress in the suspended nanowires [5], causes local buckling of the suspended nanowires and induces clearly >1.5 GPa uniaxial tensile stress in the channel, measured from the arc length of the buckled NWs.

The electrical characterization was carried out at different temperatures using a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer. Figure 2 depicts the I_D-V_G and I_D-V_D characteristics of a 2 µm long channel AMOSFET, including an array of 10 parallel Si nanowires, at 298 K. According to [6] and as described in Figure 3, the flat-band condition in an AMOSFET is pretty close to the threshold voltage and the accumulation layer will be created after reaching the flat-band condition while a heavily doped JL MOSFET, due to having the main current at the middle of the channel above threshold voltage, is mainly operating below the flat-band voltage and the flat-band condition will be reached while reaching the density of carriers on the surface to the doping concentration. Note that in the subthreshold region ($V_G<V_{TH}$) the conduction in both AMOSFET and JLFET is in the bulk of the NW.

The threshold voltage, V_{TH}, of the AMOSFET was extracted using the transconductance change (TC) method [7] which is quasi-independent of device series resistance and does not require the use of any accurate analytical model. Interestingly, as shown in Figure 4, the TC peak is appearing almost at the expected (theoretical) threshold voltage from the linear region of the I_D-V_G curve. By considering the current in the accumulation channel as the main dominant current in the GAA nanowire and using an earlier developed analytical model in [8], the flat-band voltage was extracted using the $I_D/gm^{0.5}$ method [9] independent of series resistances and mobility attenuation factor and the results were plotted in Figure 4, providing systematically higher value than V_{TH} [6].

The transfer characteristics of the AMOSFET at 298-398 K are reported in Figure 5. The low field electron mobility at different temperatures was extracted using the slope of the $I_D/gm^{0.5}$ vs. V_{GS} in the linear region (V_{DS}=100 mV), minimizing the influence of series resistances and mobility attenuation factor and plotted in Figure 6. As Figure 6 shows, the electron mobility in highly doped AMOSFET is reducing as $T^{-0.97}$ which is lower than for intrinsic or low n-doped Si and in agreement with prior reports [10], being explained by the dominant role of ionized impurity scattering in highly doped Si MOSFETs. Similar lower dependence on temperature is expected in JL FETs.

We report a threshold voltage reduction coefficient with temperature of -0.92 mV/K, a flat-band voltage coefficient with temperature of -1.73 mV/K and, finally, a subthreshold slope degradation of -0.43 %/K or -0.456 mV/dec.K (with a 106 mV/dec. subthreshold slope at 298 K), as reported in Figure 7.

As a conclusion, we have demonstrated the first AM gate-all-around nMOSFETs on SOI substrates with electron mobility enhanced by process-induced uniaxial tensile strain and reported their performance from 298 K to 398 K.

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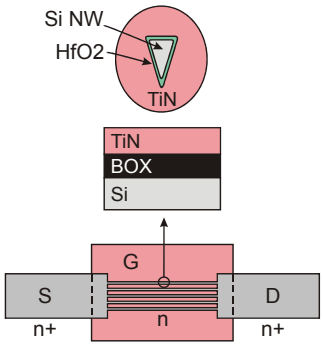
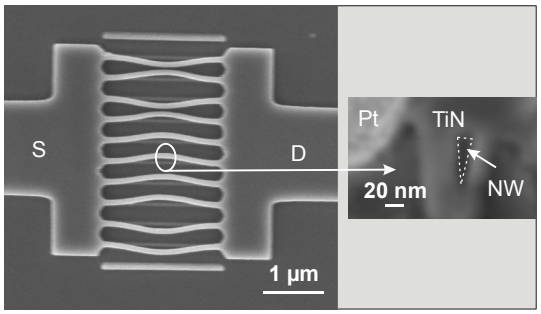
[1] J.-P. Colinge et al., *Nature Nano.* (2010). [2] J.-P. Colinge et al., *Jpn. J. Appl. Phys.*, vol. 48, (2009). [3] J. Wu et al., *ECS Transactions*, vol. 33 (2010). [4] M. Najmzadeh et al., *Microelec. Eng.* (2009). [5] N. Singh et al., *IEEE EDL* (2007). [6] A. Nazarov et al., *Springer,* 1st ed. (2011). [7] H.-S. Wong et al., *SSE* (1987). [8] J.-P. Colinge et al., *IEEE TED*, vol. 37, (1990). [9] G. Ghibaudo, *Electronics Letters* (1988). [10] S. Reggiani et al, *IEEE TED*, Vol. 49, 2002.

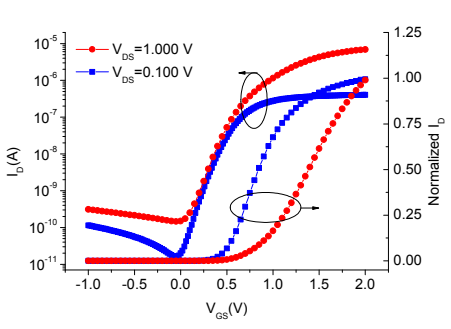
- (100) Unibond 4” SOI, ~intrinsic p-type
- Channel ion imp/ann. (Phosph., 1e18 cm^{-3})
- LPCVD silicon nitride hard mask dep.
- Active layer pattern by e-beam lithography
- Sacrificial dry oxidation + strip hard mask
- BOX etching to suspend the Si nanowires
- High-k/metal gate stack deposition
- Gate pattern – optical lithography and etch
- S/D imp./anneal (Phosph., ~2e20 cm^{-3})
- Metallization (AlSi-1%)

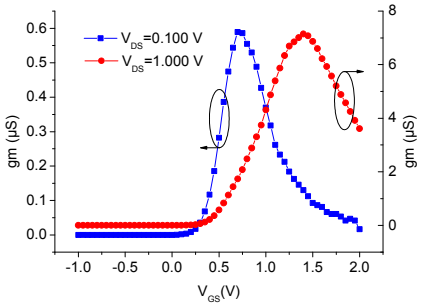


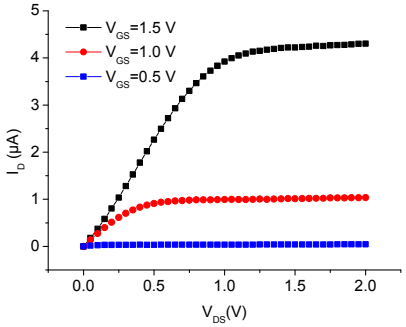


(a) (b) (c)

Fig. 1. Process flow to make GAA Si nanowire AMOSFET using a top-down Si NW platform (a), the schematic of the GAA Si NW AMOSFET (b), the SEM picture of an array of strained Si NWs after the gate stack step and the cross-section of a suspended GAA NW AMOSFET (right).







(a) (b) (c)

Fig. 2. Transfer and transconductance characteristics of a GAA *strained* AMOSFET at 298 K.

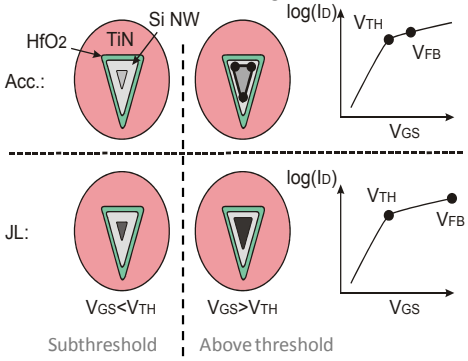


Fig. 3. Depiction of conduction path in GAA accumulation and junctionless MOSFETs vs. V_{GS}.

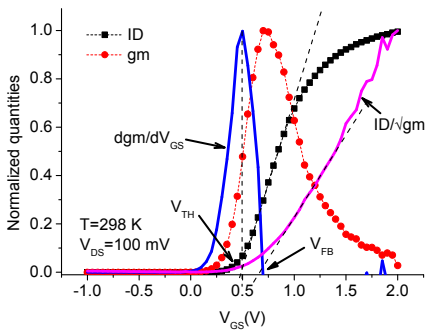


Fig. 4. Extraction of V_{TH} and V_{FB} of a GAA AMOSFET using TC and ID/$gm^{0.5}$ methods.

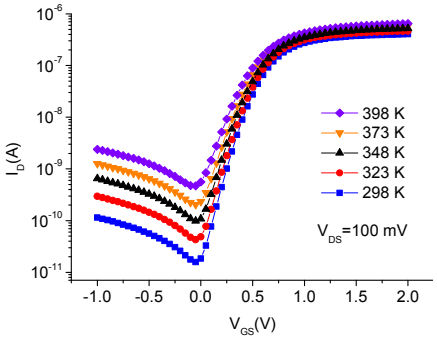


Fig. 5. Transfer charac. of a GAA *strained* AMOSFET at different temperatures.

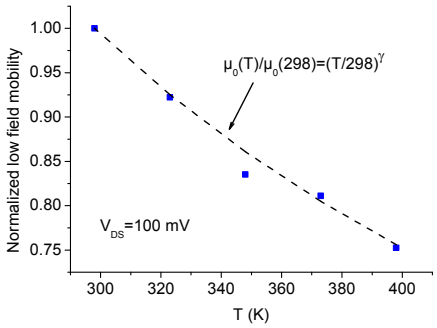


Fig. 6. Normalized low field electron mobility dependence on temperature for a GAA *strained* AMOSFET. The extracted γ is -0.966.

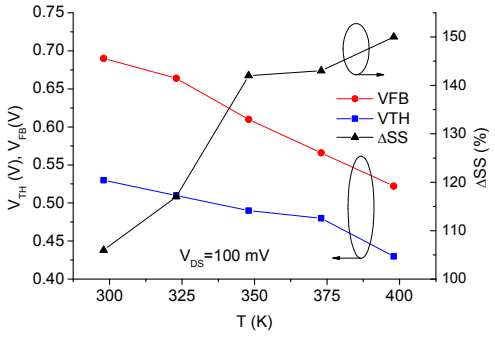


Fig. 7. Variation of extracted threshold voltage, flat-band voltage and subthreshold slope of a GAA *strained* AMOSFET with temperature.