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Research Letters

Resistive Programmable Through-Silicon Vias for Reconfigurable 3-D Fabrics

Davide Sacchetto, Michael Zervas, Yuksel Temiz, Giovanni De Micheli, and Yusuf Leblebici

***Abstract*—In this letter, we report on the fabrication and characterization of titanium dioxide (TiO_2)-based resistive RAM (ReRAM) cointegration with 380 μm-height Cu through-silicon via (TSV) arrays for programmable 3-D interconnects. Nonvolatile resistive switching of $Pt/TiO_2/Pt$ thin films is first characterized with a resistance ratio up to five orders of magnitude. Then, cointegration of $Pt/TiO_2/Pt$ or Pt/TiO_2 memory cells on 140 and 60 μm diameter Cu TSVs is fabricated. Repeatable nonvolatile bipolar switching of the ReRAM cells is demonstrated for different structures.**

***Index Terms*—Memristive systems, memristor, resistive RAM (ReRAM), titanium dioxide (TiO_2), through-silicon via (TSV), 3-D integration.**

I. Introduction

THE KEY reason of the historical CMOS success lies with the exponential increase of device density that the silicon industry kept true for more than 40 years while reducing the unit cost of ICs. Recently, the pace of scaling has slowed down due to approaching fundamental limits at the device level. On one hand, researchers are striving to obtain more performant circuits by focusing on improvement of the Front-End-of-the-Line technology, for instance, innovating materials, device structures, and introducing novel state variables [1] for computation. On the other hand, the Back-End-of-the-Line technology is also addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in 3-D wafer/chip stacking solutions utilizing through-silicon vias (TSVs) [1], as well as in reconfigurable interconnect fabrics.

Considering new device technologies, the recent realization of Stanley Williams' memristor [2] [also classified as resistive RAM (ReRAM)] based on metal–insulator–metal structures, gave new push to solid-state research for logic and memory applications that can be implemented into the Back-End-of-the-Line technology. For instance, ultradense crossbar memristive memory arrays can be made thanks to the compactness of the two-terminal junction [3]. The physical realization of the memristor, whose behavior was postulated by Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6].

In this letter, the authors demonstrate the cointegration of TSVs with ReRAM stacks, offering a new path for reprogrammable 3-D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3-D chip interconnects.

II. Fabrication

A. Planar ReRAM Devices

First, high resistivity p-type ($N_A \approx 10^{15}$ atoms/cm^2) bulk-Si wafers are prepared by 500 nm thermal oxidation in H_2O atmosphere. Then, the deposition of the resistive switching materials is performed by sputtering of $Pt/TiO_2/Pt$ layers with 270/80/270 nm thicknesses, respectively. A conceptual picture is shown in Fig. 1(a). The top electrode area of 100 μm $\times$ 100 μm were patterned by standard lithography and etched by the ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

B. TSV Devices

The resistive switching materials were integrated with TSVs producing two different devices.

1) 140 μm TSV diameter in 380-μm thick wafer, using the $Pt/TiO_2/Pt$ memory stack.
2) 60 μm TSV diameter in 380-μm thick wafer, using the $Cu/TiO_2/Pt$ memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

The TSVs are fabricated using the same process in both the cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through-wafer etch, RCA wafer cleaning, and thermal oxidation in water atmosphere to grow a 3-μm thick oxide. A 750-nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step, the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

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D. Sacchetto, M. Zervas, Y. Temiz, and Y. Leblebici are with the Laboratory of MicroElectronic Systems, Ecole Polytechnique Federale de Lausanne, Vaud 1015, Switzerland (e-mail: davide.sacchetto@epfl.ch; michael.zervas@epfl.ch; yuksel.temiz@epfl.ch; yusuf.leblebici@epfl.ch).

G. D. Micheli is with the Laboratory of Systems Integration, Ecole Polytechnique Federale de Lausanne, Vaud 1015, Switzerland (e-mail: giovanni.demicheli@epfl.ch).

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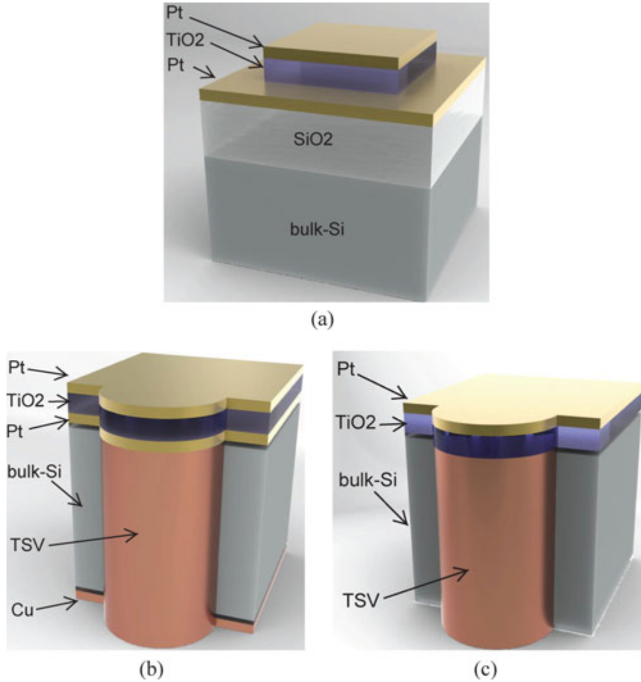

Fig. 1. (a) Concept image of planar ReRAM made of the $Pt/TiO_2/Pt$ stack. (b) Concept image of the ReRAM–TSV using the $Pt/TiO_2/Pt$ programmable fuse. (c) Concept image of the ReRAM–TSV using the $Cu/TiO_2/Pt$ programmable fuse.

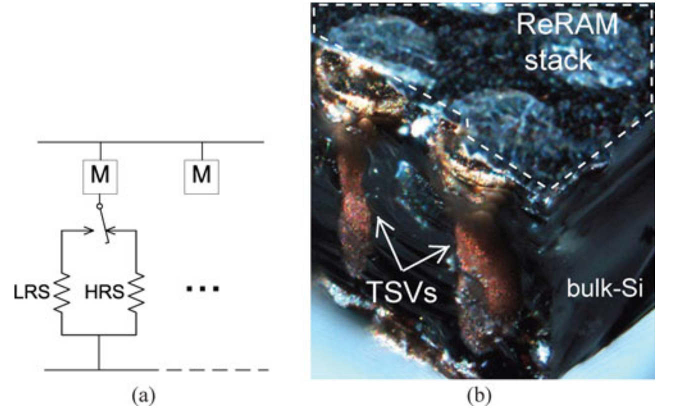

Fig. 2. (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element *M*). (b) Reconstructed 3-D photograph of the $TSV–Cu/TiO_2/Pt$ device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

1) TSV With $Pt/TiO_2/Pt$ *ReRAM:* For the first type of devices, once the TSVs are fabricated, the front side of the wafer is processed with the chemical mechanical polishing (CMP) technique to form a flat surface. The $Pt/TiO_2/Pt$ stack is sputtered with layer thicknesses $270/80/270$ nm, accordingly. A concept picture of the fabricated structure can be seen in Fig. 1(b).

2) TSV With $Cu/TiO_2/Pt$ *ReRAM:* For the second type of devices, the wafer is polished using the CMP technique on both sides to remove the seed layer and to planarize the surfaces. Cu was, then, cleaned using an $NH_4 : H_2SO_4$ etching solution at room temperature for 10 min. Then, the wafer was loaded into a vacuumed sputtering chamber and a TiO_2/Pt layer was deposited with thicknesses of 80 and 270 nm, respectively. Cu of the TSV is acting as the bottom electrode of the ReRAM [see Fig. 1(c)]. Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Fig. 2(a) and (b), respectively.

III. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station under dark conditions. For electrical contacts, standard tungsten needles with $15\ \mu m$ apex diameter were placed on the top electrode area very softly, since the dependence of the switching on needle pressure has been observed, similarly to the observation of local pressure-modulated conductance with atomic force microscopy tips [7]. Then, double *I–V* dc sweeps have been used to investigate the resistive switching behavior. In all the cases, the bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table I.

A. Planar ReRAM Devices

First, the planar $Pt/TiO_2/Pt$ devices are characterized and it showed stable and repeatable bipolar switching behavior between $10\ \Omega$ and $1\ M\Omega$ read or measured at $+1$ V (see Fig. 3). Originally, the devices are in the high-resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low-resistance state (LRS) occurs at $+1.8$ V. After the SET event, the voltage sweep continues until $+2$ V and, then, move back toward the negative-voltage region. When -1.3 V is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about five orders of magnitude is read at $+0.5$ V.

B. $TSV–Pt/TiO_2/Pt$ Devices

Next, $TSV–Pt/TiO_2/Pt$ devices with the same layer thicknesses are measured, showing resistance switching below ±1 V (see Fig. 4). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks, as well as to surface states acting as dopants for the TiO_2 [8]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only $+0.6$ V, while the RESET voltage is measured at -0.5 V. Using a reading voltage of $+0.2$ V, an HRS of $2\ M\Omega$ and LRS of $666\ \Omega$, with the resistance ratio of 3000 are measured.

C. $TSV–Cu/TiO_2/Pt$ Devices

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the

TABLE I
OBTAINED ReRAM ELECTRICAL PARAMETERS FOR DIFFERENT DEVICES

Device	SET	RESET	HRS	LRS	HRS/LRS	Reading
Planar $\mathrm{Pt/TiO_2/Pt}$	$+1.8$ V	-1.3 V	10 MΩ	10 Ω	10^5	$+1$ V
$\mathrm{TSV-Pt/TiO_2/Pt}$	$+0.6$ V	-0.5 V	2 MΩ	666 Ω	3003	$+0.2$ V
$\mathrm{TSV-Cu/TiO_2/Pt}$	-4.2 V	$+5$ V	500 MΩ	5 Ω	10^5	$+1$ V

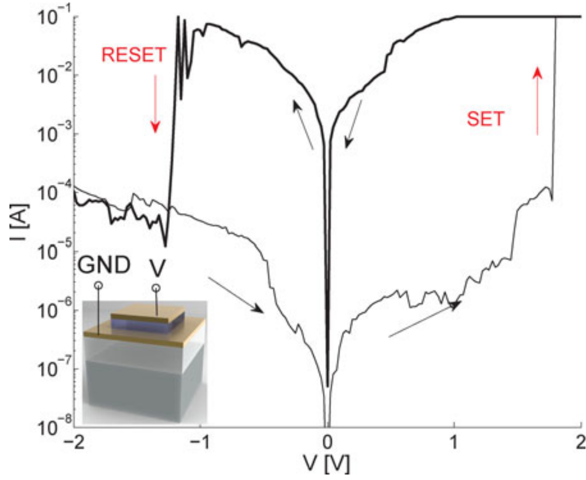

Fig. 3. Resistive switching through *I–V* sweeps for planar $\mathrm{Pt/TiO_2/Pt}$ devices.

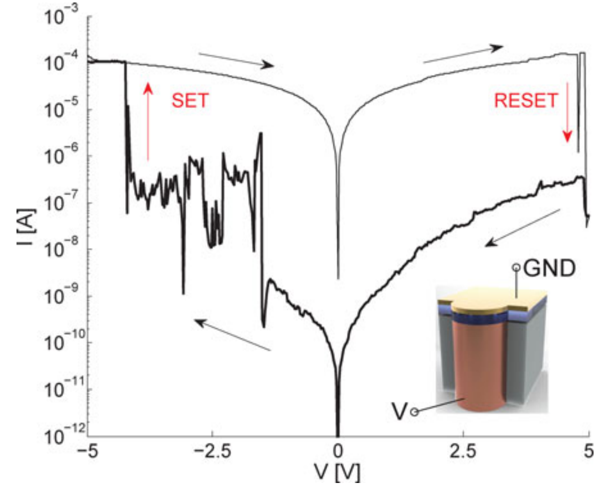

Fig. 5. Resistive switching through *I–V* sweeps using the $\mathrm{TSV–Cu/TiO_2/Pt}$ programmable fuse.

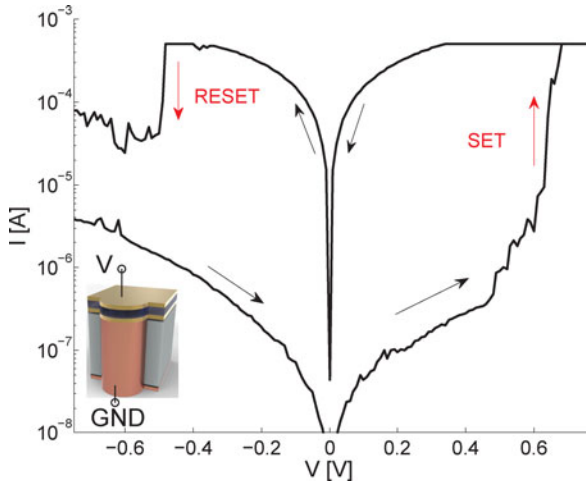

Fig. 4. Resistive switching through *I–V* sweeps using the $\mathrm{TSV–Pt/TiO_2/Pt}$ programmable fuse.

$\mathrm{TiO_2}$ layer [9], [10], which is an n-type semiconductor, an alternative device is obtained by depositing $\mathrm{TiO_2}$ and Pt directly on top of the $\mathrm{Cu–TSV}$. Thus, thanks to a larger Schottky barrier height at the $\mathrm{Cu–TiO_2}$ interface, a larger programming window is obtained (see Fig. 5). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. An HRS of $500\,\mathrm{M\Omega}$ and LRS of $5\,\mathrm{k\Omega}$ are read at $+1\,\mathrm{V}$.

IV. CONCLUSION

In this study, $\mathrm{Pt/TiO_2/Pt}$ obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with the LRS to HRS resistance ratio up to five orders of magnitude. The device is successfully integrated on top of 140 and 60 $\mu\mathrm{m}$ TSV arrays either in the full $\mathrm{Pt/TiO_2/Pt}$ stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The cointegration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3-D chip interconnects.

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