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Monolithic Integration of Silicon Nanowires With a Microgripper

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***Abstract*—Si nanowire (NW) stacks are fabricated by utilizing the scalloping effect of inductively coupled plasma deep reactive ion etching. When two etch windows are brought close enough, scallops from both sides will ideally meet along the dividing centerline of the windows turning the separating material column into an array of vertically stacked strings. Upon further thinning of these NW precursors by oxidation followed by oxide etching, Si NWs with diameters ranging from 50 nm to above 100 nm are obtained. The pattern of NWs is determined solely by photolithography. Various geometries ranging from T-junctions to circular coils are demonstrated in addition to straight NWs along specific crystallographic orientations. The number of NWs in a stack is determined by the number of etch cycles utilized. Due to the precise lithographic definition of NW location and orientation, the technique provides a convenient batch-compatible tool for the integration of NWs with MEMS. This aspect is demonstrated with a microgripper, where an electrostatic actuation mechanism is simultaneously fabricated with the accompanying NW end-effectors. Mechanical integrity of the NW–MEMS bond and the manipulation capability of the gripper are demonstrated. Overall, the proposed technique exhibits a batch-compatible approach to the issue of micronanointegration. [2009-0084]**

***Index Terms*—Manipulators, microactuators, nanotechnology, silicon-on-insulator technology.**

I. Introduction

CONVENTIONAL photolithography is an intrinsic part of batch fabrication. It provides a rapid and low-cost fabrication process when compared to other high-resolution top-down techniques such as charged-particle-beam lithographies. These techniques, including e-beam lithography, are commonly used to pattern nanostructures with high precision regarding their location and orientation. However, their use remained confined to pilot production due to the associated cost and lengthy exposure times. Although exposure tools with multiple e-beam columns or hybrid tools utilizing both e-beam lithography and photolithography are geared towards resolving issues of cost and throughput, such technologies are at their infant stages [1]. On the other extreme, self-assembly techniques can provide a good level of control on structural and dimensional aspects [2]. However, the precision for alignment and registration provided by photolithography is unmatched by that of self-assembly-based bottom-up approach, where reducing randomness requires prepatterning and guiding of the self-assembly phenomenon, thereby raising the necessity for top-down intervention [3].

In spite of its advantages, the capabilities of photolithography are often challenged by the quest for miniaturization into the nanoscale. Although, currently, the use of 193-nm-wavelength deep-ultraviolet (UV) immersion lithography with its first industrial sale in 2005 can provide a resolution of 40 nm [4], such enhancement in resolution is accompanied by exposure tool prices in excess of $12 M [5]. Increased costs drew attention to alternatives such as nanoimprint lithography with its promising aspects regarding high resolution and throughput at a low cost. The technique is mentioned among "postoptical" alternatives in the 2007 edition of the International Technology Roadmap for Semiconductors [6] with issues such as defect density, template production, and template lifetime remaining to be addressed. Regarding its suitability for systems integration, nanoimprint lithography was shown to have a 500-nm overlay accuracy over an entire 4-in wafer in a case study on a four-mask MOSFET process [7]. Although promising, such alternatives will require much more investment to be fully developed for mainstream use.

The issue addressed in this paper is about combining batch compatibility and monolithic integration of micro- and nanoscales within the boundaries of photolithography. In many instances, the answer lies in creating a nanoscale "mold" or a template through conventional photolithography with a resolution of 1 μm. The template can then be utilized as a growth platform for nanostructures. Anisotropic etching of single-crystalline substrates provides an ideal venue for such template formation. Among examples reported in the literature, one can mention the growth of carbon nanotubes on top of Si pyramids [8] and filling of KOH-etched grooves with Sb [9]. Filling of nanocracks in multilayers also provides a similar mold effect, where the patterning of the crack network occurs through stress-guided assembly [10]–[12]. Furthermore, timed etch of single crystals [13], pattern-dependent oxidation [14],

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and “size-reduction lithography” [15] all represent efforts to realize batch compatibility at the nanoscale.

This paper is based on a similar approach using conventional photolithography, where advantage is taken of the scalloping effect during inductively coupled plasma deep reactive ion etching (ICP-DRIE). The employed technique was originally introduced in 2001 with the objective of fabricating lateral field emission devices [16]. When two parallel rectangles are defined with a separation on the order of 1 μm and etched by ICP-DRIE, they will turn into deep trenches. If the amount of scalloping, a side effect of chemical etch, is adjusted correctly, the scallops from both sides will meet along the dividing centerline leading to the formation of an array of nanowire (NW) precursors. Further reduction of diameter can be achieved through subsequent oxidation followed by sacrificial etching of oxide.

In the original work [16] demonstrating NW formation due to the scalloping effect of ICP-DRIE the technique was utilized to define sharp tips for field emission. In a quest of increasing the emitted current, emphasis was placed on increasing the line density of tips and tip sharpness. The line density of tips was reported to change with etch depth. For NW growth, sharp corners were used in the layout, where scallops from sidewalls met at the tip of the corner forming a nanoscale protrusion. They were placed either along the edge of the cathode leading to the formation of emission tips or the cathode and the anode were bridged by NWs when sharp corners were placed at opposing spots on both electrodes. The span, i.e., NW length, was kept on the order of 1 μm. The maximum length attained was 6 μm for a microgrid for modulating the emission current.

This paper further elevates our understanding of this process due to the following reasons.

1) A limit to the etch depth is established beyond which all scallops vanish. This is important from a MEMS-based perspective. As the device layer thickness on an SOI wafer is determined by the electromechanical design, the survival of NWs during a thru-etch until buried oxide (BOX) layer is now established as an additional design criterion.
2) Process parameters are well laid out, including:
   a) the amount of oxidation to separate the Si column into NW precursors as a function of the duration of SF_6 etch step;
   b) the linewidth necessary for the merging of opposing scallops.

   Sharp corners were shown not to be necessary for NW definition. Furthermore, in order to prevent NWs from breaking, the harsh environment of wet etching is omitted. For this purpose, HF vapor is introduced for the sacrificial oxide etch while thinning of NWs.
3) A new approach is developed where narrow trenches are defined as contour lines around a device rather than etching away all unwanted Si. Increasing the planarity of the processed surface, this is shown to ensure the applicability of further lithography steps after the formation of NWs.
4) NW aspect ratios around 400 are obtained (a NW length of 20 μm for a diameter of 50 nm), which is much higher than NW spans reported before.
5) Patterns other than straight NWs are shown to be feasible. These include various junctions and coillike circular shapes.
6) Since previous applications were predominantly electrical, the strength of NW-bulk Si attachment was of no concern. In this paper, the process is also evaluated from a mechanical-integrity point of view.

The discussion on the details of NW fabrication will be followed by a case study of the integration of such NWs with a microsystem in the form of an electrostatically actuated gripper. Gripper is chosen as an integration challenge, where NWs are to be positioned right at the tips of multiple end-effectors. Any misplacement of NWs would render electrostatic actuation useless. The shape and orientation of NWs are also important as they would facilitate the gripping action. Hence, such grippers constitute a field, which traditionally emphasizes serial and high-resolution growth techniques such as electron-beam-induced deposition. In contrast, this problem is addressed within the boundaries of photolithography in this paper. An assessment of the proposed technique’s applicability to batch-compatible micronanointegration is provided in the end.

II. NW Fabrication

A. Approach to Batch Compatibility

Batch compatibility in this paper is achieved through the lithographic definition of the location and orientation of Si NWs. In this technique, one starts with conventional lithography, as shown in Fig. 1(a), where two parallel windows are patterned with a gap of length on the order of 1 μm. This gap forms the NW region. Patterning is followed by the cyclic etching and deposition steps of the Bosch process [17], as shown in Fig. 1(b)–(f). Since the masked linewidth between the two trenches is narrow enough, parts of the Si column separating both trenches are almost completely consumed in regions where scallops from both sides meet. These gaps divide the middle Si column into separate strings running parallel to the mask orientation. Si strings then serve as precursors of NWs through further thinning and smoothening by thermal oxidation followed by oxide etching [Fig. 1(g) and (h)].

The process yields a vertical stack of NWs. Their number is equal to the number of etch cycles utilized during ICP-DRIE. Furthermore, the pattern of the original mask defining the NW region is adopted by the resulting NW stack. In the following, details of the fabrication process will be provided along with various examples of NW stacks.

B. Fabrication Process

The layout for the NW fabrication consists of two layers, which are shown in Fig. 2 in the case of a T-junction. The first layer shown as lines in Fig. 2(a) defines contour lines forming a continuous trench around the anchors and the NW region. Anything outside the circumscribed region will be removed by isotropic Si etch following the formation of NWs. The second layer shown as block masks in Fig. 2(a) provides protection for NWs during this etch process. In the contour layer, the widths of the trench and the NW region are designed to be 1 and 2 μm,

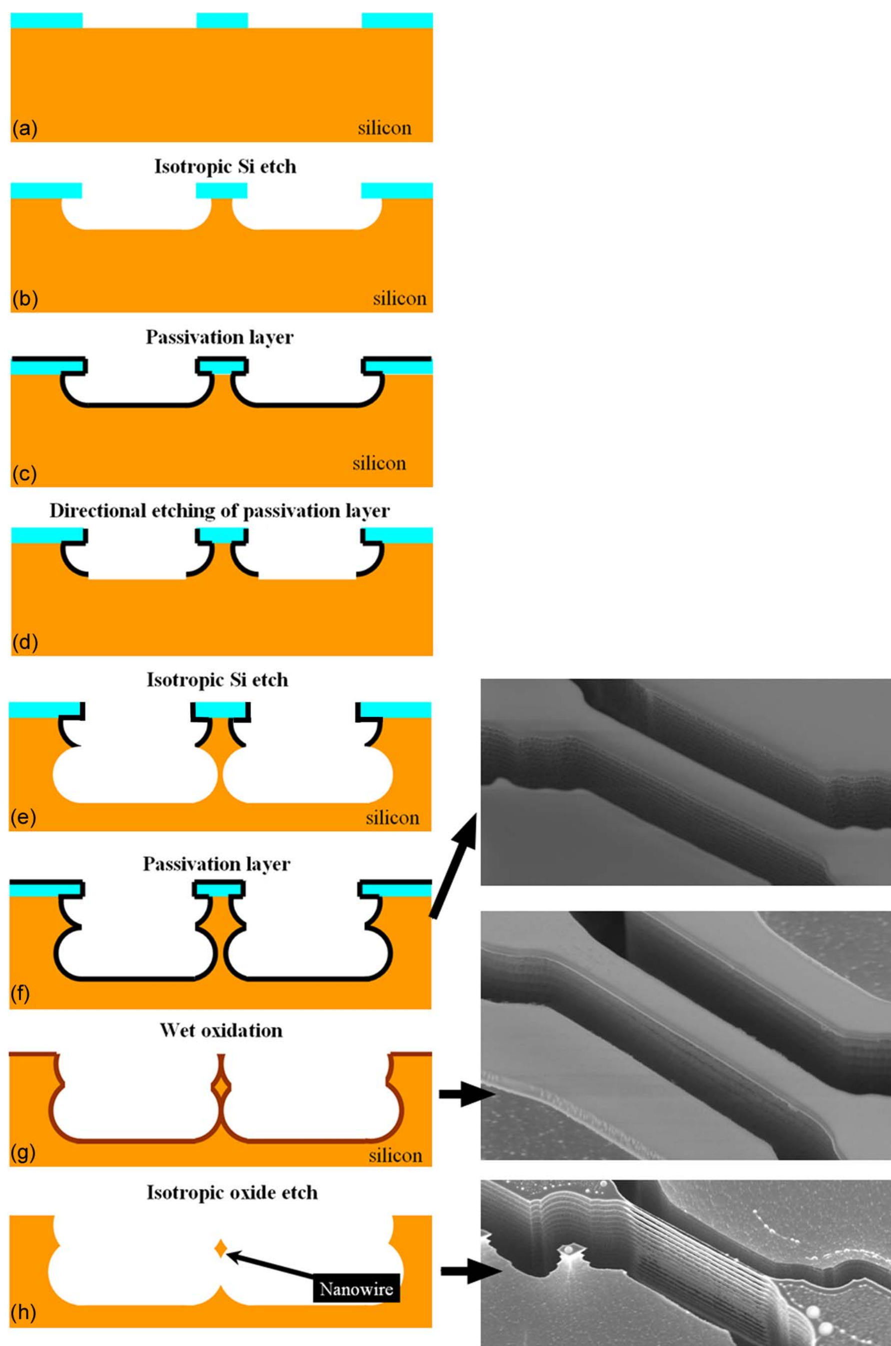

Fig. 1. NW fabrication technique with electron micrographs. One starts with a conventional lithography, where two parallel windows are defined. Scallop formation on sidewalls due to the subsequent Bosch process leads to Si cores running along the dividing centerline between the windows. Further size reduction is realized through oxidation and etching.

respectively. The choice of these dimensions, combined with the resolution limits of the photomask preparation utility, Heidelberg DWL200 laser lithography system, and the undercut associated with thinned AZ9260 photoresist, which is around 500 nm, is observed to lead to a widening of trenches and a reduction of the width of the NW region. Hence, as shown in Fig. 2, the width of the NW region continuously shrinks from the layout to the lithography mask and to the actual pattern on the wafer surface. At the end of the lithographic process, the NW region assumes a width of 1 μm, whereas the trench width increases to about 2 μm. This way one is able to attain a linewidth of 1 μm.

At this point, one might question the necessity of defining a contour layer, since it would as well be possible to form NWs with a single patterning step, where both layers of Fig. 2(a) can be merged into one. This additional patterning stage would be necessary only for planarization, and hence device integration purposes. A discussion of this issue will be provided in the next section, where NW integration to a microgripper is discussed.

The process starts with a 4-in Si wafer coated with a 500-nm oxide mask [Fig. 3(a)]. Wafers are primed with vapor-phase hexamethyldisilazane (HMDS) at 150 °C in YES III primer oven followed by spin coating of thinned AZ9260 positive-tone photoresist of 2-μm thickness and UV exposure in Suss

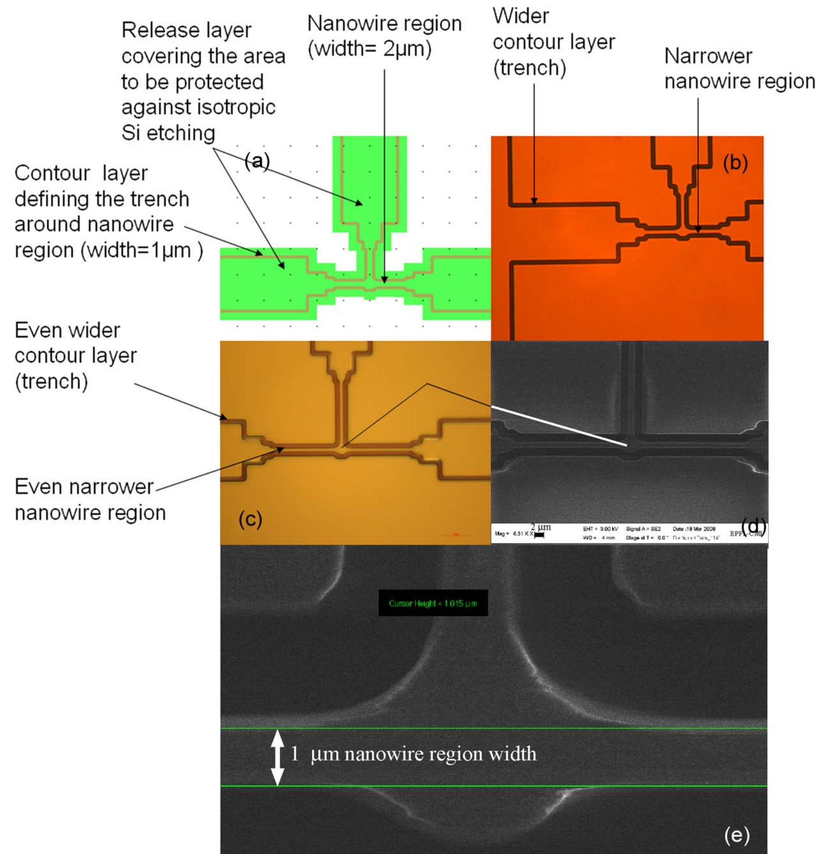

Fig. 2. Obtaining a 1-μm linewidth is accomplished through a series of reduction steps from the layout to the photoresist layer. (a) Layout showing both masks. (b) Contour layer on Cr mask. (c) Contour layer on the wafer. (d) SEM image showing increase in trench width and decrease in the width of the NW region. (e) Close-up of the NW region shown in (d).

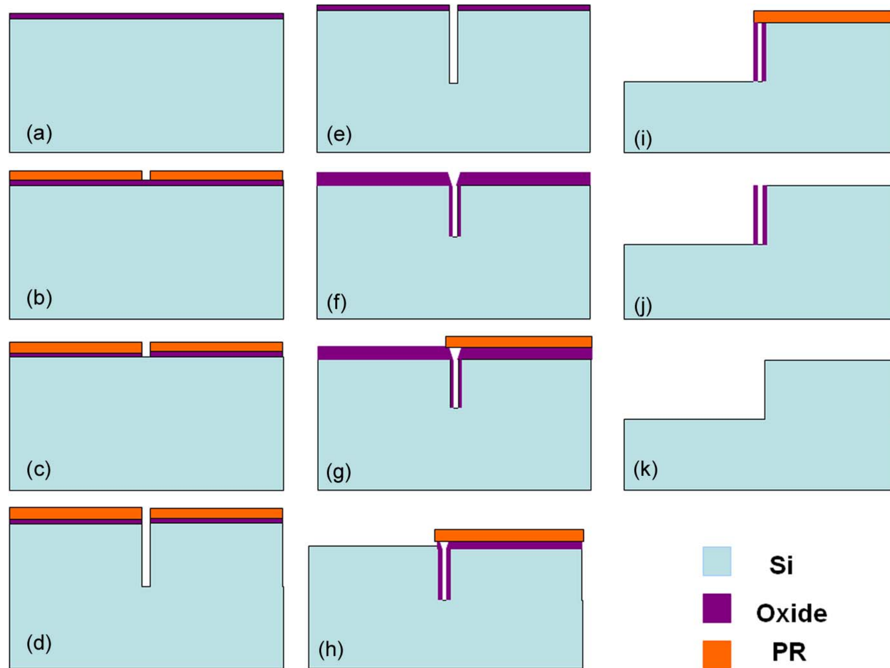

Fig. 3. Fabrication sequence.

MA6/BA6 with 10 mW/cm^2 dose for 10 s [Fig. 3(b)]. After development, the oxide mask is etched anisotropically with a rate of 300 nm/min for 2 min 45 s in Alcatel AMS 200. This provides the necessary hard mask for the subsequent ICP-DRIE process [Fig. 3(c)], which is required to exhibit the critical dimension of 1 μm as discussed in the previous paragraph.

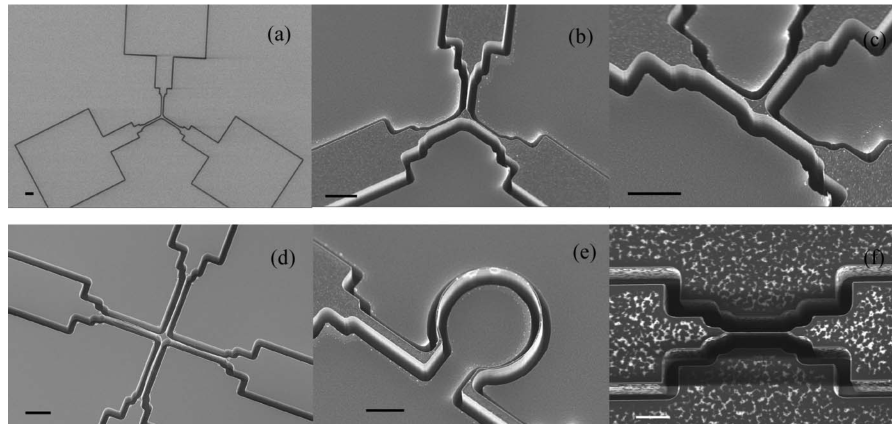

Fig. 4. Variety of NW geometries can be achieved through the process thanks to photolithographic pattern definition. Scale bars designate 10 μm.

Formation of the hard mask is followed by the Bosch process. It is carried out on the same equipment for 4 min with substrate biasing at 40 W of low-frequency pulses and C_4F_8 plasma of 2-s duration [Fig. 3(d)]. At the end of this process, Si strings running along the centerline between etched trenches should form as NW precursors. SF_6 time is varied between 6 and 12 s for different wafers. Resist removal is performed on Oxford PRS900 Asher for 60 min [Fig. 3(e)].

Thermal oxidation is carried out as the next step [Fig. 3(f)]. The purpose of oxidation is twofold. First, it serves as an etch barrier during Si isotropic etching. Second, it thins and smoothens NWs that have formed after Bosch process and protects the NW stacks [Fig. 1(g)]. Since electronic properties of oxide are of no concern, wet oxidation is preferred due to reduced process time. In fact, further annealing of NWs can be carried out to improve their electrical properties. Depending on the duration of SF_6 plasma, different thermal oxidation schemes are applied, where for some processes more than one oxidation step is required until NWs are formed.

For the second lithography, which serves the purpose of protecting NWs during removal of surrounding Si, 3-μm-thick S1818 is chosen as the photoresist due to its good plasma resistance. Alignment is performed with Suss MA6/BA6 and wafers are UV exposed for 15 s with 10 mW/cm^2 dose and developed [Fig. 3(g)]. Anisotropic oxide etching is performed on AMS 200 with C_4F_8 plasma for 2 min 45 s [Fig. 3(h)] followed by isotropic Si etch [Fig. 3(i)] in SF_6 plasma for 3 min with a lateral etch rate of 2 μm/min and a vertical etch rate of 4 μm/min. At this stage, thermal oxide serves as an etch stop and protects NW stacks. Resist is then removed on Oxford PRS900 Asher [Fig. 3(j)].

For the release of NWs from their oxide envelope, HF vapor at 36 °C is utilized on Idonus HF VPE-100 [Figs. 1(h) and 3(k)]. Wafers are overexposed to HF vapor and oxide thickness is measured with Nanospec 6100 before and after oxide etching. At the end of this step, NW stacks of various shapes spanning a pair of electrodes are formed.

C. Fabrication Results

The layout is designed to encompass different NW geometries, such as two-terminal straight lines, T-junctions, crosses,

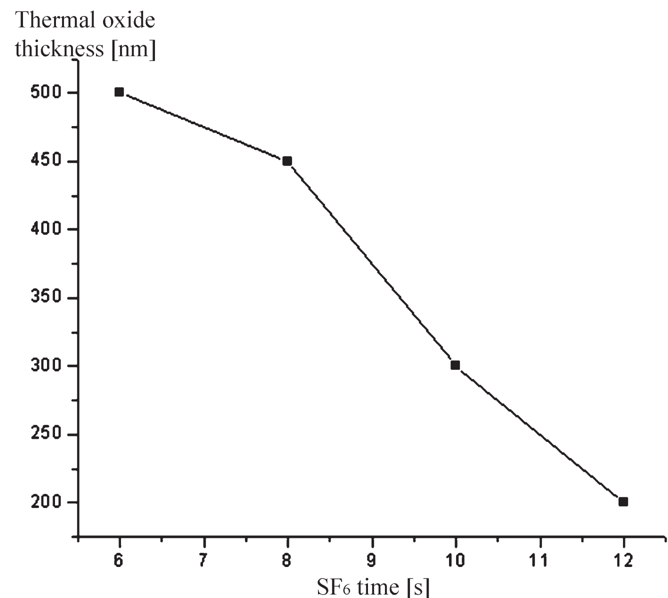

Fig. 5. Relation between isotropic etch duration in ICP-DRIE and the required amount of oxidation for the separation of Si column into NWs. In this plot, all samples had an initial trench separation of 1 μm.

and coils, as shown in Fig. 4. The dimensions of the resulting NWs are observed to be a function of both the duration of the isotropic etch cycle in ICP-DRIE (SF_6 plasma, as shown in steps b and e in Fig. 1) and the amount of oxidation (step g in Fig. 1). The required oxide thickness for complete separation of the Si column into Si strings is measured and shown as a function of SF_6 time in Fig. 5. It is to be noted that this plot provides an indication of the onset of NW formation. Further reduction of NW diameter is always possible with oxidation. Some of the issues associated with the thinning stage of NWs are compressive stress buildup due to volumetric expansion during oxidation and associated buckling and fracture of the structures. Nevertheless, sub-100-nm NWs are easily obtained, as shown in Fig. 6(a) and (b). It is possible to reduce the diameter to about 50 nm [Fig. 6(c)].

Compressive stresses build up due to the volumetric expansion of oxidized Si combined with the mechanical confinement of the double-clamped-beam geometry. For Si NW precursors with relatively high slenderness ratios obtained by the Bosch process, the effect of the compressive stress buildup during

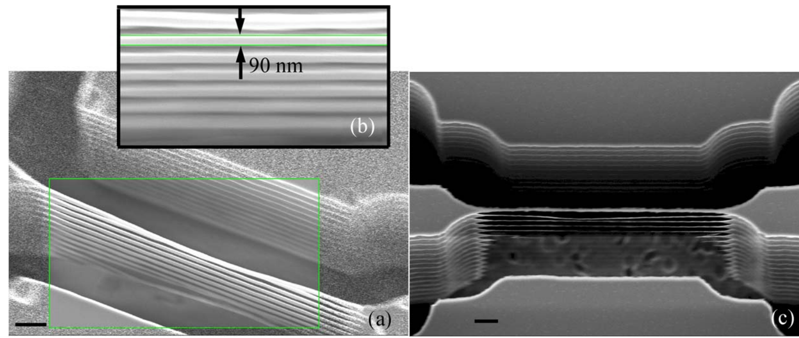

Fig. 6. NWs of different diameters. (a) and (b) Sub-100-nm NWs are easily obtained through this technique. (c) Diameter can be reduced to about 50 nm. Lower NWs, which seem to be discontinuous due to loss of contrast against the background, in fact, span the whole length between the electrodes. Scale bars stand for 1 μm.

oxidation can be dramatic. When the level of compressive stress within a single beam exceeds a critical value, the beam becomes unstable and buckling occurs as a result. Based on the observation that buckling is a direct outcome of the slenderness ratio of double-clamped NW precursors formed via ICP-DRIE, the following points are established as a means of eliminating buckling.

1) The critical compressive stress, beyond which the straight configuration of a double-clamped NW is unstable, is only a function of the slenderness ratio of the NW in addition to its elastic modulus. Furthermore, the compressive stress in an oxidized Si NW is directly proportional to the amount of oxidation because of the volumetric expansion. Hence, the chance of buckling and breaking of NWs can be reduced, if multiple oxidation runs—each time with a limited thickness of oxide—are carried out rather than oxidizing an NW in a single step. This becomes particularly important when NWs with a diameter less than 50 nm are targeted, where the slenderness ratios become appreciable. In this paper, it is observed that perfectly straight NWs with diameters less than 50 nm can be obtained over the course of multiple oxidation and etching steps, where HF vapor phase removal of the oxide is utilized instead of wet etch.
2) Finally, since buckling occurs due to mechanical confinement, one can also prevent the buildup of compressive stresses if one employs the cantilever geometry rather than the double-clamped beam. Having a free end, uniaxial strain developing in the cantilever is mainly due to the volumetric expansion of oxide. The cantilever is free to expand with no elastic strains, and hence, no compressive stress will develop. This was exactly what was observed during our fabrication trials. Cantilevers were employed mainly as end-effectors of grippers discussed in the following section. No single cantilever was observed to suffer buckling-related deformation.

In this section, critical process parameters such as the width of the NW region, the required amount of oxidation as a function of isotropic etch duration for the initial separation of Si column into Si NW precursors and the elimination of buckling are discussed. The following section deals with the integration of such NWs with an actual microsystem in the form of a microgripper.

III. Integration of NWs With a Microgripper

The suitability of the technique for integration with microsystems is demonstrated using a gripper design. A gripper provides a challenging platform with demanding requirements on the location and orientation of the NWs. NWs are to be placed at the tip of multiple end-effectors driven by thermal or electrostatic actuators. Any misplacement of NWs might lead to possible short circuits rendering the microgripper useless. Hence, NW attachment to grippers is usually carried out by careful focused-ion-beam [18] or e-beam-induced deposition [19] instead of self-assembly. In this section, the challenge of employing NWs as functional structures on a microsystem will be addressed. Device design and fabrication of the gripper will be explained first. The section will be concluded with fabrication results and gripper characterization.

A. Device Design and Fabrication

Fabrication methodology shown in Fig. 3 is employed in the device fabrication. This does not only ensure the simultaneous fabrication of NWs along with the device; at the same time, the strength of adhesion between the device and NW extensions is also expected to be very high because they will be fabricated from the same crystal. Hence, NWs become an integral part of the structure without any postprocessing steps for attachment or growth.

Fig. 7 shows major components of the device along with the employed layout. The design consists of a fixed base, comb fingers, anchors, springs, and gripper arms. Except for the fixed base, the whole structure is released from the substrate. The actuation is provided by the electrostatic attraction between comb fingers upon application of a potential difference between the fixed base and released arms. Since the released comb finger arrays on both sides of the fixed base are connected to the gripper arms, their movement due to electrostatic attraction is linearly translated to the gripper arms resulting in a closure of the nanotips. In order to prevent pull-in to the substrate, both movable shuttle and the handle Si wafer are kept at the ground potential. Actuation voltage is applied to the stationary part of the device. NWs are not visible in Fig. 7(a) due to the scale of the micrograph.

In parallel to the fabrication sequence of NWs shown in Fig. 3, device layout consists of two layers [Fig. 7(b) and (c)].

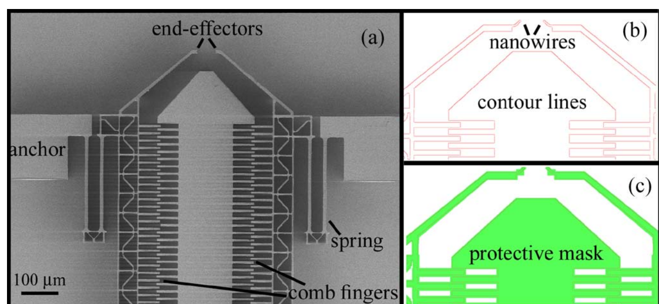

Fig. 7. (a) Tip of a generic device with basic components. (b) First mask defining contour lines around the device. Location and orientation of NWs are determined at this stage. This lithographic step is the same as the one shown in Fig. 3(b). (c) Second mask providing protection of Si device during isotropic Si etching [the same as Fig. 3(g)].

The first layer is the contour layer defining a trench around the device body, comb fingers, anchors, and NW region. The other one is the release layer covering the area to be protected against Si isotropic etching. In the contour layer, the trench width is again designed to be 1 μm. Other details of the fabrication sequence are similar to those reported for the fabrication sequence of NWs.

If one needs to build further on top of the existing device, a topography with minimum deviations from planarity is required for subsequent lithographic steps. One such example is a three-finger gripper, where the third finger sits on top of the stationary electrode separated from it by a thick oxide [20]. The necessity of the trench becomes evident at this point, because it is the only way of avoiding an extreme topography that would inhibit further fabrication. Hence, the contour layer defining the trench around the Si device is unnecessary in case of omission of further layers. However, its presence extends the applicability of the technique to further device integration.

SOI wafers with a device layer of 10 μm, a BOX layer of 1 μm and a handle layer of 380 μm are used for fabrication. Wafers are first primed with HMDS and then coated with thinned AZ9260 positive-tone photoresist of 2-μm-thick UV exposed in Suss MA6/BA6 for 10 s with 10 mW/cm^2 dose and developed. Bosch process is held with AMS 200 for 4 min with substrate biasing at 40 W of low-frequency pulses, 12 s of SF_6 plasma, and 2 s of C_4F_8 plasma. With this recipe, scallops are observed to completely vanish after 20 min of etching due to elevated undercut associated with the process. Since SOI wafers with device layers thicker than 10 μm require longer etch times, a through-thickness etch in such wafers always leads to the disappearance of NWs. Resist removal is performed with Oxford plasma asher for 60 min followed by a 200-nm-thick wet oxidation [Fig. 8(a)]. Before second lithography, HMDS priming is carried out. For the second lithography, a 3-μm-thick S1818 is chosen. Alignment is performed with Suss MA6/BA6 and wafers are UV exposed for 15 s with 10 mW/cm^2 dose and developed. After development, anisotropic oxide etching is performed in Alcatel 601E for 90 s. In order to ensure complete removal of oxide, it is overetched. After isotropic Si etching on Alcatel 601E for 6 min, resist is removed with Oxford for 90 min [Fig. 8(b)]. Finally, oxide release is performed in HF vapor for 2 h at 36 °C [Fig. 8(c)]. A pair of end-effectors are shown in detail in the tilted micrographs of Fig. 9.

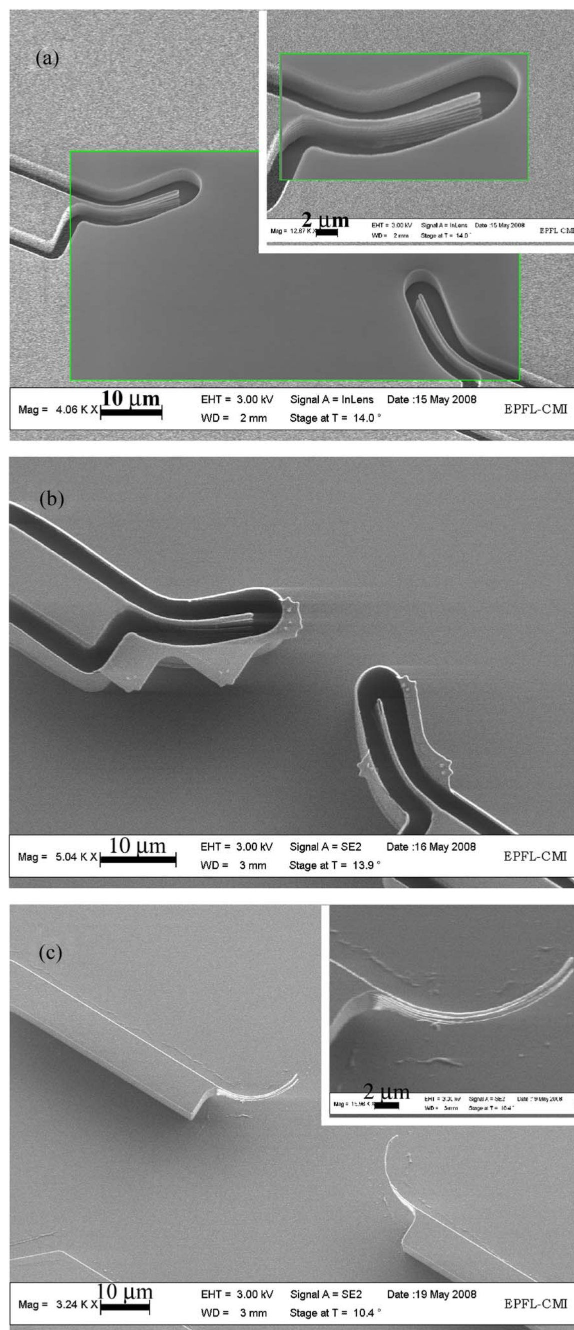

Fig. 8. Close-up of NWs etched in the tip of Si end-effector at various stages during fabrication. (a) After wet oxidation. (b) After isotropic Si release (notice thin oxide walls). (c) After isotropic oxide etch in HF vapor.

B. Device Characterization

One of the most important criteria against which the success of the microgripper fabrication is to be evaluated is the structural integrity and strength of the NW-microgripper bond. In our case, this bond is expected to be very strong, since both structures are carved from the same crystal, and hence, there is no interface that would be encountered in a conventional NW growth study.

For this purpose, NWs are mechanically loaded at their tip with a 5-μm tip-diameter tungsten probe. The probe is attached to a DCM-205 micropositioner (Cascade Microtech) with a

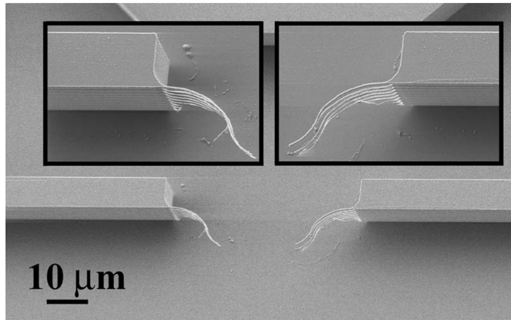

Fig. 9. Tilted micrographs showing a pair of end-effectors with integrated NW stacks.

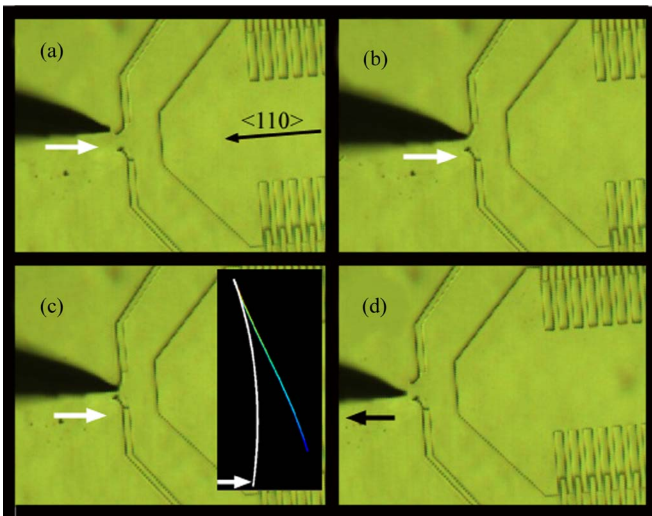

Fig. 10. Pushing of an NW stack with a tungsten probe with loading (a)–(c) and unloading (d) steps. Picture in (c) corresponds to peak loading with the corresponding finite element stress analysis shown in the inset.

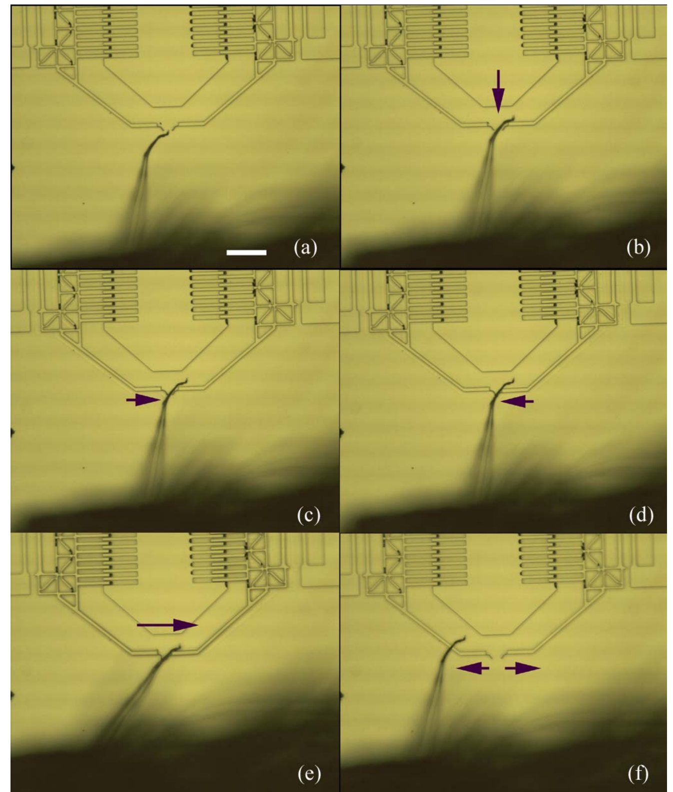

Fig. 11. Manipulation of a paper fiber by the microgripper with NW end-effectors. Scale bar in (a) is 80 μm.

screw resolution of 50 TPI. Once the tungsten probe tip is brought in contact with the NW, the probe is slowly (manually) translated parallel to the plane of the wafer. The direction of probe motion is parallel to the long axis of the microgripper, coinciding with the $\langle 110 \rangle$ orientation of Si. The NW is thus deformed. One complete loading and unloading cycle is shown in Fig. 10. Fig. 10(c) shows the peak loading case where the tip of a 17-μm-long NW with a 100-nm diameter deflects by 15 μm. A finite element analysis of this case is carried out using ANSYS. The load is distributed at the NW tip over a length comparable to that of the actual tungsten probe-NW contact zone. Utilizing large deformation analysis, an equivalent stress of 850 MPa is obtained at the base of the NW, where it is attached to bulk Si. When the probe is retracted, the NW returns to its original configuration [Fig. 10(d)] indicating full elastic behavior.

In the literature, it is argued that the strength of Si NWs is a function of their length [21]. In this regard, the calculated stress value of 850 MPa is observed to be higher than the fracture strength measured on Si NWs at the same length scale [22]. Although values in [22] were obtained specifically on NWs grown along $\langle 111 \rangle$ direction and there is no fixed crystallographic orientation associated with the curved NW of this paper, the obtained level of stresses can still be considered as an indication of a good bond between NWs and MEMS.

Finally, a manipulation trial is carried out. First, a knife edge with protruding paper fibers is prepared as a platform carrying manipulation objects. For this purpose, a tissue paper is pressed against a knife edge covered with a thin layer of glue and pulled away. Upon tearing of this paper, a series of fine fibers remain on the knife edge, protruding from it perpendicularly. Then, the knife edge is attached to a component positioning system (M-562F-XYZ three-axis stage by Newport positioned on an M-UTR160 rotary stage by Newport). A microgripper is also mounted on a multiaxis stage and brought in contact with the fibers. Both the multiaxis stage and the component positioning system are operated manually under an optical microscope. Fig. 11(a) shows the gripper and one such fiber. In Fig. 11(b), the gripper approaches the fiber. The right-hand and left-hand fingers close upon actuation in Fig. 11(c) and (d), respectively. Once the fiber is tightly held, the gripper is moved sideways with respect to the knife edge, thereby pulling the fiber [Fig. 11(e)]. When the end-effectors are retracted in Fig. 11(f), the fiber is released. NWs are observed to remain intact after stretching of the fiber.

IV. Conclusion

Vertical Si NW stacks were fabricated using the scalloping effect during Bosch process. The location and orientation of NWs were determined by photolithography, whereas their number was controlled by adjusting the number of etch cycles. NW

arrays spanning a pair of electrodes were fabricated in various geometries ranging from T-junctions to coils. Since the location and orientation of NW arrays were lithographically defined, one could easily integrate these structures with microsystems. This aspect was demonstrated with a microgripper, whose both end-effectors were fabricated to entail NW arrays. Overall, the following points are concluded.

1) The proposed technique is suitable for a batch-compatible integration of Si NWs with microsystems. A single patterning stage is required to define the location and orientation of NWs along with the bulk of the microsystem.
2) Since NWs and microsystems are carved from the same Si crystal, their bond is very strong, and hence, the integration technique is suitable for demanding mechanical applications such as probing and manipulation.
3) The duration of the Bosch process is observed to be a limiting factor, since scallops disappear with increased etch time. With the reported etch recipe of this paper, a maximum depth of 10 μm is achievable.
4) Further study is required on factors that affect the dimensions of the resulting NW stack. NW diameter is determined by an interplay between the isotropic Si etch stage of the Bosch process and the following oxidation and oxide etch steps. In this paper, diameters ranging from about 50 nm to above 100 nm are obtained in straight NWs. NW orientation is one major factor to be considered in the determination of the final diameter. For straight NWs, the freedom of assigning a certain crystallographic orientation is also to be considered as an advantage of this technique.

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