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Three-level stencil alignment fabrication of a high-k gate stack organic thin film transistor

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ABSTRACT

In this work a high-k double-gate pentacene field-effect transistor architecture is presented. The devices are fabricated on a flexible polyimide substrate by three aligned levels of stencil lithography combined with standard photolithography. ALD-deposited high-k HfO_2 and parylene D device passivation, together with Pt top-gate deposition provide very good electrostatic control of the channel, showing low leakage current and improved subthreshold. The ION/IOFF ratio is of the order of 10^6 and the IOFF lower than 0.1 pA/μm. We also report a comparison of the *normal*, FET-like ($VD < 0$) and *reverse*, diode-like ($VD > 0$) modes of the p-OFET. We find a higher current drive in the *reverse* diode-like mode compared to normal FET-like mode. The reverse mode has clearly defined OFF and ON states versus the drain voltage and non-saturated output characteristics, which makes it suitable for the use in RF and analog applications of OFETs.

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1. Introduction

Organic thin film transistors have gained attention as possible building blocks for electronic application. Various architectures have been demonstrated, combining bottom-gate or top-gate electrodes [1] with top or bottom source and drain. The main goal of these approaches is to improve the electrostatic control of the gate over the pentacene conductive channel as well as to reduce the contact resistances at the source and drain regions [2]. A high gate capacitance combined with a high mobility of carriers in the organic semiconductor is crucial for high performance OFETs operating at frequencies higher than tens of MHz. Hafnium oxide (HfO_2) with high dielectric constant going from 11 up to 25 depending on deposition method [3,4] is today a well-controlled and understood high-k dielectric with low-current leakage, used in modern CMOS ICs. Therefore, its use to improve the performance of OFET is well-motivated.

In this work we present a double-gate architecture of pentacene OFET in which a single (bottom) gate controls the on-current, using a thin gate dielectrics (<50 nm), with top-contacted source and drain regions, fabricated on an organic flexible substrate. Other reported works have used either thicker dielectric layer or top-contact but with longer channels (∼50 μm) [3,4]. In our previous work [5] we have reported on the role of a second top metal gate to control the OFF-current and the subthreshold swing in such OFET devices. This double-gate solution is implemented in the new device without using a high-k dielectric for the top-gate, as the role of the top gate is not for dictating the on-current level.

We also concentrate on the operation of high-k double-gate OFETs in the normal and reverse regimes, corresponding to positive and negative drain voltages respectively used together with a negative gate voltage in the ON state. We will show that the operation in reverse regime is able to offer increased current drive and higher transconductance than normal mode enabling higher frequency operation of the analog OFET transistor.

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2. Fabrication of high-k OFET

High-k gate Organic Field-Effect Transistors (OFETs) are structures composed of several thin layers: metal gate and dielectric layers on top of which thin film of pentacene is deposited through a stencil, and source and drain areas and electrodes made of gold. OFETs are fabricated using a combination of standard and stencil lithography methods [5,6]. First step is a deposition of flexible (12 μm thick, Fig. 1a and b) polyimide substrate by spin-coating on a silicon wafer. The deposited layer is then soft-baked at 70 °C to remove the solvent and hard-baked for 4.5 h at 300 °C in order to gain sufficient level of polymerization. Afterwards (Fig. 1c) the gate metal electrode, 5-nm thick Ti adhesion layer and 35 nm thick Pt layer, are deposited by standard lithography lift-off process using EVG150 coater and developer system for positive resist and e-beam evaporation process in Leybold Optics Lab 600H evaporator (rate of 4 Å/s). Next, 50 nm layer of HfO_2 is deposited by atomic layer deposition (ALD) at 200 °C as gate dielectric (Fig. 1d). Another standard lithography step (Fig. 1e) for defining the location of vias holes for gate contacts is done. Dry etching through the vias holes is performed in Adixen AMS200 etcher system, optimized for Deep Reactive Ion Etching. Next, 10 nm thick Ti adhesion layer, positioned bellow source and drain contact pads is deposited using another lift-off lithography process (Fig. 1f). The deposition of the active semiconductor material, triple-purified 50 nm thick pentacene from Sigma–Aldrich is done by evaporation through an aligned full-wafer stencil in a Vacotec thermal evaporator (rate: 1 Å/s), at a pressure of $9.1 \cdot 10^{-7}$ mbar, shown on Fig. 1g. A second aligned stencil is used for the e-beam evaporation of 100 nm thick Au source and drain contacts (Fig. 1h). The top passivation layer, 200 nm thick parylene D, is deposited by CVD process in Comelec C-30-S parylene deposition system (Fig. 1i). Finally, the top-gate, 100 nm thick layer of Pt was deposited by e-beam evaporation process using Leybold Optics Lab 600H and it is shown on Fig. 1j. Every step, except the deposition of parylene D passivation layer is done in a cleanroom environment. Flexible polyimide substrate is easily detached from a rigid Si handle wafer simply by peeling off the film, shown on Fig. 1k. The device cross section and an example of flexible substrates with various fabricated structures are shown in Fig. 2.

Electrical characterization of devices is performed using a Microtech Cascade probing system through the top passivation layer.

3. Characterization of the high-k dielectric

A high-k HfO_2 layer as a gate dielectric is fabricated by ALD at deposition temperature of 200 °C. This process is compatible with polyimide flexible substrate given the fact that polyimide has a high temperature stability and can handle temperatures as high as 300 °C. A very high capacitance (330 nF/cm^2) was obtained by a film thickness of 50 nm giving the dielectric constant of $k = 18.6$. Several parallel MIM (metal–insulator–metal) plate capacitors of plate areas from 50 × 50 μm to 150 × 150 μm were fabricated. Dielectric properties of this material were characterized using capacitors having the biggest plate area (150 × 150 μm). Leakage current was very low; in the order of few to few tens of pA. Two different characterizations tools were used to confirm the value of capacitance. Hewlett–Packard 4284A Precision LCR meter at 1 kHz frequency shows the $C = 74.2$ pF value for the capacitor with the plate surface of 150 × 150 μm, which corresponds to a dielectric constant of $k = 18.6$. This value was further confirmed using Quasi-static Agilent 4156C DC analyzer (Fig. 3, red, left scale). Comparison with low-k dielectric capacitor of the same plate surface area but different dielectric thickness (230 nm of spin-coated polyimide) is also shown on Fig. 3. (right, blue scale). QSCV measured value of capacitance is 1.9 pF, which corresponds to $k = 2.3$. Equivalent Oxide Thickness (EOT) of the high-k capacitor is 10 nm, while EOT of the low-k capacitor is 393 nm. This huge difference in EOT is the result of higher dielectric constant of HfO_2 (18.6 compared to 2.3) but is also the result of higher thickness of low-k dielectric (230 nm of polyimide compared to 50 nm of HfO_2).

The continuity of pentacene layer on the high-k dielectric is very satisfactory, having an average grain size of 50–100 nm, as it is shown on Fig. 4; this result suggests that the high-k co-integration process with the pentacene shall provide devices with good channel electrical properties.

4. Dc electrical characterization in normal p-OFET mode

The reported high-k OFETs, fabricated with three-level aligned stencil lithography have as smallest channel dimensions $W = 10$ μm and $L = 5$ μm. The transfer characteristics in the normal p-mode (bottom-gate voltage: $V_G < 0$, drain voltage: $V_D < 0$) show a

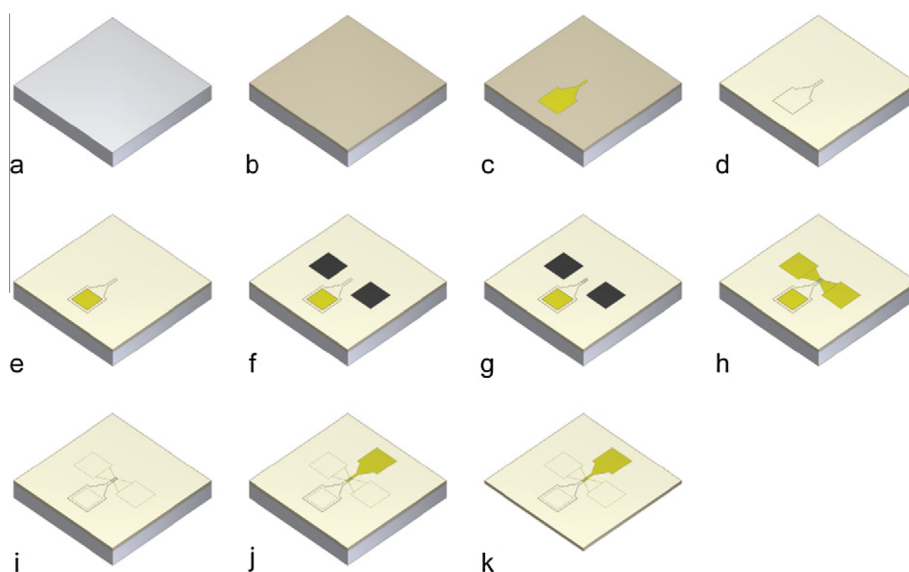

Fig. 1. Processing steps for the fabrication of the double-gate pentacene TFTs.

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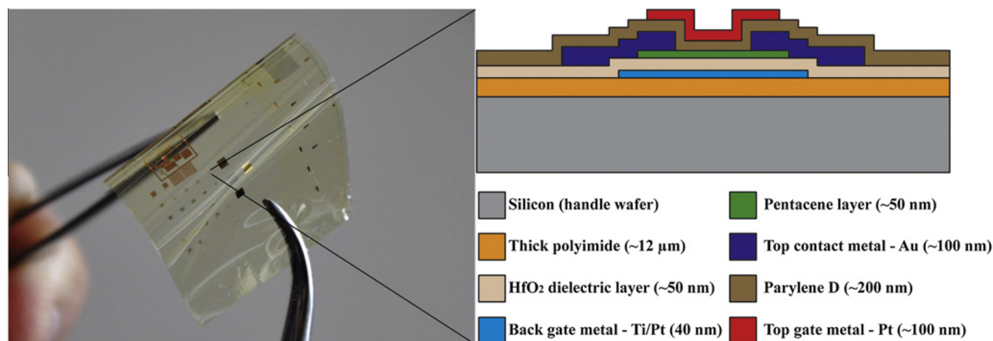

Fig. 2. Photograph (left) of OFET devices on a flexible substrate once detached of a carrier Si-wafer; also shown are other passive and test devices (high-k capacitors and inductors) as well as small test circuits, co-integrated with the same process and schematic cross section (right) of a double-gate pentacene OFET with 50 nm HfO_2 dielectric for the bottom gate.

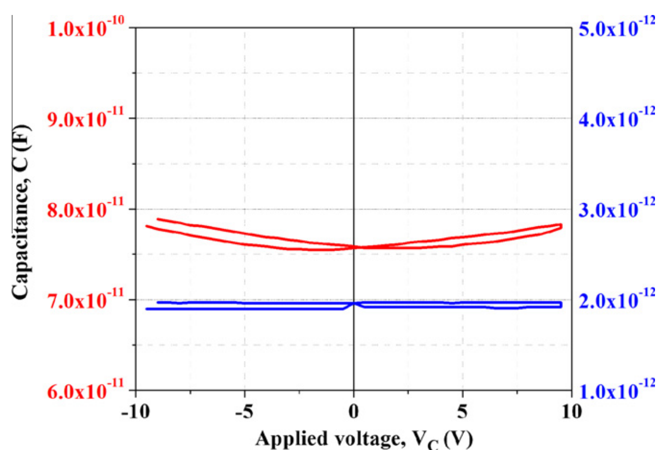

Fig. 3. Capacitance of high-k (red, left scale) and low-k dielectric (blue, right scale) of 150 × 150 μm capacitors; 50 nm ALD grown HfO_2, and 230 nm of spin-coated polyimide. (For interpretation of the references in colour in this figure legend, the reader is referred to the web version of this article.)

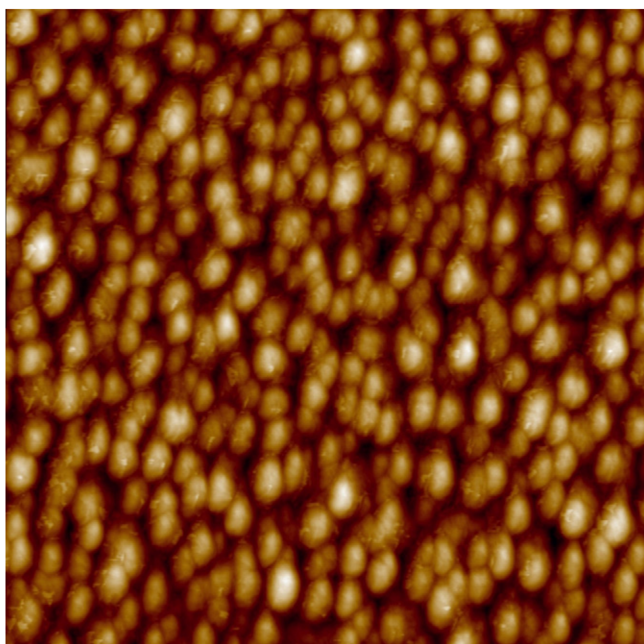

Fig. 4. AFM image of deposited pentacene taken from the middle of an OFET channel (area: 2 × 2 μm).

very good I_{ON}/I_{OFF} ratio of the order of 10^6 as well as rather small value of subthreshold slope, sub-1 V/decade (Fig. 5a) especially after parylene D coating and fabrication of passivation-acting top-gate Pt layer. Fig. 5a also shows the beneficial effect of the parylene coating and top-gate processing on the transistor I_{ON}/I_{OFF} and subthreshold swing characteristics, in agreement with other similar works [5,6,9]. Low-field mobility is extracted using a standard method ($I_D \times g_m^{-0.5}$) applied for silicon MOSFETs [8] assuming that there is no dependence of the contact resistances at the source and drain on the gate voltage. The value obtained was $\mu_0 \sim 2{\cdot}10^{-2}$ cm^2/vs. This relatively low mobility value could be related to the presence of dielectric polar charges and other surface charges in the conducting channel reducing the quality of the pentacene/HfO_2 interface, as reported earlier [4,10,11].

The output characteristics (Fig. 5b) of an OFET with channel width $W = 10$ μm and channel length of $L = 5$ μm show excellent linearity in the region of low V_D, demonstrating good contact between Au and pentacene with low contact resistance [7] as well as good saturation in the region of V_D voltage bellow −6 V. Note that in both transfer and output characteristic the transistor is completely off for $V_G > 0$ and conduction is enabled by applied negative gate voltages. However, a particular behavior exists for positive drain voltages, as it will be discussed in the next section.

5. Comparison and analysis of normal, FET-like versus reverse, diode-like, device operation mode

First, it is important to notice that we call the ‘reverse' mode of operation of the p-type OFET the characteristics obtained at positive drain voltage, $V_D > 0$, when the gate voltage can vary from positive to negative values. Further than the different drain voltage sign, the major difference of the reverse mode operation is that what was the drain in normal mode becomes source in reverse mode and, therefore, the gate-to-source voltage is not fixed anymore as V_{DS} changes.

In Fig. 6a and b we compare for the first time the normal FET-like and the reverse diode-like modes in the output characteristics, in linear and semi-log scales, of a pentacene OFET under same external applied biases on gate, drain and source (this last terminal is always grounded) and find that:

(a) The drain current can reach much higher values in reverse mode at same external biases; (b) in contrast with the normal mode the reverse mode is non-saturated, following the predictions made in Deen's theory. Fig. 6b depicts the existence of a threshold voltage in the reverse mode characteristics, which makes it similar to a diode-like operation, opening all the related types of analog applications of diodes, in this particular mode.

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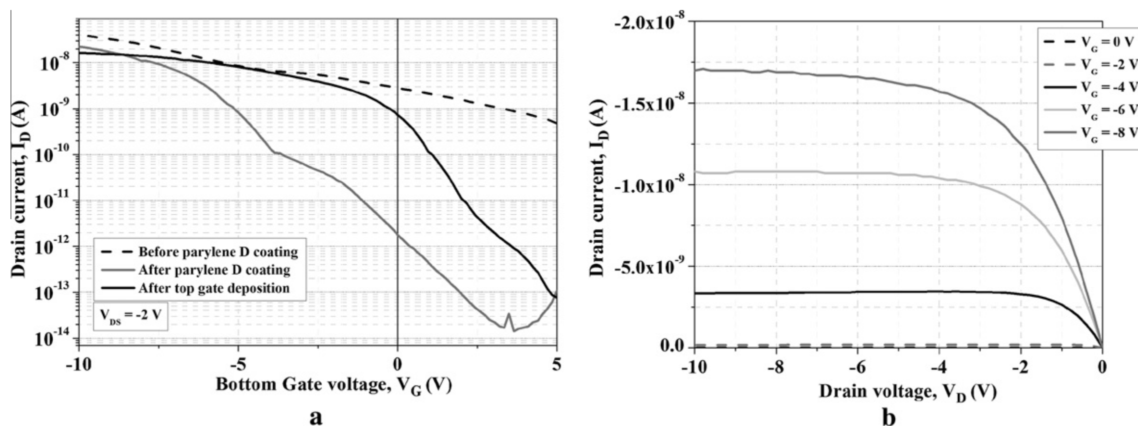

Fig. 5. (a) Transfer characteristics, I_D–V_G, of the fabricated OFET in successive steps: before and after parylene D coating, and after top gate deposition. The final device has the steepest OFF to ON transition, stable characteristics and low OFF current; (b) Output characteristics of an OFET with high-k gate dielectric, parylene D coating and top gate, showing a very good p-OFET transistor behavior with well saturated output characteristics, supporting circuit design. The dimensions of the channel are $W = 10\ \mu m$ and $L = 5\ \mu m$.

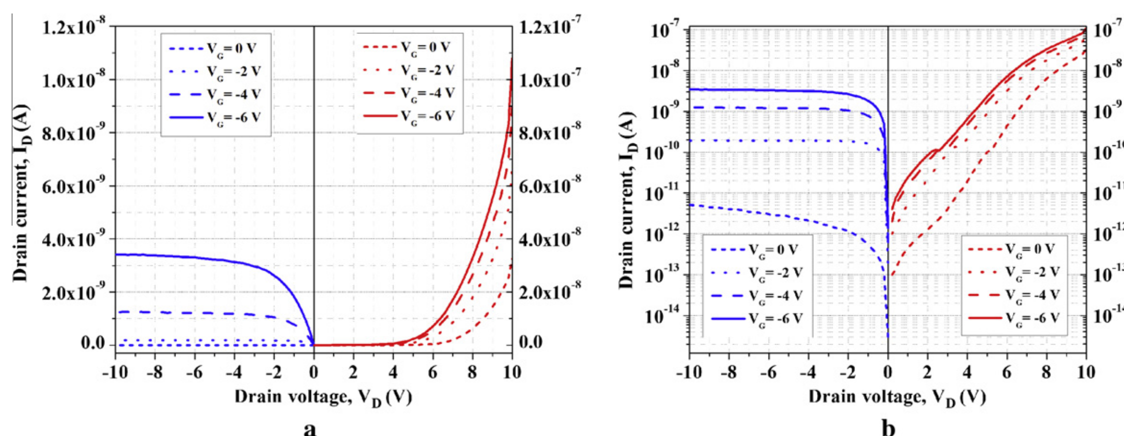

Fig. 6. Linear (a) and semi-log (b) output characteristics (I_D–V_D) in normal (blue) $V_D < 0$ and reverse (red) $V_D > 0$ modes of OFET with $W = 10\ \mu m$ and $L = 5\ \mu m$ organic transistor. A threshold voltage is identified in the reverse mode, with quasi-exponential subthreshold operation. (For interpretation of the references in colour in this figure legend, the reader is referred to the web version of this article.)

In [12], when reporting on the contact effects in polymeric thin film transistors based on in poly3-alkylthiophen thin film field-effect transistors with gold contact electrodes and bottom contact configuration, Deen et al. have investigated the modeling of a similar reverse mode operation, for $V_D > 0$ and proposed an analytical modeling based on the theory of space-charge-limited conduction in OFETs, suggesting a non-saturated I_D–V_D.

6. Conclusion

In this work double-gate architecture for pentacene OFETs fabricated on flexible substrate has been presented and its electrical characteristic investigated. The major focus has been on the experimental comparison between the normal FET-like ($V_D < 0$) and reverse diode-like ($V_D > 0$) modes of operation of the transistor. We highlighted, for the first time that under same external biases, the reverse mode can offer drain current and transconductance boosting compared to normal mode, with gain factors close to 2. The reverse mode has a non-saturated behavior and shows an equivalent threshold voltage and subthreshold regime, which makes it similar to a diode-like mode for which many future appropriate analog and RF applications can be identified.

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References

[1] Z. Bao, J. Locklin, Organic field-effect transistors, CRC Press, 2007. ISBN 0-8493-8080-4.
[2] G. Horowitz, Journal of Material Research 19 (2004) 7.
[3] C.-Y. Wei et al., IEEE Electron Device Letters 30 (2009) 10.
[4] X.-H. Zhang, S.P. Tiwari, S.-J. Kim, B. Kippelen, Applied Physics Letters 95 (2009) 223302.
[5] D. Tsamados, N.V. Cvetkovic, et al., Solid State Electronics 54 (9) (2010) 1003–1009.
[6] K. Sidler, N.V. Cvetkovic, et al., Procedia Chemistry 1 (1) (2009) 762–765.
[7] X.-H. Zhang, S.P. Tiwari, B. Kippelen, Organic Electronics 10 (2009) 1133.
[8] G. Ghibaudo, Electronics Letters 24 (1988) 9.
[9] D. Simeone et al., Thin Solid Films 517 (2009) 6283–6286.
[10] X.-H. Zhang, B. Domercq, X. Wang, S. Yoo, T. Kondo, Z. Wang, B. Kippelen, Organic Electronics 8 (6) (2007) 718–726.
[11] J. Veres, S. Ogier, G. Lloyd, D. de Leeuw, Chemistry of Materials 16 (23) (2004) 4543.
[12] M.J. Deen, M.H. Kazemeini, S. Holdcroft, Journal of Applied Physics 103 (2008) 124509.

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