Design of a 2.4 GHz BAW-based CMOS Transmitter

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Abstract

In recent years, bulk acoustic wave resonators (BAW) in combination with RF circuits have shown a big potential in achieving the low-power consumption and miniaturization level required to address wireless sensor nodes (WSN) applications. A lot of work has been focused on the receiver side, by integrating BAW resonators with low noise amplifiers (LNA) and in frequency synthesis with the design of BAW-based local oscillators, most of them working at fixed frequency due to their limited tuning range. At the architectural level, this has forced the implementation of several single channel transceivers.

This thesis aims at exploring the use of BAW resonators in the transmitter, proposing an architecture capable of taking full advantage of them. The main objective is to develop a transmitter for WSN multi-channel applications able to cover the whole 2.4 GHz ISM band and enable the compatibility with wide-spread standards like Bluetooth and Bluetooth Low Energy. Typical transmissions should thus range from low data rates (typically tens of kb/s) to medium data rates (1 Mb/s), with FSK and GFSK modulation schemes, should be centered on any of the channels provided by these standards and cover a maximum transmission range of some tens of meters.

To achieve these targets and circumvent the limited tuning range of the BAW oscillator, an up-conversion transmitter using wide IF is used. The typical spurs problems related to this transmitter architecture are addressed by using a combined suppression based on SSB mixing and selective amplification. The latter is achieved by co-integration of a high efficiency power amplifier with BAW resonators, which allows performing spurs filtering while preserving the efficiency. In particular the selective amplifier is designed by including in the PA analysis the BAW resonator parameters, which allows integrating the BAW filter into the passive network loading the amplifier, participating in the drain voltage shaping. Finally, the frequency synthesis section uses a fractional division plus LC PLL filtering and further integer division to generate the IF signals and exploit the very-low BAW oscillator phase noise.

The transmitter has been integrated in a 0.18 μm standard digital CMOS technology. It allows addressing the whole 80 MHz wide 2.4 GHz ISM band. The unmodulated RF frequency carrier demonstrates a very-low phase noise of -136 dBc/Hz at 1 MHz offset. The IF spurs are maintained lower than -48 dBc, satisfying the international regulations for output power up to 10 dBm without the use of any quadrature error compensation in the transmitter. This is achieved thanks to the rejection provided by the SSB mixer and the selective amplifier, which can reach drain efficiency of up to 24% with integrated inductances, including the insertion losses of the BAW filter. The transmitter consumes 35.3 mA at the maximum power of 5.4 dBm under 1.6 V

(1.2 V for the PA), while transmitting a 1 Mb/s GFSK signal and complying with both Bluetooth and Bluetooth Low Energy relative and absolute spectrum requirements.

Keywords: MEMS, Bulk-acoustic wave resonators, WBAN, WSN, Transmitter, RF CMOS

Résumé

Dans les dernières années, la combinaison de résonateurs à onde de volume (BAW) avec des circuits RF a démontré un grand potentiel qui permet d'atteindre les besoins de basse puissance et de miniaturisation requis par les applications de réseaux de capteurs sans fils (WSN). Beaucoup d'efforts ont été investis du côté du récepteur, en particulier pour l'intégration des résonateurs BAW dans les amplificateurs à faible bruit (LNA), ou dans la synthèse de fréquence. Un des plus grands désavantages liés à l'utilisation des résonateurs BAW en combinaison avec les oscillateurs est une plage de réglage très réduite. D'un point de vue architectural, cela a forcé l'implémentation de radios à un seul canal.

Cette thèse vise à explorer l'utilisation des résonateurs BAW dans la partie émetteur, en proposant une architecture capable de tirer profit de leurs spécificités. Le but principal est de développer un transmetteur pour des applications de réseaux de capteurs sans fils à plusieurs canaux capables de couvrir toute la bande ISM à 2.4 GHz et de garantir la compatibilité avec des standards communs comme Bluetooth ou Bluetooth Low Energy. Typiquement, les transmissions seront entre débit faible (quelque dizaine de kb/s) et débit moyen (1 Mb/s), utiliseront des modulations à enveloppe constante comme FSK ou GFSK, seront centrées sur n'importe lequel des canaux de la bande ISM et auront une portée de quelques dizaine de mètres.

Pour atteindre ces objectifs et contourner la limitation liée à la gamme de réglage réduite de l'oscillateur BAW, un émetteur en up-conversion a été utilisé. Les problèmes de spurs qui caractérisent cette architecture sont résolus en utilisant une technique de réjection basée sur un mixage à bande latérale unique et un amplificateur sélectif. Ce dernier est réalisé par la combinaison d'un amplificateur de puissance à haut rendement de type E et des résonateurs BAW, qui permet d'atteindre le filtrage des spurs tout en préservant l'efficacité énergétique. En particulier, l'amplificateur sélectif est conçu en incluant directement dans la phase de design les paramètres du résonateur, ce qui permet d'intégrer le filtre BAW dans le réseau passif de l'amplificateur. La section de synthèse de fréquence utilise une chaine composée d'une division fractionnaire suivie d'un filtrage par PLL LC et une division entière pour générer des signaux IF avec un bruit de phase comparable à celui de l'oscillateur BAW, ce qui permet de ne pas dégrader les performances de bruit à la fréquence RF.

Le transmetteur, qui permet de couvrir entièrement la bande ISM à 2.4 GHz, a été intégré dans une technologie CMOS 0.18 μm. En absence de modulation, la porteuse montre un bruit de phase très réduit correspondant à -136 dBc/Hz à 1 MHz de fréquence d'offset. Les signaux parasites liés à la fréquence IF sont inférieurs à -48 dBc et satisfont les normes internationales pour des puissances de sortie allant

jusqu'à 10 dBm, sans l'utilisation de technique de compensation d'erreurs de quadrature dans l'émetteur. Cette performance est possible grâce à la réjection apportée par le mélangeur à bande latérale unique et par l'amplificateur sélectif qui peut atteindre un rendement de 24% avec des inductances intégrées et en incluant les pertes dues au filtre BAW. L'émetteur, alimenté à une tension de 1.6 V (1.2 V pour l'amplificateur de puissance), consomme 35.3 mA pour une puissance maximale de 5.4 dBm, peut transmettre un signal GFSK à un débit de 1 Mb/s et atteint les spécifications d'occupation spectrale de Bluetooth et Bluetooth Low Energy.

Mots clés: MEMS, Résonateurs BAW, WBAN, WSN, Emetteur radio, RF CMOS

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Chapter 1

Introduction

1.1 Context

In the last decade, the advances in microelectronics enabled the implementation of wireless systems targeting long autonomies and high level of integration. Mobile phones, GPS devices, RFID are only some of the different examples of the countless devices which have become cheaper, more mobile, more distributed and more pervasive in daily life. From this perspective, the emergence of wireless sensor networks (WSN) can be seen as the latest trend of Moore's law toward the miniaturization and ubiquity of wireless devices.

Wireless sensor networks consist of many small sensor nodes distributed through an area of interest. Typically, each wireless sensor node provides sensing, computing, communication and sometimes actuation capabilities. The task of each node is to monitor the local environment, store the data and make it available to the other nodes, in order to enable the data routing up to a central base station. Such *ambient intelligence* can be applicable to environmental control of buildings, industrial monitoring, automotive and health care. Nevertheless, to enable a seamless integration of these networks in everyday life, wireless sensor nodes have to provide low-power, low volumes and low costs.

The use of MEMS technologies in combination with integrated circuits can allow an improvement of the nodes performance. In particular, Bulk Acoustic Wave (BAW) resonators provide very high quality factors, which could be exploited for achieving sharp filtering and reduced power consumption. Moreover, the small form factors of such resonators, together with the compatibility with silicon standard techniques, makes them very interesting for achieving high levels of integration.

Since the first appearance of Bulk Acoustic Wave (BAW) resonators, a large number of devices have exploited these features, demonstrating that they can be used to meet the stringent needs of wireless sensor networks. A lot of research has been done both at the block level, with the implementation of oscillators and low-noise amplifiers and at the architectural level. This has enabled the realization of several transceivers achieving extreme low-power consumption.

Nevertheless, these systems target applications using only one or few channels for implementing the wireless communication and do not provide compatibility with wide

spread standards such as Bluetooth and Bluetooth Low Energy, thereby limiting the network integration with existing technologies. At a certain point, in fact, the wireless network may need to communicate with devices like laptops and mobile phones, which can analyze the data collected by the network and provide access to infrastructures such as Wi-Fi, GSM or 3G. The 2.4 GHz ISM band is an excellent candidate to close this gap, since it can be used freely for performing the communication within the sensor network, while covering at the same time the frequency band of a widespread standard such as Bluetooth.

1.2 Aim of the project

This thesis work is part of the efforts made at the Swiss Center for Electronics and Microtechnology (CSEM) to develop a complete BAW-based transceiver capable of addressing multi-channel applications. The main overall objective fixed at CSEM was to achieve a system exploiting the use of BAW resonators in the synthesis, the receiver and the transmitter sections, while allowing to cover the whole 2.4 GHz, 80 MHz wide ISM band and being thus potentially compatible with Bluetooth and Bluetooth Low Energy.

In this context, this thesis has the aim of developing the transmitter section of such a BAW-based transceiver, by finding a suitable architecture which could take advantage of the BAW resonators. In particular, a co-integration of the BAW resonators with one of the blocks composing the transmitter is preferable, since the co-integration is a key design technique to allow achieving circuits with improved performance, as demonstrated for the LNAs in the receiver section and the local oscillators in the synthesis section.

In the first part, the radio requirements of a WSN transceiver targeting multi-channel applications in the 2.4 GHz ISM band are identified. A BAW-based transceiver implementation able to fulfill those requirements is presented. In particular, the transceiver takes advantage of a wide-IF architecture which allows keeping the BAW local oscillator at a fixed frequency, thus preserving its excellent phase noise and power consumption performance. At the same time, the wide IF covers a frequency range wide enough to allow addressing all the channels of the ISM band.

Then, two possible up-conversion architectures exploiting the use of BAW resonators are proposed to match the transceiver need of a fixed frequency BAW oscillator. The first architecture contemplates the use of BAW resonators exclusively as filtering elements for rejecting the image frequency and the spurs of the intermediate frequency resulting from the use of a double sideband (DSB) mixer. The second transmitter architecture proposes the joint rejection of a single sideband (SSB) mixer and a selective BAW-based amplifier to achieve the needed spectral purity to comply with the spurs standard requirements, while improving the transmitter efficiency.

The work is then focused on the analysis and implementation of the selective amplifier. To allow reaching good efficiencies, the use of a switching class E like amplifier is proposed. Since the integrability requirement imposes the use of integrated inductances, two different analysis approaches for a class E amplifier with realistic losses and finite DC feed inductance are compared. Afterwards, the integration of BAW res-

onators in the passive network of a class E amplifier is proposed to achieve the wanted co-design. Single ended and differential amplifier implementations are briefly described and compared to allow choosing the best possible configuration.

Finally, the implementation of the transmitter architecture is realized. The selective amplifier exploits the co-integration of a class BE cascoded power amplifier (PA) with a BAW lattice filter to provide frequency selectivity and preserve the efficiency. Moreover, the use of the BAW filter strongly relaxes the rejection requirements on the SSB mixer, thus allowing the use of a simple RC-CR phase shifter to provide the needed quadrature on the local oscillator. The final circuit is then measured to check the transmitter performance and verify the compliance with the output spectrum requirements.

1.3 State-of-the-art

In the last years a lot of effort has been devoted to the development of radio transceivers targeting wireless sensor networks. For the transmitter section two main design trends could be identified.

The first design trend led to the development of extremely low power transmitters able to achieve high overall efficiencies. These transmitters use very simple architectures to reduce the power consumption, proprietary standards based normally on a single or few channels and OOK or FSK modulations. Among them we can cite:

- The transmitters developed by T. Melly at the Swiss Federal Institute of Technology, and in particular a 10 dBm, 433 MHz, 38% efficiency FSK transmitter [1].

- A 900 MHz FSK direct modulation transmitter implemented by A. Molnar, delivering -6 dBm output power with an overall efficiency of 19%, for a data rate of 100 kb/s [2].

- The active antenna transmitter developed at the Berkeley University by Y.H. Chee, reaching an outstanding overall efficiency of 46% for an output power of 0.8 dBm, and achieving OOK modulation at a data rate up to 330 kb/s [3]. This work exploits the use of FBAR resonators in two distinct local oscillators to create two different channels at 1.9 GHz.

In the second trend more complex transmitter architectures are used, in order to provide compatibility with standards working at the 2.4 GHz such as Bluetooth or IEEE 802.15.4. Some examples are:

- A direct conversion transmitter implemented by Y.S. Eo delivering 0.5 dBm output power for an overall efficiency of 3.7% and supporting 802.15.4 250 kb/s OQPSK modulation [4].

- A double conversion transmitter developed by T. B. Cho reaching an overall efficiency of 1.4% while providing 0 dBm output power, compliant with Bluetooth 1 Mb/s GFSK modulation [5].

- A direct modulation transmitter proposed by W. W. Si achieving a maximum output power of 2 dBm with an overall efficiency of 2.8% at 1 Mb/s Bluetooth modulation [6].

At the time this thesis started, the use of a BAW filter in the transmitter chain had already been demonstrated. In [7], a bandpass ladder BAW filter is used after an EDGE power amplifier to filter the PA harmonic frequencies and the out-of-band noise caused by a $\Delta\Sigma$ modulator. The power amplifier, integrated in a 0.25 μm BiCMOS technology using SiGe-C heterojunction bipolar transistors for the first two stages and NLDEMOS for the power stage, demonstrates an output power of 32 dBm and an efficiency of 50% working at 3.6 V supply. At 28 dBm, the amplifier efficiency was 35%. Nevertheless, no real co-design was provided between the amplifier and the filter. Only standard impedance matching was used to link the amplifier with the filter.

1.4 Dissertation outline

The thesis is organized as follows:

Chapter 2 describes some basic concepts related to transmitter architectures. The fundamental functions constituting a wireless transmission are analyzed, indicating the main challenges and trade-offs concerned. Then the most important figure of merits characterizing a transmitter are presented. Finally some widely used transmitter architectures for constant envelope modulations are briefly described.

Chapter 3 introduces the reader to the design of a 2.4 GHz BAW-based transmitter. A possible wireless sensor network application which could exploit the whole 2.4 GHz ISM band is presented and its requirements are described. The BAW resonator is described deriving a simple lumped element model which can be used as a building block for the circuit design. Then, a BAW-based transceiver architecture capable of addressing these needs is presented. Two different transmitter structures based on an up-conversion scheme are proposed in order to avoid the problems of image frequency and spurs.

Chapter 4 describes the design approach used for designing a BAW-based power amplifier. The circuit side is analyzed to allow choosing the most suitable amplifier configuration to achieve the wanted co-design. Two different analysis approaches are used to study the amplifier performance in a full IC implementation and to find the optimum design point. Finally, the BAW-IC co-integration is described. Both single ended and differential implementations are investigated. The chapter ends with a differential BAW-based PA design example.

Chapter 5 details the design of the blocks which constitute the BAW-based transmitter. The description is focused on the up-conversion transmission chain and its related blocks, starting from the selective amplifier and then addressing the design of the phase shifter and the single sideband mixer. Simulation results are presented, together with design and layout considerations. This transmitter implementation allows to achieve the needed spurious signal rejection with the

use of a single stage BAW filter, thus decreasing the insertion losses, which benefits the output power and efficiency. Finally, some of the blocks composing the BAW-based transceiver frequency synthesis section are described.

Chapter 6 presents the measured results of the BAW-based transmitter. The first part describes the measurements of the selective amplifier integrated as a standalone circuit. The second part presents the measurements of the complete transceiver, including the synthesis section, to validate the quality of the RF signal. The spurious suppression mechanism is checked, together with the fulfillment of the mask requirements for signals targeting Bluetooth and Bluetooth LE compatibility.

Chapter 2

RF Transmitters

This chapter describes some basic concepts related to transmitter architectures. The fundamental functions constituting a wireless transmission are analyzed, indicating the main challenges and trade-offs. Then the most important figure of merits characterizing a transmitter are presented. Finally some widely used transmitter architectures for constant envelope modulations are briefly described.

2.1 Transmitter basics

The RF transmission can be defined as the emission of a carrier modulated by the information signal through an antenna. This apparently simple definition includes the three basic functions that every transmitter has to provide: modulation, upconversion and power amplification. The baseband information bearing the information has in fact to be transferred at the RF frequency specified for a given application, where it will be embedded in the *carrier* signal. Even though these two different functions are often carried out by the same circuit, they will initially be treated separately. Once the information signal has been translated to the RF, it has then to be properly conditioned before being fed to the antenna. Power amplification provides this latter function, by transforming the DC power supplied by the battery into the RF power needed to cover the wanted transmission range.

2.1.1 Modulation

The modulation is the process by which the parameters of a carrier waveform are modified in accordance with a low frequency signal bearing the information. The three key parameters which can be changed by the modulation process are the carrier amplitude, phase and frequency. The variations they have to undergo can be continuous or discrete, depending on the analog or digital nature of the modulating message signal. In addition to that, the carrier waveform can have an analog or digital representation, practically doubling the number of possible modulations.

Modulation schemes exhibit a general trade-off between bandwidth efficiency, power efficiency and detectability. As a consequence, the choice of the modulation type can directly impact the transmitter architecture and thus its performance. A classification

of the different modulation schemes is presented here, then the performance trade-offs are briefly explained with some examples.

Modulation schemes classification

The different modulation schemes can be classified into two main families, *continuous-wave* (CW) modulation and *pulse wave* modulation. Here their main features are summarized:

- **CW modulation** uses a sinusoidal waveform carrier, whose amplitude or angle can be varied in accordance with the analog or digital message signal. In case of an analog information signal, we have respectively *amplitude modulation* (AM) and *phase modulation* (PM) or *frequency modulation* (FM) depending on whether the phase or the frequency of the carrier signal are modified. Their digital counterparts are represented by amplitude shift keying (ASK), phase shift keying (PSK) and frequency shift keying (FSK) modulation respectively.
- In **Pulse modulation** the carrier consists of a periodic sequence of rectangular pulses. In case of *analog pulse modulation*, the amplitude, duration or position of a pulse is varied with the sample value of the analog signal (PAM, PDM and PPM respectively). In *pulse code modulation* (PCM), the standard digital form of pulse modulation, the process is similar to PAM but uses a set of discrete amplitudes.

Power efficiency: constant vs. variable envelope modulation

An alternative classification can be used to divide modulation types into *constant envelope* and *variable envelope* modulation. This is very useful because modulation based on constant and variable envelope signals present highly different power efficiencies, i.e. different spread of the RF power into adjacent channels, when they experience nonlinearities in the amplification chain.

To simply demonstrate that, it is sufficient to apply to a constant envelope and variable envelope signals, an amplification with the same memoryless nonlinearity, for example a third order nonlinearity expressed as:

$$y(t) = k_3 x(t)^3, \tag{2.1}$$

where $x(t)$ is the modulated carrier. In case of constant envelope signals:

$$x_{ce}(t) = A\cos\left[\omega_c t + \phi(t)\right], \tag{2.2}$$

where A is the envelope amplitude. A variable envelope signal, instead, presents an amplitude term which depends on time. In case simultaneous angle and amplitude variations are performed, the RF signal takes the following form:

$$x_{ve}(t) = A(t)\cos\left[\omega_c t + \phi(t)\right]. \tag{2.3}$$

Substitution of the constant envelope signal in (2.1) gives the following expression:

$$y_{ce}(t) = \frac{3k_3A^3}{4}\cos\left[\omega_c t + \phi(t)\right] + \frac{k_3A^3}{4}\cos\left[3\omega_c t + 3\phi(t)\right]. \tag{2.4}$$

Consequently, if a constant envelope signal is amplified by a high efficiency nonlinear amplifier, the products coming from nonlinearities will lie at harmonics of the carrier frequency, which are normally widely spaced from one another. For this reason, even if the bandwidths of the nonlinear products are bigger than that of the original signal (Carson's rule), the signal spectrum centered around ω_c will not be affected. This can be intuitively understood by thinking that in case of constant envelope modulation the signal information resides in the position of the zero-crossing points only, which are not affected by amplitude nonlinearities.

On the other hand, for variable envelope modulations, nonlinear amplification will generate components centered on the carrier frequency and with a spectrum broader than the wanted signal (since the spectrum of $A(t)^3$ is generally broader than that of $A(t)$), causing *spectral regrowth* [8]. For this reason variable envelope modulation are less power efficient.

Bandwidth efficiency and detectability

Another important feature of a modulation scheme is the bandwidth efficiency, which estimates the spectral occupancy of the ideal modulated signal.

An example can be given by analysing constant envelope digital frequency modulation, which encode the information into a binary or more generally a M-ary baseband signal representing the carrier frequency variations over time. The information signal, having a digital nature, presents steep transitions in the time domain, which correspond to high spectral occupancy, i.e. low bandwidth efficiency. This is the case for example in a binary FSK, where the carrier signal is modulated by a square wave over two discrete frequency values deviated $\pm\Delta f$ from the unmodulated carrier frequency value.

To mitigate this problem, filtering can be performed on the baseband data in order to smoothen the sharp edges and decrease the needed bandwidth. A possibility is to use Gaussian frequency shift keying (GFSK), which employs a Gaussian filter to reduce the spectral occupancy of the signal. Figure 2.1 depicts the spectrum of a 1 Mb/s FSK modulated signal (with frequency deviation $\Delta f = 250$ kHz, i.e. modulation index mi $= 2\Delta f / f_{mod} = 0.5$) compared to a GFSK modulation with time-bandwidth product (BT) of the Gaussian filter equal to 0.5. The plot clearly shows how the Gaussian filtering reduces considerably the signal bandwidth, thereby decreasing the disturbances over nearby channels. The lower the BT product is, the narrower the signal spectrum will be.

Unfortunately, the bandwidth reduction introduces a new problem in time domain. Owing to the filtering effect, in fact, the filtered baseband signal pulses are no more confined to their symbol time, hence spreading over adjacent symbol intervals. This causes increasing *intersymbol interference* [9] and consequently higher probability of errors in the detection as the value of BT is reduced. As a consequence, an additional trade-off between detectability and spectral compactness arises.

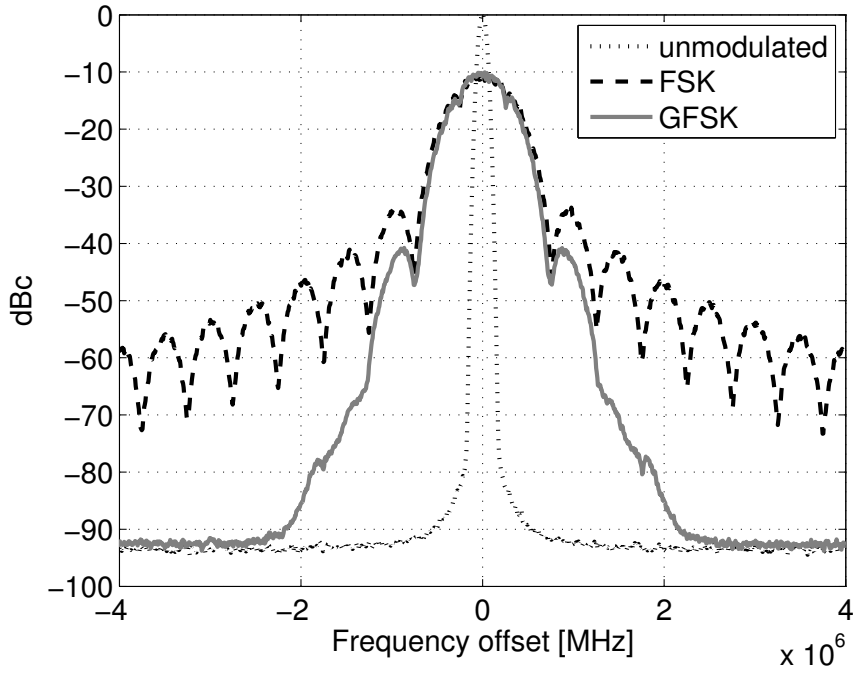


Figure 2.1: 1Mb/s FSK versus GFSK spectra, normalized to the unmodulated carrier power. Modulation index mi = 0.5, BT = 0.5.

2.1.2 Upconversion

The baseband signal is normally processed at low frequencies to reduce the power consumption. Nonetheless the transmission requires emitting the information signal around a precise RF carrier frequency. Frequency upconversion is the process which involves the translation of the baseband signal spectrum at the carrier frequency.

Upconversion is needed for different reasons, but probably the fundamental one is that the signal cannot simply be transmitted at the baseband by an antenna with reasonable dimensions. In fact, to achieve a sufficient gain, the antenna size should be comparable with the signal wavelength, calling thus for high transmission frequencies, at least for hand-held devices.

Moreover, in order to regulate the continuous emerging applications and limit the interferences between devices using different communication systems, the frequency bands are strictly allocated by the international regulations such as the Federal Communication Commission (FCC) and the European Telecommunication Standards Institute (ETSI). This practically forces one to design for a certain RF frequency band depending on the chosen application.

2.1.3 Power amplification

Power amplification represents the last step in the transmission chain. It covers the role of conditioning the RF signal in such a way that the low impedance (normally 50 Ω) antenna is driven correctly and with the wanted power. A power amplifier is characterized by mainly four different figures of merit: *output power*, *efficiency*, *gain*

and *linearity* (see Appendix A). Trade-offs between these different figures of merit exist, driving the choice of the amplifier topology depending on the system requirements.

Power amplifiers are mainly classified as linear and non-linear amplifiers. However, since in reality all the amplifiers present some nonlinearities, the proposed classification is based on how the power stage transistor is driven. Two main families are identified: in the first one, the swing of the input waveform is assumed not to be large enough to push the transistor into the linear region. In the second family, on the contrary, the driving waveform (ideally a square wave) is large enough to switch the transistor on and off during operation. These two families are briefly described here, while for more detailed information the reader is requested to refer to Appendix A.

Non switching power amplifiers

The first family of power amplifiers includes all the amplifiers driven with a relatively low swing input signal. The different classes (from class A to C) are characterized by different values of the transistor conduction angle, α, during operation. The conduction angle indicates the portion of the RF cycle, normalized to 2π, for which conduction occurs. All these amplifiers are basically implemented with the same circuit configuration and the class of operation is simply set by controlling the DC value of the input waveform.

By using a simple analysis to calculate the amplifier output current at different harmonics of the input signal (see Appendix A), a clear trade-off between efficiency and linearity appears. Class A amplifiers, generally identified as linear amplifiers having a conduction angle equal to 2π, are characterized by lower efficiency, ideally equal to 50%. Lowering the conduction angle causes more nonlinearities to arise, together with an increase of efficiency. For the extreme case of a conduction angle near to zero degree (amplifier in deep class C), the drain efficiency reaches ideally 100%. The amplifier efficiency versus conduction angle curve is sketched in Figure 2.2, together with the normalized output power and the DC power drawn from the supply. From the plot, another interesting trade-off appears: high efficiencies can be reached at lower conduction angles at the cost of low output power, since more DC power is transferred at harmonics of the input signal frequency.

A particular power amplifier which is part of this family is the class F amplifier, which is implemented differently from the other reduced conduction angle amplifiers. While being driven with the same conduction angle of a class B, it uses series resonators tuned at odd harmonics of the signal frequency to square the drain voltage and thus increase the efficiency (Appendix A). The trade-off with linearity still remains, but this amplifier allows achieving higher efficiencies and output powers with respect to a class B, making it a very interesting solution for low-power consumption transmitters.

Switching power amplifiers

From the study of the first amplifier family it can be seen that the efficiency is improved by reducing the overlap existing between the drain voltage and current waveforms, thus minimizing the power dissipated by the transistor. This concept is pushed to the limit by the switching power amplifiers, for which the input waveform amplitude is high,

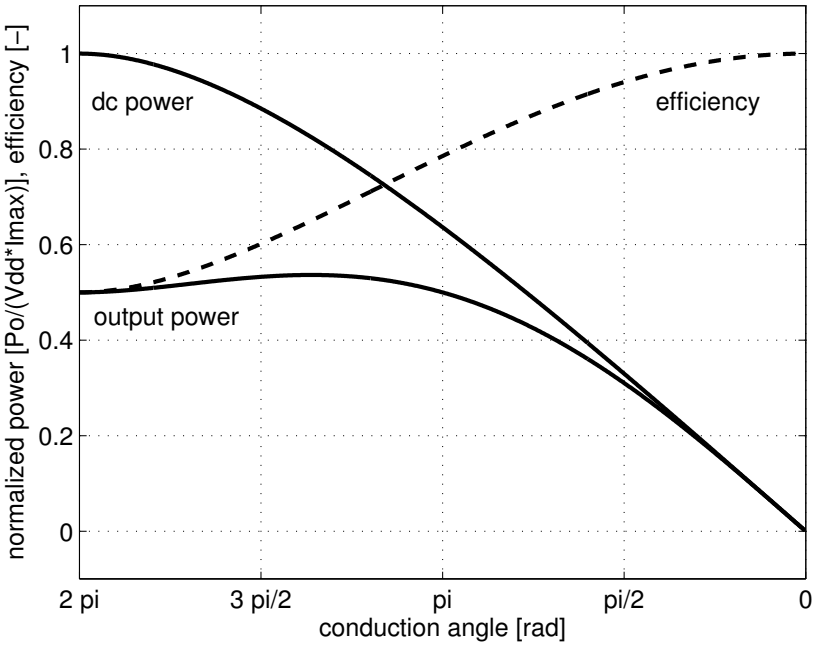


Figure 2.2: Amplifier power and efficiency curves while changing the conduction angle.

which allows one to assume that the input transistor acts as a simple switch. Consequently, no overlap between drain current and voltage waveform occurs and an efficiency of 100% can be ideally achieved. In these conditions the output power becomes, for a given load, a function of the supply voltage only. Nevertheless, due to the highly nonlinear behavior of the switch, significant DC power is transferred to harmonics of the input signal, thus requiring a tuning network to avoid this power being lost in the load resistor.

In between the switching amplifiers we can mention class D power amplifiers, which use a complementary amplifier similar to a digital inverter and class E power amplifiers [10], which exploit a passive network to achieve a higher efficiency with a single transistor amplifier. The most important difference in between these two families is the way the switching action is performed, which determines the amplifiers maximum efficiency in real implementations. Detailed explanation of class E amplifiers will be given later, while for the class D analysis the reader is requested to refer to Appendix A.

2.2 Transmitter requirements

Depending on the target application, the transmitter must satisfy different requirements. Some of them are fixed by the international or national regulations, while the others are determined by the particular application and operation condition. The most important requirements are the transmitter output power, the overall transmission efficiency, the maximum data rate achievable and the output spectrum limitations.

2.2.1 Output power

The signal at the output of the power amplifier undergoes different transformations before being captured by the receiver antenna and is thus a function of different circuit and environmental parameters.

The signal power needed at the output of the power amplifier can be calculated by inverting the Friis equation:

$$P_o = \left(\frac{4\pi}{\lambda}\right)^2 \frac{R^n}{\eta G_T G_R} P_{rx}. \tag{2.5}$$

$\lambda = c/f$ is the signal wavelength, while the term R^n represents the distance between the transmitter and receiver, weighted by the path loss exponent n, which gives an indication of the path losses in different environments. For free space $n = 2$, while for indoor environments $n = 3$ or $n = 4$ is more appropriate. G_T and G_R represent the transmitter and receiver antenna gains respectively, which take into account the antenna efficiencies and directivities ($G = \eta_{\text{ant}} D$). Finally, η takes into account the impedance mismatches between the antennas and the circuit and P_{rx} is the receiver sensitivity.

2.2.2 Efficiency

The efficiency is an important requirement for a transmitter aimed at portable devices. In fact it directly impacts the battery lifetime and thus the autonomy of the device. The parameter used to evaluate the efficiency of a transmitter is the *overall efficiency*, which takes into account the consumption of all the circuits making up the transmitter:

$$\eta_{ov} = \frac{P_o}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,BLK,i}}, \tag{2.6}$$

where P_o represents the output power at the target frequency.

2.2.3 Data rate

The maximum data rate achievable depends on the bandwitdh which is allocated for the transmitted signal. The data rate upper bound, or channel capacity, is given by the Shannon formula:

$$C = B \log_2(1 + \frac{S}{N_0 B}), \tag{2.7}$$

where B is the channel bandwidth, S represents the signal power and $N_0/2$ is the two sided power spectral density of the Gaussian noise. Even if practical modulations only achieve a fraction of C, all the circuits composing the transmitter should provide sufficient bandwidth to perform modulation at data rates equal or higher than the channel capacity.

2.2.4 Emission spectrum requirements

The RF signal emitted by the antenna has to comply with a series of rules imposed by wireless regulations. The *modulation mask*, for example, fixes the limit under which the transmitted spectrum must lie. In addition to that, some standards use also the *adjacent channel power* requirement, which represents the transmitted power integrated over the adjacent channels and can be defined relative to the carrier power or in absolute values. Moreover, the maximum values allowed for harmonics and spurs are specified, since they could interfere with other devices causing problems like receiver desensitization. Finally, in some particularly demanding applications, the maximum output thermal noise is limited, since it raises the noise floor of the receiver causing reduced signal-to-noise ratio.

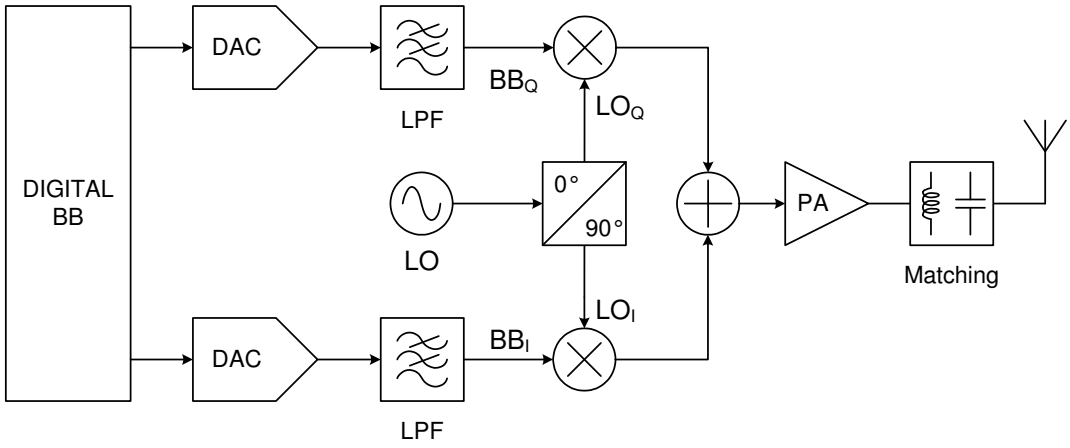


Figure 2.3: Direct conversion transmitters block diagram.

2.3 Transmitter architectures

Due to power efficiency considerations and the relatively low data rate needed, the networks aiming to cover sensor applications use constant envelope modulations [11]. This section provides an overview of the different transmitter architectures that can be used for constant envelope modulation schemes, highlighting their advantages and disadvantages.

2.3.1 Direct conversion architecture

In direct conversion transmitters the modulated signal coming from the baseband (BB) modulator is directly translated to the RF carrier frequency. Both the modulation of the carrier signal and the upconversion are performed by the same circuit, a single sideband (SSB) mixer, as depicted in Figure 2.3. Single-sideband upconversion is used to avoid the image frequency appearing at the mixer output, increasing the signal to noise ratio (SNR) after demodulation. The modulator is then followed by a power amplifier and a network used to match the antenna impedance. Matching is necessary to provide maximum power transfer to the antenna and perform attenuation of the harmonic components generated by the amplifier nonlinearities.

The direct conversion transmitter is extremely versatile and can support any modulation scheme, but the utilization of such architecture can be limited by disturbances that can degrade the LO spectrum. The RF amplifier signal, can in fact leak into the chip and induce disturbances on the oscillator. This phenomenon, known as *injection pulling* [8], is possible because the frequencies of the LO and the RF signal at the power amplifier output are not exactly the same during modulation. When the frequency of the injected signal is near that of the oscillator, the LO output is affected proportionally to the magnitude of the disturbing tone, eventually locking to the frequency of the injected signal if it reaches sufficient power.

Another potential problem of the upconversion architecture is represented by the amplitude and phase mismatches of the quadrature baseband (BB_I and BB_Q) and local oscillator (LO_I and LO_Q) signals. The presence of such errors cause a reduced

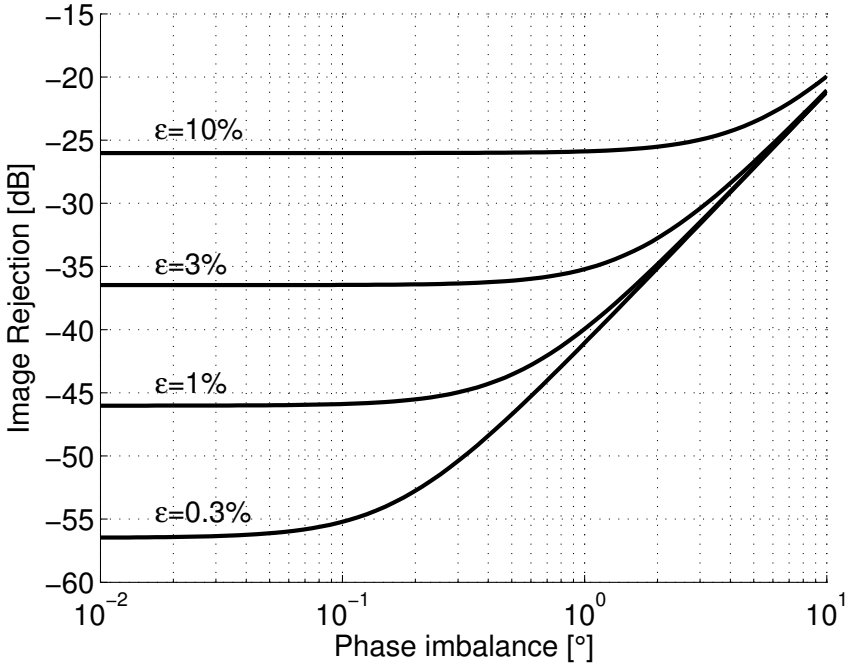


Figure 2.4: Theoretical IRR versus phase and amplitude imbalances of the input quadrature signals.

rejection of the image spectrum, forcing in certain cases the use of a bandpass filter before the power amplifier. By assuming low relative phase $\Delta\varphi$ and amplitude ε errors, the achievable image rejection can be approximated with the following formula [8]

$$IRR \approx \frac{\varepsilon^2 + \Delta\varphi^2}{4}, \tag{2.8}$$

where $\varepsilon = \sqrt{\varepsilon_{LO}^2 + \varepsilon_{BB}^2}$ represents the relative amplitude mismatches and $\Delta\varphi = \sqrt{\Delta\varphi_{LO}^2 + \Delta\varphi_{BB}^2}$ is the phase error expressed in radians.

Figure 2.4 depicts the achievable image rejection for different phase and amplitude imbalances. From the plot it can be seen that high image rejections (e.g. 40 dB IRR) are achievable only with precisely controlled quadrature signals, with errors of the order of 1% in the amplitude and 1° in the phase respectively. Moreover, since the errors add quadratically, the higher imbalance tends to dominate the IRR degradation. This is the case for example, for signals generated with passive RC shifters, for which the amplitude errors can be generally more important than the phase errors.

2.3.2 Two-step architecture

The pulling phenomenon can be avoided if the LO and the RF frequencies are sufficiently far from one another, in such a way that the LO is insensitive to the PA disturbances. The two step transmitter ensures this condition by shifting the LO and the RF by an amount which corresponds to the intermediate frequency (IF). The baseband signal is thus at first upconverted to the IF and then translated to the RF by

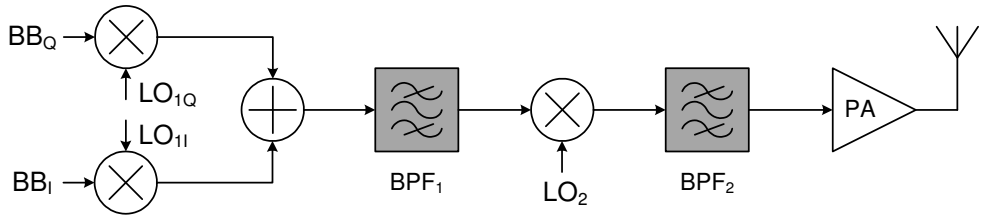


Figure 2.5: Block diagram of a two-step transmitter. The baseband section corresponds to that depicted in Figure 2.3.

multiplication with a second LO, as depicted in Figure 2.5. Quadrature modulation is performed at the first upconversion, since the quadrature generation provides higher I and Q matching, and thus higher image rejection, at low frequencies. This represents another advantage with respect to direct conversion architectures. Additional by-pass filtering may be needed to suppress the IF harmonics and the signal image after the second mixing, depending on the output spectrum requirements.

2.3.3 Direct modulation architecture

The direct modulation architecture allows translating the baseband modulated signal directly around the target carrier frequency, similar to a direct conversion transmitter. Instead of using a mixer to upconvert and modulate the carrier, direct modulation transmitters use a phase locked loop PLL, as depicted in Figure 2.6, to modulate the local oscillator.

The PLL is a negative feedback system that keeps the error signal after the phase / frequency detector equal to zero, thus forcing the oscillator frequency to be N times the reference frequency. Modulation of the reference frequency or the divided feedback frequency causes the LO transferring the modulated spectra around the carrier RF frequency, thus performing upconversion. Figure 2.6 depicts the second method, where the modulation is performed by controlling a $\Delta\Sigma$ modulator with the baseband datastream, while the modulator in turn drives the PLL feedback division ratio.

Contrary to the direct upconversion transmitter, the direct modulation transmitter is less prone to injection pulling, because the modulated LO signal is directly fed to the power amplifier and thus the RF and LO frequencies always correspond exactly during the modulation process. Apart from the lower sensitivity to the injection pulling, the direct modulation by PLL presents other interesting advantages which makes it a very competitive solution in today's RF circuits. The first is the noise suppression capability. All the noise contributions of the blocks used inside the PLL are filtered (in a way which depends on their position inside the loop) so that the noise of the synthesized signal can be kept to very low level. Another interesting advantage is that, by using the direct modulation by PLL, the number of nodes at RF is reduced to the VCO outputs and the amplifier chain only, thus minimizing the transmitter power consumption. Moreover, it avoids the use of quadrature signals on the LO, simplifying the transmitter and further reducing the power consumption.

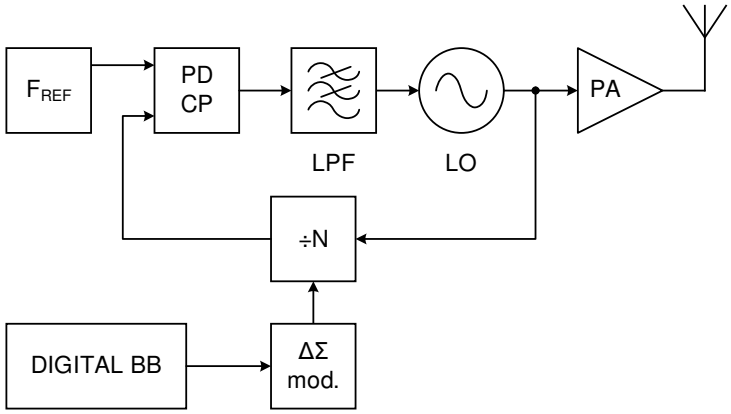


Figure 2.6: Direct modulation transmitter block diagram.

2.4 Summary

A brief introduction to the RF transmitter was presented in this chapter. The three basic functions that a transmitter has to provide, modulation, up-conversion and amplification have been described. Then the basic transmitter requirements have been introduced. Finally, the most popular architectures used for constant envelope modulation have been briefly described. To give an insight to the challenges involved in the transmitter design, throughout the chapter the attention has been focused on the main advantages, disadvantages and trade-offs related to each of the treated points.

Chapter 3

BAW-based Radio

This chapter aims to introduce the reader to the design of a 2.4 GHz BAW-based transmitter. After a short introduction of wireless sensor networks, a possible application which could exploit the whole 2.4 GHz ISM band is presented and its requirements are described. The BAW resonator is described deriving a simple lumped element model which can be used as a building block for the filter design. Then, a BAW-based transceiver architecture capable of addressing multi-channel WSN applications is presented. Two different transmitter structures based on an up-conversion scheme are proposed in order to match best the use of a fixed frequency BAW oscillator and to avoid the problems of image frequency and spurs.

3.1 Wireless Sensor Networks

A wireless sensor network (WSN) consists of many small sensor nodes distributed throughout an area of interest. Each node monitors its local environment, processes the collected data and stores it. The sensor nodes then share this information via a wireless link and route it, typically with a multi-hop communication scheme, to a central base station [12, 13, 14].

The application fields of wireless sensor networks are numerous and can range from environmental control of buildings to industrial monitoring, automotive and health care applications. The wide spread of these networks in everyday life can however only be made possible by providing small (< 1 cm^3) and cheap (< 1 \$) network nodes [12]. Moreover, these nodes must consume low power, in order to reduce the battery replacement needs.

A battery powered wireless sensor node working at low data rate (LDR) (typically 10 kb/s) and with a maximum transmission range of 10 m should consume an average power level of the order of $10-100$ μW to provide autonomies over two to five years [11, 15]. This value roughly corresponds to the power that can be delivered by a storage or an harvesting device having a volume of about 1 cm^3 [16]. Energy scavenging represents an interesting solution to enable the node self-powering. At the time of starting this thesis, the complete autonomy of a sensor node had already been demonstrated under particular favorable environmental conditions and for volumes higher than the targeted 1 cm^3 [17].

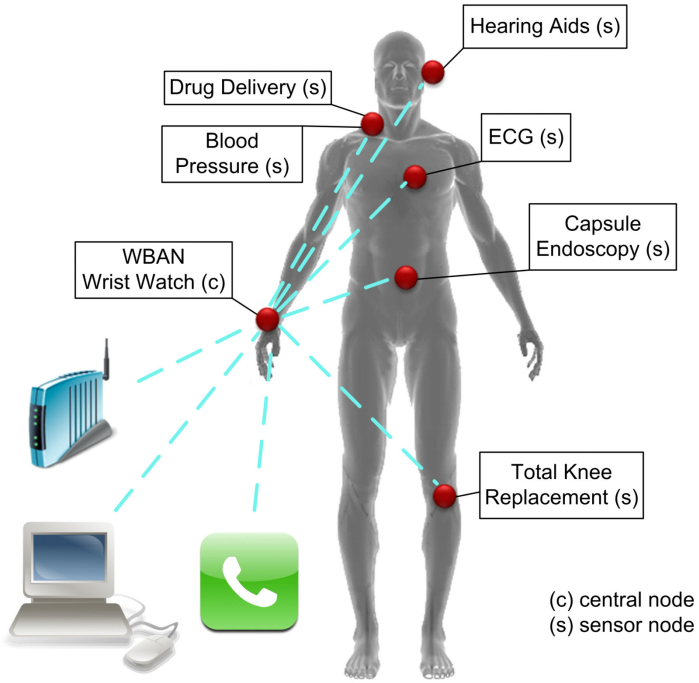


Figure 3.1: Typical scenario of WBAN applications.

Power consumption reduction is achieved in wireless sensor applications with hardware and software co-design. In fact, as the circuit power consumption in both active and sleep mode plays an important role in determining the node consumption, protocols providing low-duty cycling and short wake-up preambles have also to be used to achieve the highest possible network energy efficiency [14].

Wireless sensor networks are often composed of circuit and protocols that does not offer the compatibility with widespread standards, thereby limiting the wireless network potential. At a certain point, in fact, the wireless network may need to have a gateway towards the external world, which could enable for example to communicate with devices like laptops and mobile phones. To be easily accessible and to target high volume applications, wireless sensor networks cannot hence leave out of consideration the compatibility with standards such as Bluetooth and Bluetooth Low Energy (LE) [18]. As a consequence, the possibility of the sensor nodes (or a least some of them) to communicate with a Bluetooth or Bluetooth LE device is a need, even if this standard does not represent the ideal communication for applications targeting years of autonomy. The next section describes a possible application scenario where the Bluetooth compatibility can be exploited.

3.1.1 A possible scenario: wireless body area networks

Wireless body area networks (WBAN) aim to cover applications in the medical and healthcare sectors, as for example the monitoring of patients' physiological parameters [19] or the remotely controlled drug delivery [20], but also sport and entertainment functions.

Among the possible network topologies that can be used to address these applications, one of the most interesting from both the power consumption and the complexity point of view relies on a mixed solution which uses two different network levels to manage the data routing [20, 21]. A short range personal area network (typically a WBAN) with a transmission range of some meters uses a simple star topology to manage the data transfer with the different nodes implanted or located on the body. Then a higher range self-configurable local area network connects the central nodes of each WBAN providing multi-hop routing towards the base station. The possibility to perform nodes localization may also be considered [22].

Figure 3.1 depicts an example of this scenario, where the wristwatch plays the role of the WBAN central node. For simplicity the figure shows only one WBAN, but in general more than one hop from one WBAN central node to another could be needed for the data packet to reach the base station (e.g. a laptop or a phone).

Each of the WBAN central nodes needs thus to assure compatibility with both the sensor network and the Bluetooth devices. For miniaturization reasons, this has to be preferably provided by one single radio. As a consequence, the WSN will work in the same band as Bluetooth and the radio requirements will be set in such a way to be compatible with this standard.

Nonetheless, a modified protocol with the aim of increasing the efficiency with respect to Bluetooth may still be used for data transfer within the sensor network. A possible example of such a protocol is described next.

3.1.2 Example of a WSN protocol

In case of rare signaling traffic, state-of-the art low-power radio protocols for WSN use carrier sense multiple access (CSMA) with preamble sampling [23] to manage the data communication. The network nodes wake-up regularly, in accordance to the needed system latency, to sense if an activity is present on a predetermined channel. This is normally done by looking at the received signal strength indicator (RSSI). In order to be detected by a receiver node, the transmitter node has to emit a preamble slightly longer than the interval between two successive wake-up. Once this connection has been established, the transmission of the actual data can be performed.

For more frequent and regular traffic, on the other hand, nodes which are already aware of each other can exchange data packets in a synchronized way using spatial time division multiple access (TDMA). By exploiting for example a 1 MHz wide channel, the transmission can be done at the peak data rate of 1 Mb/s in such a way to reduce the time for which the radio is active. Moreover, this technique allows to get rid of the TX preamble, thereby reducing the power consumption [23]. The maximum idle time between two transmissions is determined by the accuracy of the nodes real time clocks (RTC) and by the maximum tolerable listening time. To give an example, with a time accuracy of ± 100 ppm and a listening time of 0.2 ms for the RSSI, the maximum interval between two subsequent transmissions is equal to 1 s.

In WBAN and WSN applications the propagation conditions (e.g. the transmission range) can dynamically change with time, thereby impacting the link budget. Once these variations are detected, for example with the help of a RSSI, they can be compensated by regulating the output power of the transmitting node. However, this

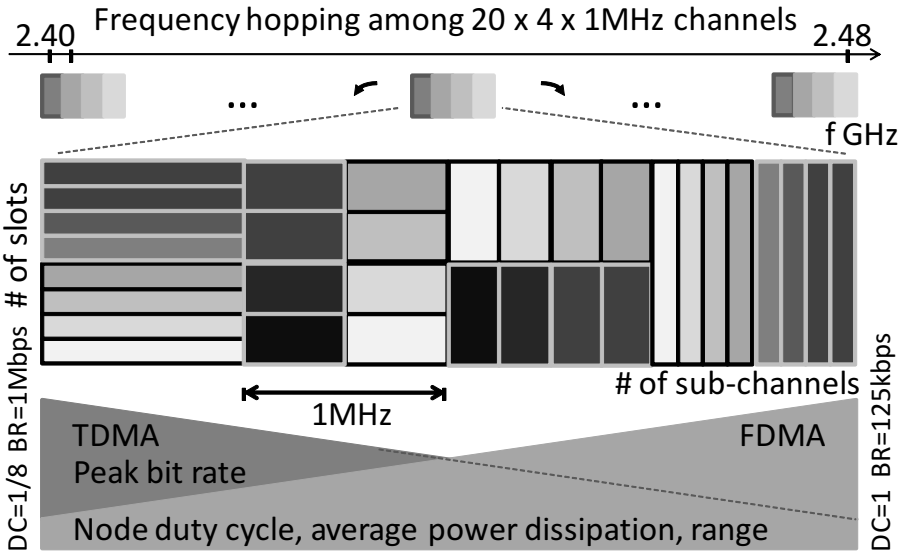


Figure 3.2: Examples of possible channel partitioning with TDMA and FDMA for dynamic adjustment of the node sensitivity.

technique could be insufficient for wireless sensor nodes, owing to the low maximum transmit power, which is bounded by volume constraints. Consequently, maintaining a reliable link budget also needs an adjustment of the receiver node sensitivity, which can be achieved by changing the channel bandwidth.

Figure 3.2 shows an example of a possible re-utilization of the ISM 1 MHz wide channels to provide a discrete adjustment of the node sensitivity by combining TDMA with frequency division multiple access (FDMA) [24]. The proposed access method is implemented on four adjacent channels which can be replicated 20 times to cover the whole 80 MHz wide ISM band and enable frequency hopping for improved co-existence. In this example, let us assume that:

- A signal requiring a transfer data rate of 125 kb/s (for example a low quality audio signal) has to be transmitted between two synchronized nodes.
- The same signal data can be transmitted in short bursts at higher data rates (up to 1 Mb/s) by duty cycling the radio.
- The peak power consumption is independent of the data rate.

Depending on the propagation conditions, TDMA, FDMA or a mix of the two can be used to perform the data transfer. In case of best propagation conditions (e.g. short transmission range), the signal can be transmitted with TDMA in the first channel, at a data rate of 1 Mb/s. The radio duty cycle, obtained dividing the original signal data rate by the transmission data rate, is equal to 1/8. As a result, eight different time slots can be allocated. In case of the worst propagation conditions (e.g. longest transmission range), pure FDMA can be used in the fourth channel. A bandwidth as low as 125 kb/s is chosen (allowing to define 8 sub-channels), thus requiring to

transmit over all the 8 time slots. The second and the third channels combine TDMA and FDMA and are used for intermediate propagation conditions.

By moving from the first channel to the fourth, the node efficiency is thus traded with the transmission range.

3.1.3 The Bluetooth standard

As already stated previously, the sensor nodes have to provide compatibility with Bluetooth. Since this thesis focuses on the transmitter side, the Bluetooth requirement for the transmitter section are briefly described next.

Bluetooth

Bluetooth is a wireless technology standard originally developed by Ericsson in 1994, as an alternative to RS-232 cabled transmission. It addresses data transfer over relatively short distances, from fixed or mobile devices, targeting an extremely wide range of applications which span from the simple data transmission between PCs and peripherals or cell phones, to the link between medical sensor and telehealth devices. Bluetooth is based on a frequency-hopping spread spectrum radio technology working on the Industrial, Scientific and Medical (ISM) 2.4 GHz short-range radio frequency band, in the range 2400−2483.5 MHz.

In standard mode, Bluetooth uses a Gaussian frequency shift keying (GSFK) modulation scheme at a datarate of 1 Mb/s, with modulation index in between 0.28 and 0.35. Three different classes are defined, depending on the RF power provided by the transmitter at the maximum power setting:

- class 1 radio: 0 dBm $\leq P_{o\_\max} \leq +20$ dBm.
- class 2 radio: -6 dBm $\leq P_{o\_\max} \leq +4$ dBm.
- class 3 radio: $P_{o\_\max} \leq 0$ dBm.

The transmitter output spectrum should comply with a relative mask requirement which limits the frequency occupation to -20 dBc at ± 500 kHz offset from the central frequency. In addition to that, adjacent channel power (ACP) requirements are specified. The ACP is defined as the sum of the power, measured with a resolution bandwidth RBW = 100 kHz, in a 1 MHz bandwidth. Maximum ACP of -20 dBm and -40 dBm are required for channels corresponding to $|M - N| = 2$ and $|M - N| \geq 3$ respectively. M defines the number of the channel used for the transmission and N the channel on which the measure is performed.

Bluetooth Low Energy

Bluetooth LE was introduced in the Bluetooth Specification Version 4.0, in December 2009. The basis of the idea of Bluetooth LE was to enhance devices already using Bluetooth technology with the availability of new coin-cell battery powered wireless

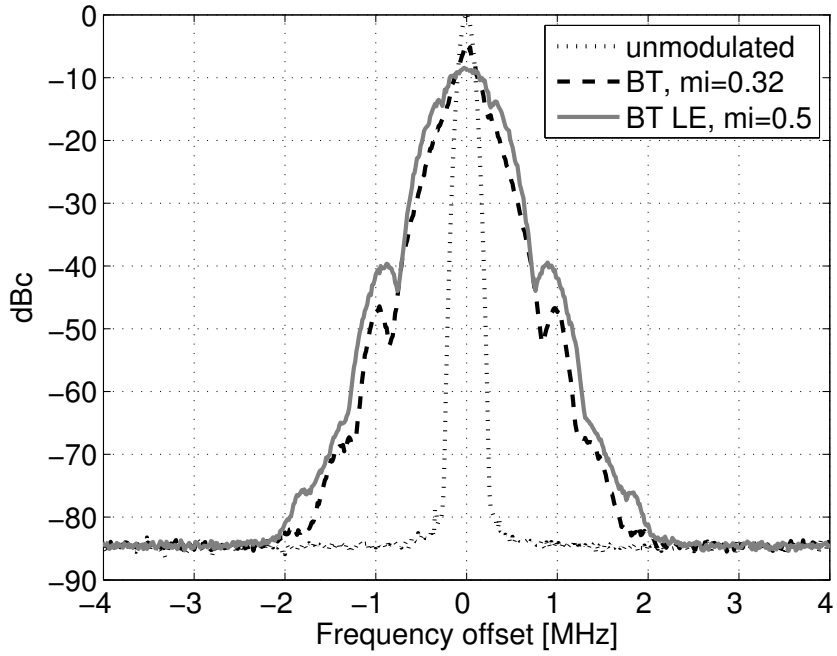


Figure 3.3: Examples of Bluetooth and Bluetooth Low Energy modulation spectra, normalized to the unmodulated carrier power.

products and sensors. This is to better target low cost and low power wireless connectivity in applications such as the health care, sports and fitness, security, and home entertainment.

The main modifications which concern the transmitter section with respect to the Bluetooth 1.2 standard are summarized below:

- 40 channels available in the 2.4 GHz ISM band, which corresponds to a channel spacing of 2 MHz.
- Output power at the maximum power setting -20 dBm $\leq P_{o\_\max} \leq +10$ dBm.
- Higher modulation index, in a range between 0.45 and 0.55.
- Relaxed in-band spurious emissions. Absolute values of -20 dBm and -30 dBm of adjacent channel power are required, measured for $|M-N| = 2$ and $|M-N| \geq 3$ respectively. No relative mask requirement is present.

Figure 3.3 compares the Bluetooth and Bluetooth LE spectra, for typical modulation index of 0.32 and 0.5 respectively. Table 3.1 summarizes the specifications of the two standards with focus on the transmitter requirements.

Table 3.1: Bluetooth and Bluetooth LE TX specifications.

Specification	BT	BT LE	Unit	comments
Channels (CH)	79	40	-	-
Ch. centr. freq.	$2402 + k$	$2402 + 2k$	MHz	$k = 0, ..., \text{CH} - 1$
Channel spacing	1	2	MHz	-
Modulation	GFSK	GFSK	-	BT=0.5
Datarate	1	1	Mb/s	-
Mod. Index	0.28−0.35	0.45−0.55	-	-
Rel. mask	−20	−	dBc	at ±500 kHz offset
ACP	−20	−20	dBm	$\lvert M - N \rvert = 2$
ACP	−40	−30	dBm	$\lvert M - N \rvert \geq 3$

3.2 Radio requirements

Wireless sensor network applications do not only need reduced power consumption, but also improved performances and great flexibility. This can allow the same network infrastructure to manage data requiring considerably different data-rates, thereby enabling at the same time applications spanning from the health care to the sport and entertainment. By taking into account the considerations made during this chapter, the following requirements can thus be delineated for a WSN node targeting multiple applications:

- **Time/frequency references:** accurate and stable time and frequency reference is needed for TDMA and FDMA in order to enable long idle time and precise channel selection.

- **Turn on time:** short turn on time allows the radio to switch on as shortly as possible from a low-power idle mode, decreasing the power consumption.

- **Phase noise:** providing a low phase noise far from the carrier is important, in particular when reduced channel spacing are used (see the FDMA example), since in this condition the adjacent channel rejection is phase noise limited.

- **Data rate:** high data rate allows low duty cycle, which impacts positively the node power consumption when the required average data rate is moderate. Moreover, having the possibility to perform fast data transfer can enable the transmission of audio or low quality video signals. A maximum data rate of 1 Mb/s will be targeted to ensure the compatibility with Bluetooth.

- **Modulation scheme:** constant envelope modulation schemes will be used, since they enable nonlinear and thus more efficient amplification. GFSK modulation has to be provided to maintain the compatibility with Bluetooth, but other phase or frequency modulations are possible, provided the baseband has sufficient flexibility to implement them.

- **Transmitter output power:** in the scenario described in Section 3.1.1 it is necessary to provide a sufficient output power to enable the connectivity between different WBAN. This can be achieved by ensuring a transmission range of several meters. To cover a maximum range of about 20 to 30 m, a 2.4 GHz communication system with receiver sensitivity of -75 dBm requires a transmit power of 5 to 10 dBm in indoor environment (see Figure 3.4). Moreover, the output power should be made adjustable to cover different transmission ranges and environmental conditions.

- **Transmitter efficiency:** is a very important requirement for a WSN node, impacting the battery lifetime. Consequently, a good balance has to be found between the improved performance needed for a flexible wireless sensor node and its overall efficiency.

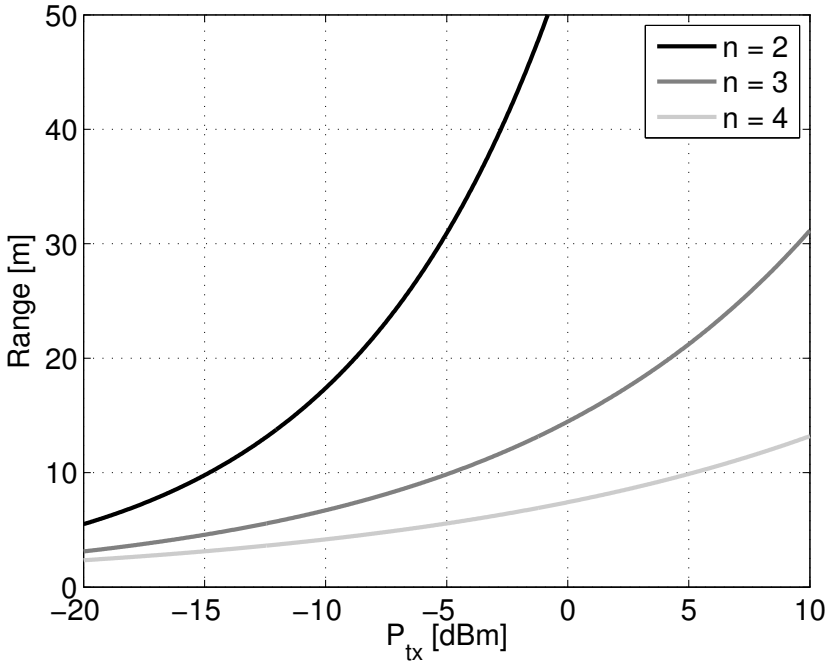


Figure 3.4: Transmission ranges of a 2.4 GHz communication system, for a receiver sensitivity of -75 dBm and different environmental conditions (n is the path loss exponent).

- **Output spectrum requirements:** the Bluetooth and Bluetooth LE spectrum requirements will be used to validate the transmitter output spectrum, together with the international regulations for the 2.4 GHz ISM band.

3.3 Bulk Acoustic Wave resonators and filters

Bulk Acoustic Wave (BAW) resonators and filters have been studied intensively for more than two decades, but their use in mobile and wireless systems started only quite recently, as an answer to the limitations of Surface Acoustic Wave (SAW) resonators for high frequency and high performance applications. SAW devices presented some important limitations such as the need of sub-micron lithography, dedicated small wafer size, expensive non-silicon substrates and poor power handling characteristics [25]. On the other hand BAW resonators promised small form factors, excellent performances and low frequency temperature coefficient (TCF), a very important advantage for accurate narrow-band filters. Finally, the additional compatibility with silicon standard techniques allowing IC integration and low-cost manufacturing made the BAW resonators very interesting devices for high levels of integration [26].

At the time this thesis is written the performance and miniaturization gap between SAW and BAW has been reduced and even completely filled for frequencies up to about 2.5GHz, mainly thanks to the use of temperature compensated SAW (TC-SAW). Nonetheless the BAW resonators are maintaining their leading role for the high end market because of their superior performance for higher frequencies, full CMOS compatibility and good power handling capabilities.

3.3.1 BAW resonator

Basics

The piezoelectric effect is a special property of materials to exchange energy between the mechanical and the electrical domain [27]. A particular distinction has to be made between *direct* piezoelectricity, which is the ability of a material to be polarized when subjected to mechanical strain, and *converse* piezoelectricity, which causes the device dimensions to change when an electric field is applied to it. In BAW resonators the second effect is exploited. When a RF variable signal is applied to the electrodes, an acoustic longitudinal wave is created in the material.

Different from SAW devices, in which elastic waves travel over the surface discontinuities of a solid, BAW resonators exploit the thickness extensional mode (TE) excitation of a piezoelectric film. As the name suggests, the wave propagation occurs in the bulk of the piezoelectric material.

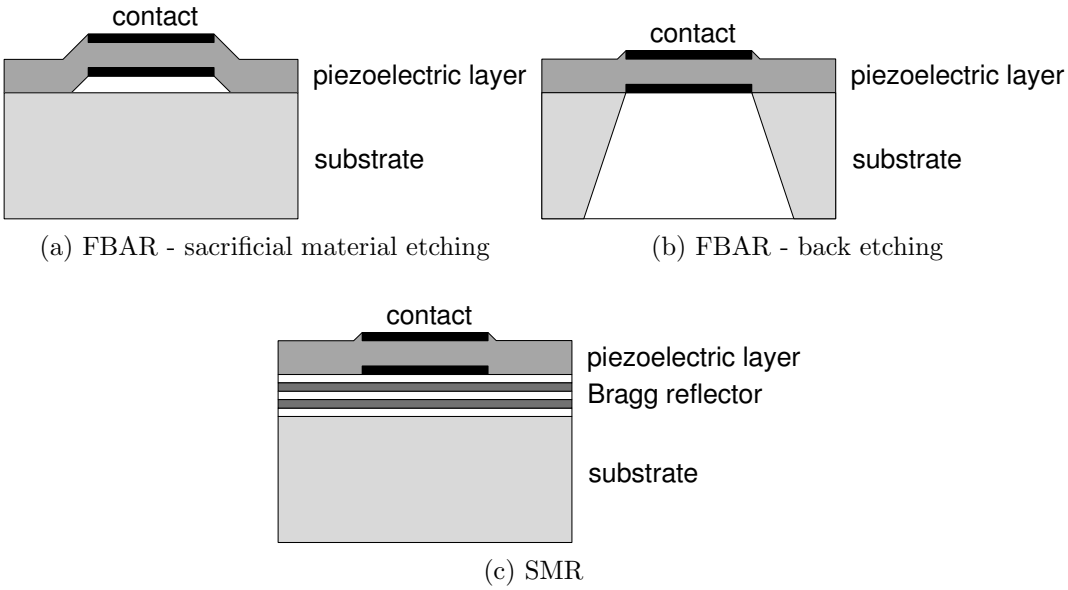
By using a rough simplification, we can see the BAW resonator as a device composed of a piezoelectric material sandwiched between two electrodes. The film is usually composed of aluminum nitride (AlN), owing to its good chemical, electrical and mechanical properties, but other materials like zinc oxide (ZnO) and lead zirconate-titanate (PZT) can also be used.

To minimize the resonator losses and achieve a high quality factor Q, the acoustic energy has to be properly confined in between the two electrodes, demanding particular care in defining the electrodes interfaces. Due to the technological steps involved in the resonator fabrication, the BAW upper electrode is normally interfaced with air (or vacuum), providing a good acoustic insulation. On the contrary the lower electrode lies normally on the substrate, causing leaks which degrade the resonator performance.

Based on the confinement of the acoustic energy at the lower electrode, two main families are presented in literature. They are depicted in Figure 3.5. In the first one, the Film Bulk Acoustic Resonators (FBARs), the energy losses are minimized by creating a cavity under the resonator bottom electrode in order to achieve the same acoustic insulation as that of the top electrode. This is generally done either by etching a sacrificial material during the resonator building steps or by releasing the resonator with a back etching of the substrate. The other family is represented by the Solidly Mounted Resonators (SMRs), for which the lower electrode is acoustically insulated from the substrate by using a stack of alternate layers of different acoustic velocities composing an acoustic Bragg mirror [28].

Model

Among the different models that have been developed in the years to describe the BAW resonator behavior, the most widely used is probably the analytical 1-D multiport transmission line model proposed by Mason [29]. In this model the acoustic wave propagation is treated by assuming that the resonator is built of a stack of infinitely large material layers. By doing that, the boundary conditions at the resonator vertical sidewalls can be omitted, hence allowing to simplify the problem to a monodimensional analysis. More complex 2D and 3D models will not be treated here, but the interested



(a) FBAR - sacrificial material etching

(b) FBAR - back etching

(c) SMR

Figure 3.5: Different types of BAW resonators.

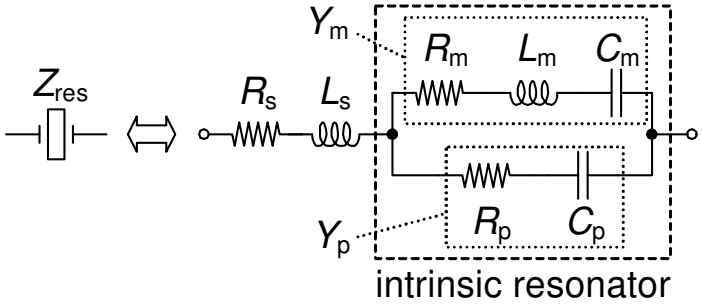


Figure 3.6: Lumped element BAW resonator model.

reader can find a formulation taking into account the planar geometry of the resonator in [30].

The Mason model can be solved analytically and it allows to calculate all the device resonance frequencies. Nevertheless, the first design steps generally do not require such a high precision, since only the behavior around the working frequency is of interest. Consequently, a simpler approach is used to derive a model useful for designing filters and circuits. By developing in series the Mason model around the main device resonance, it can be seen that the resonator behavior can be described by a lumped equivalent circuit known as Butterworth Van Dyke (BVD) model [27], depicted in Figure 3.6. The two parallel admittances Y_m and Y_p, representing respectively the acoustic and the electrical domains, constitute the *intrinsic* resonator model. Y_m, also called the *motional* branch, models the BAW resonance in the acoustic domain. It is composed of a series resonator formed by the motional capacitance C_m, the motional inductance L_m and its associated resistor R_m. Y_p, known as the *static* branch, comprises C_p and R_p, which represents the dielectric capacitance across the resonator electrodes

and its associated losses through the piezoelectric material respectively. Other elements can be added to the model in order to account for additional non-idealities. This is the case for example of R_s and L_s, which can be used to model the access to the pads and the bond parasitics.

The intrinsic resonator admittance can be calculated as:

$$\begin{aligned} Y_i(s) = Y_m + Y_p &= \frac{1}{sL_m + \frac{1}{sC_m} + R_m} + \frac{1}{R_p + \frac{1}{sC_p}} \\ &= \frac{s\left(s^3 + s\frac{R_m + R_p}{L_m} + \frac{C_p + C_m}{C_p C_m L_m}\right)}{R_p\left(s^3 + s\frac{R_m}{L_m} + \frac{1}{C_m L_m}\right)\left(s + \frac{1}{C_p R_p}\right)}. \end{aligned} \tag{3.1}$$

The BAW resonance and anti-resonance frequencies lie, for an ideal lossless resonator, at $\omega_s = 1/\sqrt{L_m C_m}$ and $\omega_p = 1/\sqrt{L_m C_{eq}}$ respectively, where $C_{eq} = (C_p C_m)/(C_p + C_m)$. Also this model predicts the behavior of the resonator far from the working frequency . In particular the intrinsic model is capacitive at low frequency and resistive at high frequency:

$$\begin{aligned} \lim_{s\to 0} Y_i(s) &= s\,(C_p + C_m) \\ \lim_{s\to\infty} Y_i(s) &= \frac{1}{R_p}. \end{aligned} \tag{3.2}$$

Even though this basic model does not account for the other BAW resonance modes, an higher precision can be achieved simply by adding in parallel to the motional admittance other motional branches Y_{mi}, one for each additional mode.

From the designer's perspective, it is useful to link the resonator physical parameters with the lumped elements used in the model. A simple flow that allows the circuit designer deriving the resonator model parameters from the device physical implementation is summarized here. The static resonator capacitance can be calculated from the resonator dimensions with the following formula:

$$C_p = \varepsilon_0 \varepsilon_r \frac{A}{d}, \tag{3.3}$$

where ε_r is the relative permittivity of the piezoelectric material used, A is the resonator electrode area and d is the thickness of the piezoelectric layer. Starting from the resonator capacitance C_p, the motional capacitance C_m is calculated. This can be done by introducing a technology dependent parameter, k^2_{eff}, known as the electromechanical coupling coefficient. From the physical point of view, k^2_{eff} represents the ratio of the energy exchange between the mechanical and the electrical domains. With this parameter, the motional capacitance can thus be written as:

$$C_m = \frac{8}{\pi^2} k^2_{eff} C_p = \rho C_p. \tag{3.4}$$

By knowing the BAW resonance frequency ω_s,the calculation of the motional inductance is straightforward:

$$L_m = \frac{1}{C_m \omega_s^2}. \tag{3.5}$$

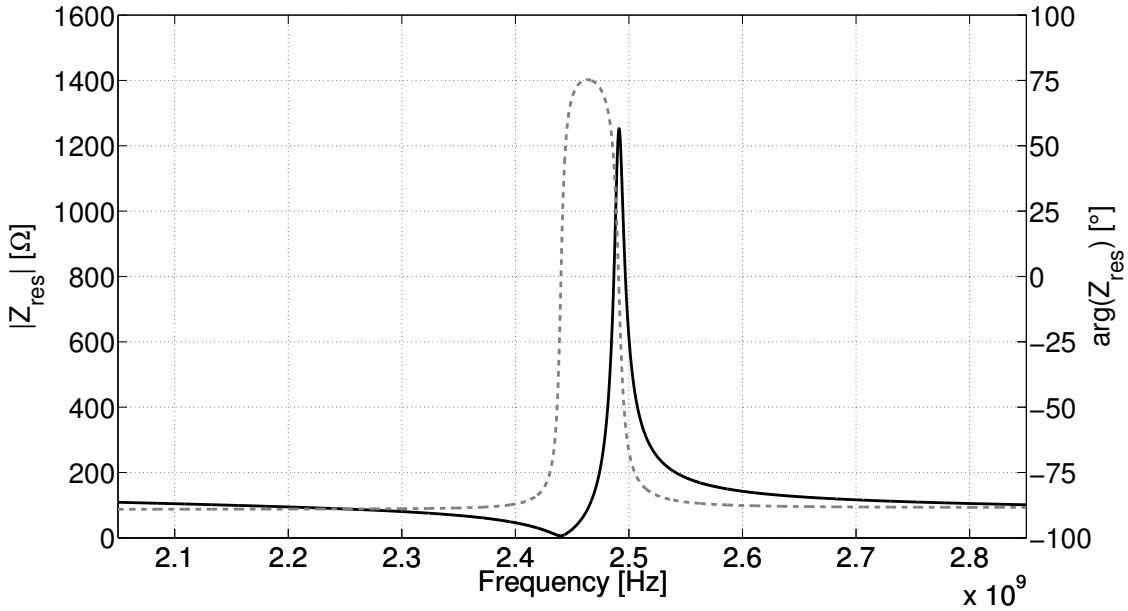


Figure 3.7: Resulting magnitude (solid) and phase (dashed) of the intrinsic resonator model.

Once the main resonator parameters have been calculated, the resonator losses can be estimated knowing the series and parallel quality factors achievable with the used fabrication process. For example, R_m can be calculated using the series quality factor Q_s in the following equation:

$$R_m = \frac{L_m \omega_s}{Q_s}. \tag{3.6}$$

Similarly R_p can be derived by using the parallel quality factor Q_p. The impedance of the intrinsic resonator model, for a typical 2.4 GHz BAW resonator with $Q = 400$, is depicted in Figure 3.7.

Even though the model presented in this section is only a rough approximation of the real device, it is very useful for circuit design purpose, at least during the first design phase. Then, in case the measurements of previously fabricated BAW resonators are available, the designer can perform a model fitting or directly use the extracted S parameters in simulation to perform the final design refinements.

3.3.2 BAW-based filters

The use of BAW resonators to build single or multistage filters presents some key advantages. The high BAW resonator quality factor allows design of steep filters with low in-band losses, while the resonator dimensions, linked to the longitudinal velocity of the the acoustic waves in the piezoelectric material, allow achieving compact implementations.

The standard approach used to design filters based on BAW resonators is to interconnect the different resonator lumped elements models in circuit configurations forming filters, such as in ladder or lattice configurations. The BAW based filters are

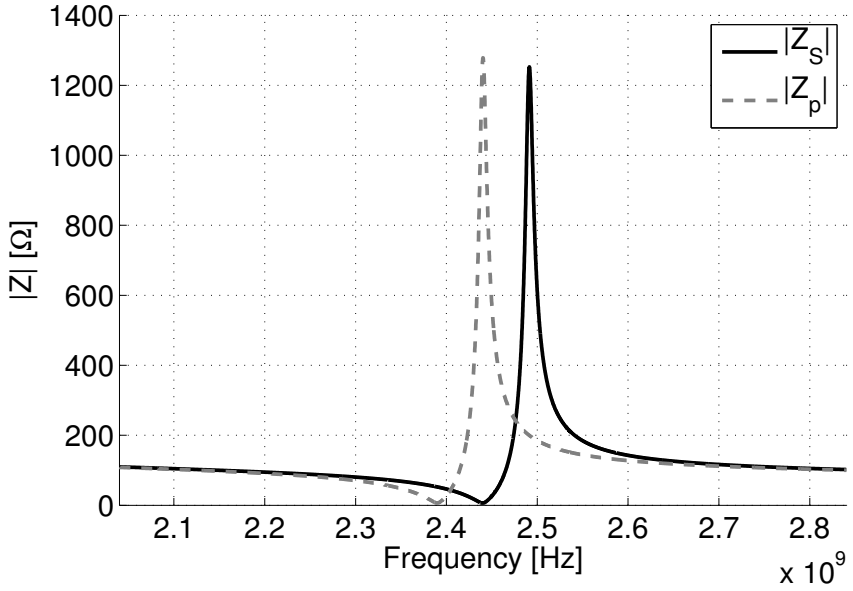


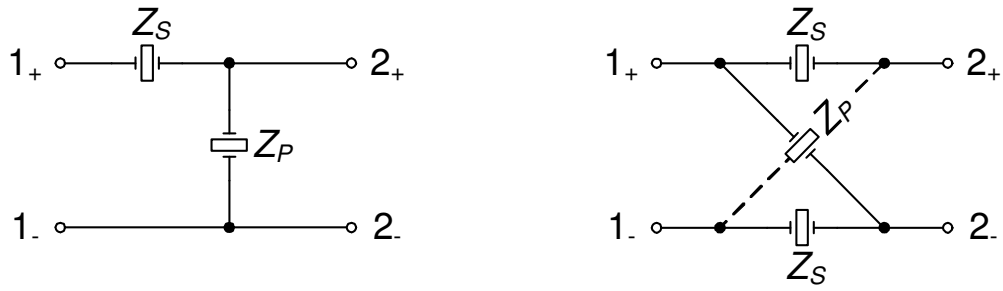
Figure 3.8: Series and parallel resonators impedances.

in general composed by combinations of resonators with different frequency characteristics, slightly shifted in frequency with respect to one another.

The translation of the resonator frequency response occurs towards low frequencies, owing to the particular technological step performed, which is known as *loading* technique. The loading is achieved at the end of the resonator fabrication process flow by sputtering deposition of SiO_2 on all the wafer and by subsequent patterning to modify only part of the resonators. Consequently, a shifted resonator is also called loaded resonator; a comparison between the impedances of a loaded resonator Z_p and an unloaded resonator Z_s is provided in Figure 3.8. The frequency shift between the resonators is typically large enough to place the antiresonance of the loaded resonator in proximity of the resonance frequency of the unloaded device. Then the ideal frequency shift is determined by a trade-off between the filter bandwidth and the in-band ripple.

The basic BAW ladder and lattice cells are shown in Figure 3.9. Both are built by using unloaded resonators as series elements and loaded resonators in parallel (or cross-coupled for the lattice cell). The main difference between these two configurations is that ladder filters can be used with both single ended and differential signals, while performing also balanced to unbalanced transformation if necessary, while the lattice filter can only be used with differential signals. Different cells can then be used in cascade to achieve the wanted filter response.

Figure 3.10 compares the typical transmission S parameters of a single stage lattice with that of a double stage ladder filter. A double stage ladder filter has been chosen for the comparison since it is composed of four resonators, hence occupying roughly the same surface as a single stage lattice. For the same number of resonators the lattice filter achieves better out-of-band rejection and higher bandwidth with respect to the ladder, but its response is less steep. On the other hand, the steeper roll-off of the



(a) Ladder (b) Lattice

Figure 3.9: BAW filter basic cells.

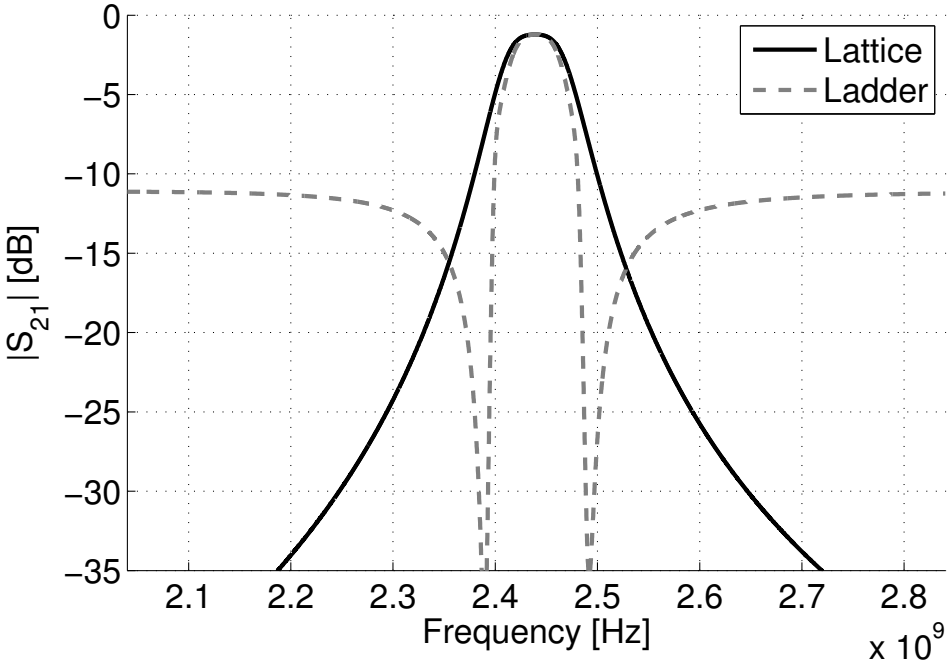


Figure 3.10: Comparison between four resonator ladder and lattice filters.

ladder is traded off for a weak out-of-band rejection.

By using lattice filters only, steeper roll-off characteristics can be achieved in two ways. The first possibility is to cascade different filter stages in series, by trading the increased selectivity with higher insertion losses. The other way is to use series and parallel resonators with intentionally different C_p. By doing that it can be demonstrated in fact that two notches appear near the filter band [31]. The higher the mismatch between the capacitances, the steeper the filter curve will be, but with the drawback of a decrease in the out-of-band rejection. An example is depicted in Figure 3.11, where the C_p of the parallel resonator has been set equal to 95% that of the series resonator. The resulting filter response is also compared with that of a standard lattice filter.

A completely different way to build BAW based filters is to couple acoustically the resonators by creating vertical stacks, in such a way that the filter response can be

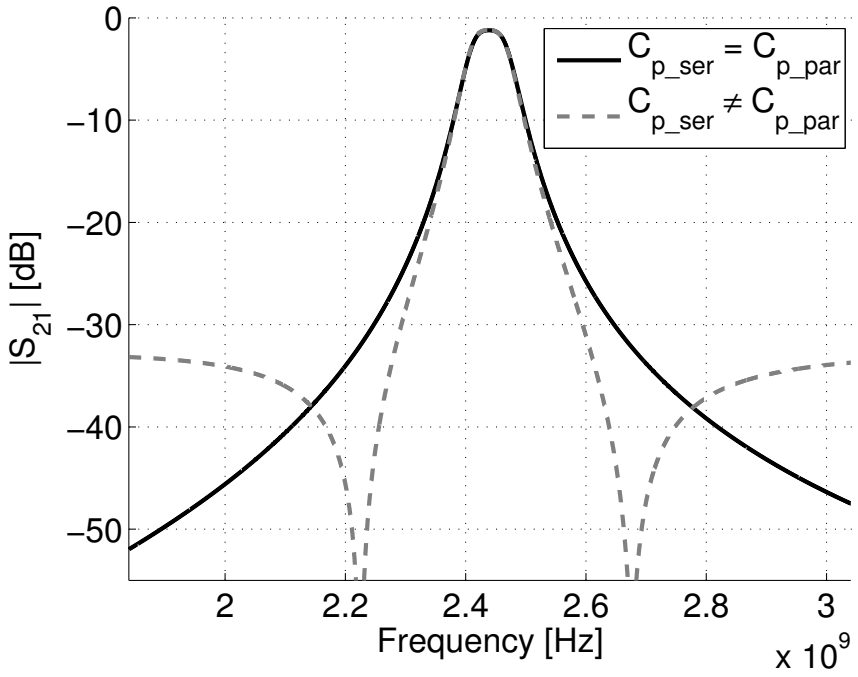


Figure 3.11: Effect of C_p mismatch in the lattice filter.

controlled. The two main techniques present in the literature are the stacked crystal filter (SCF), where two resonators are stacked across a ground plane and the coupled resonator filter (CRF) where the two resonators are separated by a coupling layer. These filters will not be treated here, and for more detailed information the reader is requested to refer to [32].

3.4 A radio for WSN application: the BAW-based transceiver

Bulk acoustic wave resonators are RF devices characterized by a very high quality factor (Q), which can reach values even higher than 2000 [33]. This feature can be exploited to implement filters and duplexers with reduced insertion losses and high out-of-band attenuations, but also to replace the LC tank of RF oscillators, thereby improving the phase noise × power consumption.

The use of bulk acoustic wave resonators in combination with RF circuits has already demonstrated excellent performance and miniaturization potential, matching well with the stringent needs of wireless sensors nodes. A lot of research has been done both at the block level, with the implementation of oscillators and selective low noise amplifiers, and at the architectural level, with the realization of several transceivers targeted to extreme low-power consumptions.

Before starting to describe the transmitters implemented in this thesis, a brief survey of the blocks and architectures taking advantage of BAW oscillators is given.

3.4.1 BAW-based circuits: state-of-the-art

The co-integration of BAW resonators with integrated circuits can yield benefits such as reduced power consumption and frequency selectivity. The two blocks that have taken the most advantage of the BAW resonator features have been, up to now, the local oscillator and the low noise amplifier.

BAW-based oscillators can achieve sensible performance improvement with respect to standard LC oscillators. Gains of about 30 dB in the phase noise $\times$ power product have been demonstrated [34, 35], corresponding to a phase noise of about -140 dBc/Hz at 1 MHz offset for a power consumption of a few hundreds of microwatts. The reason for this outstanding performance can be explained with the fact that this figure of merit is proportional to $1/Q^2$ [36], with Q being the loaded resonator quality factor. However, this advantage is counterbalanced by a very poor tuning range, which is of the order of 1% [36].

Several BAW based oscillators have been recently proposed [37, 38, 35]; nevertheless, for all of them the achieved tuning range was barely wide enough to allow the implementation of temperature and aging compensations only. At the time of writing this thesis, improved tuning capabilities have been demonstrated only at the expense of reduced phase noise $\times$ power product. In [39] a tuning range of 10% is achieved by tuning out the BAW parallel capacitance with a negative active capacitance. Even though this technique allows approaching the tuning range of an LC oscillator, it inevitably impacts the tank Q. As a consequence, a phase noise of -136 dBc/Hz can still be achieved at 1 MHz offset frequency from the 2.2 GHz carrier, but for an oscillator power consumption of 6 mW.

Another block which can take advantage of the integration with BAW resonators is the low noise amplifier [40]. In [41], a selective LNA is achieved by co-integrating BAW resonators with a g_m- boosted common gate amplifier [42], providing 20 dB image rejection. The filtering action performed by the LNA is then improved to 50 dB by using an additional BAW lattice pre-filter stage. This high attenuation allows relaxing the receiver linearity requirements and hence the front-end power consumption.

At the time this thesis started, the use of a BAW filter in transmission had already been demonstrated for a linear transmitter architecture. In [7], a bandpass ladder BAW filter was used after an EDGE power amplifier to filter the PA harmonic frequencies and the out-of-band noise caused by a $\Delta\Sigma$ modulator. Interstage impedance matching was provided between the power amplifier and the filter and between the filter and the antenna. The power amplifier, integrated in a 0.25 μm BiCMOS technology using SiGe-C heterojunction bipolar transistors for the first two stages and NLDEMOS for the power stage, demonstrated an output power of 32 dBm and an efficiency of 50% working at 3.6 V supply. At 28 dBm, the amplifier efficiency was 35%. Nevertheless, no real co-design was provided, apart from the impedance matching.

3.4.2 BAW-based transceivers: state-of-the-art

The reduced power consumption achievable by integrating the BAW resonators with RF circuits naturally led to the implementation of several transceivers targeted at wireless sensor networks.

In [43] a 5 kb/s OOK modulation is implemented by on/off cycling the transmitter, which is composed of a power amplifier directly driven by a fixed frequency BAW oscillator working at 1.9 GHz. The receiver section exploits a super-regenerative architecture to reduce the power consumption, while frequency selectivity is provided with the use of a BAW resonator. The power consumption is 450 μW in receive mode and 1 mW in transmit mode, for an output power of -6 dBm.

Another BAW based transceiver targeting tire pressure monitoring systems (TPMS) [44] implements a 50 kb/s FSK modulation with a current consumption of 6 mA in transmit mode (delivering 1 dBm output power) and 8 mA in receive mode. BAW resonators are integrated in the local oscillators, working at a fixed frequency of 2.12 GHz, and used in combination with the LNA to provide filtering.

By keeping the architectural complexity relatively low, these transceivers achieve extreme low power applications. On the other hand, they are limited to the use of a single or few channels only, owing to the BAW-oscillator reduced tuning range. This can decrease the network flexibility and does not allow interfacing with widespread standards as Bluetooth.

3.4.3 A 2.4 GHz multi-channel BAW-based transceiver

This thesis work is part of the effort made at CSEM to develop a complete BAW based transceiver able to address multi-channel applications in the 2.4 GHz ISM band. The main overall objective is to achieve a system which could take advantage of the BAW resonator features in the synthesis, the receiver and the transmitter sections, while allowing to cover the whole 80 MHz ISM band and being thus potentially compatible with Bluetooth and Bluetooth LE.

Figure 3.12 depicts a simplified schematic of the BAW-based multi-channel transceiver [45]. The tunability needed to address the ISM band is reached with the use of a wide-IF architecture [36] which avoids the limitation of the reduced BAW oscillator tuning range. Provided the intermediate frequency can range from 80 to 160 MHz, the 2.4 GHz ISM band is covered with the BAW oscillator working at the fixed frequency of 2.32 or 2.56 GHz (depending on the desired up/down conversion scheme, low-side or high-side injection). As a consequence, the oscillator high$-Q$ tank is not degraded and its excellent phase noise and power consumption performance are unaffected. The choice of the IF has been basically set by the image frequency occupation, which in case of low-side injection is situated just above the UMTS primary band.

Thanks to its high spectral quality, the BAW oscillator does not need to be locked within a multi-MHz quartz-reference PLL to achieve acceptable close-to-carrier phase noise levels. However, the temperature coefficient and aging can affect the oscillator long term frequency stability. To compensate for those drifts, which are assumed to have a large time constant, a PLL with a low-frequency reference (e.g. 32 kHz XTAL) and low bandwidth can be used. Alternatively, the same reference frequency can be provided with the use of an electronically temperature compensated silicon resonator [24], which achieves RTC functionalities with $\pm$10 ppm frequency accuracy over a 0-50°C, for a power consumption as low as 3.2 μW.

The combination of the BAW oscillator with a low frequency referenced PLL allows maintaining low-power consumption when the transceiver is in an idle state and

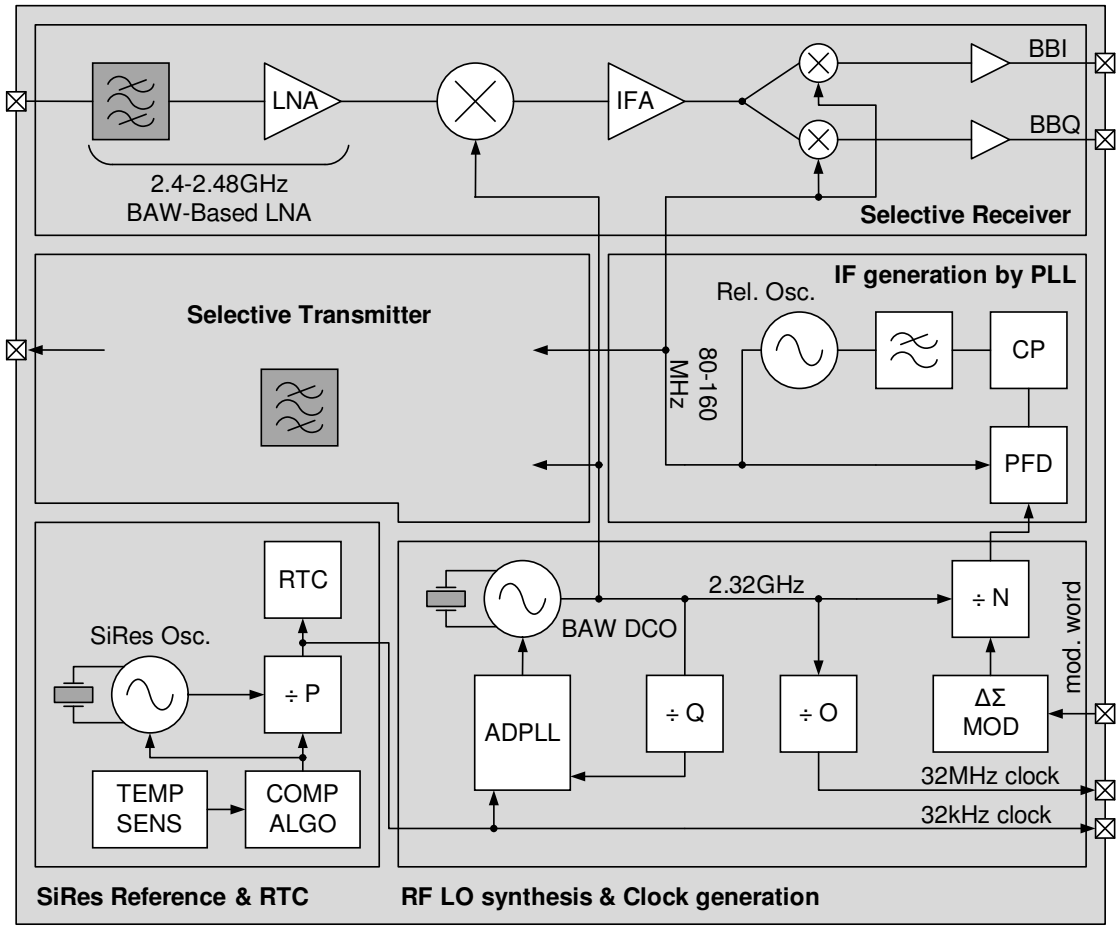


Figure 3.12: Block diagram of the 2.4 GHz multi-channel BAW-based transceiver. The transmitter section is intentionally not shown.

avoids the use of a multi-MHz radio XTAL, which is needed in frequency synthesizers to ensure fast settlings of the local oscillator and low in-band noise. To avoid the long settling times of the low bandwidth PLL, the BAW-based transceiver takes advantage of a digital implementation of the PLL. The use of an all-digital PLL [46] allows to save the lock conditions when the BAW-oscillator is switched off and only the RTC runs. If the radio activity has to be restored, the saved data is simply recharged in the ADPLL registers, ensuring to restart in an almost locked state and thus reducing considerably the settling time. The all digital PLL requires an oscillator having a digital control interface. Consequently, the BAW-oscillator is implemented as a digitally controlled oscillator (DCO) with a limited tuning range. Sub-ppm control of its oscillation frequency is achieved thanks to the use of switched capacitors banks and a $\Delta\Sigma$ MASH modulator [45]. The ADPLL is then completed with a phase-frequency detector (PFD) followed by a time-to-digital converter (TDC) and a digital loop filter.

The BAW DCO signal is then divided with a fractional division (N) to generate a first intermediate frequency. The division ratio, ranging continuously from 13 to 35, is achieved by controlling dynamically a chain of multi-modulus dividers [47]. This is done thanks to the use of a 20 bit MASH 1-1 $\Delta\Sigma$ modulator, whose control word can

be imposed with an external FPGA or a micro-processor. The nominal value of N is obtained from the target channel frequency and the ratio (Q) between the BAW DCO oscillation frequency and the 32 kHz reference frequency.

The first IF cannot be directly used in the transmitter and receiver chains. This is because the fractional division with $\Delta\Sigma$ modulation causes a shaping of the quantization noise that would pollute the higher end channels of the ISM band. As a result, an additional PLL is needed to filter out this high frequency noise and to generate the transceiver final IF. In this transceiver implementation, a relaxation oscillator with high tuning capabilities covers the whole IF range [36]. The use of the high frequency divided DCO signal as the PLL frequency reference has the advantage of allowing large PLL bandwidths (up to 2 Mb/s [45]), while still ensuring sufficient attenuation of the modulator quantization noise and of the reference clock spurs. The choice of the PLL bandwidth results from the trade-off between the rejection of the reference noise and the maximum achievable modulation rate.

Finally, the receiver section [45] exploits the co-integration of BAW resonators with an LNA. The resulting selective LNA provides 50 dB image rejection and relaxation of the receiver linearity requirements, hence avoiding the use of a filter stage between the LNA and the down-conversion mixer. Then, the heterodyne receiver provides a first down-conversion with the BAW oscillator and a second frequency translation to the baseband by multiplication with the quadrature IF signals.

3.5 Two BAW-based transmitter implementations

Two transmitter structures have been implemented in this context, both of them taking advantage of the great flexibility provided by the wide-IF up-conversion architecture.

The BAW resonators play two main roles in the designed transmitters: the first is to suppress the signal image present in the output spectrum after frequency up-conversion; the second is to reduce all the additional IF spurs, which represent the main drawback related to this architecture.

BAW resonators can allow suppressing those unwanted output components thanks to their high quality factors, providing steep out-of-band filtering and low insertion losses, thereby preserving the transmitter efficiency. In addition to that, the BAW filtering action will be beneficial to the suppression of the RF harmonics, which are located far from the ISM band. Last but not the least, BAW resonators are also ideal candidates for the implementation of filters in the transmitter path, thanks to their good power handling capabilities [7, 48].

The IF signals, implemented in both of the proposed transmitters as rail-to-rail digital waveforms, carry high odd harmonic content. Since the IF frequency lies in between 80 to 160 MHz, those spurs appear outside the ISM band and can be hence classified as out-of-band spurious emissions. To avoid those spurs interfering with devices working at frequencies adjacent to the ISM band, a frequency selectivity has to be provided in the transmitter chain.

The spurs level requirement used to benchmark the two transmitters is specified by the Federal Communication Commission (FCC) [49] and the European Telecommunication Standard Institute (ETSI) [50]. Maximum spurs of -30 dBm are allowed on

the output spectrum. In addition to that, the modulated signal inside the ISM band has to also comply the Bluetooth and Bluetooth LE requirements reported in Section 3.1.3.

Let us imagine to have an ideal square wave IF signal, switching between 0 and V_p, to be up-converted to the ISM band. If its duty cycle is perfectly equal to 50%, this signal is composed of only odd harmonics of its fundamental frequency and it can be written as

$$x_{if}(t) = \frac{V_p}{2} + \sum_{n=1,3,5,\cdots}^{\infty} \frac{2V_p}{\pi n} \sin(n\,\omega t), \tag{3.7}$$

where n identifies the signal harmonic. The amplitude associated with each harmonic will thus be equal to:

$$A_n = \frac{2V_p}{\pi n}. \tag{3.8}$$

As a consequence, the relative amplitude (and power) of each harmonic with respect to the fundamental is equal to:

$$A_{\text{rel}} = 20 \log \left(\frac{1}{n} \right) \text{dBc}. \tag{3.9}$$

By assuming an ideal up-conversion of the IF signal to the ISM band, all these harmonics will be translated to the RF output spectrum with unchanged relative amplitudes. As a consequence, the third IF harmonic will be at -9.5 dBc with respect to the power of the wanted signal, the fifth harmonic will be at -14 dBc and so on.

As a result, a transmitter employing a single notch at the image frequency will comply with the standard spurs requirements only for very low output power levels, owing to the presence of the third IF harmonic. Maximum output power of -20.5 dBm could be reached with a similar implementation, which is not sufficient to cover the transmission ranges for the targeted application.

The proposed transmitter implementations address this limitation in two different ways. In the first implementation, the BAW resonators are used as filtering elements to provide the needed spurs attenuation. In the second implementation, a joint suppression provided by a single sideband (SSB) mixer in combination with a selective power amplifier takes care of the output spectrum cleaning.

3.5.1 Inter-stage BAW filtering architecture

Let us assume the case of an ideal up-conversion achieved by multiplying a 80 MHz IF signal with a 2.32 GHz BAW LO (low-side injection). Owing to the considerations made in the previous section, the RF spectrum will appear as presented in Figure 3.13, indicated by the cross signs, if no filtering is applied. Please note that the spectrum is normalized to the power of the wanted tone, lying at the frequency $f_{BAW} + f_{if}$.

On the same graph, a typical curve representing the S_{21} parameter of a single stage BAW lattice filter covering the 2.4 GHz ISM band is shown (gray curve). The filter transfer function is modeled by substituting each resonator with its equivalent lumped element model. The resonators quality factor is chosen equal to 400.

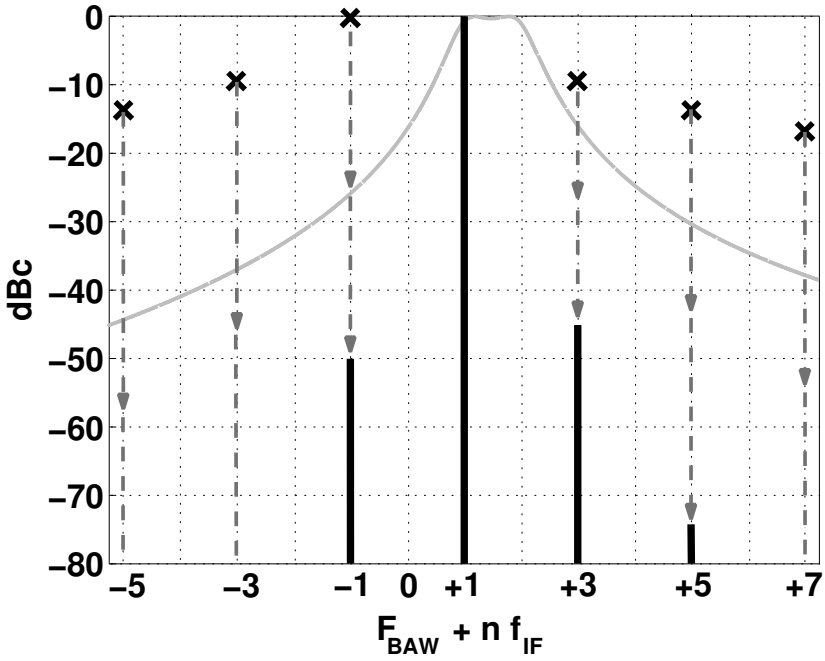


Figure 3.13: Qualitative spurious signal filtering suppression in case of one or two BAW lattice stages are present in the transmitter chain. Each arrow corresponds to the ideal suppression provided by a single stage filter.

The particular condition of $f_{if} = 80$ MHz represents the worst possible condition for the spurious signal suppression, since at this frequency the spurs are the nearest with respect to each other and thus experience the minimum possible filter suppression. The attenuation that a single stage BAW filter can provide at the image frequency ($n = -1$) and at the third IF harmonic (n=+3) are equal to 24.9 dB and 17.6 dB respectively. To comply with the spurs requirements, the maximum output power should be as low as -5 dBm.

Since higher output power levels are targeted, the use of two filter stages is compulsory. In this case, the image frequency will be at about -50 dBc, while the third harmonic will be at -44.7 dBc with respect to the power of the wanted tone. As a result, a maximum output power of about 14.7 dBm is ideally achievable, while still ensuring compliance with the -30 dBm spurs requirement.

Transmitter chain implementation

The first transmitter chain implementation had as main aim that of gaining some experience with the use of BAW filters in combination with RF circuits. As a consequence, the target maximum output power was relaxed to 0 dBm. To achieve a good integration level, it was chosen to limit the use of the external components to the two filters only.

A simplified block diagram of the transmitter is depicted in Figure 3.14. The modulated IF signals are up-converted by multiplication with the BAW DCO. The double sideband (DSB) mixer is loaded by a single stage BAW filter to suppress the unwanted sideband. Then, the resulting RF signal is amplified by a pre-amplifier plus

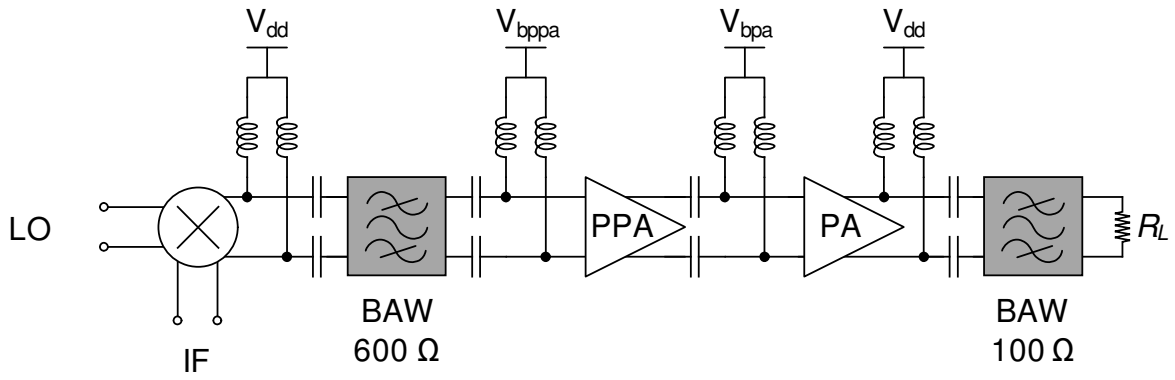


Figure 3.14: Simplified block diagram of the first transmitter implementation.

power amplifier chain, before being filtered by another single stage BAW lattice and sent to the antenna.

The DSB up-conversion mixer is based on a Gilbert cell with pseudo-differential pair, loaded by an integrated differential inductance and connected to the first BAW lattice filter. Since the BAW filter is quite sensitive to unmatched terminations, its impedance, which is set by the resonator dielectric capacitance C_p, should be made equal to that presented by the integrated circuit. The latter is given by the parallel between the mixer output impedance and the inductance equivalent impedance at resonance. In the case of the implemented architecture, it corresponds to a single ended impedance of about 300 Ω. Consequently, a BAW lattice filter with differential impedance equal to 600 Ω is used between the mixer and the preamplifier. An additional LC impedance transformation network matches the filter impedance with that presented by the preamplifier input. The LC resonance is made adjustable by using banks of switchable fringe capacitors.

The preamplifier stage is a differential class B push-pull amplifier. At its output, a differential integrated inductance is used to tune out the power amplifier gate capacitance, in such a way to maximize the swing and reduce the power consumption.

Finally, the needed power amplification is achieved with a differential cascoded class AB amplifier. This choice allows increasing the amplifier reliability by lowering the drain-gate voltage swing, provided the cascode stage is properly biased. At the same time, this implementation increases the amplifier input-output isolation by decreasing the Miller multiplication effect, thus improving the stability [51]. The amplifier output impedance is transformed to a differential impedance of 100 Ω in order to match with the BAW filter characteristic impedance.

Measurements

The transmitter, integrated in compatible 1P6M 0.18 μm CMOS process, occupies a surface equal to 1.5 × 0.48 mm^2. The micrograph of the implemented chip is depicted in Figure 3.15.

The use of the 600 Ω BAW lattice filter in the transmitter architecture was discarded after some measurement results indicating degraded performances and high in-band

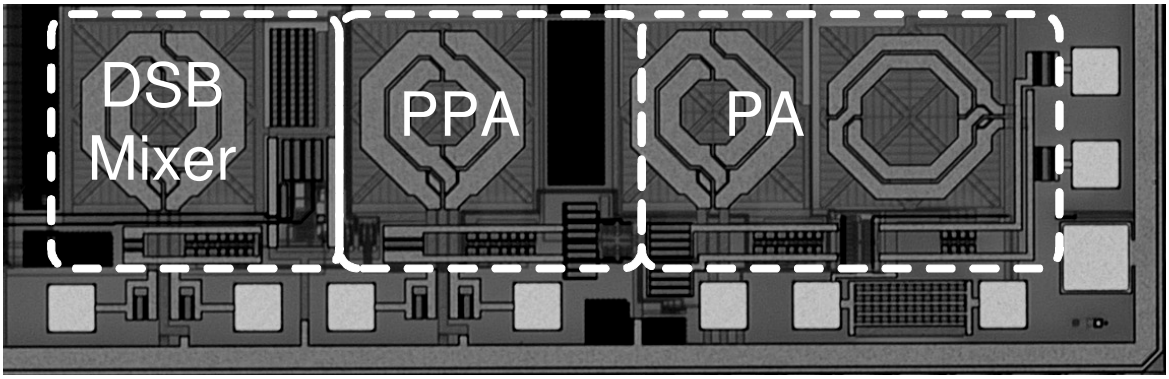


Figure 3.15: Micrograph of the first transmitter implementation.

Table 3.2: Overall consumption in TX mode

Description	**Current [mA]**
BAW oscillator	0.9
Divider chain	1.2
ADPLL + ext.clock	1
BAW frequency tuning	0.2
Filtering PLL	0.65
Up-converter	3.3
Preamplifier	2
Power amplifier	10.8
Total TX mode	20.05

ripple. To perform the measurements of the whole transmitter, the mixer output pads were thus bonded through the PCB to the preamplifier inputs. Consequently, the output spectrum violated the −30 dBm spurs requirement set by the standard regulations.

The losses due to the integrated inductances, together with the connection parasitics, limited the maximum achievable output power to −3.73 dBm, for an overall current consumption of the transmitter chain equal to 16.1 mA under 1.5 V supply voltage. The detailed current consumptions for the whole chip in transmit mode are reported in Table 3.2.

To conclude this section, the implementation of the first transmitter architecture with interstage filtering was not successful. Even if 1 Mb/s Bluetooth modulation was demonstrated [45], the spurs requirements on the output spectrum were not met. Consequently, another architecture has been proposed to avoid the use of an interstage filter while allowing at the same time to comply with the spectrum requirements.

3.5.2 Selective amplifying BAW-based architecture

To improve the transmitter efficiency and suppress the image and IF harmonic spurs, a selective architecture employing only one single BAW filter stage has to be found. Moreover, output power levels higher than 5 dBm have to be achieved, in order to cover transmission ranges of some tens of meters and enable the transmitter to be used in the targeted application.

The power amplifier, designed in this transmitter chain to reach the maximum efficiency, will be the most non-linear block in the signal path. Consequently, it is compulsory to use the single stage BAW filter after the PA, in order to clean the spectrum before it is sent to the antenna. In particular, a merging of the power amplifier with the BAW filter is proposed, which allows achieving frequency selectivity while preserving the amplifier efficiency. This co-integration will be detailed in Chapter 4.

The selective amplifier alone will not allow satisfying the spurs requirements on the output spectrum. This is because the attenuation at a given frequency will be the same as that provided by a single stage BAW filter. To solve this problem, a transmitter chain combining the suppression of a single sideband (SSB) mixer and the selective amplifier is proposed. The joint suppression mechanism used in this transmitter is depicted in Figure 3.16. Starting from the same normalized DSB spectrum described previously (identifiable by the cross signs), it will be shown qualitatively how the spurious requirements are met.

Let us assume to apply a frequency selectivity to the signal resulting from the DSB up-conversion. Each of the IF harmonic spurs will experience a suppression corresponding to the amplifier attenuation provided at a given frequency. This spurs suppression is represented on the figure by the dashed arrows. The spectrum resulting from this filtering action would allow complying with the spurious requirements only for an output power lower than -5 dBm, as seen in Section 3.5.1. Nevertheless, it can be also noted that all the spectrum components related to IF harmonics with order > 3 and < -1 are sufficiently rejected by this suppression to allow achieving the targeted output power while being compliant with the spurs requirements. As a consequence, a method allowing to reject the remaining two spurs (image and $+3^{rd}$ harmonic) has to be found. The needed attenuation has been achieved in the transmitter chain by substituting the DSB mixer with a SSB mixer.

The SSB mixer allows rejecting, after up-conversion, the unwanted sideband present at the image frequency. It can easily be shown that, if the up-converted quadrature signal presents some harmonic components, also those harmonics will be rejected. The interesting fact is that this mechanism acts alternately on positive and negative spurs around the wanted signal frequency. If ω_{BAW} is the frequency of the BAW oscillator and ω_{IF} is that of the first IF harmonic, the quadrature BAW and IF signals can be written as

$$x_{\mathrm{BAW}}(t) = e^{\imath\omega_{\mathrm{BAW}}t} \tag{3.10}$$

$$y_{\mathrm{IF}}(t) = \sum_{n=0}^{\infty} (-1)^n \, e^{\imath(-1)^n(2n+1)\omega_{\mathrm{IF}}t}, \tag{3.11}$$

where the Fourier coefficients of the IF square wave signal are not shown for simplicity.

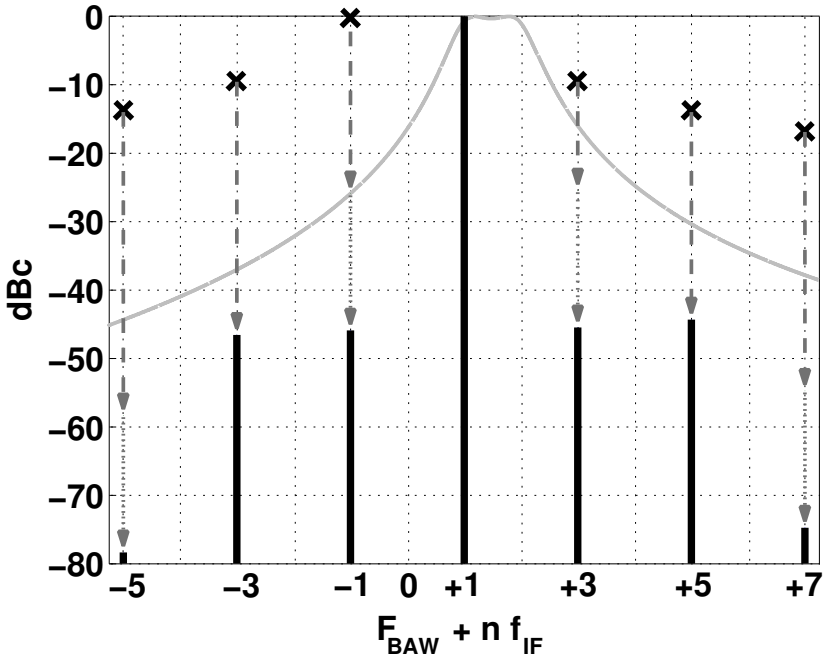


Figure 3.16: Qualitative spurious signal filtering suppression mechanism used in the transmitter. The arrows show the cumulative suppression of the selective amplification (dashed lines) and SSB mixer (dotted lines) in case of rail-to-rail IF signal.

The resulting simplified RF signal thus takes the following expression:

$$z_{\mathrm{RF}}(t) = \sum_{n=0}^{\infty} (-1)^n \, e^{\imath(\omega_{\mathrm{BAW}} + (-1)^n (2n+1)\omega_{\mathrm{IF}})t}, \tag{3.12}$$

from where it can be seen that all the components having order equal to $4m+3$, where m is an integer, are missing. In fact, the components related to the IF harmonics number -1, $+3$, -5, $+7$ are rejected by the SSB mixing action. Now, the first two rejected harmonics represent the two spurs which needed the additional suppression in Figure 3.16, in order to meet the spectrum requirements. For this reason, the interstage filter proposed in the first architecture can be avoided by using a SSB mixer in the transmitter chain. Figure 3.16 shows an example of the output spectrum (black curve) achievable with the joint filtering approach, if a hypothetical rejection of 20 dB (dotted gray arrows) is provided by the mixer.

The block diagram of the proposed transmitter is depicted in Figure 3.17. Since the SSB mixer needs quadrature signal at both the IF and the LO ports, a phase shifter is used to generate the quadrature from the BAW DCO signal.

To conclude, another thing can be noted by inspection of Figure 3.16. The use of the selective amplification strongly relaxes the image rejection specification that the SSB mixer has to achieve. This in turn results in relaxed quadrature mismatch requirements for the generation of the complex signals driving the mixer, which has a positive effect on the transmitter power consumption and area. A detailed explanation will be given in the next chapters.

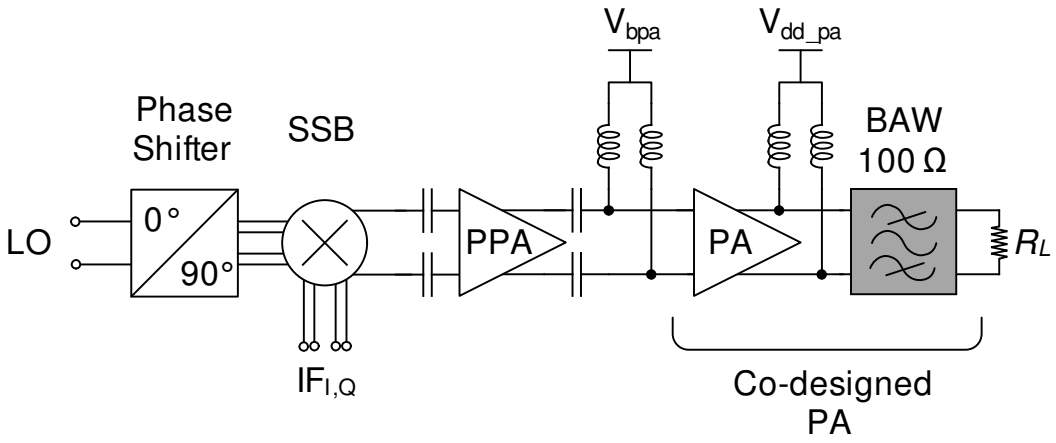


Figure 3.17: Simplified block diagram of the transmitter implementation exploiting SSB mixing and selective amplification.

3.6 Summary

In this chapter a possible scenario for the use of a BAW-based transceiver in WSN has been presented. The radio requirements have been specified, with focus on the transmitter side. A BAW resonator simplified model has been described, which allows to use the BAW as a building block to design filters. Then, the BAW-based transceiver architecture has been presented. To match best the needs of a BAW oscillator working at a fixed frequency, two possible transmitter architectures exploiting the up-conversion scheme have been proposed. The suppression techniques used to comply with the requirements have been described, together with an overview of the two transmitter implementations. The improved final transmitter, able to meet the spurious requirements with the use of a co-designed amplifier, is the topic of the next chapters.

Chapter 4

BAW-based Power Amplifier Analysis

In this chapter the design approach for a BAW-based power amplifier is described. The circuit side is analyzed to allow choosing the most suitable amplifier configuration to achieve the wanted co-design. Two different analysis approaches are used to study the amplifier performances in a full IC implementation and to find the optimum design point. Finally, the BAW-IC co-integration is described. Both single ended and differential implementations are investigated. The chapter ends with a differential BAW-based PA design example.

4.1 Integrating BAW resonators with the power amplifier

In Section 2.1.3 it has been noted that power amplifiers achieve high efficiencies at the expense of low linearity. In most of the RF applications this forces the use of external filters, which are needed to decrease the RF power at the harmonics of the working frequency to avoid interference with other frequency bands. Nevertheless, the design of the power amplifier and that of the filter remain normally distinct, and the only design step which links them is the impedance matching, which has to be performed for providing maximum power transfer [7].

The main aim of this work is to demonstrate that better performances can be achieved by performing a co-design between the BAW resonators and the power amplifier. A true co-integration will be possible only if the resonator becomes a functional part of the amplifier behavior; consequently, the approach followed to find the most suitable amplifier configuration to perform this integration is quite simple: the BAW resonator has to substitute a constituent element of a particular class of power amplifiers.

The co-integration can be done either with the aim to exploit the high Q of the BAW resonator to decrease the amplifier losses, or for filtering purpose or, if possible, for achieving both the targets at the same time. For example, the resonator intrinsic dielectric capacitance could be used in place of the shunt capacitance employed in the reduced angle amplifiers; a more interesting alternative is the replacement of discrete

resonating circuits in high efficiency amplifiers. While the first option can be applied to a wide variety of amplifiers, the second is applicable mainly to two amplifiers, the class F and the class E.

The class F amplifier, employing resonators for achieving a high efficiency, seems to be a perfect candidate for the co-integration. Nevertheless, some fundamental problems prevent its BAW-based implementation. In Appendix A it is shown that the class F amplifier needs different resonators tuned at odd multiples of the working frequency to reach high efficiency values. If all the resonators are replaced by BAWs, different parallel fabrication processes will be needed, increasing the complexity and the costs. The class E power amplifier also promises high efficiencies, but contrary to the class F it uses only resonators which are in the proximity of the working operating frequency, allowing the use of a single batch for the production of the amplifier BAWs. This reason, together with the good output power and the excellent efficiency performances achievable by class E PA, suggests this amplifier as the most promising for the BAW-PA co-integration.

Before starting with the amplifier co-design, a study of the class E power amplifier has to be performed first. In particular, due to the integrability requirements set for a transmitter targeting WBAN applications, all the passives used in the amplifier design (except the BAW resonators) will be integrated on-chip. This needs a careful validation of the amplifier behavior with this strict condition.

4.2 Optimum design for a high efficiency Power Amplifier

High efficiency power amplifiers exploit a very simple principle: during the instants for which the drain voltage and the drain current are both different from zero, the transistor dissipates energy that cannot be delivered to the load. The shorter is the time over the whole working period for which this occurs, the higher the efficiency will be.

This concept was already partially present in the reduced conduction angle amplifiers, which achieved higher efficiencies with a decrease of the conduction angle α. With class D and class E switching amplifiers, the switching action of the transistor causes no overlap between the two curves to occur, resulting in ideal efficiencies of 100%. This condition is achieved in two different manners by the two amplifiers. The class D PA performs a *hard switch*, i.e. forces the drain voltage to switch from V_{dd} to V_{ss} with the input voltage. On the contrary, the class E amplifier exploits a passive network to shape the drain voltage when the switch is off, achieving *soft switch* condition. The reason why the latter technique is preferable is explained here.

A class E PA model including the main losses is depicted in Figure 4.1. The transistor is represented by a switch, with its associated on-resistance R_{on}. To supply the needed DC current to the power amplifier, an inductor L_{dc} is connected to V_{dd}. The passive network is then completed by a shunt capacitor C_{sh}, a series resonator (C_0, L_0) tuned at the working frequency, with its associated losses (R_0) and an additional series inductance L_x, also called *excess* inductance, which is connected to the ideal resistive

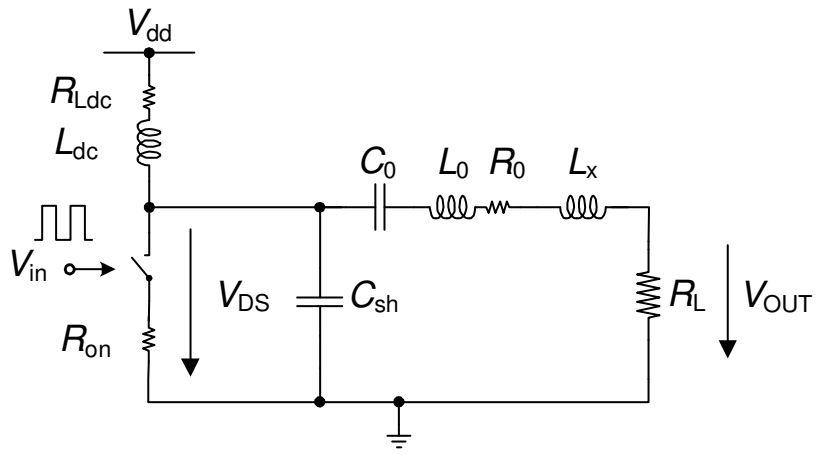


Figure 4.1: Class E Power Amplifier model with losses.

load R_L. The losses related to the excess inductance can be directly included with those of the series resonator, since L_x is merged with L_0 in a real implementation to minimize the number of passive components.

The behavior and performance of a class E amplifier are strongly dependent on the design of the passive network. The component pair (L_{dc}, C_{sh}) has the aim to induce a second order response shape to the drain voltage when the switch opens (and thus when ideally a step from 0 to V_{dd} is applied to the drain). Then, the series resonator filters out the working frequency harmonic components generated by the amplifier non-linearities to further increase the efficiency, while the excess inductance tunes the series resonator to provide the class E design requirements.

The most significant time domain waveforms for a lossless class E model are depicted in Figure 4.2. For a properly designed passive network, there is ideally no interval of time for which the drain current and the drain voltage are both different from zero. In particular, the transistor switch-on is performed at the instant for which the drain voltage returns to zero thanks to the drain voltage second order response. This condition represents the *soft* switch, which, contrarily to the class D hard switch, causes no charges being wasted towards ground at the switching instant.

To achieve an ideal class E behavior, the set of conditions which have to be ensured at the transistor switch-on instant is [52]:

$$\begin{cases} v_{ds} = 0 \\ \dfrac{dv_{ds}}{dt} = 0, \end{cases} \tag{4.1}$$

where the second equation makes the amplifier less sensitive to the variation of the design parameters.

Even if the class E PA transistor losses can be minimized (and theoretically set to zero) thanks to the drain voltage shaping, the amplifier still cannot reach efficiencies of 100%. This is due to the losses associated with the passive components forming the amplifier loading network, and in particular to the quality factor of the inductors. The aim of achieving a compact amplifier implementation, where the BAW resonators

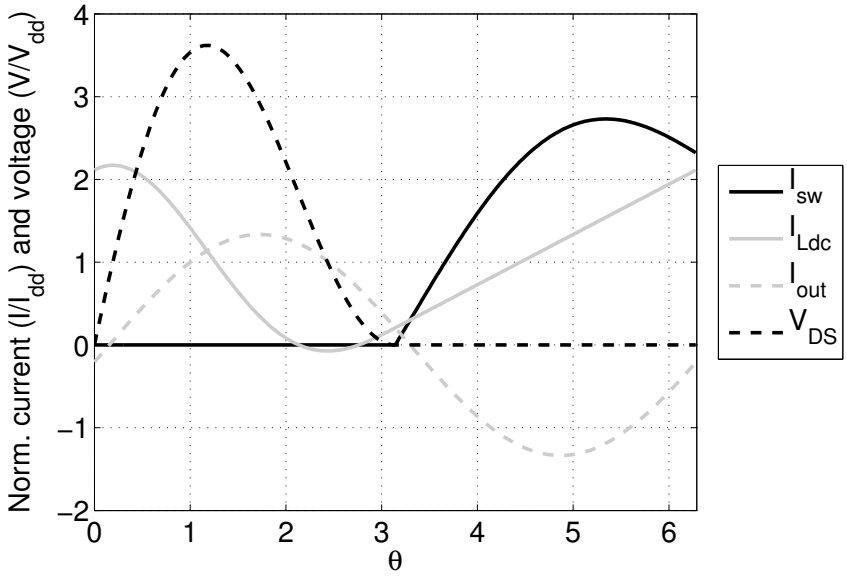


Figure 4.2: Normalized ideal waveforms for a class E PA.

are the only off-chip elements, calls for the use of integrated inductors, which have quality factors of the order of 7-8 in a standard digital 0.18 μm CMOS technology. As a consequence, the passive network losses have to be carefully taken into account in the amplifier design, since their effect could make the optimum design solution to deviate considerably from the ideal class E design.

To ensure the designed PA achieving the most efficient solution, an accurate study of the losses mechanism has to be done. While the early studies of class E power amplifiers [10, 52] did not develop any strategy to take into account all the different sources of losses (and very few studied non-idealities like the non-sinusoidal output current [53, 54] or the effect of switch only losses [55]), during the past few years mainly two approaches have become popular for the accuracy in studying the power amplifier efficiency, one based on an analytical formulation [56] and another one on numerical computations [57]. Both approaches account for all the main losses of the power amplifier, but with different initial hypothesis. In the next sections two class E PA models built with the mentioned approaches are presented and compared in order to find the optimum design point for a 2.4 GHz class E PA with finite on-chip inductances.

4.2.1 Fully analytical approach

To keep the model complexity relatively low and allow reaching an analytical solution, some ideal conditions are used in the first part of the study for calculating the amplifier behavior. Once the power amplifier is fully characterized in the time domain, the losses can be added to the model for finding the optimum design point. The analysis presented here has been derived from that used originally in [56].

The class E power amplifier design depends on quite a large set of variables like the supply voltage, the load resistor value, the transistor dimensions and of course all

the values of the different components used in the amplifier passive network. To allow a relatively simple analytical formulation, a simplification of the analysis space has to be performed. The switch dimension for example can be omitted for the waveform calculation, since it can be integrated in the design parameter C_{sh} through the transistor drain capacitor. Other parameters like the supply voltage and the load resistor can be masked by waveform normalization. With all these simplifications, it can be demonstrated that the analysis space can be in practice reduced to a one-dimensional space described by the parameter x, which is related to the class E power amplifier parameters L_{DC} and C_{sh}:

$$x = \frac{\omega_0}{\omega} \quad \text{with} \quad \omega_0 = \frac{1}{\sqrt{L_{dc}C_{sh}}}, \tag{4.2}$$

ω being the operating frequency. The whole analysis presented here aims thus to express all the waveforms and the amplifier performances as a function of this parameter.

In addition to the previous simplifications, the main hypothesis used to solve the analytical model is that the losses do not influence the waveforms behavior and thus can be initially omitted in the model formulation ($R_{L_{dc}} = R_{on} = R_0 = 0$). As a result, the model will always show, for example, a perfect sinusoidal output current, which is only possible by assuming that one has a perfect series resonator L_0, C_0 in the amplifier output network.

With these hypothesis, the drain voltage time behavior during the switch off-state half-cycle is calculated by imposing two initial conditions. The first condition is derived from the fact that at each opening of the switch the drain voltage is supposed to start from zero, since during the previous semi-period the switch was closed. The second condition comes from the derivative of the drain voltage at $t = 0^+$ and can be found by imposing the integral of the voltage across the inductor L_{DC} equal to zero over a whole cycle. By substituting the time variable with the angular time θ, the resulting normalized expression for the drain voltage during the switch-off half-cycle is:

$$\begin{aligned} v_{d_n}(\theta, x) =& 1 - \cos(x\theta) + \pi x \sin(x\theta) + \frac{Mx^2}{x^2-1}[sin(\phi)cos(\theta)+ \\ &+ cos(\phi)sin(\theta) - sin(\phi)cos(x\theta) - \frac{2x^2-1}{x}cos(\phi)sin(x\theta)]. \end{aligned} \tag{4.3}$$

This is valid for $0 \leq \theta \leq \pi$, with $\theta = \omega t$ and $M = L_{DC}I\omega/V_{DD}$. I represents the amplitude of the sinusoidal output current and ϕ its phase.

Now, by imposing the class E conditions (4.1) at the end of the off semi-cycle (i.e. $\theta = \pi$) it is possible to calculate M and ϕ as a function of the design parameter x, so that the drain function can be fully described by this parameter only. Figure 4.3 shows the drain voltage behavior and its variations in the switch-off half-cycle for different x values. Class E conditions are of course always satisfied for each value of the study parameter, since they are directly imposed in the model to calculate the analytical form of the voltage waveform.

The last step to complete the model consists in calculating the drain voltage first harmonic phase as a function of x. This is possible by calculating the Fourier coefficients of the drain voltage waveform for the first harmonic and thus computing the phase shift

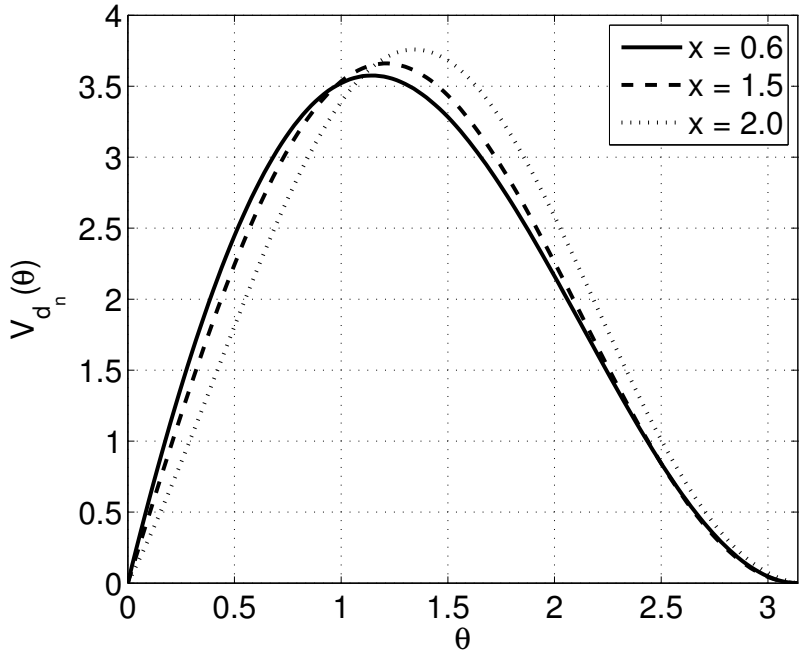


Figure 4.3: Drain voltage behavior in the switch-off half-cycle for different values of x.

which the output network introduces from the drain to the output current. Once the first harmonic phase shift has been calculated, all the waveforms describing the circuit can be fully characterized, as depicted in Figure 4.2.

Up to the moment no losses have been taken into account in the formulation, hence all the waveforms are completely ideal. The design approach proposed in [56] to find the optimum design point is to compute the losses of the different elements by applying their equivalent lossy resistance to the ideal waveforms. This obviously assumes that the losses do not have any impact on the amplifier working condition. Since all the waveforms are dependent on x, it is possible to maximize the amplifier efficiency over this parameter. The resulting efficiency plot for a power amplifier with integrated inductors ($Q = 8$) working at 2.4 GHz is depicted in Figure 4.4. Once the x value corresponding to the maximum efficiency is found, it can be thus substituted into the model equations to find all the class E PA parameters.

4.2.2 Numerical approach

The analytical approach becomes very tedious to be solved if the losses have to be accounted for directly in the waveform definition. To facilitate the study of class E amplifiers with finite inductances and realistic losses, numerical approaches can be used. They allow to foresee more precisely the optimum design point thanks to their complete formulation that includes all the main amplifier losses.

The numerical approach presented in [57] is based on a model that describes the class E PA with two sets of state equations. This is possible because under ideal conditions the amplifier transistor acts as a switch, thereby presenting only two possible

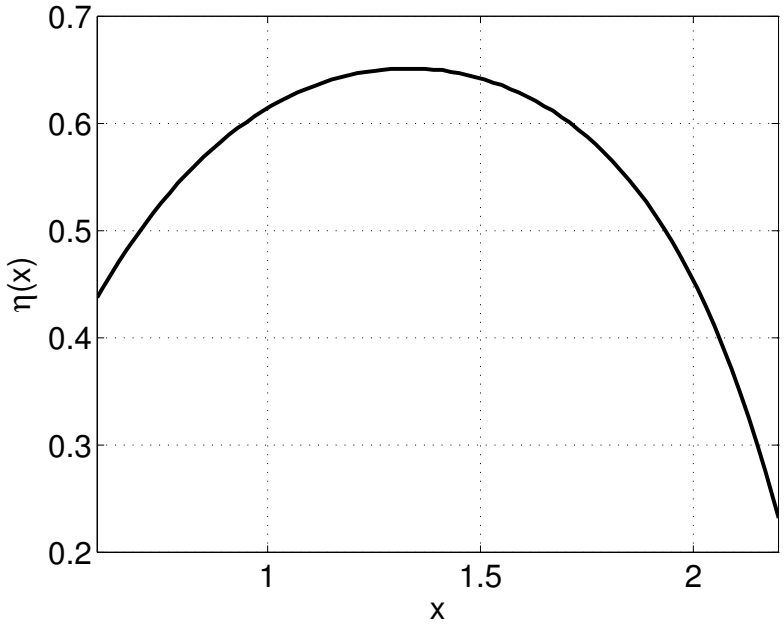


Figure 4.4: Example of a power amplifier efficiency curve over x, as predicted by the analytical model.

states. Referring to the simplified model of Figure 4.1, when the switch is open the equation sets describing the amplifier behavior can be written as

$$\begin{cases} L_{DC}\dfrac{di_{L_{DC}}(t)}{dt} = V_{dd} - i_{L_{DC}}(t)R_{DC} - v_{sw}(t) \\ (L_x + L_o)\dfrac{di_x(t)}{dt} = v_{sw} - i_x(t)(R_L + R_o + R_x) - v_o t \\ C_1\dfrac{dv_{sw}(t)}{dt} = i_{L_{DC}} - i_x(t) \\ C_o\dfrac{dv_o(t)}{dt} = i_x(t), \end{cases} \tag{4.4}$$

while for the switch closed the only modification concerns the third equation, which becomes:

$$C_1\frac{dv_{sw}(t)}{dt} = i_{L_{DC}} - i_x(t) - \frac{v_{sw}(t)}{R_{on}}. \tag{4.5}$$

The general solution of each of the two systems is given by

$$\begin{aligned} q_i(t) &= e^{A_i t}q_o + \int_0^t e^{A_i(t-\tau)}B_i d\tau \\ &= e^{A_i t}q_o + A_i^{-1}(e^{A_i t} - I)B_i, \end{aligned} \tag{4.6}$$

where the matrices A_i and B_i are respectively:

$$A_1 = \begin{bmatrix} \frac{-R_{DC}}{L_{DC}} & 0 & \frac{-1}{L_{DC}} & 0 \\ 0 & \frac{-(R_x+R_0+R_{DC})}{L_x+L_0} & \frac{1}{L_x+L_0} & \frac{-1}{L_x+L_0} \\ \frac{1}{C_{sh}} & \frac{-1}{C_{sh}} & \frac{-1}{C_{sh}R_{sw}} & 0 \\ 0 & \frac{1}{C_0} & 0 & 0 \end{bmatrix},$$

$$A_2 = \begin{bmatrix} \frac{-R_{DC}}{L_{DC}} & 0 & \frac{-1}{L_{DC}} & 0 \\ 0 & \frac{-(R_x+R_0+R_{DC})}{L_x+L_0} & \frac{1}{L_x+L_0} & \frac{-1}{L_x+L_0} \\ \frac{1}{C_{sh}} & \frac{-1}{C_{sh}} & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & 0 \end{bmatrix},$$

$$B_1 = B_2 = \begin{bmatrix} \frac{V_{dd}}{L_{DC}} & 0 & 0 & 0 \end{bmatrix}'.$$

Once the two equation sets are written, the initial conditions of each equation set have to be found. These initial conditions are steady state, since they repeat cyclically, with the additional requirement that each initial condition of a particular state variable has to be equal to the value of the same variable an instant before the change of the switch state occurs. This is because state variables are ruled by energy considerations and their values cannot be discontinuous. Thus the exponential matrix of A_1 has to be calculated for t_1 (end of the switch-closed half-cycle) in order to find the initial condition for the switch-open half-cycle and the matrix A_2 has to be calculated for t_2 (end of the switch-open half-cycle) to find the initial conditions for the switch-closed semi-period. This is done by solving a third system of equations:

$$\begin{cases} q_{0_2} = q_1(t_1) = e^{A_1 t_1} q_{0_1} + A_1^{-1}(e^{A_1 t_1} - I)B_1 \\ q_{0_1} = q_2(t_2) = e^{A_2 t_2} q_{0_2} + A_2^{-1}(e^{A_2 t_2} - I)B_2. \end{cases} \tag{4.7}$$

Once the initial conditions are known we can solve the differential equation systems by specifying the amplifier parameters and plot all the voltage and current PA waveforms. Then, the amplifier efficiency and output power can be calculated numerically. If the design of a class E amplifier is aimed, an algorithm can be formulated in order to iterate over the amplifier parameters and minimize the drain voltage and its derivative at the switch-on instant, as described by the two conditions in (4.1).

In the particular case of a design with fully integrated inductances, the interest is not to find a pure class E solution, but instead to find the maximum efficiency point over the amplifier parameters design space and then to compare it to the standard class E solution. This can be done by using the numerical model to sweep the different design parameters and find the optimum design point by inspection of the results. Alternatively an algorithm can be built to search for efficiency local maxima while the sweeps are performed, in order to try to limit the computation time.

Plotting contour graphs on the swept parameters is helpful to locate the optimum design point on the design space and to understand how variations in the parameters can affect the amplifier performances. Figure 4.5 depicts the efficiency contour plot

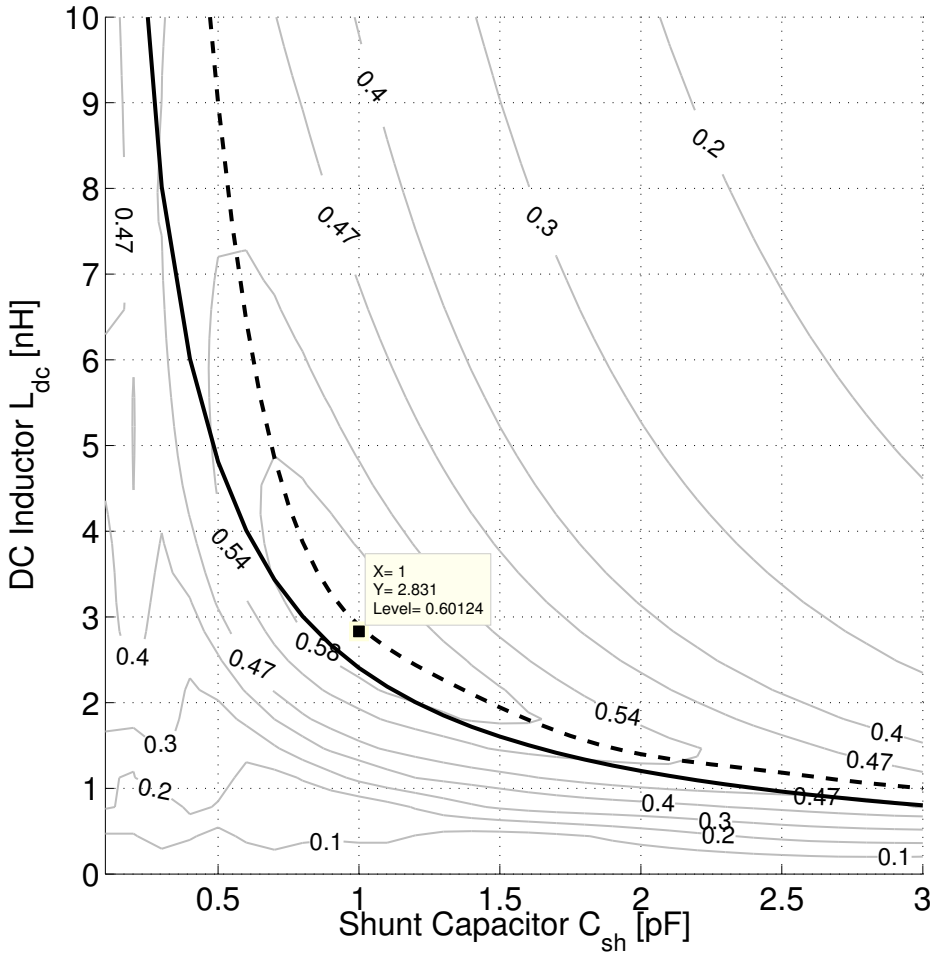


Figure 4.5: Efficiency as calculated from the numerical model and comparison with the analytical forecast.

of a 2.4 GHz power amplifier modeled with the numerical approach, while sweeping the power amplifier parameters L_{DC} and C_{sh}, for a fixed excess inductance L_x. The inductor losses are taken into account by calculating the resistors R_{DC}, R_0 and R_x assuming inductor quality factors of 8. The load resistor R_L is equal to 50 Ω. In this particular case, for L_{DC} = 2.8 nH and C_{sh} = 1 pF, a maximum drain efficiency of 60% can be reached. Variations of about 20% in the value of the shunt capacitor and the DC inductor will still allow the design to operate at efficiencies always higher than 53%.

In order to try to compare these results with those found with the analytical model for the same amplifier working conditions (represented by a single x value, corresponding to the solid curve in the (L_{DC},L_x) plane) of Figure 4.5, the crest of the efficiency surface calculated numerically has been extracted and plotted by dashed line. By inspection of the graph it can be noted that the two different curves do not coincide. The analytical approach introduces errors both in forecasting the optimum design point,

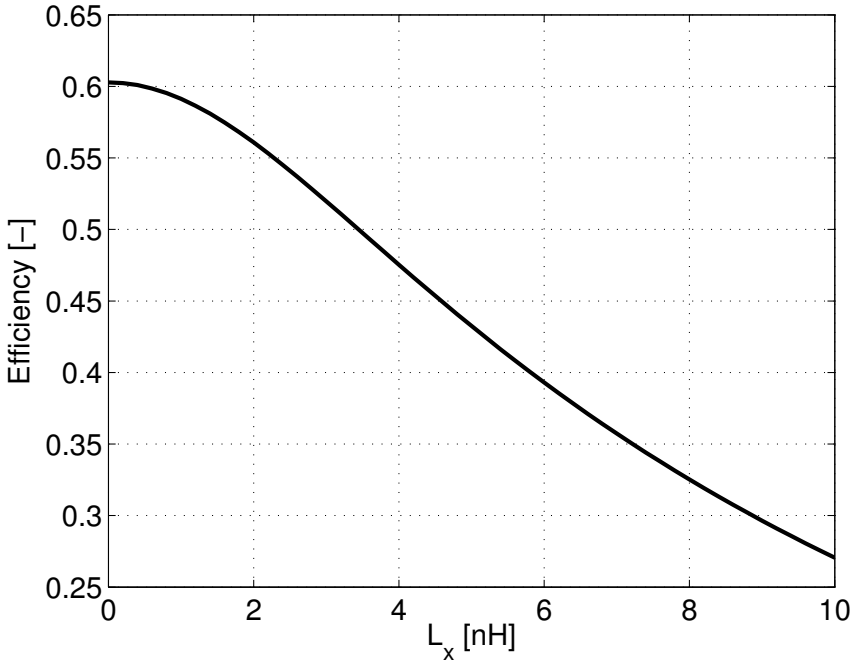


Figure 4.6: Efficiency over a sweep of the parameter L_x for the optimum (C_{sh}, L_{DC}) couple.

which is not crossed by the solid line, and in calculating the maximum efficiency that can be reached (the analytical model forecasts a 65% drain efficiency). Moreover it has to be noted that the solid line represents a locus of design points having all the same efficiency, while the dashed line includes design points which achieve different efficiency values, as indicated by the contour plot. Only one of these points, highlighted in the figure, represents the optimum design point for the numerical approach. Nevertheless, the distance between the optimum design forecast by the numerical model with respect to the analytical curve is quite limited, confirming the validity of the analytical model, which could be used in obtaining a first estimate of the component dimensions.

When the design space is explored with the numerical method, a particular feature of the finite inductance class E amplifier appears. If a sweep of the excess inductance parameter is performed for a given (C_{sh}, L_{DC}) pair, it turns out that for all the pairs considered in the design space the optimum efficiency either corresponds to or approaches the condition $L_x = 0$. As an example, the efficiency curve corresponding to the parameters (C_{sh}, L_{DC}) = (1 pF, 2.8 nH) is plotted in Figure 4.6 for a sweep of the excess inductance. This condition, already found in [57, 58], has been identified in the literature as class BE or class CE design. It represents the optimal power amplifier design point for a class E-like functioning, where the losses typical of a fully integrated implementation are accounted for. Therefore it represents the target that has to be aimed for the design of the BAW-based power amplifier.

The normalized waveforms of the optimum efficiency amplifier found with the numerical method are depicted in Figure 4.7. With respect to the ideal class E design the effect of the losses is now clearly visible. For example, the output current waveform is no more sinusoidal due to the non-idealities of the series resonator. As can be clearly

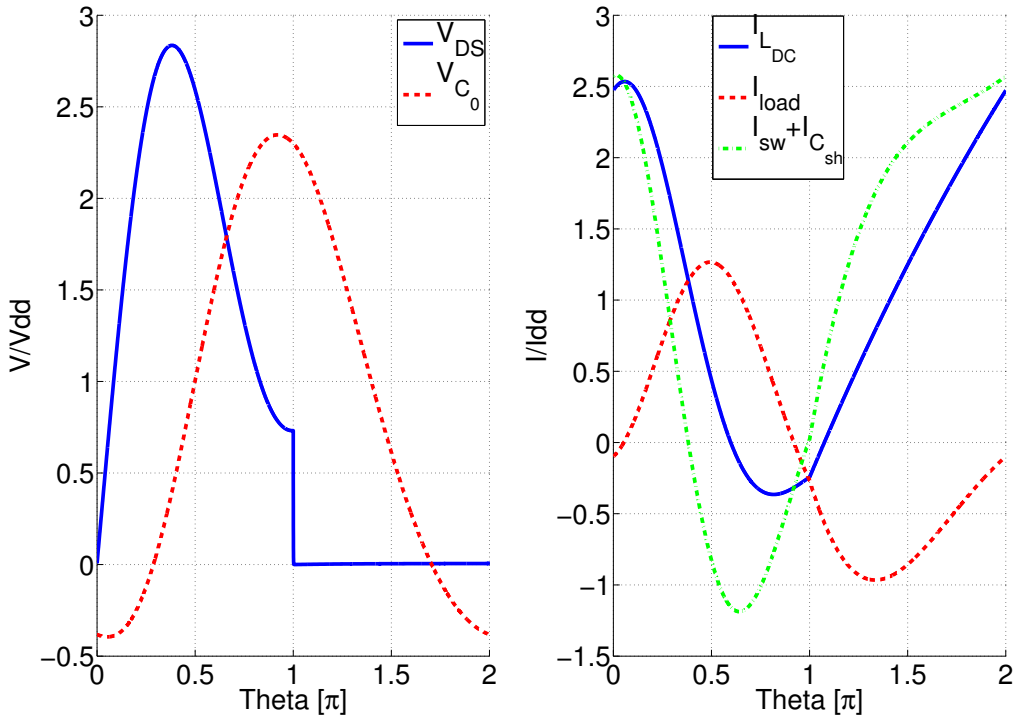


Figure 4.7: PA waves for the highest efficiency spot resulting from the numerical model.

observed from the drain voltage waveform, the numerical solution does not fulfill the typical class E conditions, since the drain voltage is far from being equal to zero at the switch-on instant. Moreover, the normalized maximum drain voltage resulting from the numerical model is lower than the analytical forecast (3.6 times the supply voltage) and during the switch-on half-cycle it is a little higher than zero, depending on the resistance value associated with the switch model.

4.3 BAW-based high efficiency PA

The main advantage BAW resonators offer to the designer is their high quality factor. In filter design this allows having low insertion losses and steep filtering curves at the same time. In power amplifier design this feature can be useful, depending on the transmitter architecture chosen and the spectrum requirements.

The availability of high-Q devices allows in fact designing *selective* power amplifiers which can be used to clean the output spectrum to help satisfy the transmitter spurs requirements. The up-conversion architecture described in Chapter 3 represents probably the most suitable architecture that can take advantage of such a selective amplifier, since it inherently suffers from the presence of spurs due to the IF harmonics.

Spectrum cleansing is not the only feature a MEMS-based selective power amplifier should provide. Since the PA is the most power hungry block in the transmitter, its efficiency and output power capability have to be preserved also. In this sense the

BAW resonator high quality factor can be exploited to improve the efficiency and output power performance, if this device is used to substitute a more lossy discrete resonator.

All these reasons call for a co-integration between the BAW resonators and the PA, which has to be performed by substitution of a particular amplifier feature by one of the BAW resonators. As seen in Section 4.2, the class BE power amplifiers exploits the use of passive elements in order to achieve the drain voltage shaping, thus ensuring a high efficiency. In particular two pairs of resonators are used for the design: a parallel resonator, that in general is slightly out of tune with respect to the working frequency and a series resonator tuned to the working frequency (the excess inductance L_x is in fact equal to zero for class BE).

In such a scenario the BAW resonators could be used directly to substitute the amplifier passive network components, with the advantage that BAW devices can bring better performance as compared to the integrated passives. This means also that the resonators will participate in the amplifier behavior definition by allowing achieving the class BE condition, while adding the new feature of high selectivity.

4.3.1 Single ended implementations

In this section, the integration of a single ended class BE PA with BAW resonators is discussed. Different options are available for the integration: a BAW resonator can be used 1) in parallel to the amplifier transistor for replacing the class E shunt components 2) in series with the load to substitute the discrete series resonator in the amplifier passive network 3) with a combination of 1) and 2) in a ladder filter configuration. Figure 4.8 depicts the first two basic configurations.

To check the performance of the two single ended BAW-based implementations, they have been compared to a standard class BE power amplifier designed by following the methodology described in Section 4.2.2. Simplified models of the BAW resonators with $Q = 400$ have been used for the co-design.

Parallel implementation

An important source of losses for a class BE amplifier is the integrated DC inductance. As a consequence, the possibility to exploit BAW resonators to substitute the amplifier parallel resonance is very attractive. While the BAW resonator presents the behavior of an inductance for frequencies between the series and the parallel resonance, unfortunately it can not be used to substitute the inductor L_{dc} of the class BE amplifier. This is due to the fact that the BAW presents a high impedance at DC that prevents the supply current from crossing the resonator.

Nevertheless, a way to use the BAW resonator in a parallel configuration is to exploit its antiresonance to perform a sort of weak band-pass action. The device has to be designed is such a way that its antiresonance frequency corresponds to the amplifier working frequency. The low impedance provided at the series resonant frequency will create a notch in the amplifier transfer function, which can be used for filtering purposes. The resulting PA, depicted at the top of Figure 4.8, is still composed of a passive network with two integrated inductors which allow to fulfill the class BE

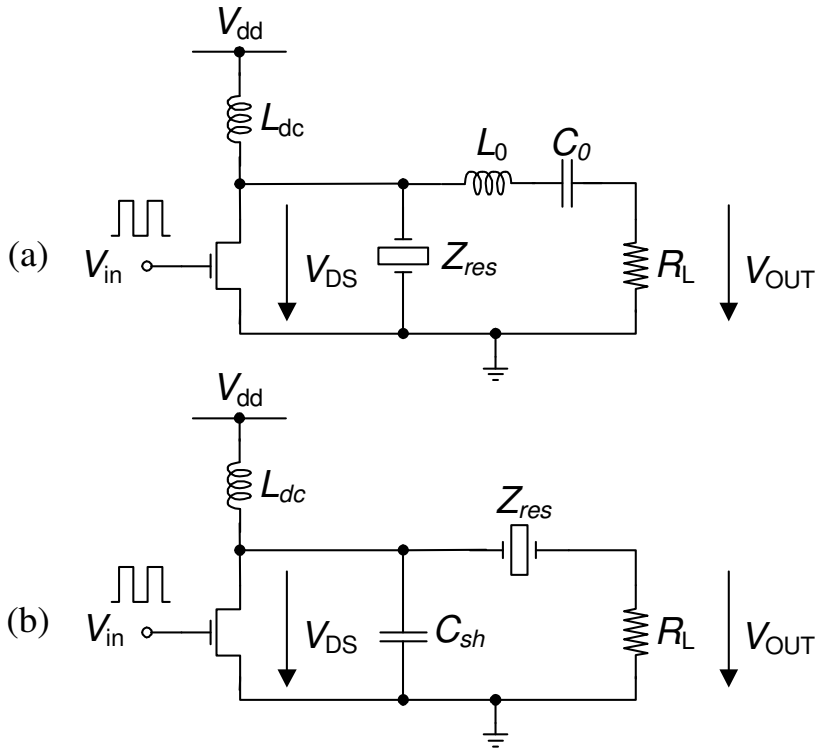


Figure 4.8: Parallel and series configurations of a BAW-based PA.

design requirements. As a consequence, this solution does not present any particular advantage compared to the standard amplifier implementation.

This effect is visible in Figure 4.9, where the efficiency of the single ended BAW-based amplifier is compared to that of a standard class BE PA (represented by the dashed curve and the dashed-dotted curve respectively).

Figure 4.10 depicts the output power achievable with a BAW-based parallel implementation. As expected, the amplifier provides a notch placed at the series resonance frequency, due to the low resonator impedance at that point, which could be exploited for filtering the signal mirror frequency. However, this would force the use of a single, or few, RF channels.

Series implementation

Another simple power amplifier design based on the integration with a BAW resonator is the series implementation depicted at the bottom of Figure 4.8. The amplifier, still in single ended configuration, exploits the resonator motional admittance to perform a pass-band action at the working frequency, thus substituting the (L_0, C_0) series resonator of the classical PA implementation. From the efficiency point of view, the power amplifier should take advantage of the BAW resonator high quality factor, thereby improving the performance compared to the standard implementation.

The amplifier efficiency extracted from simulation, depicted in Figure 4.9 (solid curve), shows an interesting result: even if the BAW resonator can provide a much higher quality factor than a classical LC integrated resonator working at the same

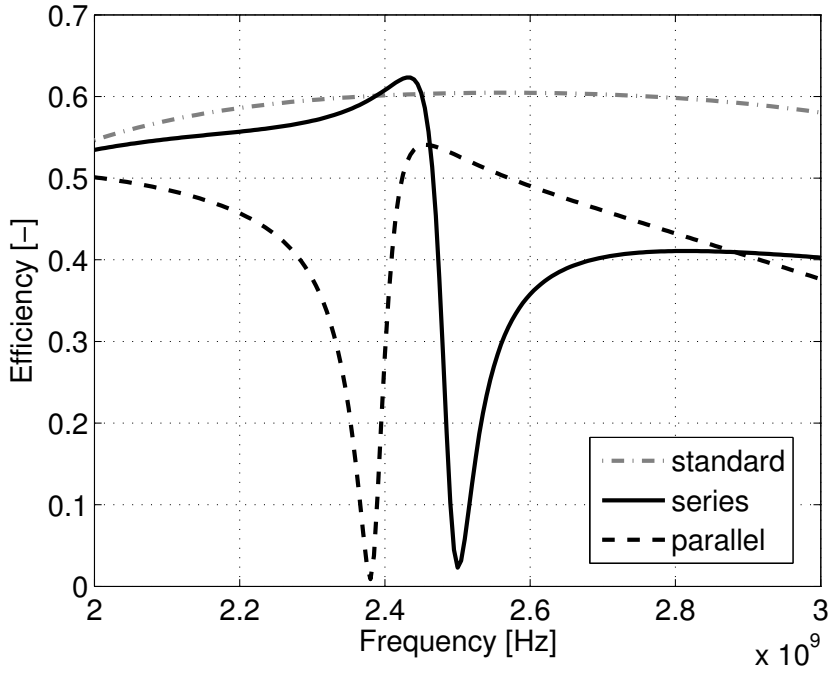


Figure 4.9: Efficiency over frequency of the BAW based single ended amplifiers, compared to the standard class BE implementation.

frequency (the simulations have been performed for a BAW resonator quality factor equal to 400, while the inductors quality factor is equal to 8), the resulting maximum drain efficiency is only slightly higher than that of the standard implementation.

This happens for two reasons. The first reason is a decrease of the amplifier drain efficiency for a given conversion efficiency: the BAW resonator model (3.1) shows that the parallel capacitance C_p decreases the resonator impedance at high frequencies, which tends towards R_p. This causes more harmonic power to be dissipated on the load, resulting in a degradation of the drain efficiency. The second reason is related to the BAW resonator intrinsic losses: while calculating the resonator model parameters it can be seen that the motional inductance is orders of magnitude higher than a typical inductor value used to perform a standard LC series resonator at gigahertz frequencies. As a consequence, the motional resistance will only be slightly lower than the series resistance of an LC implementation, at least for reduced resonator quality factor.

Both the efficiency and output power plots (Figure 4.9 and 4.10, solid curve) show a minimum situated at the parallel resonance frequency. This is expected since the resonator impedance reaches a maximum at that frequency and thus the current is blocked from flowing into the load. As for the parallel implementation, here also a transmitter using a single or few channels could be implemented, since the notch will filter out the image frequency after up-conversion. With respect to the parallel implementation, here a higher amplifier efficiency could be reached.

By observation of the two BAW-based amplifiers power curves of Figure 4.9 it can be noted that, not surprisingly, their combination results into a ladder filter characteristic, similar to that of Figure 3.10.

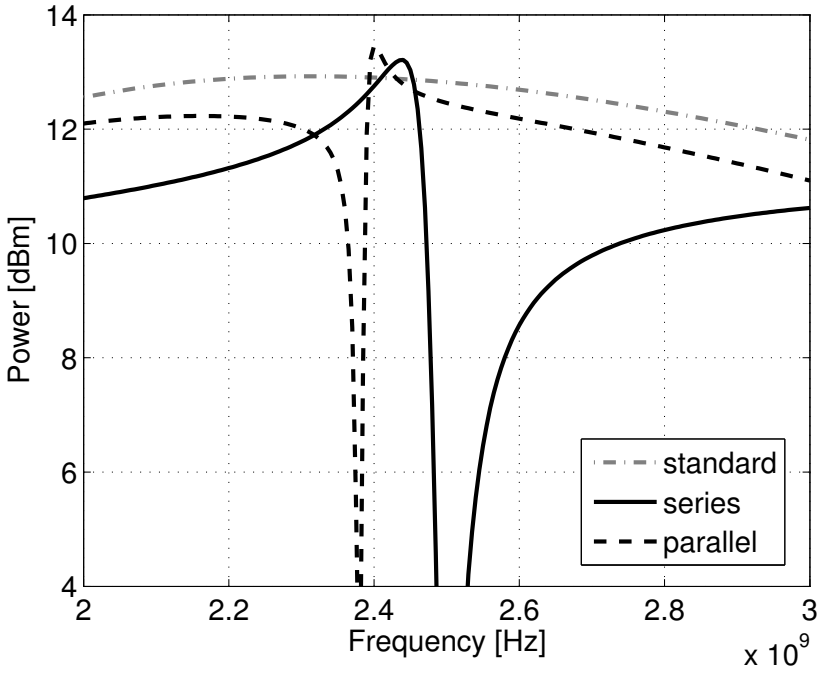


Figure 4.10: Output power over frequency of the BAW based single ended amplifiers, compared to the standard class BE implementation.

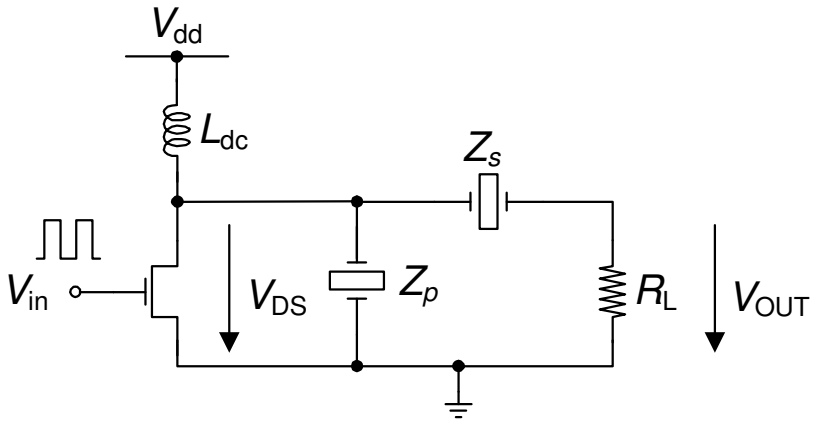


Figure 4.11: BAW-based class BE power amplifier with ladder filter.

Ladder implementation

By using a combination of a parallel and a series BAW resonator, properly detuned with respect to one another, a single ended BAW-based amplifier implementation can be achieved, as depicted in Figure 4.11. This implementation takes advantage of the two frequency characteristic shown previously to build a bandpass shape typical of a ladder filter.

The simulated amplifier efficiency and output power are compared to those of a class BE standard implementation in Figure 4.12 and Figure 4.13 respectively. By using

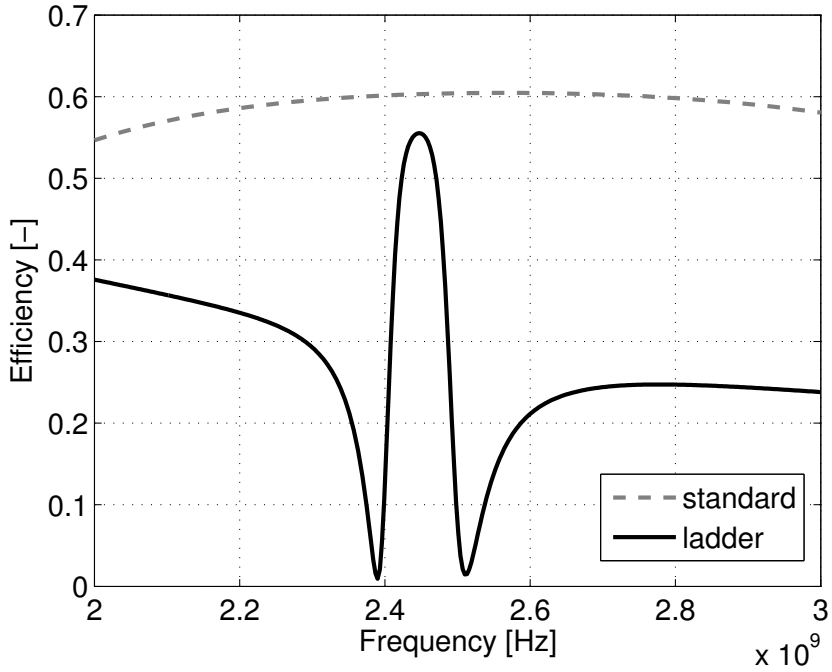


Figure 4.12: Efficiency over frequency of the ladder BAW based single ended amplifier, compared to the standard class BE implementation.

resonators with a quality factor $Q = 400$, the maximum efficiency reaches 55% and the amplifier output power is comparable to that achievable with a standard class BE. With respect to the single resonator amplifier implementations, this solution presents the advantage of providing a bandpass suppression which would allow to address several channels in the 2.4 GHz ISM band.

By properly loading the parallel BAW resonator and using the series resonator as replacement of the LC resonator used in the classical amplifier implementation, a time domain behavior typical of a class BE amplifier can still be ensured in-band. This confirms that the BAW devices participate in the amplifier drain voltage shaping, as confirmed by the simulated waveforms shown in Figure 4.14.

This amplifier implementation presents a frequency selectivity which has the same disadvantage than the ladder filter, i.e. a reduced out-of-band rejection. As a consequence, if only two BAW resonators are used in the amplifier passive network, the suppression out of the band will be as low as 3 dB.

Assuming rail-to-rail IF signals, a SSB mixer with perfect image rejection and a target output power of 10 dBm, the higher spur present in the output spectrum will be that corresponding to the -3^{rd} IF harmonic. This spurs will be at -9.5 dB with respect to the power of the wanted tone. Consequently, the selective amplifier would need to provide a suppression of about 30.5 dB to comply with the -30 dBm spurs requirement. This rejection can be achieved by cascading five ladder stages, resulting in an increase of the insertion losses which limits the simulated drain efficiency to about 32%.

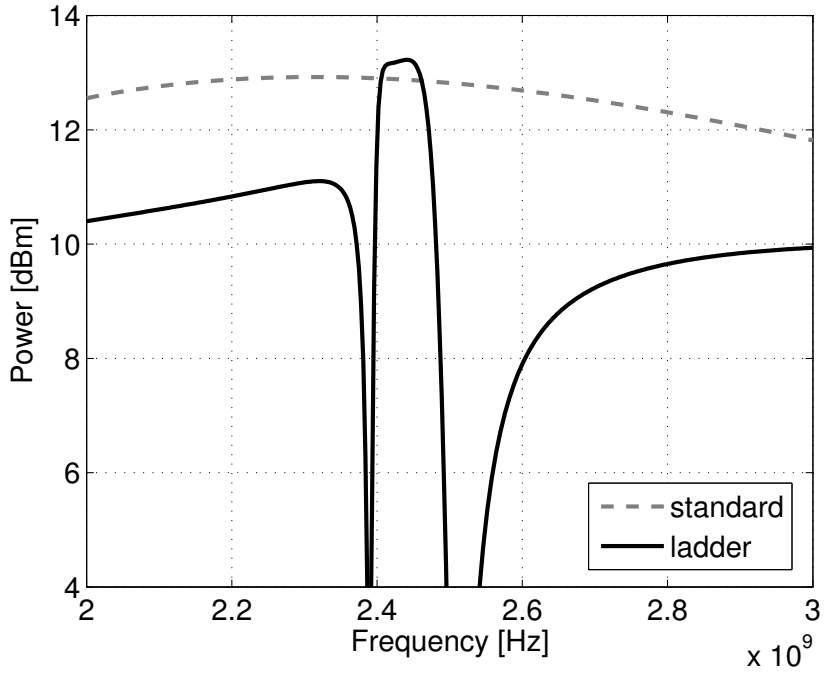


Figure 4.13: Output power over frequency of the ladder BAW based single ended amplifier, compared to the standard class BE implementation.

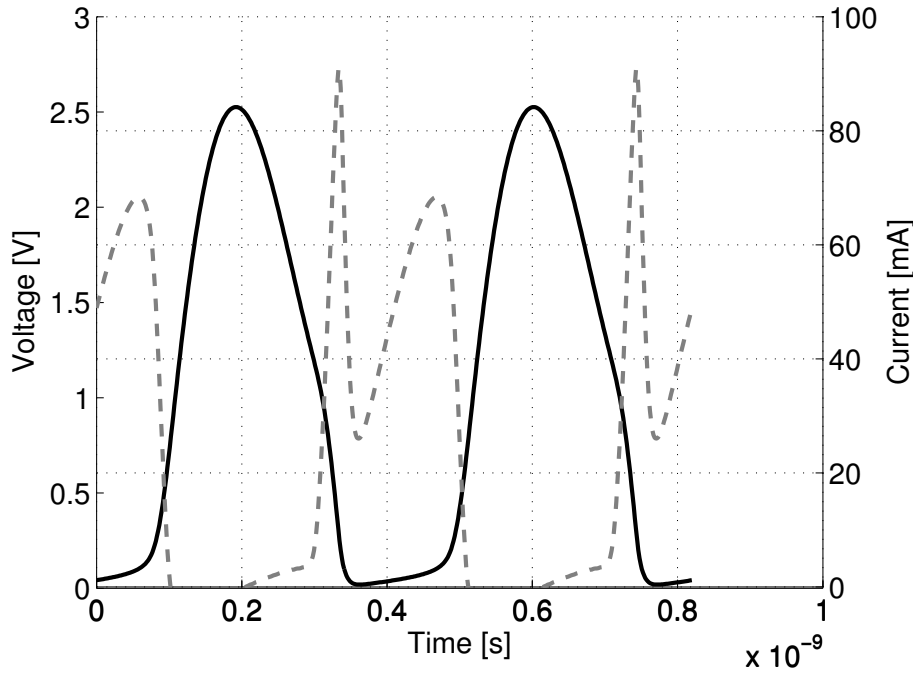


Figure 4.14: Drain voltage (solid) and current (dashed line) of the BAW PA with ladder configuration, for BAW quality factor equal to 400.

4.3.2 Differential BAW-based class BE power amplifier

The single ended BAW-based amplifier implementations present an important fundamental limitation. The use of a single resonator in the PA does not allow to achieve a bandpass characteristic able to address multi-channel applications and suppress the spurious related to the heterodyne architecture. An amplifier implementation exploiting several resonators in ladder configuration can be used, but the amplifier efficiency decreases considerably if a sufficient out-of-band rejection has to be provided.

Moving towards a differential configuration allows using both the ladder and the lattice filter structures for building the amplifier passive network. The lattice filter represents the best choice, since it provides an higher available bandwidth for a given coupling factor of the resonator and it achieves better out-of-band attenuation characteristics. This allows avoiding multiple filter stages in cascade, which in turn translates into a higher amplifier efficiency. As will be explained later, the lattice filter suits well the co-integration with a class BE power amplifier. The main disadvantage in using a lattice configuration resides in the fact that it does not provide balanced to unbalanced transformation, thereby requiring a differential load.

For the design of the power amplifier, the most important advantage a differential configuration brings compared to a single ended amplifier is probably the reduction of the current ripple that is drawn from the supply for a given output power. The differential configuration in fact presents current peaks that are smaller and shifted 180° with respect to one another, resulting in a supply current with a lower ripple and a main frequency component at the double of the amplifier working frequency [59]. This merely translates into less supply noise for the neighboring blocks and into a lower on-chip decoupling capacitance, resulting in area savings.

Mason transformation

The key of the co-design between a class BE power amplifier and a lattice filter relies on a filter transformation known as Mason equivalence [60].

As seen in Section 3.3.2, the lattice filter is composed of series and parallel resonators, shifted in frequency with respect to one another. Each of these resonators can be represented by a lumped element model which describes its admittance Y_i. If we do not take into account the connection parasitics, the resonator admittance can be written as $Y_i = Y_{mi} + Y_{pi}$.

The series and parallel resonators used in the BAW filter have different motional admittance Y_m but the same static admittance Y_p. This is due to the fact that the loading process, performed on the parallel resonators, impacts only the acoustic properties of the device, while the electrical parameters remain intact, since the resonator dimensions (the area and piezoelectric layer thickness) are unchanged.

The Mason equivalence states that if all the admittances used in a lattice filter have a common part, the filter can be transformed in an equivalent form, for which the common admittance is removed from all the filter branches and appears in parallel to the input and output ports only. Owing to the loading process, the parallel and the series resonators can be written as:

$$Y_1 = Y_{m1} + Y_p \tag{4.8}$$

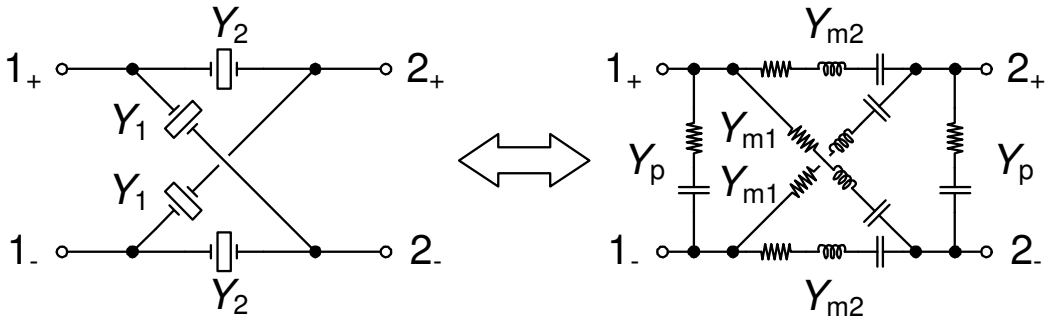


Figure 4.15: Mason Equivalence applied to a BAW lattice filter.

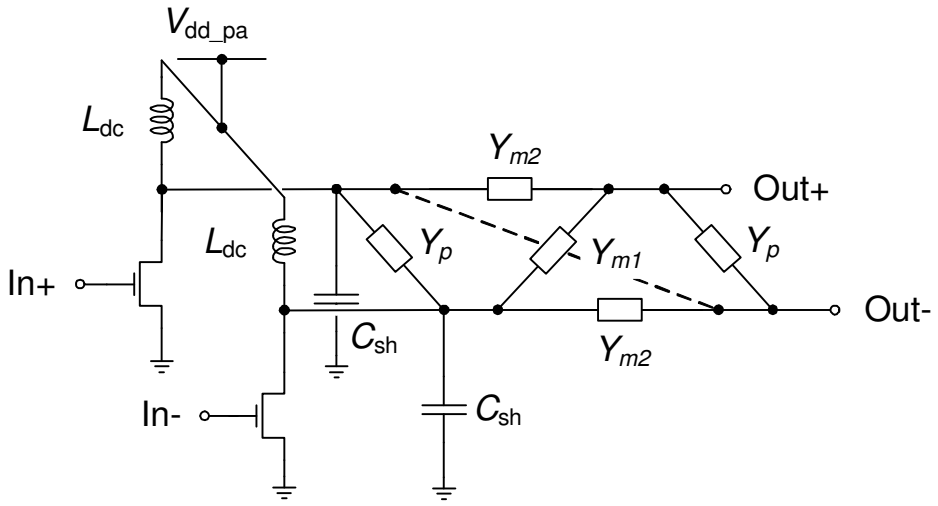


Figure 4.16: Schematic of the BAW-based power amplifier.

$$Y_2 = Y_{m2} + Y_p, \tag{4.9}$$

where $Y_{m1} \neq Y_{m2}$. As a result, the common admittance Y_p can be moved from the filter branches to the input and output ports and the lattice can be transformed in its equivalent form, depicted in Figure 4.15.

This is particularly interesting because now the static admittance, which is mostly capacitive, appears in parallel to the power amplifier transistors on one side and to the load on the other side, as shown in Figure 4.16. This opens new possibilities for the design of the amplifier, since it means that the resonator capacitance can be integrated into the amplifier design parameter C_{sh}. It is thus possible to say that thanks to the bandpass characteristic of the lattice filter and to the possibility to account for the resonator features in the amplifier design, true co-integration can be provided.

Design considerations

Taking into account the aforementioned transformation, the design of the differential BAW-based PA is achieved by accounting for the resonator dielectric capacitance into

the model amplifier parameter C_{sh}. The preliminary results achieved with the numerical model are then refined by transistor level simulations.

Figure 4.17 shows the efficiency of the BAW-based 2.4 GHz differential amplifier compared to that of a class BE standard differential implementation. As done before, the resonators quality factor is set to be equal to 400, while the inductor quality factor is 8. Both the amplifiers have been designed for a supply voltage of 1.2 V and a differential resistive load of 100 Ω. The transistor width has been maximized for both the amplifiers in such a way to exploit completely the design parameter C_{sh} and decrease the losses due to the switch on-resistance R_{on}. As expected, the efficiency of the BAW PA decreases quickly while exiting the filter bandwidth, contrary to that of the standard implementation which can be considered constant over a reasonably narrow band. From the efficiency plot, it can be also noted that the peak value reachable with the BAW-based PA is limited to about 51% for Q = 400, while it equals that of the standard class BE (56%) for resonator quality factor of 750.

To explain this result some considerations have to be made. For the co-designed amplifier the design parameter C_{sh} includes not only the transistor drain capacitance, but also the resonator capacitance. This reduces the fraction of C_{sh} which can be absorbed by the transistor, leading to a lower transistor width and consequently to an increase of the switch-on resistance R_{on}. Moreover, with respect to a standard differential class BE amplifier, which has two series resonators towards the load, here four different resonators (two in series and two cross-coupled) are used.

While keeping the other amplifier parameters fixed, this efficiency loss is completely compensated if the BAW resonators have Q $\geq$ 750. The same result is shown in Figure 4.18, where the amplifier efficiency is plotted for a fixed frequency of 2.44 GHz while sweeping the resonator quality factor. Interestingly, the plot shows that for quality factors approaching 2500, reachable with high quality above-IC FBARs, the efficiency saturates to a value only slightly higher than 60%. This occurs because the efficiency becomes limited by other elements when the series network losses are decreased, mainly represented by the integrated DC inductance and the switch-on resistance.

The advantage of using the co-designed selective amplifier becomes clear when the comparisons are made for the same conditions, i.e. when a filter is used after a standard switching amplifier. This is often the case in practical implementations, since the use of a strongly nonlinear amplifier imposes to filter the harmonics of the RF signal not to interfere with other RF bands. In this case, assuming to load the classical BE amplifier with a filter having 1.5 dB insertion losses (the same as that of the BAW filter), its overall efficiency drops to about 39%, compared to the 51% of the co-designed amplifier with resonator quality factor equal to 400.

Figure 4.19 depicts the output power of the BAW amplifier for a sweep of the input signal frequency, compared to the standard class BE design. While the latter does not present any frequency selectivity, the BAW-based implementation takes advantage of the BAW filter frequency behavior to achieve a passband characteristic. The amplifier output power at the band center frequency is equivalent to that of the standard implementation, while the out-of-band rejection follows the same behavior of the BAW lattice filter. The output power curve is in reality slightly pulled towards low frequencies with respect to that of a perfectly matched filter, with a resulting in-band ripple

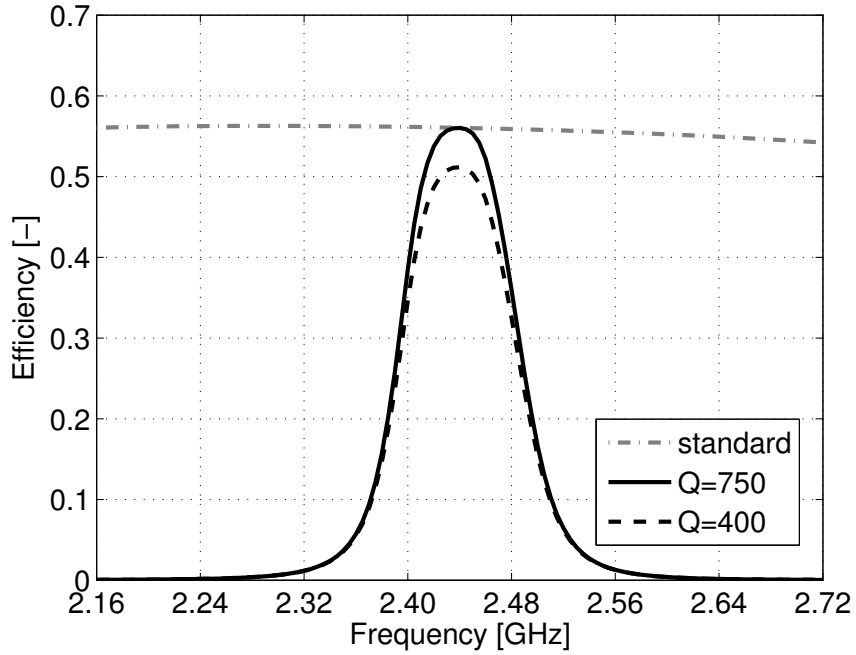


Figure 4.17: Comparison between the standard LC class BE PA and the BAW-based PA efficiency, simulated for resonators Q of 400 and 750.

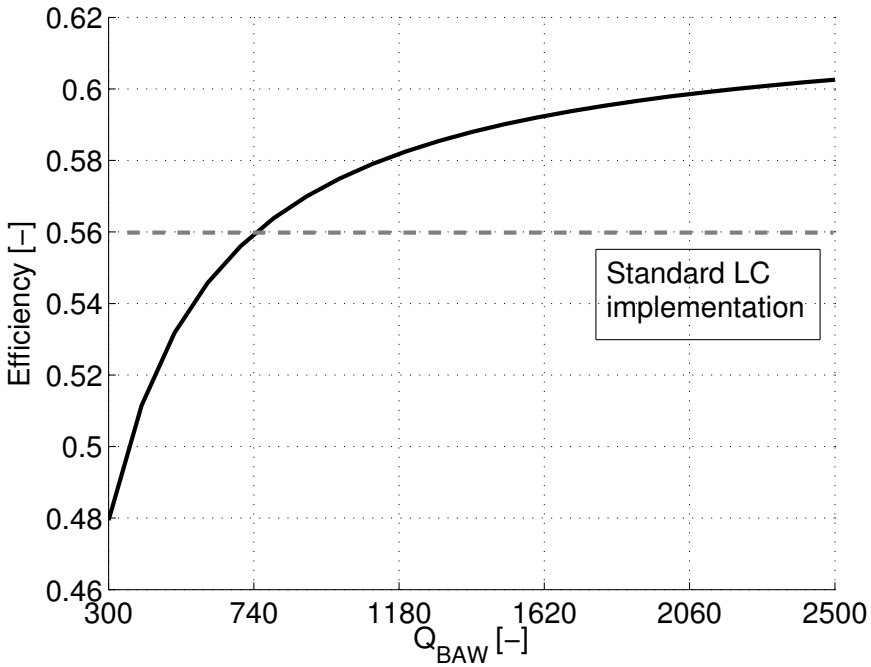


Figure 4.18: BAW-based PA efficiency at the center of the filter band over a sweep of the resonators Q.

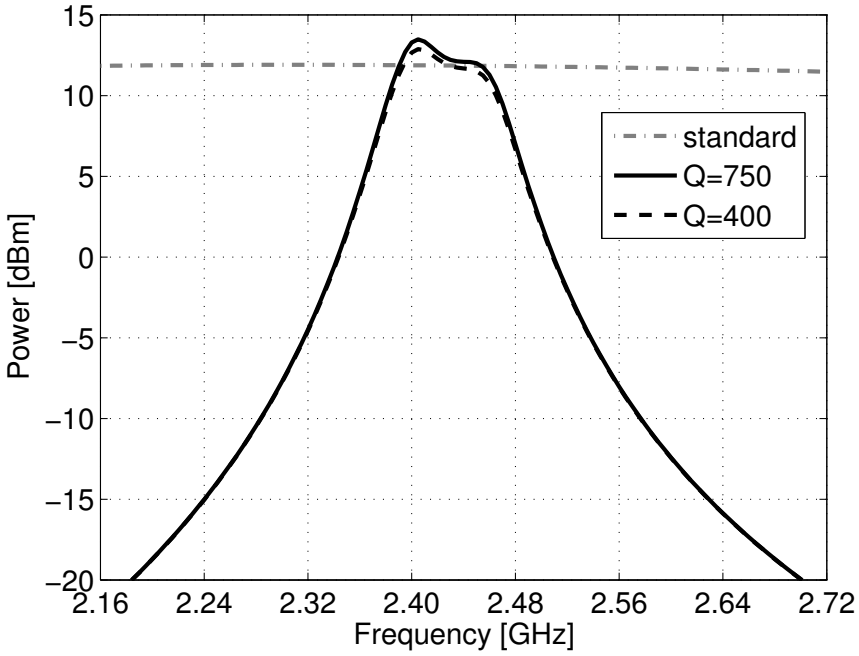


Figure 4.19: Comparison between the standard LC class BE PA and the BAW-based PA output power, simulated for resonators Q of 400 and 750.

equal to 1.4 dB. This is due to the fact that in the design example a maximum efficiency has been targeted, regardless of the filter impedance matching. This effect can present a disadvantage for the use of BAW filters in the power amplifier, since they are particularly sensitive to the impedance termination variations. This problem is addressed in the next chapter where the integrated version of the power amplifier is presented.

To demonstrate that the BAW-based PA still achieves the class BE behavior while integrating the BAW lattice filter in its passive network, the drain voltage and current time waveforms of one of the two amplifier branches are depicted in Figure 4.20 for a working frequency of 2.44 GHz.

4.4 Summary

In this chapter, a design approach for achieving co-integration between a power amplifier and BAW resonators has been presented. The design of a high efficiency power amplifier has been studied by using an analytical and a numerical model, to allow achieving an optimum design in case of presence of non-idealities like the on-chip integrated inductances and the transistor losses. The integration between the circuit side and the resonators has been described, and an example has proven its potential in terms of performance. The resulting amplifier allows achieving out-of-band suppression by substituting the LC series resonator of a class BE amplifier with a BAW lattice filter. At the same time, the BAW resonators participate in the drain voltage shaping and

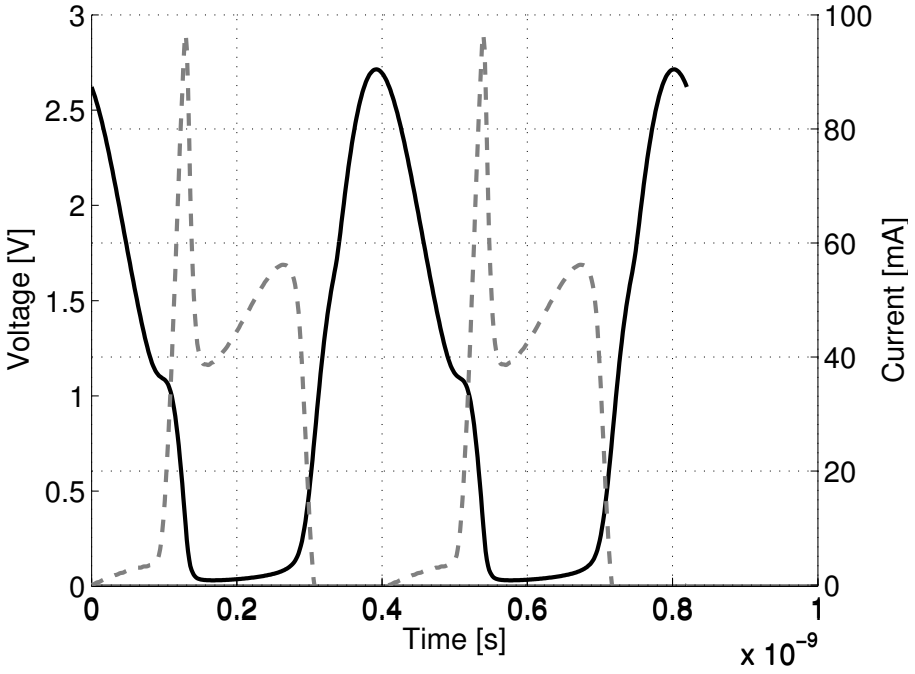


Figure 4.20: Single ended drain voltage (solid) and current (dashed line) of the BAW PA for BAW quality factor equal to 400.

allow achieving better efficiency than the classical amplifier implementation if $Q \geq 750$ are available.

Chapter 5

Transmitter Design

This chapter details the design of the blocks which constitute the transmitter architecture introduced in Chapter 3. The description is focused on the up-conversion transmission chain and its related blocks, starting from the selective amplifier and then addressing the design of the phase shifter and the single sideband mixer. Simulation results are presented, together with design and layout considerations. This transmitter implementation allows achieving the needed spurious signal rejection with the use of a single stage BAW filter, thus decreasing the insertion losses, which benefits the output power and efficiency. Finally, some of the blocks composing the frequency synthesis section are described.

5.1 System overview

The BAW-based transmitter, shown in Figure 5.1, has been designed with the aim to fully exploit the advantages that BAW resonators can bring in terms of phase noise and signal quality, while addressing multi-channel applications at the same time.

The synthesizer is mainly composed of a fixed frequency BAW oscillator and a variable IF ranging from 80 MHz to 160 MHz. This allows circumventing the reduced BAW LO tuning range, as seen in Chapter 3. In this new implementation, the IF generated by fractional division of the 2.32 GHz signal (divider N) is filtered by a LC PLL plus frequency divider (divider P). A low bandwidth ADPLL referenced to a temperature compensated silicon resonator (or an alternative 32 kHz crystal) is used to correct for the BAW drifts due to aging and temperature variations. The LO and IF signals generated in the synthesis section are then combined with a SSB mixer and selectively amplified by the power amplifier to provide a clean spectrum at the antenna.

The following sections detail the design of the selective amplification, quadrature generation and up-conversion.

5.2 Power Amplification

Once the IF signals are up-converted to the 2.4 GHz ISM band, power amplification has to be performed. Owing to the PA input gate capacitance, the up-conversion mixer will not be able to provide sufficient amplitude to drive the power stage correctly.

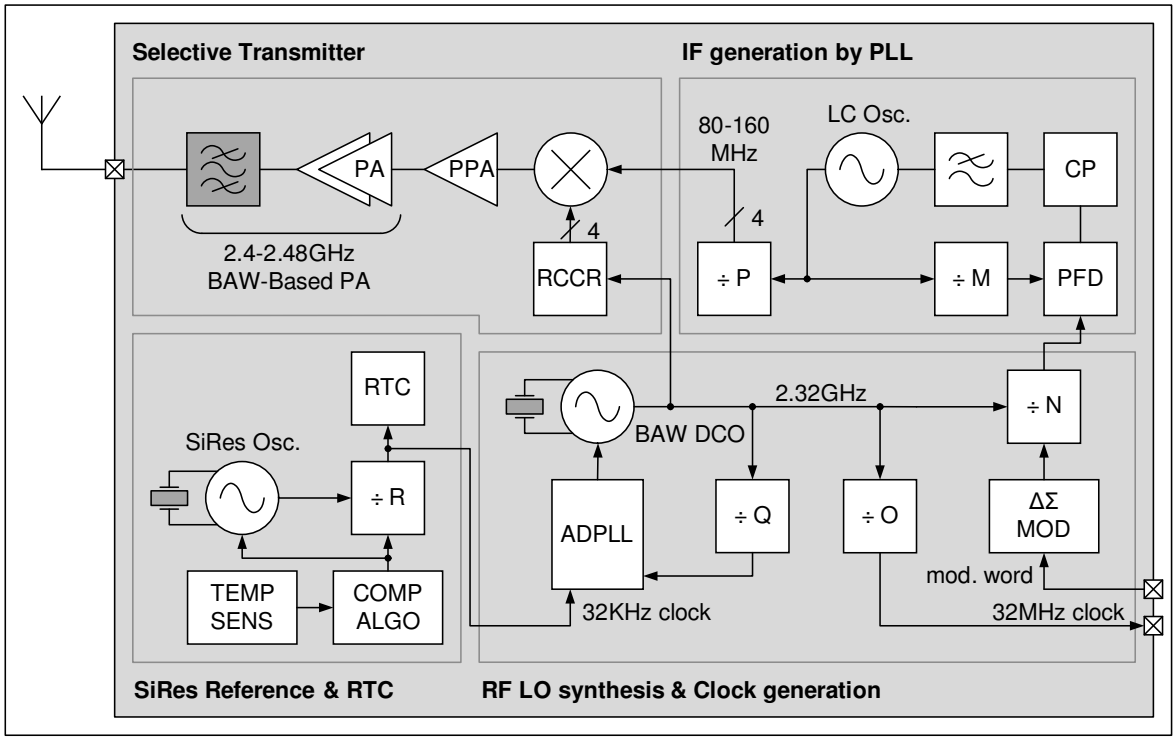


Figure 5.1: Complete architecture of the 2.4 GHz multi-channel BAW-based transmitter.

Consequently, the use of a pre-amplifier stage is necessary to achieve sufficient gain and lower the input capacitance seen by the up-converter. Due to the relatively low output power targeted for this transmitter, a good balance between the pre-amplifier and the PA consumption has to be found to preserve the overall transmitter efficiency.

5.2.1 Load impedance

The load impedance, one of the key parameters in the power amplifier design, is defined as the impedance the amplifier sees looking towards the antenna. Since impedance transformation is often used after the power amplifier, the load impedance is in general different from the antenna impedance. Normally, a transformation presenting a load impedance $R_L < R_{\text{ant}}$ is used, since it allows increasing the amplifier output power.

In case of a high efficiency switching amplifier, the output power in ideal condition is only dependent on the supply voltage and the load resistor. For an ideal class E power amplifier, this translates into the following formula [10]:

$$P_o = \frac{8}{(\pi^2+4)}\frac{V_{DD}^2}{R_L} \approx 0.5768\frac{V_{DD}^2}{R_L}, \tag{5.1}$$

where R_L is the load impedance. With a fixed amplifier supply voltage, the target output power can be achieved by finding the ratio between the antenna impedance and the amplifier load impedance. In the case of $R_L < R_{\text{ant}}$, the power enhancement provided by the impedance transformation network is given by [61]:

$$E = \frac{P_{o,t}}{P_o} = \frac{R_{\text{ant}}}{R_L}, \tag{5.2}$$

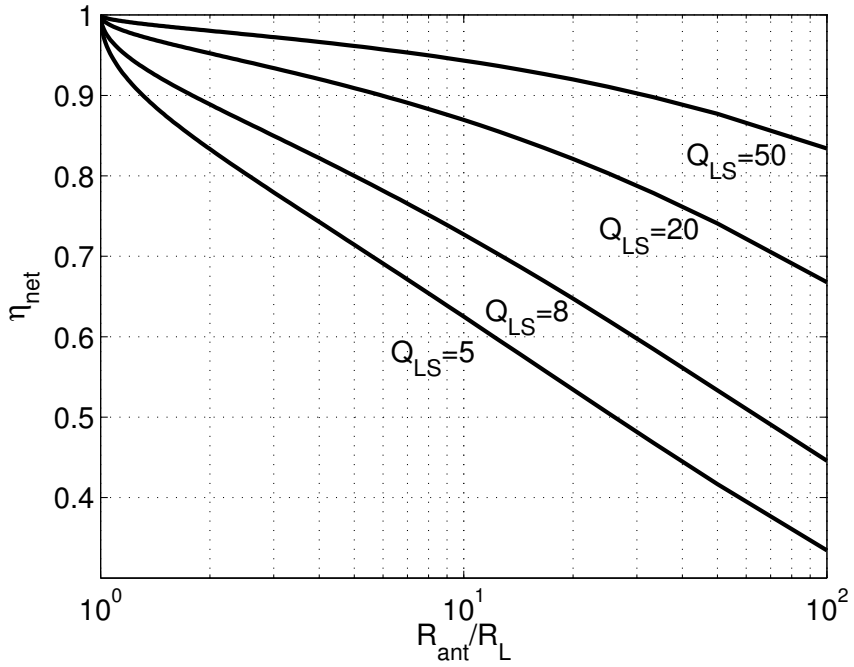


Figure 5.2: Efficiency of the L impedance transformation network versus the R_{ant}/R_L ratio, for different inductor quality factors.

where $P_{o,t}$ and P_o are the output power with and without the use of transformation network, respectively.

Even though an impedance transformation network can be used to achieve the wanted output power, it introduces losses which degrade the efficiency of the amplifying chain. For example, in the case of an impedance transformation provided with a simple L network integrated on-chip, the dominating losses come from the inductor series resistance R_{LS}. For low-pass LC transformation, the network efficiency can be written as:

$$\eta_{\text{net}} = \frac{R_L}{R_L + R_{LS}} = \frac{Q_{LS}}{Q_{LS} + Q_n}, \tag{5.3}$$

where Q_{LS} is the inductor quality factor and $Q_n = \sqrt{R_{\text{ant}}/R_L - 1}$. With an impedance ratio as low as 2 and an inductor quality factor of 8, the network efficiency is about 88%.

Figure 5.2 depicts the L matching network efficiency while varying the impedance ratio for different inductor quality factors. For integrated inductances and transformation ratios higher than two, at least 10% of the amplifier output power is wasted by the network. Since the overall amplifier efficiency is equal to $\eta = \eta_{\text{PA}} \cdot \eta_{\text{net}}$, it is clear that higher the transformation ratio, the lower the efficiency will be. The network losses could be considerably reduced by using high-Q external components, but this contradicts the miniaturization requirements set for the BAW transmitter.

5.2.2 BAW filter impedance

The choice of the filter impedance is determined by a trade-off between the filter overall dimensions and the need for additional components to match with the circuit and the antenna impedances.

Since the BAW filter impedance is basically determined by the dielectric capacitance C_p through the resonator physical dimensions, as indicated in (3.3), targeting low impedance filters implies a high area occupancy. If a 50 Ω resonator covers a surface of about 15,000 μm^2, a 25 Ω resonator occupies an area of 30,000 μm^2, which is the surface normally needed for an integrated inductance. Moreover, each single resonator used in the filter is split in two (or in four, depending on the implementation) series elements with lower impedance. This allows having easy access to the resonator pads and facilitates the resonators connectivity, which can be performed with thick top aluminum metal interconnections, but further increases the area.

Compact filter implementations thus require the use of high impedance resonators, but the advantage of the lower area is counterbalanced by the need of additional components to match with the antenna impedance. As seen previously, this cause the efficiency to decrease.

Taking into account these considerations, a 100 Ω differential BAW lattice filter has been chosen for the BAW-PA implementation. In fact, it represents a good compromise between overall filter dimensions and performance; moreover, by using standard impedances, the in-house filter could be more easily replaced with high volume BAW filters produced by industrial suppliers. In the ideal application, the filter will be connected to a differential antenna with impedance equal to 100 Ω without the need of any additional components, while in the case of a standard 50 Ω single ended antenna, a common SMD balun will be used to perform balanced to single ended transformation.

5.2.3 Supply voltage

For a fixed load resistance, the output power of a switching amplifier is proportional to the square of the supply voltage V_{dd} only, as shown in (5.1). Since the efficiency of a class E amplifier is, in theory, constant over the supply voltage [62], it is thus preferable to set the amplifier output power by properly choosing the supply voltage, instead of using impedance transformation.

With a nominal supply voltage equal to 1.8 V (TSMC 0.18 μm CMOS technology) and a differential load impedance of 100 Ω, the theoretical output power reached by a class E differential amplifier is 19 dBm. As a consequence, a decrease of the supply voltage would be sufficient to allow reaching the maximum output power targeted for the wireless sensor application. By inverting (5.1), the calculated supply voltage needed to achieve an output power of 10 dBm is equal to 0.66 V. This is obviously an underestimated value, since in reality, owing to the transistor and passive elements losses, a class BE amplifier will present reduced drain voltage swings with respect to an ideal class E design. As a consequence, a higher supply voltage will be needed to ensure a maximum output power of 10 dBm.

Finally, the maximum allowable amplifier supply voltage is limited by reliability constraints. In power amplifiers the possible failures may come mainly from three

different sources: *hot carrier injection*, *junction breakdown* and *oxide breakthrough*. They are briefly explained below.

- **Hot carrier injection** occurs when carriers (electrons or holes) exceeding the energy barrier between the silicon substrate and the silicon dioxide film are injected to the gate oxide film. This needs high electric fields and thus happens at the drain end. This effect results in increased device threshold voltage, degrading the amplifier performance [63].

- The drain **junction breakdown** is a destructive phenomenon. In case of zero drain current, the breakdown drain voltage of a CMOS technology is typically in between two to three times the nominal supply voltage, i.e. $3.6\,\mathrm{V} < V_{\mathrm{dbrk}} < 5.4\,\mathrm{V}$ for a 0.18 μm CMOS technology, thus requiring attention if high voltage swings are present on the device drain.

- The **oxide breakthrough** is another destructive phenomenon occurring when the field across the oxide approaches its critical value (∼1 V/nm); it thus forces to take care of the transistor drain-gate swing during operation. Conservative designs tend to limit this swing to maximum 2 V_{dd_nom} to ensure long device lifetime [64]. V_{dd_nom} is the nominal technology supply voltage.

For an ideal class E power amplifier, which can theoretically achieve drain peak voltages as high as $3.57 \cdot V_{dd}$, these limitations translate into the following requirements. From the drain breakdown constraint, the amplifier supply voltage V_{dd} should be:

$$V_{dd} \leq \frac{2V_{dd\_\mathrm{nom}}}{3.57} \approx 1\mathrm{V}, \tag{5.4}$$

for a $V_{dd\_\mathrm{nom}} = 1.8\mathrm{V}$. By assuming that the waveform driving the power amplifier has a peak to peak swing equal to V_{dd_nom} and the amplifier is polarized at 50% duty cycle, i.e. the input waveform DC value is equal to the transistor threshold voltage, the maximum drain-gate voltage that the transistor can experience is

$$V_{DG\_MAX} = 3.57 \cdot V_{dd} - V_{th} + \frac{V_{dd\_\mathrm{nom}}}{2}. \tag{5.5}$$

The constraint on the power supply is hence:

$$V_{dd} \leq \frac{1.5V_{dd\_\mathrm{nom}} + V_{th}}{3.57} \approx 0.64\mathrm{V}, \tag{5.6}$$

with $V_{th} = 0.4$ V. The oxide breakthrough is thus the requirement that limits most the class E amplifier output power. Concerning the hot carrier injection phenomenon, the ideal class E power amplifier shows a complete immunity to this problem since there is theoretically no overlap between the non-zero portions of the drain current and voltage waveforms. Even if a certain overlap is present in practical class E (and more in class BE) implementations, the drain voltage value is in general of the order of some hundreds of millivolts when the switch is on, allowing the hot carrier injection degradation to be neglected.

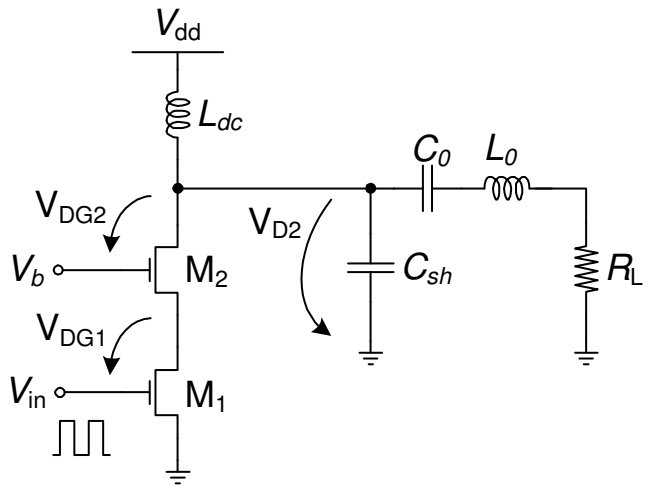


Figure 5.3: Cascode class E amplifier.

It is interesting to see that, with the maximum supply voltage calculated for safe operation, the output power achievable with a differential load of 100 Ω is equal to 9.7 dBm in ideal class E operation, which is too low with respect to the target maximum output power, especially taking into account the losses. Since the impedance transformation network has to be avoided not to impact the efficiency and to limit the additional passive components, limiting the integrability, another possibility to reach the wanted output power is to increase the amplifier supply voltage. This can be done without impacting the reliability by using a cascode amplifier implementation [65, 66].

5.2.4 Cascode switching amplifier

A cascode switching amplifier is composed by a combination of a common source stage with a common gate, as normally done for the cascode amplifier. Figure 5.3 depicts the schematic of the class E cascode amplifier. During operation the common source transistor acts as a simple switch owing to the hard driving action of the input waveform. If the voltage reaches sufficiently high values, the common gate transistor is also switched, provided the cascode bias voltage V_b is high enough to put transistor M2 in triode region.

The use of the common gate stage has the big advantage of decreasing the drain-gate stresses with respect to a standard class E switching amplifier. As done before, let us assume to have an input waveform with peak-to-peak swing equal to V_{dd_nom} and a DC value equal to V_{th}. Thanks to the cascode implementation, the maximum swing experienced now by the lower device is

$$V_{DG1\_\mathrm{MAX}} = V_b - 2V_{th} + \frac{V_{dd\_\mathrm{nom}}}{2}, \tag{5.7}$$

where V_b is the common gate transistor bias voltage. This value is considerably lower than that indicated by (5.5). On the other hand, the swing between the gate and the drain of transistor M2 is given by:

$$V_{DG2\_\mathrm{MAX}} = 3.57 \cdot V_{dd} - V_b, \tag{5.8}$$

which also is reduced with respect to that of the standard class E amplifier.

A possible way to choose V_b is to balance the oxide stress equally on the two devices, solving $V_{DG1\_MAX} = V_{DG2\_MAX}$. The optimum cascode bias voltage (from the reliability point of view) is thus given by

$$V_b = 1.79 \cdot V_{dd} + V_{th} - \frac{V_{dd\_nom}}{4}. \tag{5.9}$$

By substitution of (5.9) into (5.7) or (5.8) and using the reliability constraints used in the previous paragraph, the condition on the supply voltage imposed by the oxide breakdown becomes now:

$$V_{dd} \leq \frac{2.25 \cdot V_{dd\_nom} + V_{th}}{1.79} \approx 2\text{V}, \tag{5.10}$$

which is more than three times higher compared to the limitation imposed by the standard amplifier.

While the requirements due to oxide electric field limitations are much more relaxed for the cascode amplifier, the constraint set by the junction breakdown remains the same compared to the standard class E, since the drain junction of M2 suffers the same swing as for the case of a common source transistor amplifier. As a result, this limitation becomes dominating for the cascoded amplifier reliability.

5.2.5 BAW Power Amplifier optimization

Since the load and the filter impedances have been chosen, the other amplifier parameters which have to be addressed are the transistor widths (common source and common gate transistors) and the finite DC inductance. Optimizing the power amplifier efficiency over these parameters basically corresponds to performing the efficiency analysis described in Chapter 4 in the (C_{sh}, L_{dc}) design space.

The most important difference is represented here by the fact that the amplifier shunt capacitance is now shared in between the drain capacitance of the common gate transistor and the resonator dielectric capacitance C_p, as demonstrated by transformation of the lattice filter with the use of the Mason's equivalence (Section 4.3.2).

Before presenting the results of the optimization procedure, the different parameters which depend on the width of the active devices will be briefly described. This will give the information needed to understand the mechanisms which have driven the optimization.

On-resistance

For hard driven devices, the transistor loss is determined by its on-resistance R_{on}. This can be calculated, provided the transistor is biased in the triode region, with the formula:

$$R_{on} = \frac{1}{\mu_n C_{ox} W/L \, (V_{gs} - V_{th} - V_{ds}/2)}, \tag{5.11}$$

which shows how the transistor ohmic losses are minimized by choosing the minimum gate length allowed by the technology and the maximum possible width.

In the cascode power amplifier implementation, also the losses related to the common gate transistor participate in the power dissipation, roughly doubling the active device losses.

Drain capacitance

In Section 4.3.2 we have seen that the transistor drain capacitance participates in the absorption of the amplifier design parameter C_{sh}. In the case of a cascode amplifier implementation, the drain capacitance comprises the drain junction capacitance C_{db2} and the overlap capacitance C_{gd2}. Neglecting the dependence on the junction reverse biasing, the drain junction capacitance of transistor M2 can be written as the sum of two different contributions:

$$C_{db2} = C_b + C_{sw} = C_j L_s W_2 + C_{jsw}(2L_s + W_2). \tag{5.12}$$

The parameters C_j and C_{jsw} are the junction capacitance per area and per length respectively; L_s represents the diffusion length and W_2 is the width of the transistor M2.

The drain capacitance depends on the transistor layout and it should also include the parasitic capacitance due to the drain connections. Consequently, it is particularly important to have at least an idea of the amplifier floorplan already at the design phase.

Gate capacitance

Normally the input gate capacitance of the power stage is not a switching amplifier design parameter, since it has no impact on the performance. However, the amplifier gate capacitance determines the preamplifier power consumption, which can heavily degrade the transmitter overall efficiency for low output power. For this reason the gate capacitance has to be carefully taken into account.

If we assume to drive the PA stage with an inverter, the driver power consumption can be written as function of the gate capacitance as

$$P_{PPA} = C_g f V_{dd}^2, \tag{5.13}$$

f being the working frequency. The gate capacitance can be approximated by:

$$C_g = \frac{2}{3} C_{ox} W_1 L + 2 C_{ov} W_1, \tag{5.14}$$

where W_1 is the width of the common source transistor, C_{ox} is the oxide capacitance per unit area and C_{ov} is the overlap capacitance per width.

Amplifier optimization

The BAW-based cascode amplifier schematic is depicted in Figure 5.4, where both the lattice filter and the load differential impedances are equal to 100 Ω. Only one of the two parallel resonators is shown in the figure for simplicity.

The optimization procedure is presented for the particular case of $W_1 = W_2$, which allows an easy interpretation of the simulation results. The BAW filter behavior is

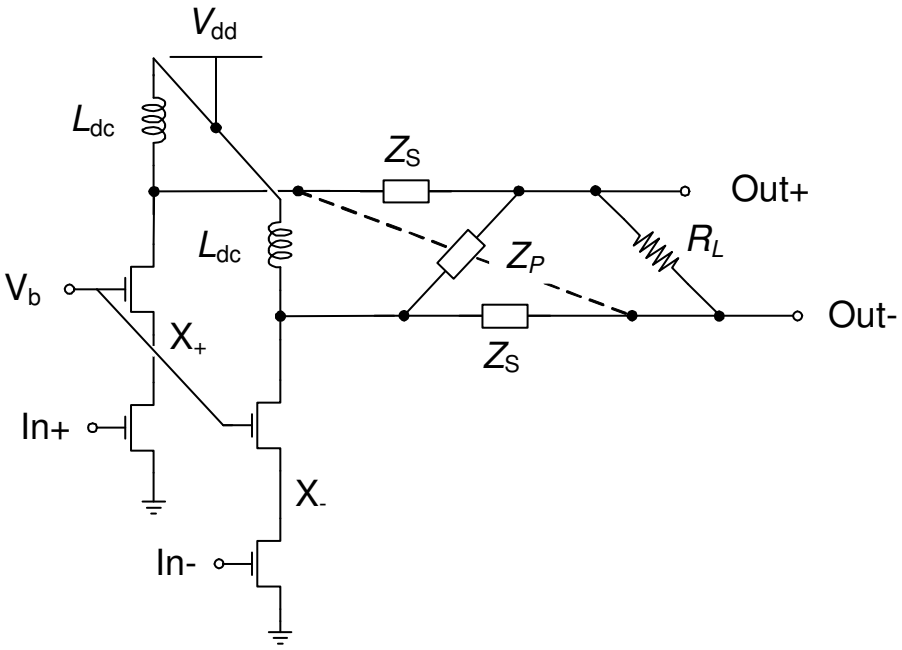


Figure 5.4: BAW-based cascode amplifier implementation.

approximated with lumped element models of the intrinsic resonators having a quality factor equal to 400. The amplifier design space, represented by the DC-feed inductor L_{dc} and the transistor width W, is analyzed to find the optimum design point which allows achieving the maximum efficiency value.

Figure 5.5 shows the locus of optimum transistor widths for a sweep of the DC feed inductor. For each point, the supply voltage has been chosen in order to achieve the maximum output power of 10 dBm. This plot basically corresponds to the extracted efficiency crest over the (C_{sh}, L_{dc}) design space which was presented in Chapter 4. As a consequence, all these points represent designs with different efficiency values. The plot confirms that the use of low feed inductances enable higher shunt capacitance values (and thus higher transistor width), which are beneficial for decreasing the amplifier ohmic losses.

To allow choosing the optimum design point, the amplifier efficiency is then plotted in Figure 5.6 as function of the transistor width only. The particular behavior of the drain efficiency curve (solid line) can be explained intuitively by referring to the design parameters aforementioned.

Starting from low device width, the losses caused by the on-resistors decrease for an increase of W, causing an increase of the amplifier drain efficiency. Then, once the transistor losses become negligible compared to the others sources (and mainly to the loss of the DC inductor with a Q of 8 in this case), the amplifier efficiency starts to saturate. Finally, if the transistors width is further increased, the efficiency decreases. This effect is enhanced by the presence of parasitic capacitances at the nodes X (in Figure 5.4), which have to be charged and discharged for every cycle of the input waveform, decreasing the amplifier efficiency.

The drain efficiency curve still does not take into account the power consumption

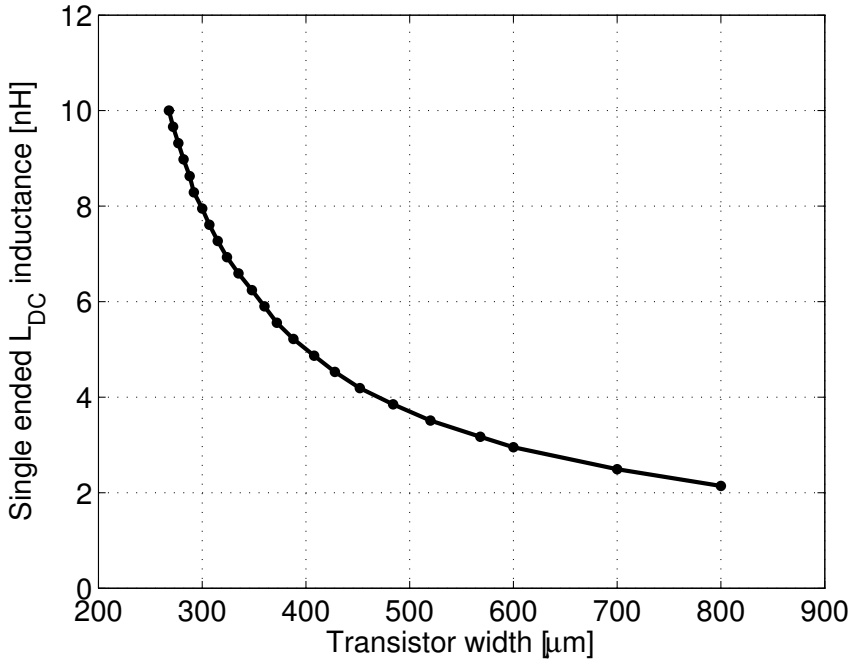


Figure 5.5: Finite DC inductor value as function of the transistor width, targeting for the maximum efficiency.

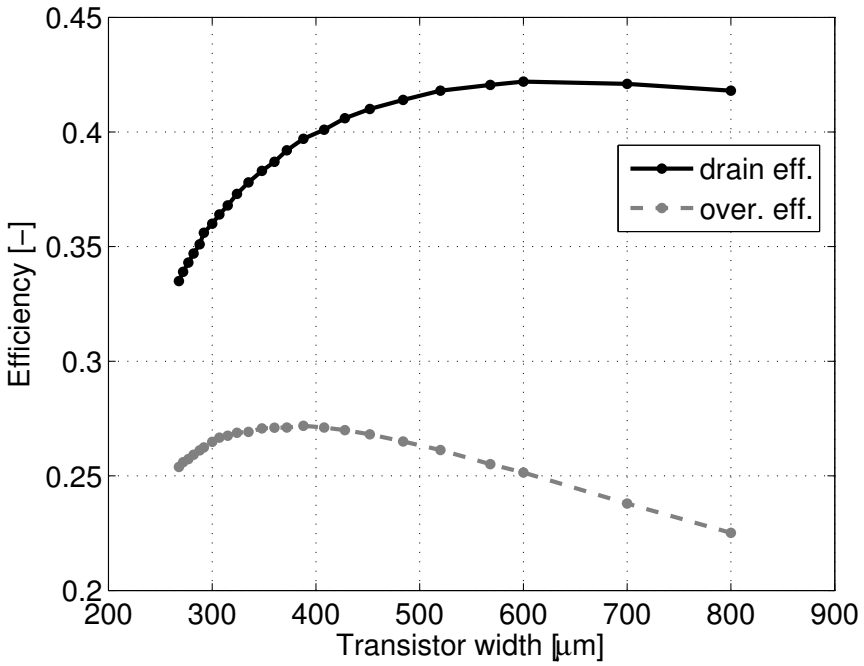


Figure 5.6: Drain and overall efficiency of the BAW-based PA as function of the transistor width.

required by the preamplifier to drive the amplifier gate capacitance. To demonstrate that this contribution can be important for a power amplifier targeting relatively low output power, the preamplifier plus power amplifier overall efficiency is also depicted in Figure 5.6, assuming that the preamplifier is used to drive the PA with a buffer whose power consumption is given by (5.13). In the first part of the curve the increase of the drain efficiency due to reduced amplifier ohmic losses is still dominant compared to the preamplifier consumption, causing an increase of the overall efficiency. For higher transistor widths the power needed to drive the PA gate capacitance starts to compensate the drain efficiency improvement, up to when a peak in the overall efficiency curve is reached. Starting from this point, the driver consumption completely dominates the other effects, producing a decrease of the overall efficiency.

The transistor width for which the highest possible overall efficiency is achieved is lower than that found for the maximum drain efficiency, for an output power of 10 dBm. For even lower output power, the overall efficiency optimum decreases in value and moves towards lower PA transistor widths, eventually showing the obvious conclusion that the use of a preamplifier is not suitable for very low output power, provided the target power can be achieved with only one amplification stage.

The BAW-based power amplifier has been designed for achieving the maximum overall efficiency at the highest output power. This choice in fact allows to minimize the maximum peak current that can be drawn by the transmitter, which is related to the power and current capabilities of the battery (or voltage regulator) supplying the chip.

Figure 5.7 shows the simulated waveforms of the class BE power amplifier designed for achieving the maximum overall efficiency. The amplifier drain voltage waveform follows a time behavior similar to that of a class BE PA, achieving the maximum drain voltage value during the half-cycle for which the two MOS switches are off. In reality during this lapse of time some current still flows into M2 (which is in saturation region) to charge the parasitic capacitance at its source. As a consequence, the maximum source voltage is equal to $V_{sc} = (V_b - V_{th})/n$. Then, when the drain voltage descends at about 1.1 V, the input causes the common source transistor to conduct. It behaves as a current source for a short duration, while the cascode transistor is already in triode region. During this period, the charge stored in the shunt capacitance is discharged towards ground. Once the drain voltage decreases sufficiently, the transistor M1 enters into the triode region, where it remains up to the end of the switch-on half-cycle.

From inspection of the voltage waveforms it can be seen that a maximum peak voltage of 2.65 V is achieved in this stacked implementation, for an amplifier supply voltage of 1 V. This allows to set the bias voltage of the cascode transistor to the nominal supply voltage V_{dd_nom} without impacting the transistor reliability. The maximum drain-gate voltage across M2 occurs when both the transistors are in the triode region and is equal to about 1.7 V, while the maximum drain-gate voltage experienced by M1 corresponds to about 1.6 V ($V_{dd\_\mathrm{nom}} = 1.8\ V$ and $V_{th} = 0.45\ V$) and occurs when the transistors are both in their off-state. Since the drain swing is lower than $2 \cdot V_{dd\_\mathrm{nom}}$, the junction breakdown requirement is also satisfied.

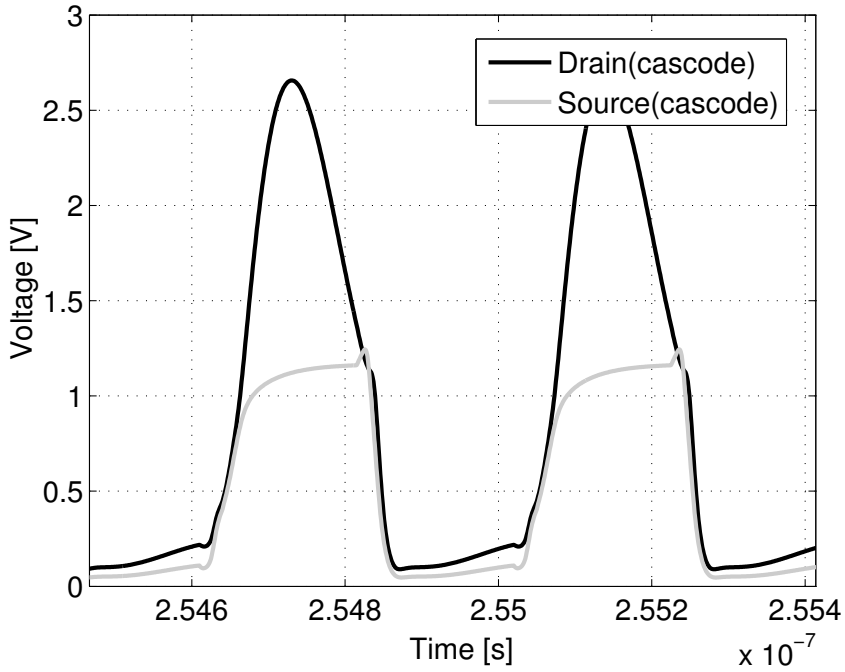


Figure 5.7: Transient simulation of the cascode class BE power amplifier.

Power control

With an amplifier maximum output power of 10 dBm, some power control should be implemented to allow covering a sufficiently wide output power range. The freedom to regulate the output power allows in fact energy savings when the distance to be covered is reduced and it is not necessary to transmit at the maximum output power.

For ideal class E amplifiers the drain efficiency is constant over the whole range of supply voltage, hence the output power is usually controlled by varying the supply [59]. This technique is also used to amplify signal in variable envelope modulation schemes, for which the low bandwidth amplitude information is used to modulate the amplifier supply voltage [67], transferring the amplitude information to the envelope of the RF signal.

Nevertheless, in the implemented amplifier, the presence of stacked transistors causes the efficiency to decrease for low supply voltage, decreasing from 40% to about 28% while passing from 1.0 V to 0.6 V supply. To keep the supply voltage unchanged while allowing to control efficiently the amplifier output power, a different technique has been used. The output power is controlled by varying the DC input voltage of the amplifier input waveform. Consequently, the maximum output power is achieved by ensuring the amplifier working in class BE operation (with a conduction angle equal to π) while for low output power, the DC value of the input waveform is gradually reduced and the power amplifier can be thus considered as a reduced conduction angle amplifier. In particular, a behavior similar to that of a class C amplifier is achieved for low biasing voltage, which allows us to take advantage of the good efficiency this class can offer for low output power (see Section 2.1.3).

The circuit used to control the amplifier output power is shown in Figure 5.8. A

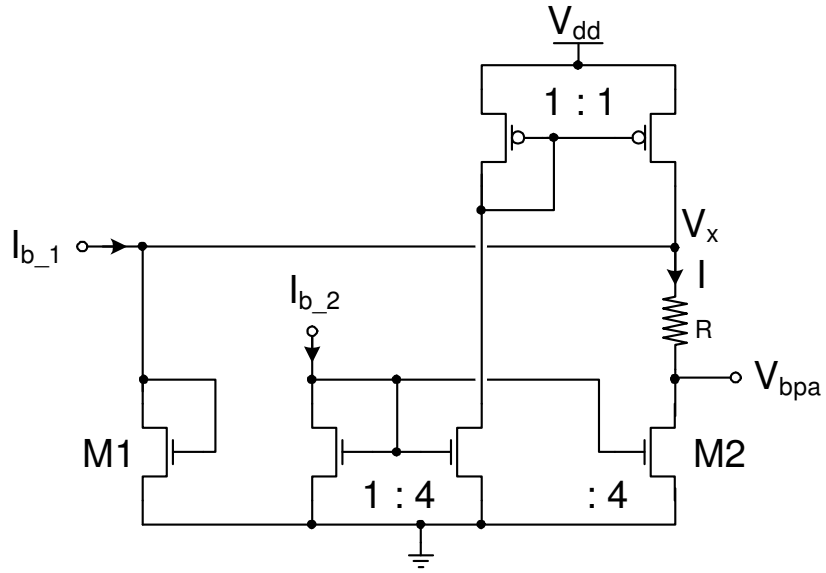


Figure 5.8: Schematic of the biasing circuit used to set the power amplifier operating condition.

DC bias voltage V_x is generated by injecting the current I_{b_1}, programmed with a DAC, into the diode connected transistor M1. Then a second current DAC sets the voltage drop across R, which determines the final value of the PA polarization V_{bpa}. This allows controlling the bias voltage linearly with the programmed current I_{b_2}, down to when the saturation voltage of M2 is approached. Since this biasing circuit allows the DC voltage going below the threshold voltage of the NMOS transistor, it is particularly suitable for biasing of reduced angle amplifiers.

5.2.6 Preamplifier Design

Bluetooth switching power amplifiers are in general driven by a cascade of inverters [68], properly sized to charge and discharge the PA transistor gate capacitance at the wanted operating frequency. This solution is generally suitable for high output power (e.g. for class 1 Bluetooth, which requires 20 dBm output power), where the consumption of some tens of milliwatts of the preamplifier stage does not impact heavily the amplifier overall efficiency. Similarly, in [1], a three stage preamplifier with feedback loop is used to drive a 10 dBm output power stage. Also in this case the consumption is not negligible, corresponding to 7 mW at 433 MHz (0.5 μm CMOS technology). A similar pseudo-differential preamplifier designed in 0.18 μm technology and working at a frequency of 2.4 GHz needs in simulation about 6 mW to drive a load capacitance of only 100 fF.

Since for low output power the preamplifier contribution to the overall consumption becomes dominant, it is absolutely necessary to find a way to reduce it. Consequently, a single stage inverter with tuned load has been used. This choice allows maintaining a simple architecture while decreasing the preamplifier capacitive load, thanks to the use of an integrated inductance designed to resonate with the power stage gate capacitance.

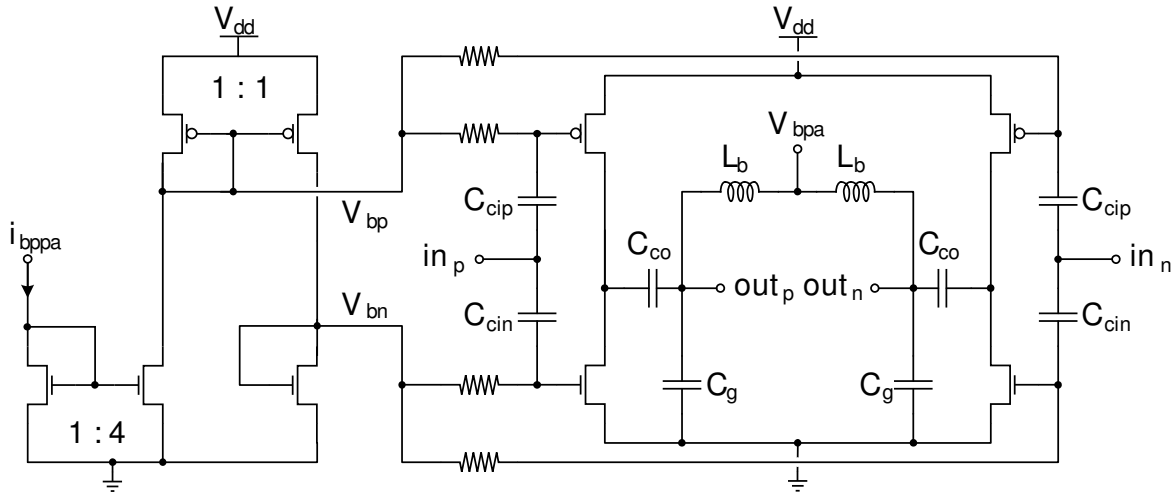


Figure 5.9: Preamplifier transistor level schematic, with bias.

The PA input impedance thus increases and the driver power consumption can be reduced for the same voltage swing.

Apart from the advantage of the power consumption reduction, the use of a resonating load allows also to perform weak filtering on the spurious content present at the SSB mixer output, which helps to reduce the preamplifier non-linearities. The main drawback resides instead on the area needed to integrate the inductor.

Figure 5.9 depicts the preamplifier implementation. The gain is provided by a single stage complementary class AB amplifier, working usually at the edge of the moderate inversion (IC = 10). The amplifier voltage bias is controlled by a programmable input current in conjunction with series resistors. The bias voltages are controllable in such a way to reduce the crossover distortion typical of complementary amplifiers by biasing the transistors far enough from the subthreshold region.

Series metal-to-metal interdigitated capacitors C_{ci} have been used to couple the input signal to the preamplifier. Owing to their high Q, which is higher than 80 [69] at 2.4 GHz, they are the only integrated capacitors used for RF signal coupling in the implemented circuits. As disadvantage, their capacitance density per area is rather low, thus requiring a large area. Typically capacitance densities in between 0.65 fF/μm^2 and 1.3 fF/μm^2 are achievable depending on the number of metal layers used.

When designing the coupling, the associated parasitic capacitance has to be taken into account, appearing in parallel to the block input capacitance and thus causing signal attenuation. By assuming to use a coupling capacitance equal to nC_{in} (where C_{in} is the input gate capacitance of the driven transistor) with associated parasitic capacitance fraction p (percentage of the coupling capacitor nominal value), the normalized output signal amplitude can simply be calculated by the following expression:

$$A = \frac{n}{n + np + 1}. \tag{5.15}$$

Figure 5.10 depicts the signal amplitude after capacitive coupling for increasing n and p equal to 2, 5 and 10%. By dimensioning the coupling capacitor ten times higher than the equivalent gate capacitance to be driven, the signal attenuation is confined

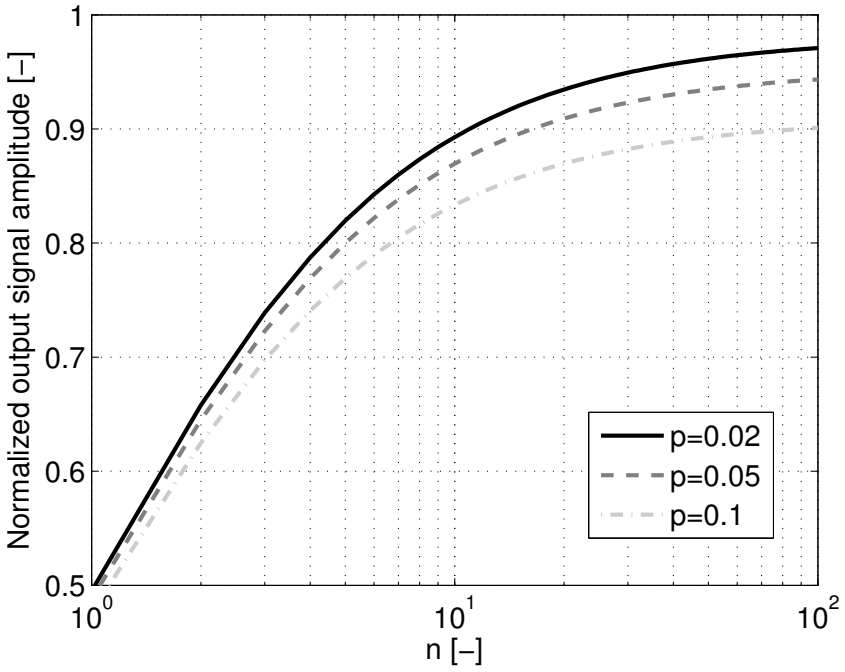


Figure 5.10: Signal amplitude attenuation vs. coupling capacitance value over load capacitance ratio, for three different parasitic capacitance contributions.

Table 5.1: Preamplifier simulated performance.

Parameter	Value	Units
Supply voltage	1.6	V
Current consumption	1.22	mA
Power consumption	1.95	mW
Voltage gain	10.7	dB
Input ref. 1 dB compression point	175	mV
Input referred IP_3	590	mV

between 11 and 17%. As a rule of thumb ratios higher than ten should always be used, even if the choice can strongly be influenced by the surface occupancy.

The RF preamplifier, including metal-to-metal finger capacitors and inductor models, has been simulated at frequencies in the 2.4 GHz ISM band. In order to reach the output peak voltage needed to strongly drive the power stage, the preamplifier needs to work slightly above than its 1 dB compression point. The preamplifier simulation results are presented in Table 5.1, where all the voltage amplitudes presented are single ended peak values.

One of the class E power amplifier hypothesis is that the power stage input waveform is driven by a square wave, in such a way the transistor can be quickly switched from the off to the on state and vice versa. It is interesting thus to check whether the use of

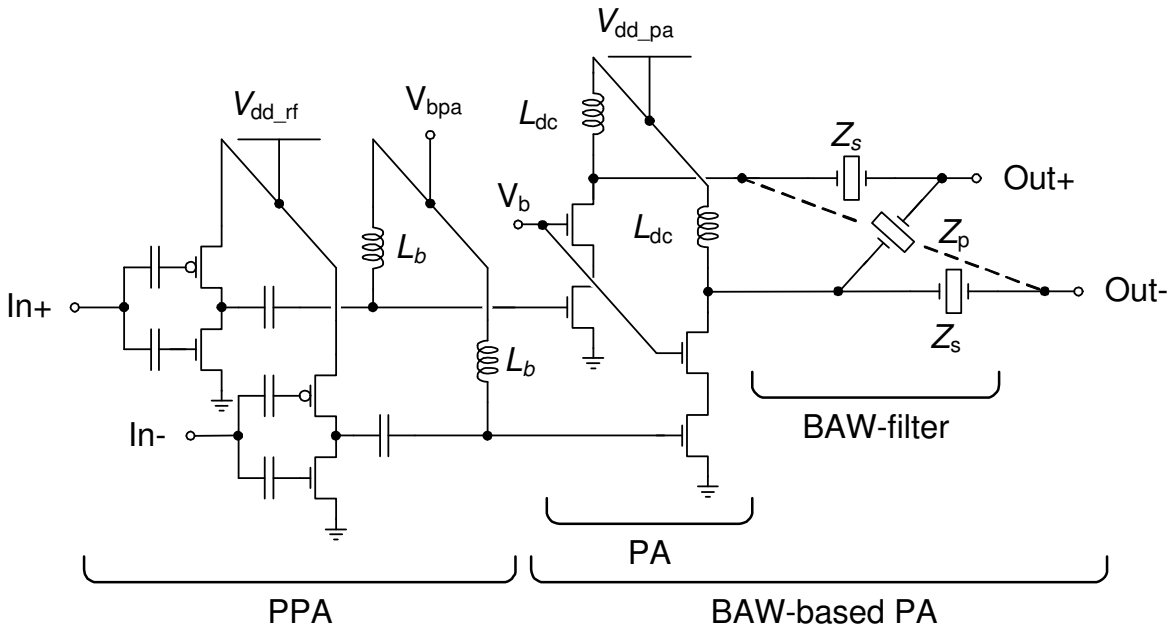


Figure 5.11: Schematic of the complete amplifying chain. Biasing circuit not shown.

the tuned load decreases the PA drain efficiency, since the waveform driving the power amplifier approaches a rail to rail sinusoidal waveform rather than a steep slope square wave signal.

Transistor level simulations demonstrate that for the implemented power amplifier the shape of the waveform driving the power stage has no big effect on the drain efficiency. Values of η equal to 41% and 38% have been found using a rail to rail inverter and the proposed preamplifier respectively. On the contrary, the overall efficiency of the amplifying chain benefits from the reduced tuned preamplifier power consumption, increasing from 27% in the case of classical inverter solution to 35% with the implemented preamplifier, for an output power of 10 dBm.

5.2.7 Simulation testbench of the amplifying chain

The amplifier optimization previously presented has been performed with the amplifying chain in an ideal environment. This means that, even if the different losses of the power amplifier had been taken into account, no other nonidealities linked to the amplifier environment were present.

In between them, the lines connecting the amplifier to the pads, the number of pads and bonds devoted to the supplies, the pads and bond parasitics are some of the most important parameters that have to be included in a simulation testbench in order to gather more realistic information on the amplifier performances. Moreover, adding those parasitics is the only means of having a reliable information on the amplifier stability, which is strongly dependent on its surroundings.

Testbench

The amplifier design has been validated by using a complete simulation testbench taking into account the signal line losses, pad parasitics, supply and bonds. In addition, an S parameter file resulting from measurement of a BAW lattice filter has been included in the simulations to model the power amplifier load. These simulations have been then used to refine the design towards the final amplifier implementation. The testbench block diagram is depicted in Figure 5.12. This configuration reflects the layout implementation of the testchip used to benchmark the amplifying chain alone.

In the simulation testbench the preamplifier and power stage have been loaded with models of differential inductors taken from the CSEM RF library and adapted to the particular inductance values needed for the design. These models fit the frequency behavior of measured inductor with a lumped element $\pi-$type network similar to that presented in [70] for differential spiral transformers. The central tap of the first inductor has been used to bias the amplifier power stage, while the central tap of the second inductor provides the supply to the power amplifier.

To model the losses due to the signal and supply lines a simple RL series network with values proportional to the line length has been used. Two capacitances towards ground (not shown in Figure 5.12) model the coupling to the ground plane. The pads have been modeled by calculating their intrinsic capacitance to ground taking into account their dimensions. To model the drain capacitance of the MOS ESD protection, an NMOS instance with gate tied to ground and same dimension of the device used for providing the protection has been added in parallel to the pad intrinsic capacitance.

To allow a compact layout and the easy integrability into the transceiver chip, only one ground pad and two supply pads have been used in the testchip implementation. This decision impacts the power amplifier performance since the impedance in series with the supply is not negligible.

To estimate the bond influence on the amplifier design, a lumped element network has been used. A simple analytical model computes the resistance and inductance of the wire bond, together with the couplings with the neighbor parallel bonds (see Appendix B). The calculated values are then used in the lumped element network depicted in Figure 5.13, which is scalable for multiple parallel bonds. Transistor level simulation showed that a bond of 0.5 mm for the ground and two bonds of about 1 mm were acceptable values and did not generate any potential instability.

For a more precise estimation of the bonds influence on the amplifier design, one of the several advanced models presented in the literature could be used. For example, the model described in [71] takes into account geometrical parameters like the wire span, the elevation difference between the wire bonds and the maximum wire loop height. However, these models need the use of electromagnetic finite element solvers and a precise knowledge of the bond geometry.

Testbench simulation results

Figure 5.14 depicts the frequency selectivity of the amplifying chain composed by the preamplifier plus BAW-based power amplifier. It has been extracted with the described testbench by sweeping the frequency of the preamplifier input signal. A maximum

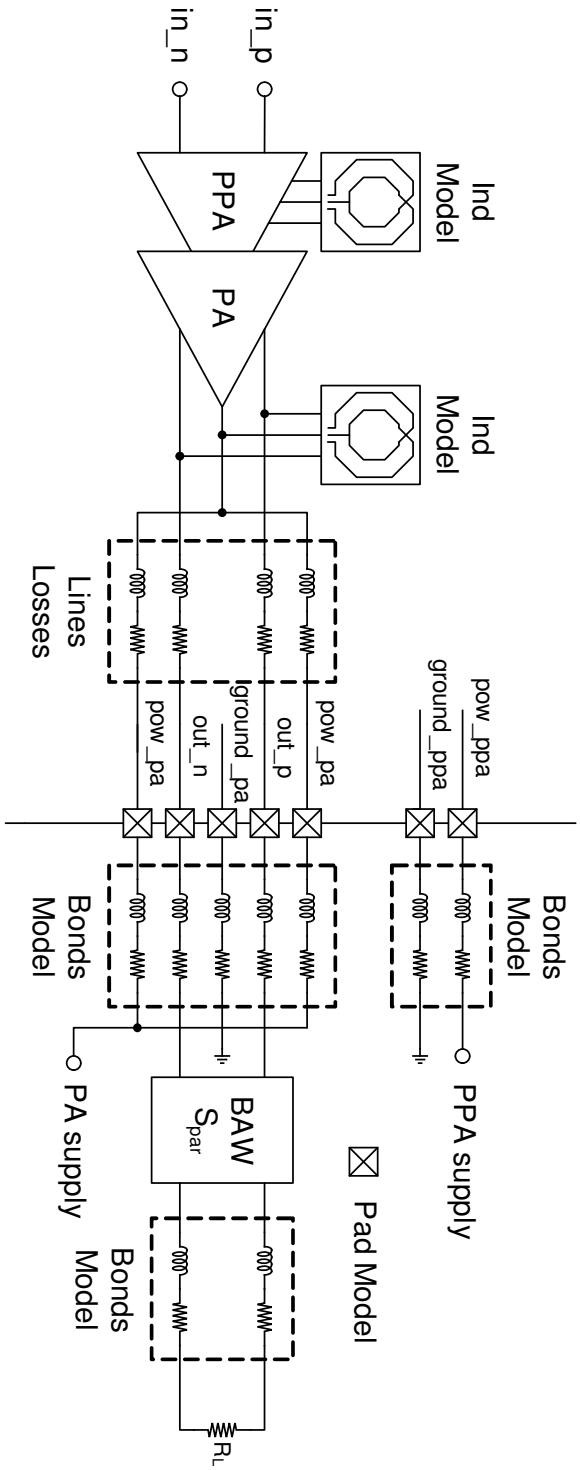


Figure 5.12: Amplifying chain test bench.

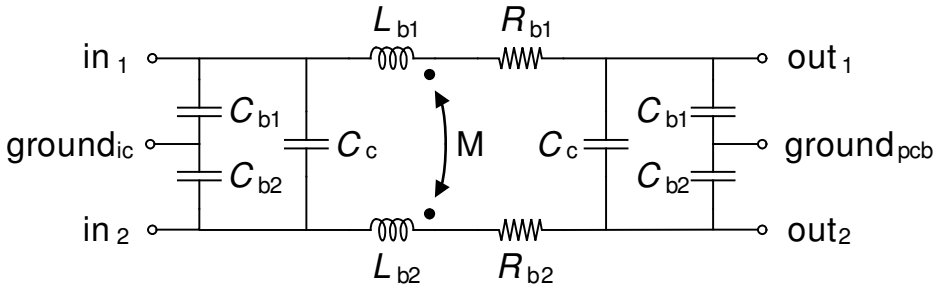


Figure 5.13: Lumped element model for two parallel bonds.

output power of 8.8 dBm has been found, for an in-band ripple corresponding to 1.1 dB. The simulated 3 dB bandwidth, measured with respect to the curve maximum, is 102 MHz. The filter center frequency is at 2.422 GHz, 18 MHz lower than the expected value of 2.44 GHz.

Even though the filter, being shifted in frequency, does not match exactly the 2.4 GHz ISM band, the suppression provided by the selective amplifier is still effective. For the worst case of $f_{if} = 80$ MHz, the suppression referred to the in-band power corresponds to about 23.7 dB at the image frequency and 19.7 dB at the spurs due to the IF 3^{rd} harmonic. This would need the SSB mixer to provide at least 15.3 dB and 9.8 dB rejection respectively for these two frequencies to comply with the -30 dBm spurious requirements.

The filter shape, slightly bent towards low-frequencies, indicates a non perfect impedance matching at the BAW filter ports. This particular effect appears typically when at one of the two filter ports the input impedance is lower than that of the filter. The choice to present at the BAW input port a slightly lower impedance than needed has been deemed necessary in order to provide a quite well controlled shape over the different power settings. By changing the operating point of the power amplifier, in fact, the amplifier output impedance changes considerably, and increases for low output power levels. This is due to the fact that while the output power decreases, the amplifier approaches the behavior of a reduced conduction angle amplifier, for which no transistor desaturation occurs.

Figure 5.15 compares the amplifier selectivity for three different amplifier power settings. The dark gray curve represents the setting for which the amplifier selectivity corresponds exactly to that of the BAW lattice filter measured alone (same in-band ripple and same dissymmetry between the two curve maxima), indicating perfect filter match. While controlling the output power, only the lower frequency part of the curve is affected, bending upward for higher power settings (black curve) and downward for lower power settings (light gray curve); on the other hand the upper part of the curve remains almost unchanged. As a consequence, the spurious suppression at the maximum power settings will be the worst possible condition, in particular for the image frequency.

The amplifier selectivity is also affected by parasitics such as the bond impedances and the pad capacitances, which have been taken into account by the simple models previously presented. All these contributions make the prediction of the amplifier

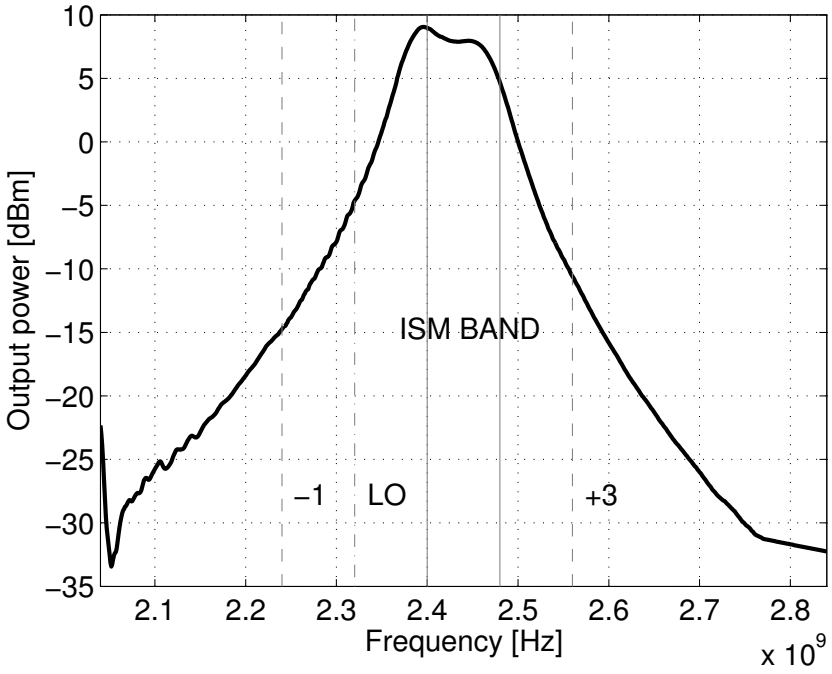


Figure 5.14: Simulated selective chain frequency behavior.

selectivity a difficult task to achieve. To solve this problem, some active circuits have been proposed in combination with BAW lattice structures to allow tuning the filter response [72]. Nevertheless, these circuits consume a considerable amount of power (up to 7 mW) and the filter insertion loss is worsened (>5 dB). For these reasons, the use of such circuits has to be avoided for power amplifiers.

Finally, Figure 5.16 shows the simulated amplifier output power control at the frequency of 2.41 GHz. By varying discretely the biasing current I_{b2} of Figure 5.8, the amplifier output power can be regulated in between −16 dBm and 8.8 dBm, reaching a maximum overall efficiency of 24.8% for P_{out} = 7.7 dBm. The simulated amplifying chain performances are summarized in Table 5.2.

Table 5.2: Final amplifying chain simulated performance.

Parameter	Value	Units	Comments
Supply voltage	1.6	V	PPA
	1.2	V	PA
Max. P_{out}	8.8	dBm	
Current cons.	25.5	mA	@ max P_{out}
η_d	26.6	%	@ P_{out} = 7.7 dBm
η_{ov}	24.8	%	@ P_{out} = 7.7 dBm

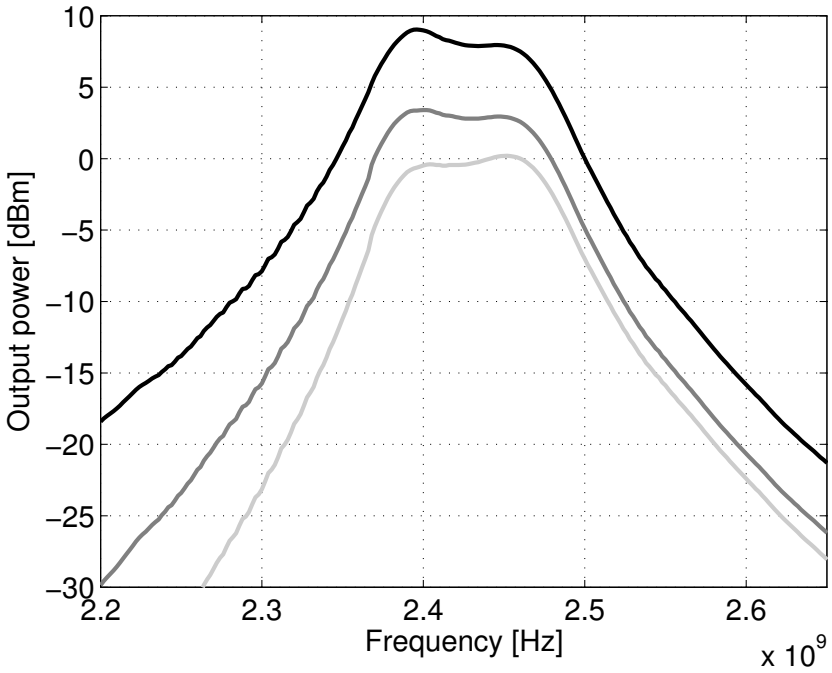


Figure 5.15: Simulated selective chain frequency behavior.

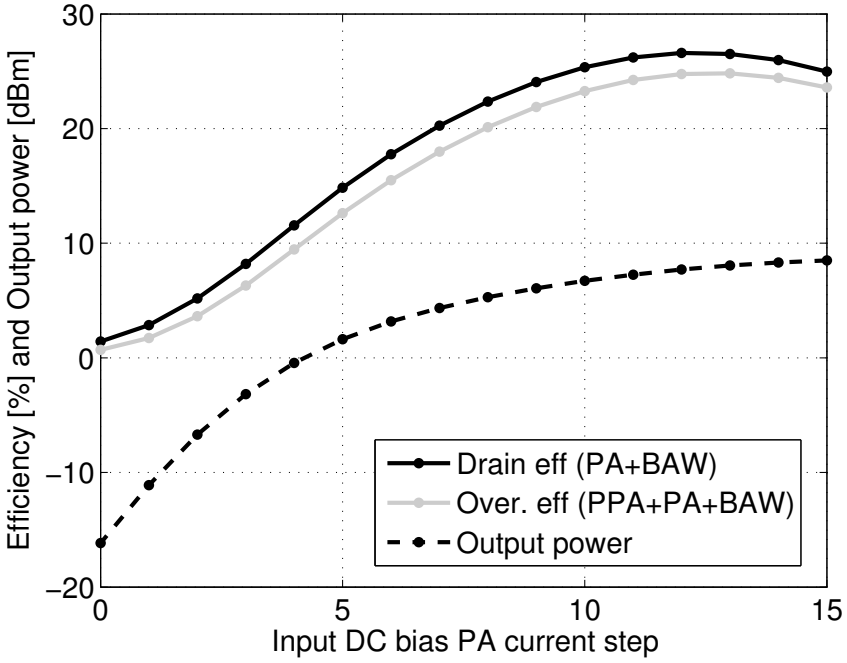


Figure 5.16: Power amplifier output power control and corresponding efficiencies.

Amplifier stability

All RF and microwave circuits including switching mode power amplifiers can exhibit instabilities. Furthermore, in addition to the linear feedback mechanism that makes the RF amplifiers oscillate, the switching mode power amplifiers are also subjected to large input drive levels that cause nonlinearities and can push them more easily into an unstable condition.

Nonetheless the implemented power amplifier topology presents two advantages from the stability point of view. The first one is that the cascode implementation reduces the drain-gate capacitance Miller multiplication effect, thus decreasing considerably the amplifier feedback [51]. The second is represented by the fact a differential structure is used, which is less prone to RF oscillations than single-ended amplifiers [62].

The amplifier has been simulated at different frequencies and load conditions with and without its circuit environment, showing unconditional stability when the cascode implementation is used. It corresponds to have always $k > 1$ and $|\Delta| < 1$, where k and Δ are defined as [62]:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}||S_{12}|} \tag{5.16}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{5.17}$$

Nevertheless, this test was necessary but not sufficient for ensuring the stability. The amplifier is in fact a multistage circuit, while the k-factor analysis is applicable to a single stage amplifier only. Moreover this is a linear analysis, while the power amplifier is a strongly nonlinear block which works in a large signal periodic regime.

To overcome this limitation and have more reliable results, harmonic balance simulations have also been used, which take into account nonlinearities of the active devices and the drain capacitance, by performing sweeps from DC to the RF. However, this method can fail if the parasitic oscillation lies at a different frequency basis with respect to the input frequency, since harmonic balance will be unable to simulate it. Consequently, also transient simulations have been performed for typical conditions with input RF frequencies in the 2.4GHz ISM band. None of these simulations showed any instability for the designed cascode amplifier.

5.2.8 Practical considerations

The design and layout of the power amplifying chain follow the same guidelines as those of a standard RF block. Nevertheless the IC implementation deserves some brief considerations concerning few important points.

Supply bypass capacitors

The implemented amplifier uses finite DC inductances that cause a high ripple on the amplifier current, with peaks at the frequency of operation. As introduced in Section 4.3.2, the use of a differential amplifier is advantageous to reduce this current ripple since the two amplifier currents, shifted by 180°, will sum up at the inductance central

tap decreasing the current swing on the supply. A complete AC current cancellation will not be possible, since the two current waveforms are not symmetrical. The main AC component of the residual ripple will be placed at twice the working frequency, i.e. at around 4.88 GHz for our design. Consequently, the needed capacitance value will be thus considerably lower than that used for a single ended amplifier, since not only the current swing is reduced, but also the impedance requirements are lower as the current ripple frequency is doubled.

Integrated decoupling capacitors have been used on the amplifier supply to deliver this high frequency current with a low impedance. A good trade-off between the capacitor quality factor and the capacitance (density) per area is achieved by using PMOS accumulation capacitors stacked with metal fringe capacitors. Specific care must be taken while laying out the PMOS, for example by using fingered structures similar to those used for RF transistors, in order to ensure a sufficient Q at the wanted frequency. As in the case of the PMOS, the connections of the capacitors to the supply rails should be carefully done so as to reduce the access resistance of the capacitors as much as possible.

Differential inductor

Integrated differential inductors available in the CSEM RF library have been used for the preamplifier and the power amplifier implementation. The differential configuration allows achieving particularly compact layout saving silicon surface. Figure 5.17 depicts the simplified schematic which describes the different connections between each metal. For both the differential inductors, metal layers 2-3 and 4-5 have been used in parallel to increase the inductor quality factor. The inductance ports are accessible in metal-6 while the common tap is at metal-1. With respect to the original inductor layout [73], intended for implementation in LNAs and VCOs, additional care has been put to improve the current capability of the inductor charging the PA. In particular the metal widths have been augmented where needed to match the amplifier current requirements, while the number of vias in between the metal layers has been increased to reduce the inductor series resistance.

5.3 Quadrature generation

The BAW-based transmitter employs a differential oscillator working at 2.32 GHz. To provide SSB upconversion, both the LO and the IF signals have to be complex, calling for quadrature generation on the LO path. This can be done in different ways.

A widely used quadrature generation technique employs divide-by-two circuits, which can be implemented for example by using a master-slave flip-flop in a cross-looped configuration [8]. Even if very low power consumptions have been reported in the literature [74] for these circuits, for output frequencies as high as 2.32 GHz the required consumption would become no more negligible, exceeding 1.5 mW at 1.6 V. More importantly, the use of such dividers in the proposed architecture would call for a 4.64 GHz BAW oscillator, requiring additional power consumption. Due to these reasons, this solution has not been adopted for the BAW-transmitter, even if it remains

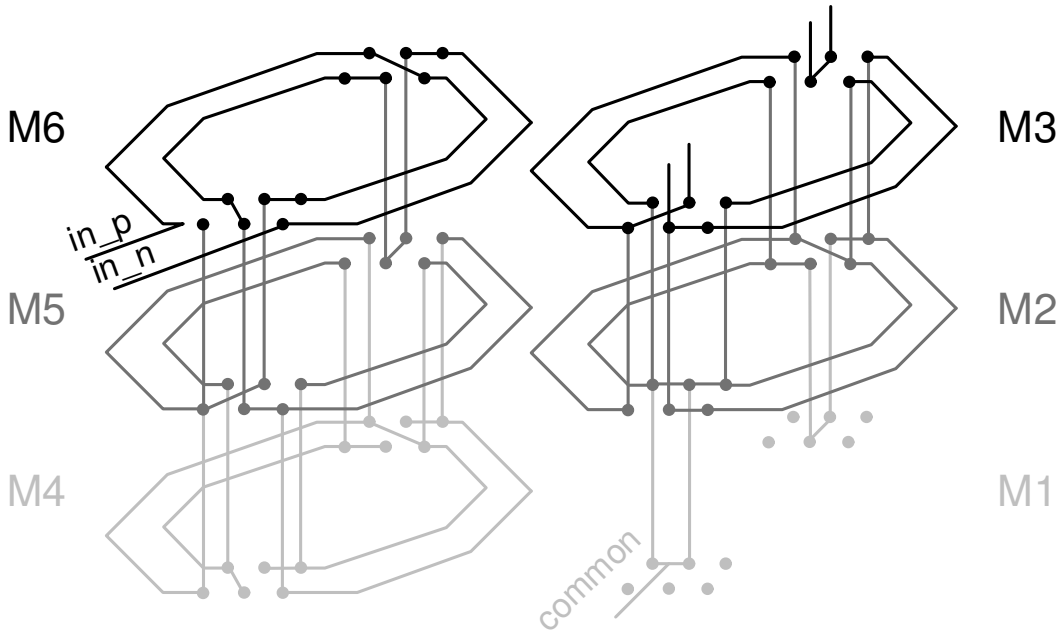


Figure 5.17: Inductance.

interesting for direct modulation architectures in which the local oscillator has to work at higher frequency to avoid pulling by the power amplifier, as for example in systems based on polar architecture [75].

Another possibility to generate quadrature signals is to use passive networks such as polyphase filters or simple RC-CR phase shifters. Both techniques use RC poles or zeros to manipulate the phase of a signal in one path relative to the other signal path. In case of an RC-CR, a pole is implemented in the in-phase path of the local oscillator, while a zero is implemented in the quadrature path. For perfect capacitors and resistors matching, a constant 90° phase shift is provided over the entire frequency spectrum, even if the values of the passive components deviate from the nominal ones, as for example due to process or temperature variations. On the other hand, these variations can cause important amplitudes imbalances on the generated I and Q signals since the two different paths used to phase shift the signals have opposite amplitude frequency behavior and are equal only at their -3 dB frequency, $f = 1/(2\pi RC)$.

The relative amplitude mismatch ε of the two quadrature signals can be expressed as function of the relative variations of the passive components from their nominal values, $\Delta R/R$ and $\Delta C/C$. For $\omega RC \approx 1$, the following expression can be found [8]:

$$\varepsilon = \frac{\Delta A}{A} \approx \frac{\dfrac{\Delta R}{R} + \dfrac{\Delta C}{C}}{\sqrt{1 + \dfrac{\Delta R}{R} + \dfrac{\Delta C}{C}}} \approx \frac{\Delta R}{R} + \frac{\Delta C}{C}. \tag{5.18}$$

Since these variations can reach 20% for each of the two components, the amplitude mismatches on the I and Q paths can achieve values as high as 37%. To reduce this problem, polyphase phase shifters are composed by different stages in cascade, with different -3 dB frequencies $f_i = 1/(2\pi R_i C_i)$ set around the wanted frequency. This

provides a relatively constant gain over a wider bandwidth, but at the cost of a higher signal attenuation and noise.

If mismatches between the passive components are present, the phase difference between the I and the Q signals of an RC-CR shifter deviates from the ideal 90°. If α and β are the relative mismatches of the resistor and capacitors used in the passive network, the phase imbalance $\Delta\varphi$ between the two quadrature signals can be calculated with the following expression [8]:

$$\Delta\varphi = \arctan\left[\frac{\alpha+\beta+\alpha\beta}{2+\alpha+\beta+\alpha\beta}\right] \approx \frac{\alpha+\beta}{2} \tag{5.19}$$

if $\alpha \ll 1$ and $\beta \ll 1$. By assuming well matched passives, $\alpha = \beta = 1\%$, the resulting imbalance is equal to 0.6°.

In most of the RF applications these quadrature errors have to be compensated in order to achieve a sufficient image rejection and allow easier demodulation at the receiver. Saturating amplifiers can be used to reduce the gain mismatch [76] between the I and Q paths, but this technique can become power consuming at RF since different stages are needed in cascade. In addition to that, a sufficient bandwidth has to be provided by the limiting stages, in order not to convert differences in amplitude into phase imbalance (AM-to-PM conversion) [8]. Quadrature mismatches can also be corrected by using feedback on variable resistors or variable capacitors. Even if this method allows reaching very good rejections performance, it is however power hungry. In [77] a 65 dB image rejection is achieved thanks to quadrature error correction, with a power budget of 23 mW at 1.8 V. This consumption would not be acceptable for our system.

Taking into account the low power constraints, the relaxation of the quadrature mismatches requirements due to the use of the BAW filter and the advantage of performing phase shifting at a fixed frequency, the RC-CR network seems to be the best choice for generating the complex LO, while achieving low power consumption and area occupation. In the following section it will be shown that even in the worst case for quadrature imbalance, sufficient rejection can be achieved to reach the wanted specifications. The schematic of the implemented phase shifter is depicted in Figure 5.18. It is composed of a buffer driven by the BAW oscillator signals and loaded with the RC-CR network. The buffer is a complementary class AB stage, with the transistors working in strong inversion. The amplifier operating point is set by resistive biasing and controlled by means of a programmable current source. The buffer allows compensating the intrinsic 3 dB losses of the passive network at $\omega = 1/(RC)$; moreover, since its input is purely capacitive, it prevents the degradation of the oscillator high-Q tank, providing isolation from the phase shifter network and preserving the BAW DCO power and phase noise performance.

The simulated phase shifter performance is listed in Table 5.3. For correlated variations of 20% in the capacitors, resistors in the slow-slow case and including the buffer transistors uncorrelated variations, Monte Carlo simulations show an average amplitude imbalance of $\mu = 37.1\%$ with a standard deviation of $\sigma = 1.6\%$ and an average phase error of 0.05° with standard deviation equal to 0.62°, confirming the values estimated previously.

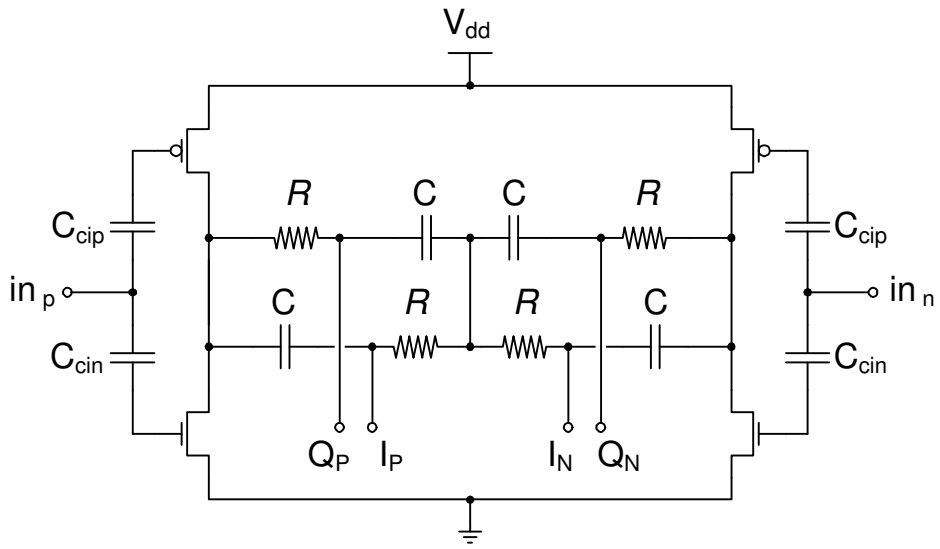


Figure 5.18: Schematic of the phase shifter. Biasing not shown.

Table 5.3: Phase shifter performance (comprised of buffer).

Parameter	Value	Units
Supply voltage	1.6	V
Current consumption	1.19	mA
Power consumption	1.90	mW
Voltage gain	≈ 0	dB
Input ref. 1 dB compression point	291	mV
Input referred IP_3	627	mV

5.4 Up-conversion mixer

The quadrature up-conversion mixer used to translate the IF modulated signal at the RF (see Figure 5.19) is based on Gilbert switching cells [78]. It uses two mixers whose input sequence defines which of the two sidebands is selected at the output. Neglecting the amplitudes and in ideal conditions, with the chosen signal configuration, described by the relation

$$\begin{aligned} I_{RF} = I_{LO} \cdot I_{IF} - Q_{LO} \cdot Q_{IF} &= \cos\omega_{LO}t \cdot \cos\omega_{IF}t - \sin\omega_{LO}t \cdot \sin\omega_{IF}t \\ &= \cos\left(\omega_{LO} + \omega_{IF}\right)t, \end{aligned} \tag{5.20}$$

only the upper sideband appears at the mixer output.

Resistive bias is used to set the operating point of the mixer transconductance transistors (nominally working in moderate inversion), while the complex LO signal, generated by the phase shifter, is AC coupled through metal-to-metal finger capacitors. The quadrature IF signals are available in the system after frequency division in the LC

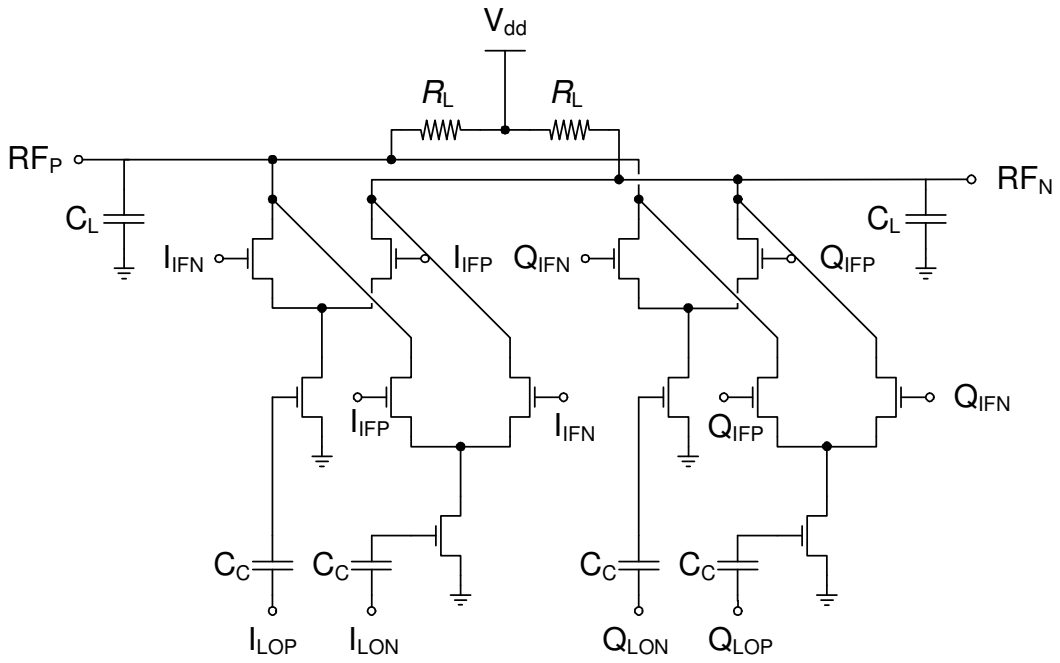


Figure 5.19: Schematic of the up-conversion quadrature mixer. Biasing not shown.

PLL (Section 5.5.2). Since they are generated with dynamic dividers, their high swing and steep transitions make them ideal to drive directly the mixer switching pairs.

The output currents are then summed on the mixer load. In order to limit the area dedicated to the whole transmitter, a resistive load (R_L) has been preferred to an inductive one. The mixer conversion gain can thus be calculated as:

$$A_{CG0} \simeq 2 \cdot \frac{2}{\pi} g_m R_L, \tag{5.21}$$

with g_m the trasconductance of one of the four lower MOSFETs. The factor of two with respect to the gain of a DSB mixer comes from the fact that the wanted signal adds at the output of the two mixers, while the image cancels out. The mixer current consumption is set for achieving a sufficient linearity, dominated by the transconductance stage. In Figure 5.19, the capacitances C_L model the pre-amplifier load, which sets the mixer bandwidth. Finally, since the pre-amplifier is only AC coupled to the mixer output, there is no need to precisely control the output common mode of the upconverter.

Table 5.4 presents the mixer simulation results. The voltage conversion gain, input -1 dB compression point and input referred IP_3 are referred to the LO amplitude since it is connected to the transconductance MOSFETs, while the quasi digital IF is used to drive the mixer switching transistors.

The mixer is one of the most noisy blocks in receiver architectures, being involved in different noise conversions and translations of flicker and white noise which have to be carefully addressed in low-IF or zero-IF receivers [79]. In transmitter architectures, the mixer noise can still present a problem since it impacts the noise floor of the transmitter. At up-conversion, the mixer noise can be approximated by taking into

Table 5.4: Up-conversion mixer performance resume.

Parameter	Value	Units
Supply voltage	1.5	V
Current consumption	1.48	mA
Power consumption	2.22	mW
Voltage gain	≈ 0	dB
Input ref. 1 dB compression point	173	mV
Input referred IP_3	502	mV

account the white noise contributions only. Under this condition, the output noise power spectral density of a single balanced switching mixer is given by [80]

$$\hat{V}_{o,n}^2 = 8kTR_L\left(1+\gamma\frac{R_L I}{\pi A}+\gamma\frac{g_m R_L}{2}\right), \tag{5.22}$$

where I is the bias current of each of the four transconsuctance MOSFETs, A is the amplitude of the switching waveform and γ is the channel noise factor. In the formula, the first term indicates the contribution coming from the resistive loads, the second the noise due to the switching transistors and the third that due to the transconductance stages. Conversion gain of $2/\pi$ has been considered for the switching pair action. In particular, it can be seen that the switches noise is reduced if high amplitude driving waveforms are used. On the contrary, when the Gilbert cell is optimized for linearity (high biasing current and low switching voltage to keep the switch transistors in saturation), the relative noise contribution of the switches can become more important and even dominate over the transconductance MOSFETs noise.

In the SSB mixer used for upconversion, there are four times as many transistors in the transconductance stages and in the switches with respect to the single balanced mixer. As a consequence, since the different noise sources are uncorrelated, the output noise becomes

$$\hat{V}_{o,n}^2 = 8kTR_L\left(1+\gamma\frac{4R_L I}{\pi A}+2\gamma g_m R_L\right). \tag{5.23}$$

Thanks to the use of quasi-digital signals at the input of the switching transistors, their relative contribution to the output noise is minimized. As a consequence, the mixer noise is dominated by the transconductance MOSFETs and their contribution is determined by the mixer power consumption through its bias current. Transistor level simulations of the RC-CR buffer plus upconverter chain showed an output noise floor at -151 dBc/Hz. The noise floor was at -156 dBc/Hz at the RCCR output.

To avoid violation of the tight output spectrum noise floor requirements in stringent applications such as WCDMA, passive voltage mixers have been recently proposed in the transmitter chain [81], which allow in addition reduced power consumption. In absence of V-I conversion, the noise of a passive mixer is mainly determined by the contribution of the switches on-resistance only. While their use has not been

initially considered for the presented version of the BAW-based transmitter, a testchip employing those mixers is in production at the time of writing this thesis.

The amplitude and phase imbalances of the quadrature input signals, as well as the mixer mismatches, cause the unwanted sideband to appear at the output. The ratio of the unwanted sideband amplitude over the desired sideband amplitude, or Image Rejection Ratio (IRR) [8], can be expressed as

$$IRR \simeq \frac{\varepsilon_{LO}^2 + \varepsilon_{IF}^2 + \Delta\varphi_{LO}^2 + \Delta\varphi_{IF}^2 + \varepsilon_{\text{mix}}^2}{4} \tag{5.24}$$

where ε_{LO}, ε_{IF}, φ_{LO} and φ_{IF} represent the relative amplitude and phase mismatches of the LO and the IF signals respectively, and ε_{mix} is the contribution coming from the mixer gain mismatch. The mixer phase error is assumed negligible. From this approximation, valid for small random and uncorrelated mismatches, it is possible to see that 30 dB image attenuation could be achieved with mismatches equally distributed on the different contributions smaller than 3%.

In case of an RC-CR phase shifter, however, the amplitude mismatches can be much higher than 3%, as predicted by (5.18) and confirmed in the simulation results previously presented. To predict a more realistic rejection ratio in the worst possible case, Monte Carlo transistor level simulations including all the aforementioned mismatches have been performed on the whole RC-CR plus upconverter chain.

The bar diagram depicted in Figure 5.20 represents the rejection achievable at the output of the quadrature mixer on the signal image at $f_{\text{LO}} - f_{\text{IF}}$, for $f_{if} = 80$ MHz. This Monte Carlo simulation has been performed on 1000 runs for correlated variation of 20% in the capacitors, resistors in the slow-slow case and uncorrelated mismatches in all the active components, with additional amplitude mismatch of 5% and phase imbalance of 2° between the IF signals. The IF mismatch has been extracted from transistor level simulations of the digital dividers used to generate the quadrature (divider P in Figure 5.1). To check also the suppression of the IF signal harmonics, the amplitudes of the different spurs near to the target band are reported in Table 5.5, referred to the wanted signal amplitude. The suppression of the two most critical components (-1 and $+3 \times \omega_{\text{IF}}$ around ω_{LO}) reaches the minimum requirements set in Section 3.5.2 and allows satisfying, together with the BAW filtering, the international regulations for the target application. Thanks to the use of double balanced mixers, the LO leakage at the output port, which will be only slightly filtered by the BAW, is limited to -53.9 dBc.

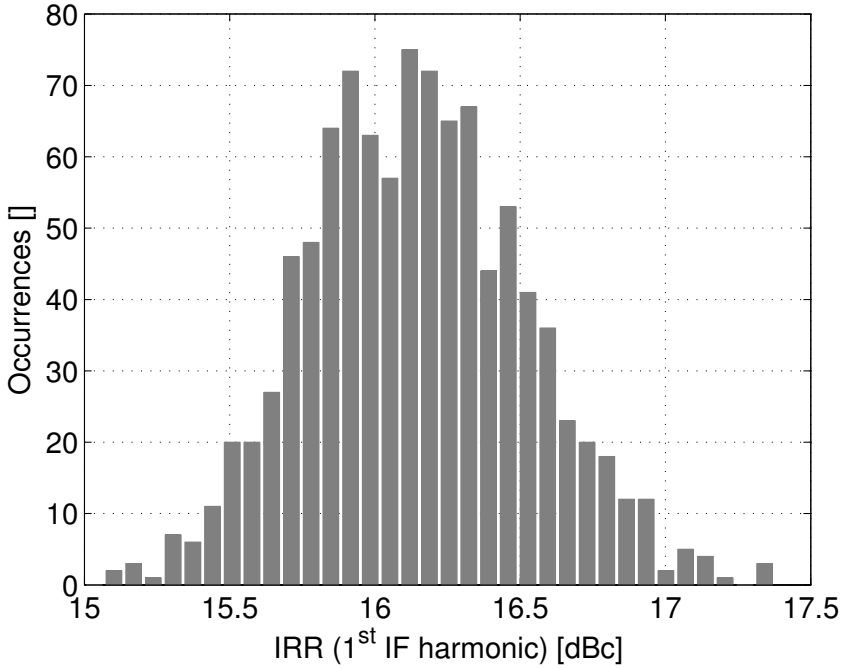


Figure 5.20: IRR at $f = f_{\mathrm{LO}} - f_{\mathrm{IF}}$.

Table 5.5: Major spur levels on the RF signal after phase shifting and frequency conversion. The Monte Carlo simulation is performed around the worst case for the values of R and C used in the phase shifter. The spurs suppressed by the mixer are indicated with the symbol *.

Spur	Suppr. [dBc]	Reject. [dBc]	1σ [dBc]
-5^*	29.3	15.32	0.25
-3	9.0	-	0.02
-1^*	16.14	16.14	0.37
LO	53.9	-	5.6
$+2$	57.6	-	5.5
$+3^*$	26.1	16.56	0.34
$+5$	15.2	-	0.02
$+7^*$	33.4	16.50	0.15

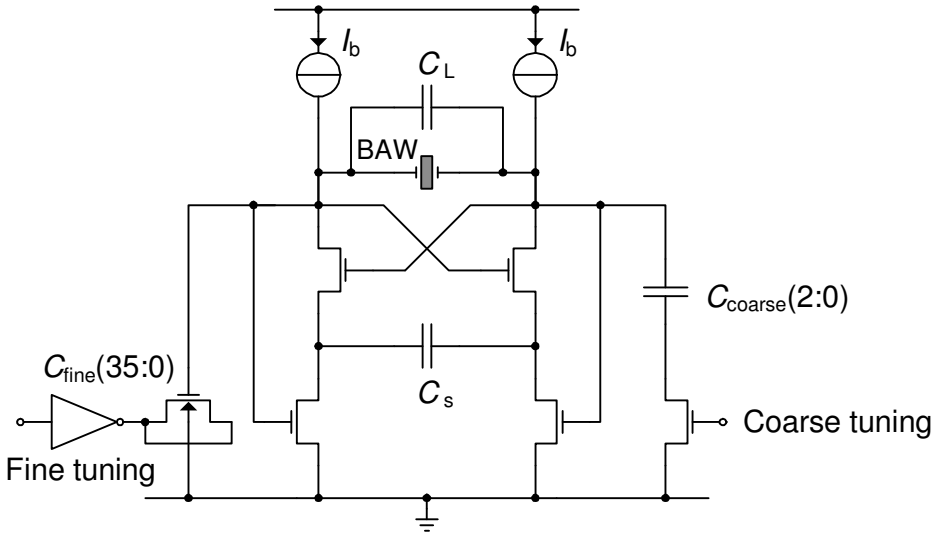


Figure 5.21: Schematic of the BAW-based oscillator. The discrete varactors are differential in the actual circuit.

5.5 Transmitter implementation: other blocks

5.5.1 Frequency synthesis

BAW DCO

As already discussed in Chapter 3, oscillators based on BAW resonators have demonstrated the potential for a considerable phase noise improvement with respect to standard LC oscillators, for the same power consumption levels. To compensate for the reduced tuning range of such oscillators and thus allow addressing multi channel applications in the 2.4 GHz band, a wide IF and up/down-conversion architecture have been used for the transmitter and receiver front-ends. This choice allows to let the BAW DCO keeping its high$-Q$ tank unchanged, and so to preserve its excellent phase-noise performance.

The BAW-based differential oscillator (Figure 5.21) used as system LO was designed by D. Ruffieux and proposed for the first time in [82] for a quartz crystal oscillator. The main feature of this circuit is that, since the BAW resonator presents a high impedance at DC, capacitive degeneration of the cross coupled pair has to be used to avoid latching and let the bottom MOS transistors set the oscillator common mode voltage by negative feedback. At higher frequencies, this feedback changes to positive in order to provide the negative conductance needed for the oscillation. Finally, to control the oscillation amplitude, the LO core is embedded into a PTAT loop, as shown originally by E. Vittoz in [83].

The low tuning range capabilities of the oscillator are exploited by implementing a high frequency resolution digitally controlled oscillator (DCO) which, integrated into the ADPLL, can ensure nearly immediate locking after returning from an idle period. Two kinds of discrete varactors have been used for the DCO: three switched metal fingered capacitances provide coarse-tuning, while fine tuning is achieved by a bank of

thirty-two 4×0.18 μm^2 inversion/depletion nMOS capacitances. Sub-ppm frequency steps are obtained by switching four additional MOS varactors with a 6 bits MASH 1-1 modulator, as proposed in [46].

By defining C_p the BAW resonator dielectric capacitor and C_L the oscillator loading capacitor (including the capacitive load of the oscillator and the blocks to which it is connected), the tank equivalent parallel conductance g_p that the oscillator has to compensate is given by:

$$g_p = \frac{\omega_0 C_p}{\rho Q} \cdot \left(1 + \frac{C_L}{C_p}\right)^2, \tag{5.25}$$

with ω_0 the operating frequency, $\rho \triangleq C_m/C_p$ the coupling factor (3.4) and Q the loaded Q-factor.

The oscillator phase noise, considering only the thermal white noise, can be expressed by [36]

$$\mathcal{L}(\Delta f) = \frac{(1 + G_m\gamma)kT}{\omega_0 C_p \frac{Q}{\rho}\left(1 + \frac{C_L}{C_p}\right)^2 V_{\text{osc}}^2} \cdot \frac{f_0^2}{\Delta f^2}, \tag{5.26}$$

where k is the Boltzmann constant, T is the temperature and γ is the circuit excess noise factor. A fair figure-of-demerit for this oscillator is represented by the current × phase noise product, which is dependent on $1/Q^2$ (assuming constant amplitude, supply voltage and noise factor). The advantage of having a high quality factor BAW component with respect to a standard LC tank is visible when calculating the loaded Q [36]:

$$\frac{1}{Q} = \frac{1}{Q_R} + \rho \cdot \frac{1}{Q_L}, \tag{5.27}$$

with Q_R and Q_L the resonator and load quality factors respectively. Since $C_p/C_m >> 1$, the loaded quality factor is boosted with respect to a standard LC implementation. As an example, if $Q_L = 50$, $\rho = 5\%$ and $Q_R = 1000$, the loaded Q is 500. With respect to an LC tank with a loaded Q of 10, the improvement in the current × phase noise product corresponds to about 34 dB (assuming the same conditions for the two oscillators). On the other hand, the drawback lies in the reduced oscillator tuning range, given by [36]:

$$\frac{\Delta f}{f_0} = \left[\frac{C_m}{C_p} \cdot \frac{C_L}{C_p} \cdot \left(1 + \frac{C_L}{C_p}\right)^{-2}\right] \cdot \frac{\Delta C_L}{2C_L}, \tag{5.28}$$

which is dependent on C_m/C_p. The term in brackets can be maximized for $C_L = C_p$, leading to a maximum tuning range of

$$\left.\frac{\Delta f}{f_0}\right|_{\max} = \frac{\rho}{4} \cdot \frac{\Delta C_L}{2C_L}. \tag{5.29}$$

Since the second term corresponds to the derivative for an LC tank, it results that, with the numerical figures given previously, the achievable BAW oscillator tuning range is about 1/80 that of a classical LC oscillator.

Dynamic dividers

Dynamic dividers represent a valid low power solution to implement frequency division in modern frequency synthesizers. Different implementations have been presented in the last years [84, 85]. In the implemented transmitter, the frequency division of the 2.32 GHz DCO signal is achieved, as well as in other sections like the PLL, by using fractional dynamic divider based on injection-locked ring oscillators, originally presented in [47].

The divider N is composed of a chain of three dual-modulus dividers by 3/4, 2/3 and 2/3, which allows covering all the instantaneous integer division ratios from 12 to 36 thanks to the use of some simple control logic. Fractional division ratios are achieved thanks to a second order MASH 1-1 $\Delta\Sigma$ modulator, whose control word can be dynamically controlled to perform carrier modulation in transmission mode.

Figure 5.22 depicts one of the 2/3 dual-modulus blocks constituting the N divider. It is composed of an internal ring oscillator whose nodes transitions are synchronized on the input clock and swallowed (when needed) thanks to some additional control MOS transistors. In Figure 5.23 the timing diagrams of the different nodes are shown for both possible division ratios (MC=0 corresponds to a division by two, MC=1 to a division by three). The division by two is achieved by swallowing two half clock cycles of the input signal over a complete divider cycle.

Some considerations have to be done concerning the design of such dividers for ensuring a correct operation. The higher output frequency allowed can in fact be estimated with the self-oscillating frequency of the inverter ring oscillator, given by:

$$f_0 = \frac{1}{2N \cdot t_p}. \tag{5.30}$$

If we suppose that the main contribution on the load of each inverter is capacitive, $t_p = CV_{swing}/I$, with C the node capacitance and I the current provided by the inverter averaged on one cycle. Trying to decrease too much the node capacitance for achieving high frequencies could worsen the capacitance ratio in between the ring internal nodes and those on the drains of the controlling MOS, which could cause incorrect operation due to the charge effect phenomenon, as described in [31]. To avoid this problem and allow dividing incoming high frequency signals as the 2.32 GHz LO, the first stage of the division chain is AC-driven by the DCO waveforms and the locking frequency is controlled by starving the current in the different stages by means of DC biased series transistors [45].

5.5.2 PLL filtering

The PLL has the aim to generate the digital IF signal used in the transmitter up-conversion chain. A low phase noise RF signal can be achieved only if the IF is able to provide similar noise performance as the BAW oscillator. To accomplish this task, two main noise contributions have to be carefully addressed in the PLL implementation.

The first contribution is the PLL oscillator phase noise. In [45], a PLL based on a g_m/C relaxation oscillator working at the IF frequency (having feedback division ratio equal to 1) was used to achieve this task. Despite similar phase noise is possible with

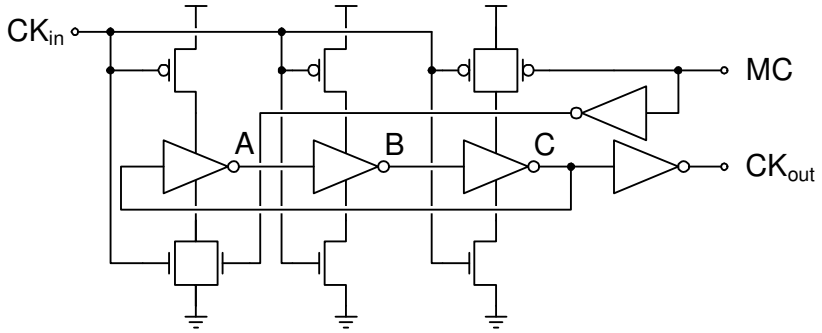


Figure 5.22: Transistor level schematic of a variable dynamic divider by 2/3.

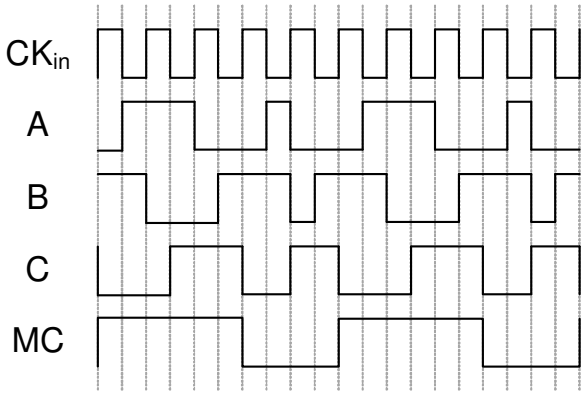


Figure 5.23: Divider chronogram.

respect to a standard LC oscillator working at RF thanks to the well-known $(f_c/\Delta f)^2$ noise behavior [86], the phase noise reached with the g_m/C oscillator was still 30 dB higher than that achievable with the BAW. Moreover, a very high tuning range (>66%) was required.

The oscillator phase noise contribution can be brought to levels similar to those of the BAW oscillator by using frequency division. To recover at the IF frequency the 30 dB phase noise gap with respect to the limit set with the BAW, the oscillator should work at a frequency which is $10^{30/20} \approx 32$ times higher than the IF. For this reason the solution adopted employs a classical LC oscillator working at the RF frequency followed by an integer fractional division P, whose output represents the IF signal. This divider, similar to the dynamic dividers described previously and composed by a chain 2−2/3−2/3−2, can perform division ratios from 16 to 36 in steps of 4, while generating I and Q signals with controlled 50% duty cycle. This requirement is necessary to decrease the second harmonic content of the IF signal, and thus to limit the corresponding spurs which can fall in the 2.4 GHz ISM band (more precisely that spur lies, after IF upconversion, exactly on the band upper edge when the IF is set to 80 MHz). To further decrease the noise, the divider M used in the feedback path is an integer divider implemented similar to P and covering the same division ratios.

The second important noise contribution belongs to the quantization noise coming from the PLL reference frequency generated by the fractional divider N. This noise, pushed to high frequencies thanks to the shaping effect provided by the second order

$\Delta\Sigma$ modulator and rejected out of the PLL band by the action of the second order loop filter, is kept low at the PLL cutoff frequency by the particular architecture chosen for the PLL, which uses the fractional divider N plus the two integer dividers. While for a standard fractional-N synthesizer the in-band contribution of the quantization noise on the PLL output is independent from the feedback division ratio and equal to [87]:

$$S_{\Phi}(\Delta f) = \frac{4\pi^2}{12 f_{\mathrm{REF}}} \cdot \left[2 \sin\left(\frac{\pi \Delta f}{f_{\mathrm{REF}}}\right)\right]^{2(n-1)}, \tag{5.31}$$

it can be show that with the chosen approach it reduces to [24]

$$S_{\Phi}(\Delta f) = \frac{M^2}{N^2 P^2} \cdot \frac{4\pi^2}{12 f_{\mathrm{REF\_BAW}}} \cdot \left[2 \sin\left(\frac{\pi \Delta f}{f_{\mathrm{REF\_BAW}}}\right)\right]^{2(n-1)}. \tag{5.32}$$

With $n = 2$ and $f_{\mathrm{REF\_BAW}} = f_{\mathrm{BAW}}/N$ the phase noise gain is expressed by

$$G = \frac{N^2 P^2}{M^2} \left(\frac{f_{\mathrm{REF\_BAW}}}{f_{\mathrm{REF}}}\right)^3. \tag{5.33}$$

As an example, in case the PLL integer division ratios are equal ($M = P$) and $f_{\mathrm{REF\_BAW}} = 160$ MHz (i.e. $N = 14.5$), the comparison of the implemented solution with a traditional PLL with $f_{\mathrm{REF}} = 26$ MHz shows an improvement of the quantization noise contribution at the PLL output of about 47 dB.

This value, considerably higher than the 30 dB needed to make it comparable with the gain on the oscillator phase noise contribution, can be degraded in order to reach faster modulation data rates. In fact, since the LC phase noise decreases with a -20 dB/dec slope and the quantization noise increases by 20 db/dec, the 17 dB in excess with respect to the target can be traded with a bandwidth increase by a factor of 2.7 with respect to a classical implementation.

5.6 Summary

In this chapter the implementation of the BAW-based transmitter with selective amplification plus SSB mixing has been presented. After summarizing the system architecture presented in Chapter 3, the detailed design and trade-offs of the different blocks composing the transmitter have been discussed and the simulation results have been presented. Finally, the description of some blocks composing the frequency synthesis section has been presented.

Chapter 6

Measurements

Measured results for the transmitter are separated into two parts. The first part describes the measurements of the selective amplifier integrated as a stand-alone circuit. The second part presents the measurements of the complete transmitter, including the synthesis section, to validate the quality of the RF signal. The spurious suppression mechanism is checked, together with the fulfillment of the mask requirements for signals targeting Bluetooth and Bluetooth LE compatibility.

6.1 Selective amplifying chain

The BAW-based amplifying chain, composed of the preamplifier and the selective amplifier, has been integrated as a stand-alone test-chip in a 0.18 μm standard digital CMOS technology. The amplifier layout is depicted in Figure 6.1, where the preamplifier and the power amplifier sections have been highlighted. The whole transmitter area, including the pads, is 1.25×0.65 mm^2. Connection of the power amplifier to the supply is provided by three pads, two for V_{dd} and one for ground. Banks of switchable capacitors have been used at the input of the power amplifier to allow adjusting the resonance with the preamplifier inductance and at its output to enable an additional fine adjustment of the power amplifier shunt capacitance.

Figure 6.2 depicts the testbench used to characterize the BAW-based amplifying chain. Both the RF IC and the BAW filter are mounted on the same printed card, and bonded with standard wire bonding. A signal generated with an Agilent E4438C vector signal generator is injected into the card through the 50 Ω RF connector, transformed to a differential signal with an SMD balun and fed to the preamplifier. Wire bonds are used to connect the amplifier directly to the BAW filter die, whose output is re-transformed to an unbalanced signal and measured with an Agilent E4440A spectrum analyzer. All the RF lines on the PCB are properly dimensioned to provide a 50Ω impedance. No external components are needed at the output of the BAW filter to achieve impedance matching with the balun 100 Ω differential port. Both the baluns are Murata LDB212G4010C, with a typical insertion loss of 0.9 dB at 25° C.

The overall amplifying chain selectivity, shown in Figure 6.3 (solid curve), has been measured by sweeping a constant power RF input signal over the frequency and setting the spectrum analyzer on *max hold*. The power amplifier is set for the maximum

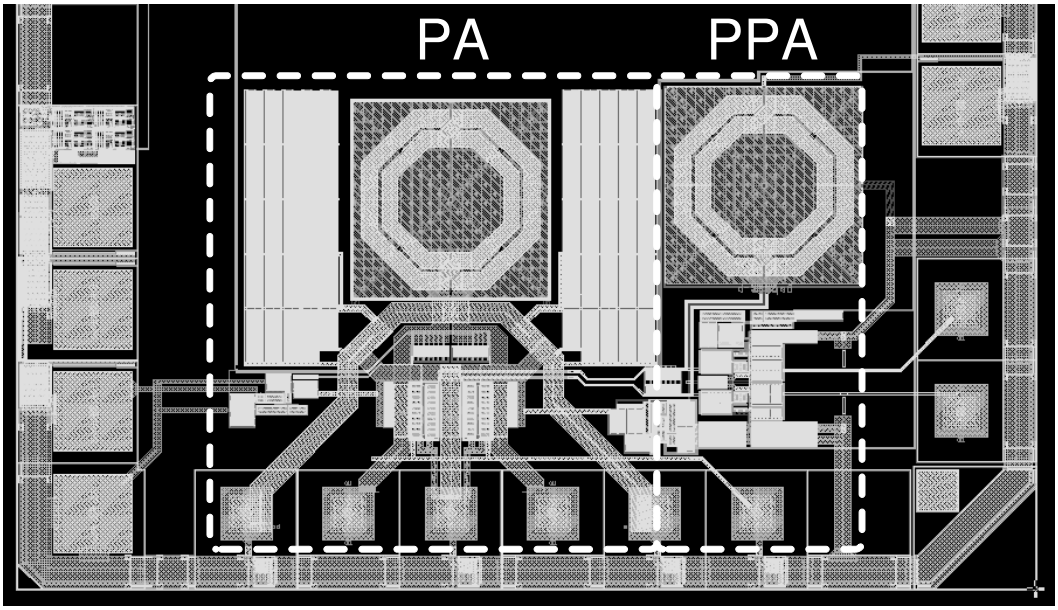


Figure 6.1: Layout of the selective amplifier test-chip.

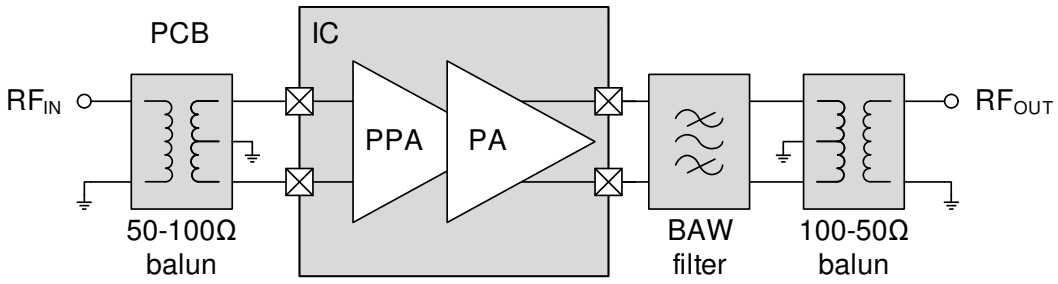


Figure 6.2: Simplified schematic of the experimental setup used to characterize the selective amplifying chain.

drain efficiency. The single ended sinusoidal amplitude at the preamplifier input gate corresponds to 200 mV_p.

Without frequency trimming of the BAW filter, the center frequency is about 35 MHz lower than the targeted 2.44 GHz. The −1 dB bandwidth is 87 MHz, with an in-band ripple equal to 0.7 dB. The achieved suppression corresponds to about 23 dB at 2.24 GHz (image) and 2.56 GHz (+3 IF harmonic). If the filter was centered on the ISM band, the two rejections would have been 25 dB and 18 dB respectively.

On the same plot, the measured amplifier selectivity is compared to the simulated curve (dashed) presented in Section 5.2.7, which has been obtained using measured S-parameters extracted before the filter assembly. The two curves match relatively well, indicating a correct modeling of the parasitics. Nevertheless, a slight discrepancy is present for frequencies higher than 2.34 GHz. It could be due to the PCB lines effect, which were not taken into account in the simulations.

Figure 6.4 depicts the amplifier output power, the drain efficiency and the overall efficiency (preamplifier plus amplifier) while sweeping the power stage bias, for a

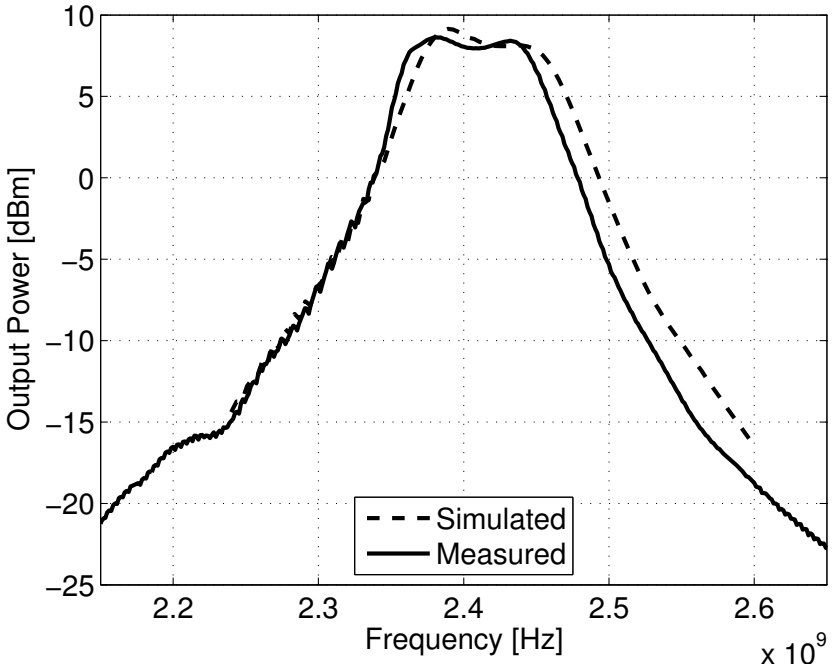


Figure 6.3: Measured (solid) and simulated (dashed) amplifying chain selectivity.

frequency of 2.4 GHz. The output power is controlled by programming the current DAC which biases the input of the amplifier power stage, as discussed in Section 5.2.7. The curves include the BAW-filter losses (1.5 dB), while the SMD balun insertion losses and the cable attenuation have been corrected. The maximum achievable output power corresponds to 8.4 dBm, while the power range spans over almost 15 dB. The programmable current allows controlling the output power with a unit step never higher than 1.8 dB. The maximum drain and overall efficiencies are equal to 24.2% and 21% respectively.

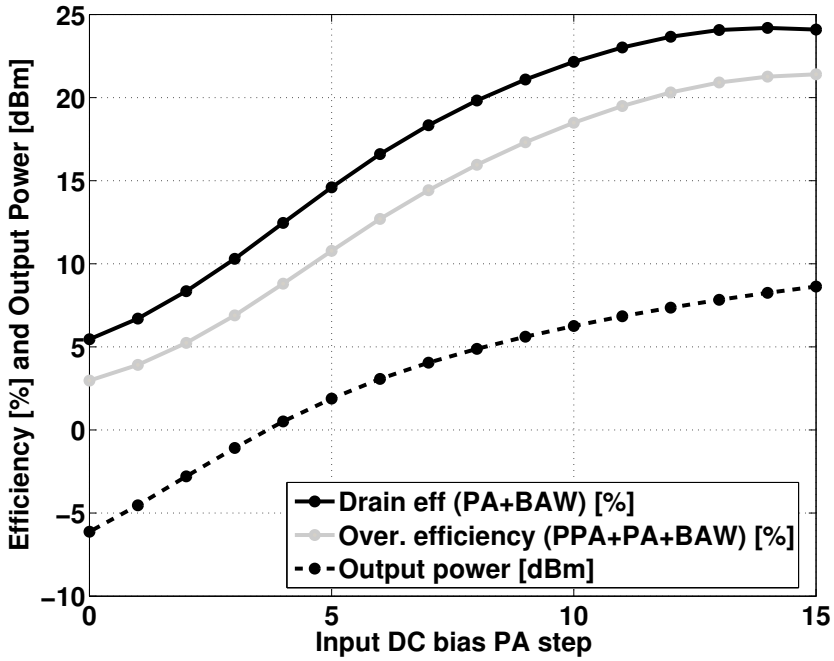


Figure 6.4: Measured output power and efficiencies of the amplifying chain, done by varying digitally the power stage biasing steps. All the curves include the BAW filter losses.

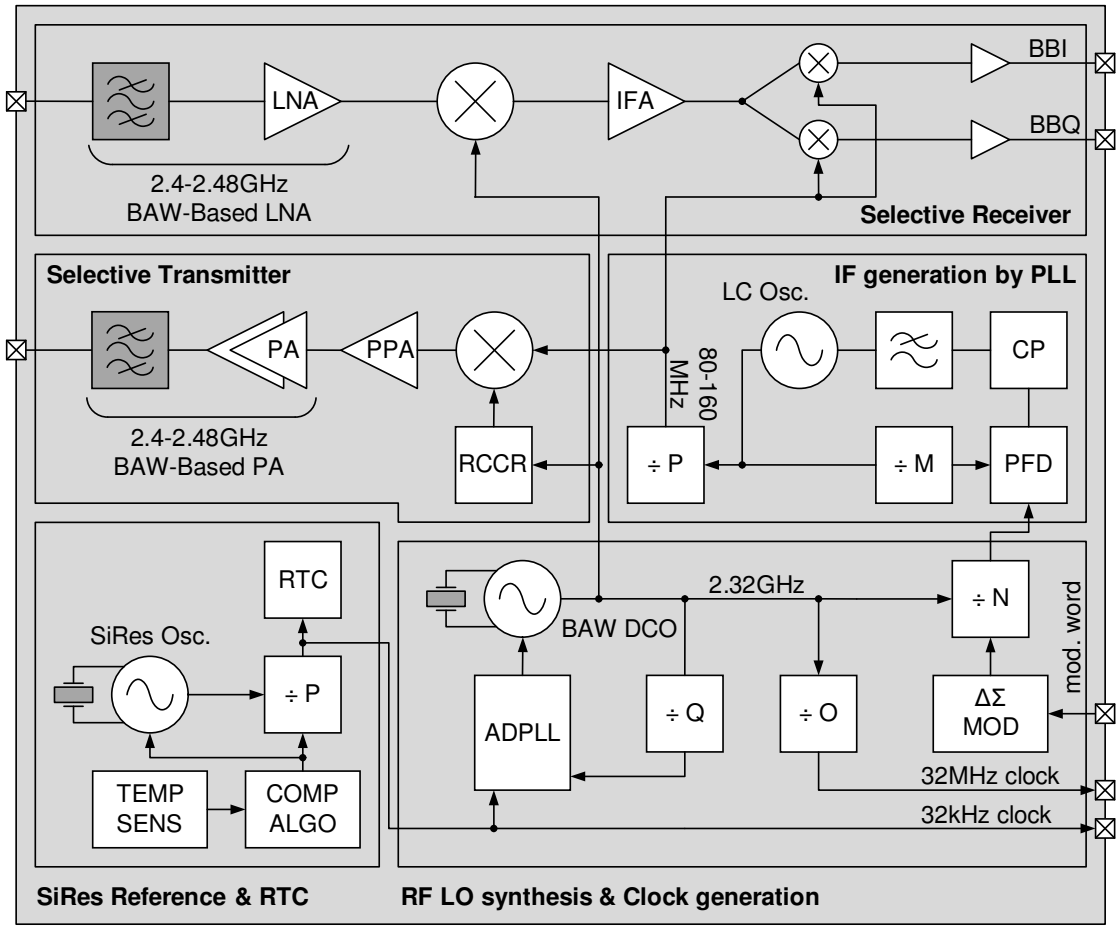


Figure 6.5: Block diagram of the 2.4 GHz multi-channel BAW-based transceiver as integrated with the CSEM Analog & RF group.

6.2 BAW-based transceiver

The selective amplifying chain has been integrated, together with the phase shifter and the SSB up-conversion mixer, in the complete BAW-based transceiver depicted in Figure 6.5 (from now on identified as TRX IC). It comprises a synthesis section composed of a BAW DCO oscillator plus ADPLL, frequency dividers and modulator, an IF generation section implemented with an LC PLL to provide the quadrature IF signals to the RF front-ends and a double down-conversion selective receiver previously integrated in [45] and based on a BAW-LNA co-integration [41]. Please note that in the figure the blocks in dark gray represent external components.

The transceiver has been integrated in a standard digital 0.18 μm CMOS technology. The chip size, comprising the pads and excluding the low-frequency section, is equal to 1.25×1.5 mm^2. The die micrograph, depicted in Figure 6.6, shows the transceiver RF front-ends and frequency synthesis section.

Figure 6.7 depicts the simplified schematic of the experimental setup. The TRX IC is mounted on the PCB together with three BAW dies (one BAW resonator and two BAW filters, one for the transmitter and one for the receiver) and the CSEM ICYCOM SoC [88] (μPR IC) which provides baseband and computational capabilities to the test

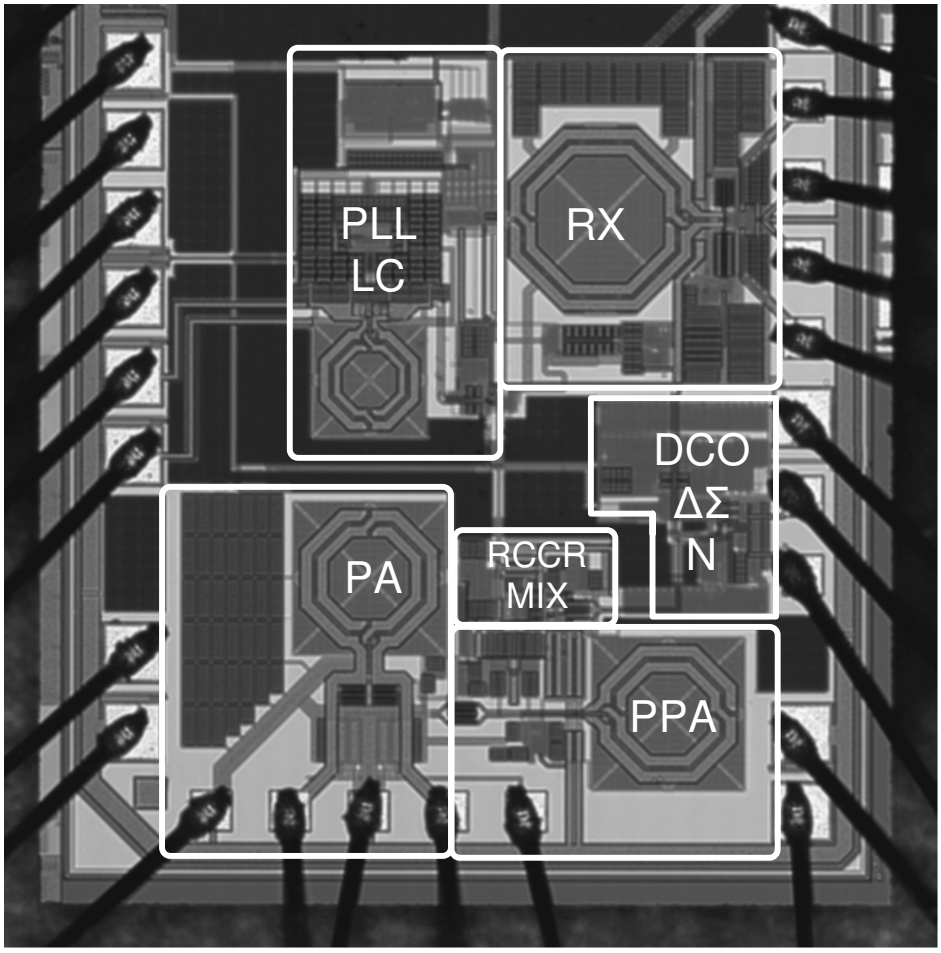


Figure 6.6: Micrograph of the TRX IC bonded on the test PCB.

setup. As for the PCB used to characterize the amplifying chain, here also SMD baluns are used to perform the single-ended to differential signal transformation and to allow accessing the RX input and the TX output with standard 50 Ω RF connectors.

To set the transceiver configurations and program the frequency synthesis, serial and parallel interfaces have been implemented on the TRX IC, providing access to the chip internal registers as well as to some analog signals. The transceiver static settings as the block biases are written with the serial interface, while the parallel bus is used in transmit mode for direct modulation and in receive mode to provide the down-converted quadrature baseband signals to the μPR IC analog baseband section, which includes channel filtering, digital conversion and afterwards processing functionalities such as demodulation, received signal strength indication (RSSI) and automatic gain control (AGC).

The whole interface between the two IC is composed of a total of 24 lines, divided into I2C data and clock, 16 lines for the bus data and 4 bits reserved for the address, and clock and read/write lines to control the parallel bus mode. To properly generate the modulation data and demodulate the incoming stream, the digital baseband section is clocked on a 32 MHz signal which is generated by fractional division of the TRX IC BAW oscillator.

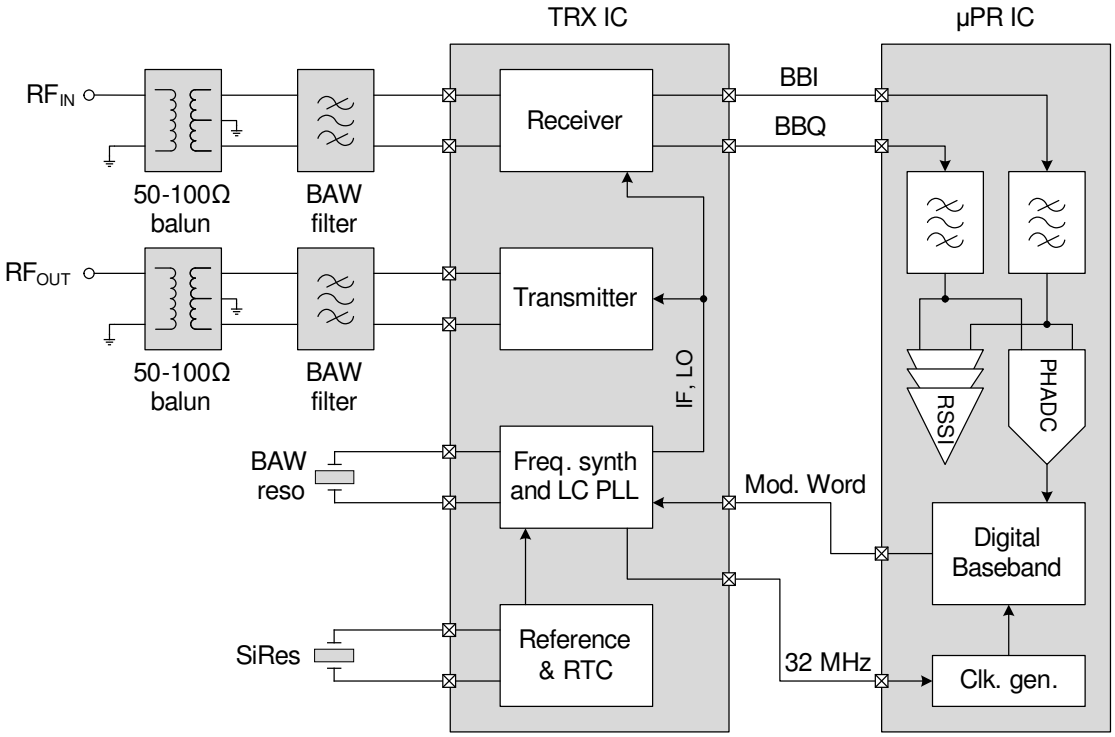


Figure 6.7: Simplified schematic of the experimental setup.

6.2.1 Frequency synthesis

Figure 6.8 shows the RF carrier phase noise measured at the power amplifier output, obtained after up-converting the IF signal with the BAW oscillator. The IF is set at $f_{\mathrm{BAW}}/32$ and the LC oscillator is locked at 28/32 f_{BAW}, resulting in an RF carrier of 2.412 GHz. This particular configuration has been chosen to avoid spurs coming from couplings of the dividers, which could have been reduced with a more careful routing of the supply lines and with the use of decoupling capacitors near the noisy blocks.

In integer division mode (black curve) the measured phase noise corresponds to −136.6 dBc/Hz at 1 MHz offset from the carrier. Starting from this frequency, and for higher frequency offsets, the transmitter noise floor limits the phase noise performance. When the fractional mode is activated to generate a continuously programmable IF frequency, the BAW oscillator phase noise is affected at high frequency (gray curve), increasing up to about −123 dBc/Hz at 1 MHz offset. There, the $\Delta\Sigma$ quantization noise seems to be not sufficiently filtered by the PLL. The degradation at low frequency offset can be explained by the fact that the RF carrier frequency changes continuously when the fractional mode is set, thus affecting the measurements.

6.2.2 Transmitter

The transmitter has been tested together with the synthesis section to validate the spurs suppression capability achievable with the proposed combination of SSB mixing and selective amplification. Compared to the amplifier chain measured in Section 6.1, here a different floorplan has been used for the selective amplifier (see Figure 6.6). In

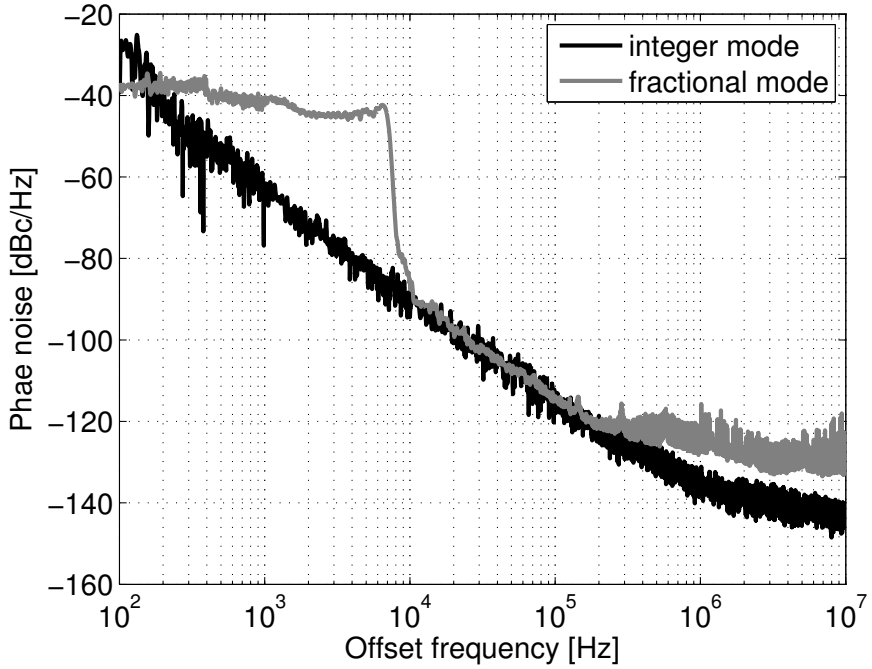


Figure 6.8: Phase noise of the synthesized RF signal measured at the power amplifier output. The carrier frequency is at 2.412 GHz.

particular, to reduce the surface occupation, a power amplifier using only one supply pad and one ground pad has been implemented; moreover, the area dedicated to the supply bypass capacitance has been reduced.

Figure 6.9 shows the unmodulated broadband output spectrum measured at the 50 Ω RF connector, when all the synthesis and transmitter blocks are activated. The curve is normalized to the carrier output power (5.4 dBm) and centered on the BAW DCO oscillation frequency (2.339 GHz for this particular sample). The IF frequency is set to $f_{\mathrm{BAW}}/32 \approx 73.1$ MHz in order to locate the RF signal at the lower edge of the BAW filter characteristic, corresponding to the worst possible case for the spurs suppression.

Different spurs are present in the output spectrum, lying both on harmonics and subharmonics of the IF frequency. The highest spurs, corresponding to the 2^{nd} harmonic of the IF frequency, is due to the non-perfect 50% duty-cycle of the IF signal. For this particular configuration, this spur falls on the filter band upper edge and thereby it does not experience any suppression. Nevertheless, it remains at values as low as −48 dBc with respect to the RF signal, indicating a very good control of the IF duty cycle (it corresponds to an error of 19 ps on the waveform duty cycle).

All the spurs at the −1, +3, −5, etc., IF harmonics take advantage of both the SSB mixer and the BAW filter rejections, experiencing suppressions always better than 63 dBc. The spurs filtered by the BAW only (−3, +5, −7 etc.), instead, lie at frequency offsets far enough from the filter band to be rejected by at least 50 dBc. The BAW DCO feedthrough is measured at −61 dBc. Finally, the other additional components present at IF subharmonics (1/4 the IF frequency) are due to couplings of the system clock

Table 6.1: Selective transmitter current consumption

Block	**Consumption [mA]**	Comments
IF buffer	0.35	-
RC/CR	1.46	-
SSB mixer	2.30	-
PPA	2.39	-
PA	21.49 (8.80)	@ 5.4 dBm (@ 0 dBm)
Total	27.99 (15.30)	@ 5.4 dBm (@ 0 dBm)

(set to $f_{\mathrm{BAW}}/128$), which is buffered outside the chip to clock the digital baseband.

Since the maximum transmission output power achieved is equal to 5.4 dBm, the spurs suppression is largely sufficient to comply with the ETSI and FCC -30 dBm requirements.

The transmitter consumption breakdown in TX mode, at the maximum output power of 5.4 dBm, is summarized in Table 6.1. All the blocks work with a supply equal to 1.6 V, while the power amplifier supply voltage is 1.2 V. The numbers in brackets provide the maximum power consumption for an output power reduced to 0 dBm.

With respect to the stand-alone amplifier chain it can be noted that the amplifier drain efficiency descends here to about only 13.6%. Since the power amplifier implementation is exactly the same for the two chips, this performance degradation can be explained by mainly two reasons. The first resides in the additional restrictions imposed by the different floorplan. These forced to use only one bond connection for the supply voltage and to the reduction of the area dedicated to the decoupling capacitance, both having an impact on the amplifier efficiency. The second reason, confirmed by post simulation extraction, is that the capacitive load at the mixer output has been underestimated. Since the SSB mixer is resistively loaded, the additional parasitic capacitance causes a significant attenuation of the signal swing at the preamplifier input, thus decreasing the amplifier output power and efficiency.

6.2.3 TX mode under modulation

Frequency modulation of the RF carrier has been performed by programming the digital baseband of the ICYCOM SoC, which is clocked on a 32 MHz signal generated from division of the BAW DCO. The resulting digital word is then used in the implemented transceiver to drive the $\Delta\Sigma$ modulator controlling the IF generation.

Figure 6.10 depicts the spectrum of two GFSK signals modulated at a data rate of 1 Mb/s and with a $BT = 0.5$.

The black line corresponds to Bluetooth modulation with index equal to 0.34. The power at ± 500 kHz offset from the central frequency is -21.7 dBc and -21.4 dBc, which is compliant with the -20 dBc specifications. The adjacent channel power is -42 dBm for a channel offset of two and -49 dBm for a channel offset of three, lower than the Bluetooth specifications of -20 dBm and -40 dBm adjacent channel power.

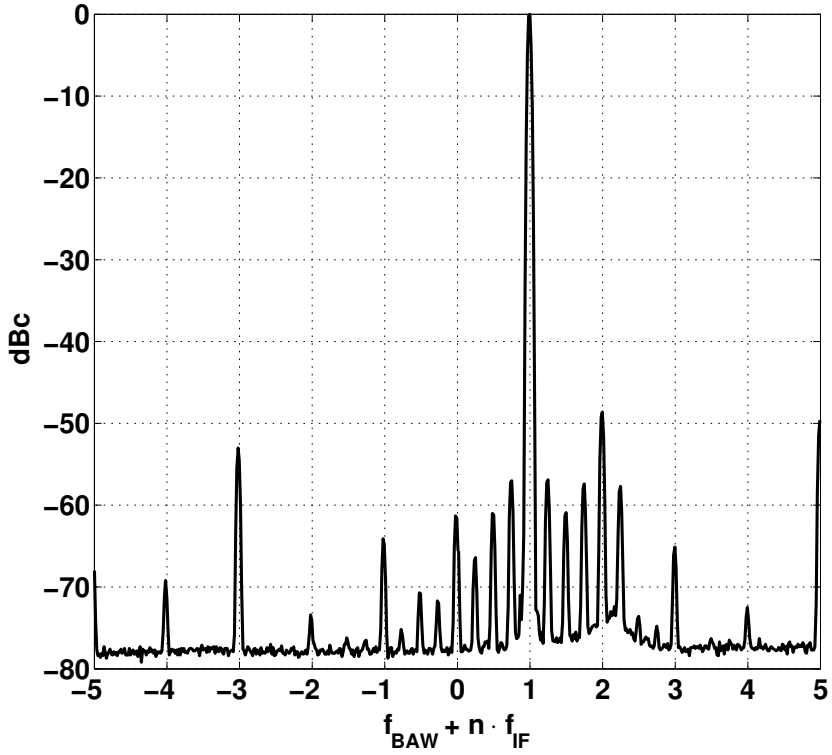


Figure 6.9: Measured broadband output spectrum normalized to the carrier power, for $f_{BAW} = 2.339$ GHz and $f_{IF} = 73.1$ MHz. RBW = 3 MHz.

The gray line represents Bluetooth Low Energy modulation, with index equal to 0.5. The adjacent channel power is −41 dBm for a channel offset of two and −44 dBm for a channel offset of three, satisfying the requirements of −20 dBm and −30 dBm adjacent channel power.

In addition, both GFSK and FSK modulations have been tested at different datarates from 100 kb/s up to a maximum of 1 Mb/s, without experiencing any problem.

Finally, a decomposition of the total consumption in transmit mode is reported in Table 6.2. The transceiver current consumption measured while modulating the 5.4 dBm carrier at 1 Mb/s is 35.6 mA (corresponding to 47.3 mW). The overall chip efficiency is thus equal to 7.4%.

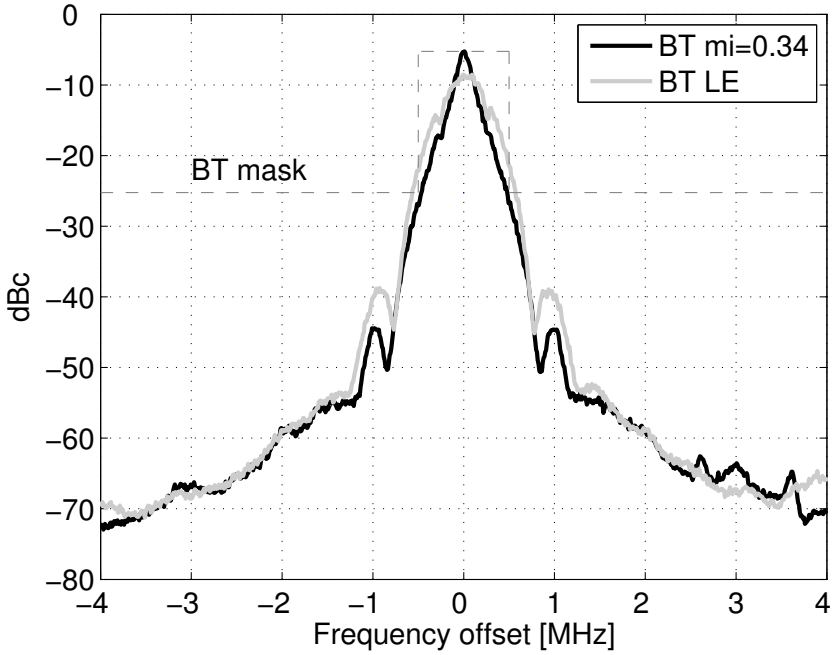


Figure 6.10: Measured Bluetooth (mi = 0.34) and Bluetooth Low Energy spectra normalized to the unmodulated RF signal. RBW = 100 kHz.

Table 6.2: Transmitter performance summary

	Cons. [mA]	**Power [mW]**	**Comments**
BAW DCO	1.48	2.37	-
Dividers (frac. mode), $\Delta\Sigma$	2.05	3.28	-
LC VCO	2.82	3.38	-
PLL dividers, PFD	1.30	2.08	-
Tot. Synthesis	7.65	11.11	-
Selective TX	27.99 (15.30)	36.19 (20.96)	@ 5.4 dBm (0 dBm)
Chip in TX mode	35.64 (22.95)	47.3 (32.07)	@ 5.4 dBm (0 dBm)

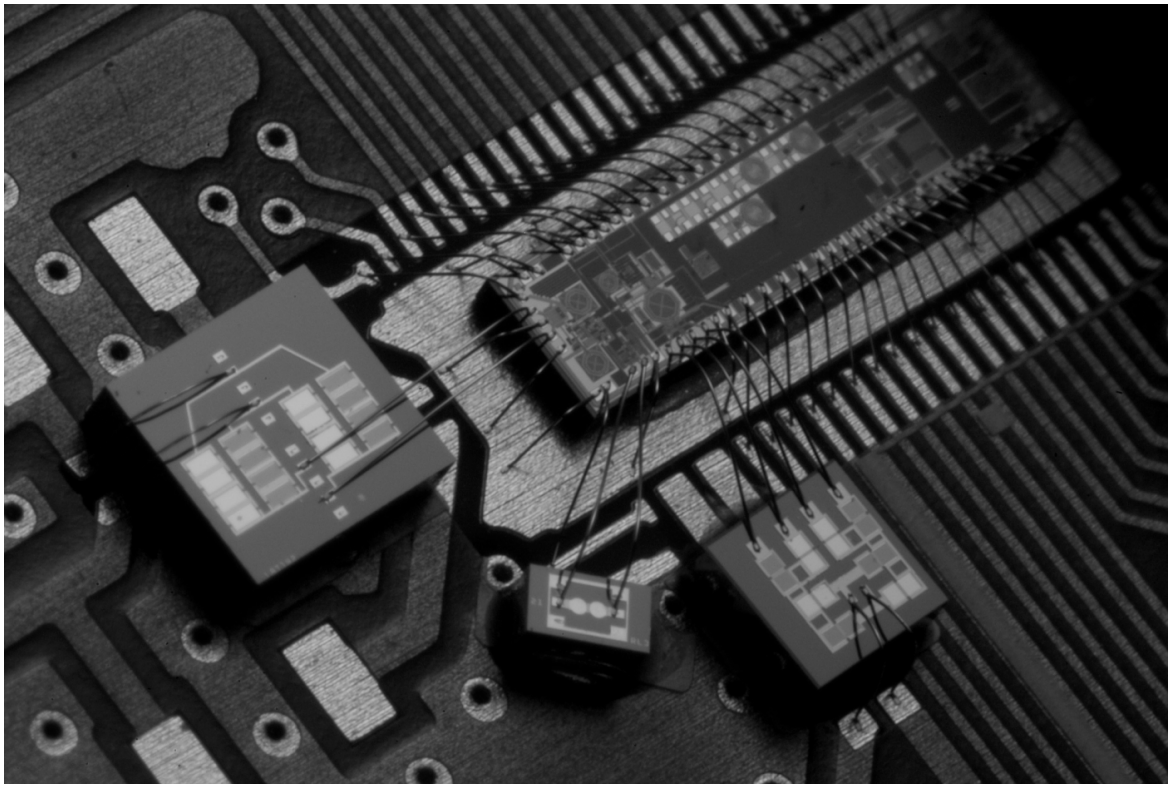


Figure 6.11: Transceiver bonded on the PCB.

Chapter 7

Conclusion

7.1 Achievements

The following conclusions can be drawn from the implementation and the validation of the 2.4 GHz BAW-based transmitter:

- A transmitter architecture allowing to cover the 2.4 GHz, 80 MHz wide ISM band has been demonstrated. This allows achieving one of the main requirements of the transmitter, i.e. the possibility to address multi-channel applications in that band.
- The selectivity provided by the use of the BAW filter, together with the rejection of the SSB mixer, validates the choice of the up-conversion architecture. In fact, the image frequency and the IF spurious are kept far below the spurs requirements.
- The frequency selectivity also relaxes considerably the image rejection requirements, enabling the generation of the quadrature LO signals with a simple RC-CR network and avoiding the implementation of any quadrature error compensation techniques.
- The integration of the BAW resonators with a class E like power amplifier has been achieved. In particular the BAW resonators replace part of the amplifier passive network participating in the drain voltage shaping. This allows exploiting the good efficiencies of the class BE amplifier while providing it with the added advantage of frequency selectivity.
- The use of the up-conversion architecture in combination with the LC PLL allows maintaining unchanged the excellent phase noise performance of the BAW DCO, thus allowing the synthesis of high purity RF carriers.
- The high PLL bandwidth enables modulations at data rates higher than 1 Mb/s. Moreover, thanks to the transmitter low phase noise, the measured output spectrum resulting from 1 Mb/s GFSK Bluetooth and Bluetooth LE modulations satisfies the relative and absolute mask requirements, demonstrating the compatibility with those two standards.

Table 7.1: A comparison with state-of-the-art WSN transmitters

	Tech.	$\mathbf{P_{out}}$ **[dBm]**	$\mathbf{P_{cons}}$ **[mW]**	$\eta_{\mathbf{TX}}$ **[%]**	**DR [kb/s]**	**Freq.**	$\mathbf{V_{dd}(V_{dd\_pa})}$ **[V]**
Melly [1]	0.5 μm	9.8	25	38	20	433 MHz	1.2
Molnar [2]	0.25 μm	-6	1.32	19	100	900 MHz	3
Chee [3]	0.13 μm	0.8	2.55	46	330	1.9 GHz	0.65
This work	0.18 μm	5.4	47.3	7.4	1000	2.4 GHz	1.6 (1.2)
Eo [4]	0.18 μm	0.5	30.6	3.7	250	2.4 GHz	1.8
Cho [5]	0.18 μm	0	72	1.4	1000	2.4 GHz	1.8
Si [6]	0.13 μm	2	56.5	2.8	1000	2.4 GHz	1.2 (3.3)

7.2 Discussion

It is quite difficult to compare the presented work with other state-of-the-art transmitters targeted for wireless sensor network applications. As written in the introduction of this thesis, two main groups can be identified, depending on whether the transmitter has been designed with the first aim to achieve the lowest possible power consumption or to provide the compatibility with widespread standards such as Bluetooth or the IEEE 802.15.4.

Table 7.1 reports the performance of different transmitters belonging to the two groups and compares them with the BAW-based transmitter measured results. The overall efficiencies achievable by designing ad-hoc systems for WSN are unattainable by high data rate transmitters compatible with standards at 2.4 GHz.

The power consumption of the proposed work would prevent its use in applications requiring long battery life. In this sense, the transmitter suffers the choice of favoring the signal spectral quality, which forces a high power consumption in the synthesis section (about 11 mW) and imposes the use of an up-conversion architecture in the transmitter chain. This structure is inherently less efficient than other architectures as the direct modulation transmitter, which has a lower number of circuits working at the RF. Nevertheless, the proposed work compares favorably with the other 2.4 GHz transmitters, thus validating the advantage of BAW resonators also in the transmitter chain. Moreover, if the BAW-based amplifier implemented in the transmitter had achieved the same performance as that measured for the stand-alone chip, the overall chip efficiency would have been potentially equal to 14%, thus placing the BAW-based transmitter exactly halfway between the two groups. This means that there are still margins for improvement. Moreover, improvement of the BAW resonators quality factors will also further increase the transmitter efficiency.

This comparison does not take into account the spectral purity of the RF signal, for which the proposed transmitter (-116 dBc/Hz at 100 kHz offset) is definitely superior to the other works, except that for the implementation presented by Chee (-124 dBc/Hz at 100 kHz offset) which exploits FBAW resonators with quality factors

higher than 1000 [3].

7.3 Future work

The obtained results prove that the use of BAW resonators in the transmitter architecture can allow achieving a high signal spectral purity while preserving the efficiency. Nevertheless, the transmitter power consumption is too high for addressing WSN applications with long battery life. Moreover, the PA and LNA BAW filters are still distinct, impacting the system compactness. At the time this thesis is written, a chip aiming to validate some improvements to the BAW-based transceiver has been laid out. The different modifications are with respect to:

- The power amplifier and low-noise amplifier: an output power of 0 dBm is targeted to achieve longer battery life. PA and LNA are co-integrated in a current-reusing structure which allows sharing the pads and using a single BAW filter.
- Up-conversion mixer: to decrease the power consumption while keeping the carrier phase noise low, a passive voltage mixer is used for the up-conversion. Moreover, when driven by the IF buffer, the mixer can provide the amplifier with a sufficient swing to avoid the need of the TX pre-amplifier, if an output power of 0 dBm is targeted. This further decreases the overall power consumption.
- LC oscillator: the LC oscillator integrated in the filtering PLL was not optimal since it was re-adapted from a totally different design. An improved oscillator exploiting the use of wire-bonds has been integrated to decrease the contribution on the overall power consumption.

Other future work will concentrate on the development of a platform exploiting the BAW-based transceiver. The temperature compensation of the low-reference frequency, control of the different operating modes of the transceiver and RF channel selection have to be implemented to demonstrate the transceiver operation in typical working environments.

Appendix A

Power Amplifiers FOMs and classification

This appendix has the aim to introduce the reader on simple but fundamental concepts on the power amplifiers features and classification. The most important figures of merit characterizing the power amplifier will be introduced, then an overview of the different amplifier classes will be done.

A.1 Power amplifier features

Four main figures of merit of a power amplifier are: output power, efficiency, gain and linearity. Their definition is here explained.

A.1.1 Output Power

The output power is defined as the active power delivered by the power amplifier to the antenna. Starting from defining the *instantaneous power* as

$$p(t) = v(t) \cdot i(t), \tag{A.1}$$

the *total output power* is calculated as

$$P_{tot} = \langle p(t) \rangle = \lim_{T \to 0} \frac{1}{T} \int_{-T/2}^{T/2} p(t) dt. \tag{A.2}$$

If the signal is sinusoidal with frequency f_c and period T_c, (A.2) can be simplified to

$$P_{tot} = \langle p(t) \rangle = \frac{1}{T_c} \int_{-T_c/2}^{T_c/2} p(t) dt. \tag{A.3}$$

Then, assuming to have a purely resistive load, we can write the following:

$$\begin{aligned} P_{o,tot} = \langle v_{out}(t) \cdot i_{out}(t) \rangle &= \frac{\langle v_{out}^2(t) \rangle}{R_L} \\ &= \frac{V_{o,rms}^2}{R_L}, \end{aligned} \tag{A.4}$$

with R_L load resistor. In most of the cases the antenna is designed to be purely resistive in the frequency range of interest. While the majority of the designs are addressed to a single ended charge of 50Ω, the effective load seen by the power amplifier can be made different, for example by the use of a matching network, so that it can assume theoretically every desired value.

A.1.2 Efficiency

The efficiency indicates the ability of the amplifier to convert the DC power drawn from the supply in AC power delivered to the antenna. The most common definitions present in the literature are reported.

To characterize the efficiency of the amplifier power stage, the *drain efficiency* η_d, and the *conversion efficiency* η_{conv}, can be used. The former represents the ratio between the power delivered to the load at the working frequency (P_o) and the DC power consumption of the power amplifier stage:

$$\eta_d = \frac{P_o}{P_{DC,PA}}. \tag{A.5}$$

On the other hand the conversion efficiency is given by the ratio of the total RF output power on the load ($P_{o,\text{tot}}$) divided by the DC power consumption, thus accounting for the signal harmonics:

$$\eta_{conv} = \frac{P_{o,tot}}{P_{DC,PA}}; \tag{A.6}$$

consequently, $\eta_{conv} \geq \eta_d$.

These two figures of merit do not take into account the supply power drawn by the pre-amplifier stages. To do that, another efficiency definition is introduced. It is the *overall efficiency*, η_{ov}, defined as [89]

$$\eta_{oa} = \frac{P_o}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,DRV,i}}, \tag{A.7}$$

where, the second term in the denominator sums the consumptions of all the driver stages. As a consequence, this figure of merit is more interesting from a system level point of view.

The last figure of merit used in literature is the *power added efficiency*, which takes into account the power of the amplifier input signal. It is calculated as

$$PAE = \frac{P_o - P_{in}}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,DRV,i}}, \tag{A.8}$$

and relates the amplifier efficiency with the power added by the amplifier.

A.1.3 Gain

The power gain is usually more used than the voltage gain for power amplifiers since the impedance level can vary considerably along the transmitter chain. The power gain takes into account those variations giving thus a more fair indication on the circuit performances. It is defined as

$$G_{p,dB} = 10 \log \frac{P_o}{P_{in}}. \tag{A.9}$$

A.1.4 Linearity

The are are two possible definitions of linearity for a power amplifier: phase and amplitude linearity. Phase linearity is in general not a big concern if the bandwidth of the transmitted signal is small compared with the carrier frequency (narrow band signal), while amplitude linearity is harder to achieve and in general it involves a lower efficiency.

The phase and amplitude distortions occurs as a conversion PM-PM and AM-AM but also other distortions can appear as for example AM-PM when the varying envelope induces phase errors and PM-AM when the frequency modulation of the carrier causes amplitude errors.

Since in modern communications highly complex signals are created, the IP3 value gives not always a complete information about the spectral components that are generated at the output of the power amplifier. Different tests like *spectral mask measurement*, *error vector* and *adjacent channel power* are thus required.

A.2 Power amplifier classes

Even if it is quite difficult to classify integrated power amplifiers, it is useful to separate them in groups depending on the operation principle used, with the aim to understand the differences in output power, gain, efficiency and linearity they imply.

A first rough classification divides the amplifiers in linear and nonlinear. While the first class contains amplifiers that present both amplitude and phase linearity, the second refers to amplifiers that have only phase linearity. The main reason to use nonlinear amplifiers resides in the improved efficiency that they can yield, that not only means lower power consumption at constant output power, but implies also less stresses in the device and so higher reliability.

In the group of non-linear amplifiers, mainly two different sub-groups can be distinguished. The first is represented by the reduced conduction angle amplifiers, while the second group of non-linear power amplifiers refers to devices used as switches. The conduction angle, indicated with the letter α, represents the portion of the RF period for which the input waveform is higher than the transistor threshold voltage V_{th}.

A.2.1 Class A

The main condition for class A operation is to have an amplifier that conducts during all the period of the input waveform, hence with a conduction angle α equal to 2π. In

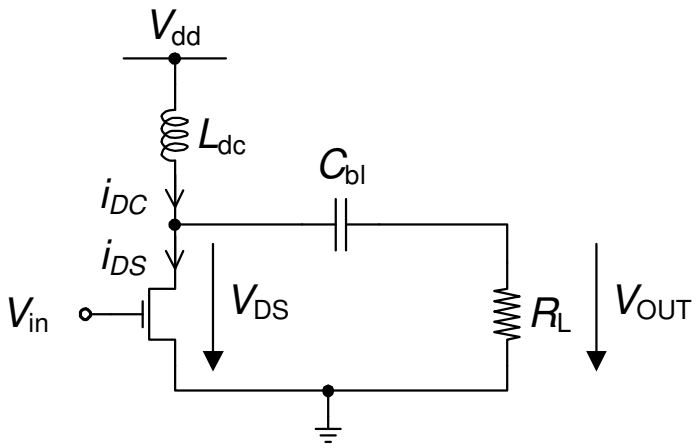


Figure A.1: Schematic of a class A amplifier.

figure A.1 a simplified circuit representing a class A amplifier is depicted. The nMOS transistor is biased in such a way the wanted DC current flows into the ideal inductor L_{dc}, while the blocking capacitor C_{bl} allows only the AC component to reach the load R_L. By assuming to drive the amplifier with a sinusoidal input, also the output current will be sinusoidal since the input stays always in the (ideally) constant g_m region of the transconductance. Consequently, the output voltage and the drain voltage will be both sinusoidal. In order to maximize the output power, the swing should be equal to $2V_{DD}$. During an input cycle the minimum drain voltage is $V_{DD} - I_L R_L$, where I_L represents the peak value of the AC current flowing into the load. It is clear that to maximize the output swing the optimum load resistor should be equal to $V_{DD}/I_L = V_{DD}/I_{DD}$, corresponding to a minimum drain voltage of zero (the transistor is assumed ideal, with a knee voltage equal to zero). In such a case the output power is equal to

$$P_o = \frac{V_o^2}{2R_L}. \tag{A.10}$$

Since the supply power can be written as:

$$P_{DC} = V_{DD} I_{DC} = \frac{V_{DD}^2}{R_L} \tag{A.11}$$

it derives that the drain efficiency of a class A power amplifier is

$$\eta = \frac{P_o}{P_{DC}} = \frac{1}{2}\left(\frac{V_o}{V_{DD}}\right)^2. \tag{A.12}$$

The maximum drain efficiency for this amplifier, in a purely ideal case, is thus equal to only 50%.

A.2.2 Reduced Conduction Angle Amplifiers: class AB, B and C

The power amplifier efficiency can be improved by reducing the conduction angle, i.e. by decreasing the DC bias at the gate, at the expense of an increase of the nonlinearities.

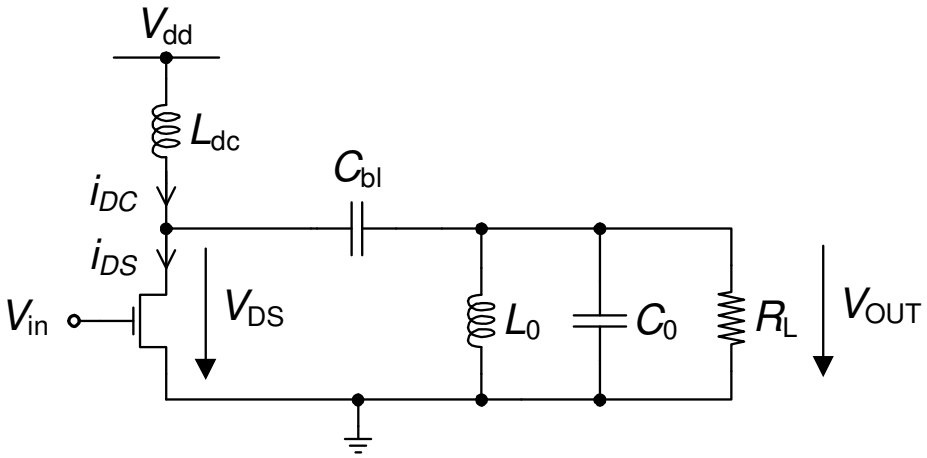


Figure A.2: Schematic of a reduced conduction angle amplifier with ideal shunt resonator.

The general idea of improving the efficiency in a power amplifier relies on the tentative of reducing the lapse of time for which both the drain current and the drain voltage are different from zero. In that period, in fact, the transistor dissipates energy that cannot be delivered to the load.

The conduction angle value is directly related to the harmonic content present on the drain current, even if a constant g_m is supposed [62, 59]. The amplifier is thus classified as non-linear. Figure A.2 depicts a simple reduced conduction angle amplifier. An ideal LC tank in parallel with the load resistor allows short-circuiting the harmonic components of the drain current, ensuring the output voltage to be sinusoidal. The maximum peak voltage on the output in ideal conditions is again equal to V_{DD}, corresponding to a sinusoidal drain voltage sweeping between $2V_{DD}$ and zero.

The next step is to calculate the amplifier output power and efficiency as functions of α. The transistor drain current can be written as [62]:

$$i_{DS}(\theta) = \begin{cases} I_{DC} + I_{pk}\cos(\theta) & -\alpha/2 \leq \theta \leq \alpha/2 \\ 0 & \text{elsewhere} \end{cases}, \tag{A.13}$$

where θ is the angular time,

$$\cos(\alpha/2) = -\frac{I_{DC}}{I_{pk}} \tag{A.14}$$

and

$$I_{pk} = I_{max} - I_{DC}. \tag{A.15}$$

Figure A.3 depicts the normalized drain current ($I/(V_{DD}/R_L)$), drain voltage (V/V_{DD}) and their multiplication, representing the instantaneous power dissipated on the transistor. By substituting (A.14) and (A.15) into (A.13), the drain current becomes:

$$i_{DS}(\theta) = \frac{I_{max}}{1 - \cos(\alpha/2)}[\cos(\theta) - \cos(\alpha/2)]. \tag{A.16}$$

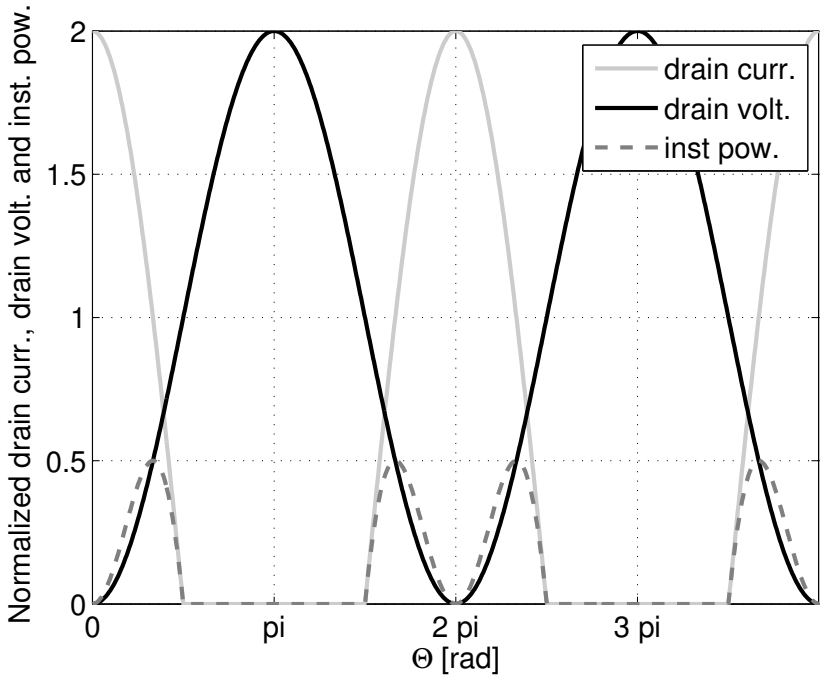


Figure A.3: Normalized drain current (black), drain voltage (light gray) and instantaneous transistor dissipated power (dashed dark gray) for $\alpha = \pi$.

In order to find the different harmonic components, i_{DS} is expanded by Fourier Series. The DC current is given for example by:

$$\begin{aligned} I_{DC} &= \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2}\frac{I_{max}}{1-\cos(\alpha/2)}[\cos(\theta)-\cos(\alpha/2)]d\theta \\ &= \frac{I_{max}}{2\pi}\frac{2\sin(\alpha/2)-\alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \end{aligned} \tag{A.17}$$

and the magnitude of the n-th harmonic current is equal to:

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2}\frac{I_{max}}{1-\cos(\alpha/2)}[\cos(\theta)-\cos(\alpha/2)]\cos(n\theta)d\theta. \tag{A.18}$$

For example, the first harmonic simplifies in

$$I_1 = \frac{I_{max}}{2\pi}\frac{\alpha-\sin(\alpha)}{1-\cos(\alpha/2)}. \tag{A.19}$$

Since the harmonics of the fundamental frequency flow in the LC trap and the ideal inductor L_{DC} allows only DC current to be drawn from the supply, the current and so the voltage on the load will be ideally sinusoidal, with an output equal to:

$$P_o = R_L\frac{I_1^2}{2} \tag{A.20}$$

The efficiency can then be calculated as usual with the ratio P_o/P_{DC}, as done for the class A amplifier.

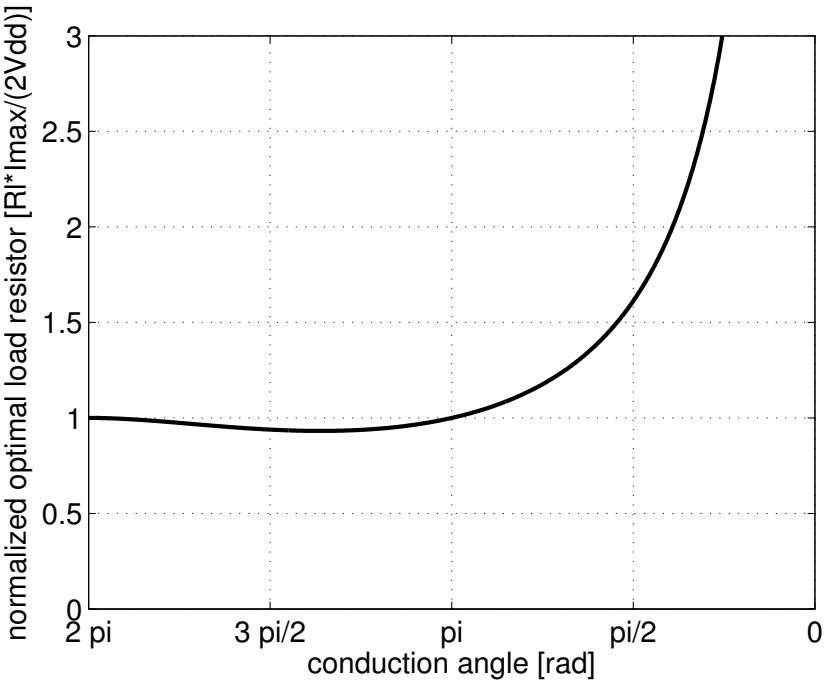


Figure A.4: Optimum load resistor.

While sweeping the conduction angle we can use two different techniques to maintain the output peak voltage constant and equal to V_{DD} (the desaturation of the transistor is still not taken into account): we can either adjust the transistor peak current or the load resistor R_L. Depending on the chosen technique, we have to use one of the two following formulas:

$$I_{max} = 2\pi I_1 \frac{1-\cos(\alpha/2)}{\alpha-\sin(\alpha)} = 2\pi \frac{V_{DD}}{R_L} \frac{1-\cos(\alpha/2)}{\alpha-\sin(\alpha)} \tag{A.21}$$

$$R_L = \frac{V_{DD}}{I_1} = 2\pi \frac{V_{DD}}{I_{max}} \frac{1-\cos(\alpha/2)}{\alpha-\sin(\alpha)}. \tag{A.22}$$

By choosing to tune the maximum current, it turns out that for low conduction angle values the transistor peak current will tend to a Dirac pulse, thus overcoming the working capabilities of the active device. On the contrary, the method which calculates the optimum resistor for a given α leads the former to tend towards infinite for the conduction angle reaching zero (Figure A.4), degrading the output power performance.

A.2.3 Class F

The reduced conduction angle amplifiers show that the efficiency increases if the time for which the drain current and the drain voltage are simultaneously different from zero decreases. Moreover, in between the different classes of reduced conduction angle amplifiers, the class B operating mode seems to be particularly interesting, since it

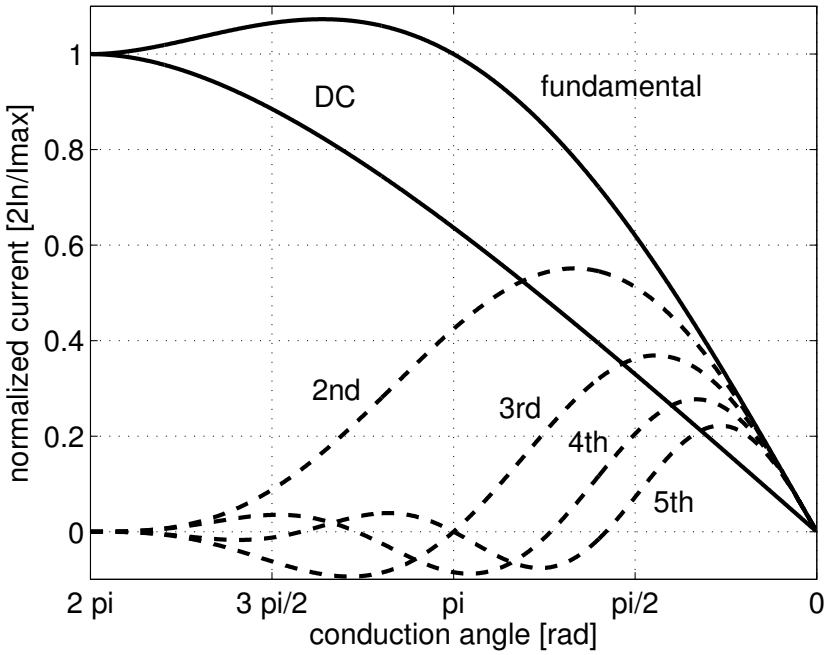


Figure A.5: Fourier analysis of the drain current.

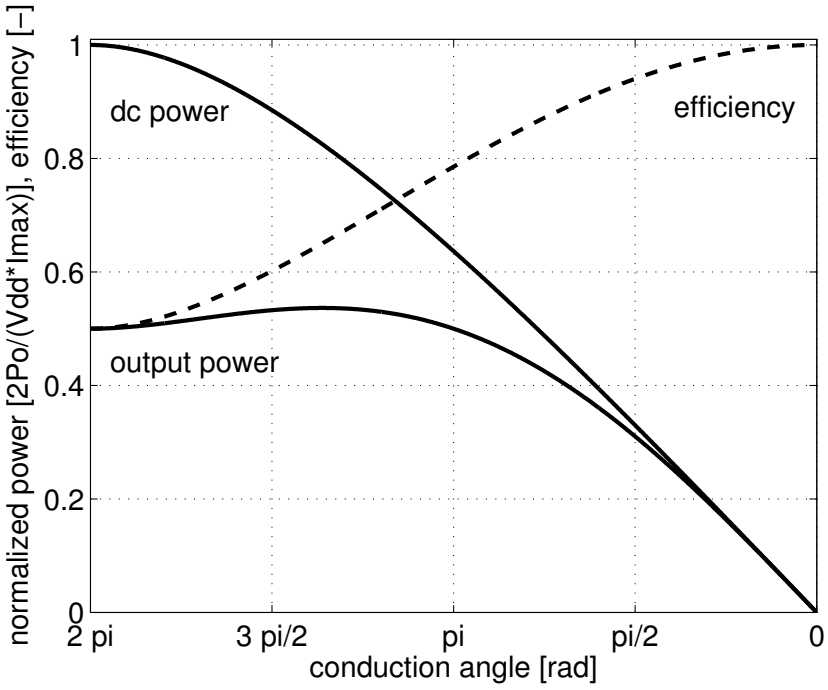


Figure A.6: Power and efficiency analysis.

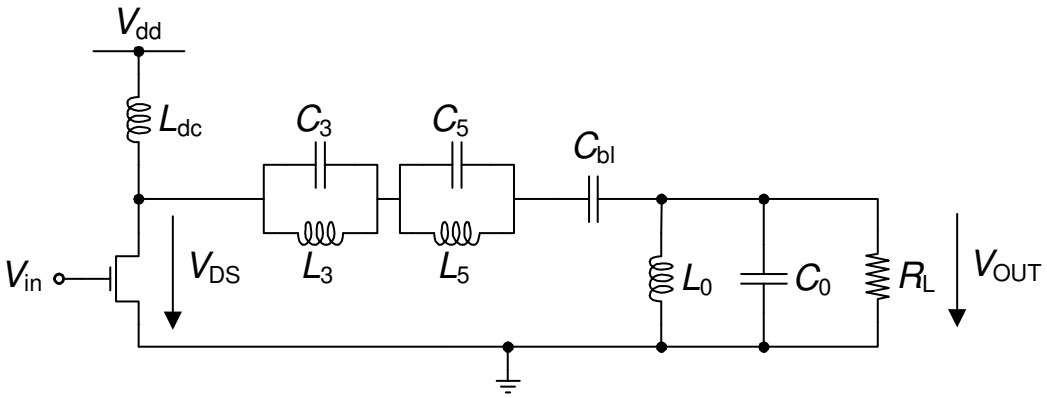


Figure A.7: Class F amplifier

allows achieving a good efficiency while maintaining the same output power of the class A amplifier.

To further improve the efficiency, class F amplifier uses harmonics of the input frequency to square the drain voltage and to reduce the energy wasted by the transistor. The amplifier schematic, depicted in Figure A.7, remains similar to that of the reduced angle amplifiers, but uses some additional resonators tuned on odd multiples of the input frequency placed in series before the load (in the figure one resonator tuned at the third harmonic and one at the fifth harmonic). The drain voltage is thus the sum of the sinusoidal output voltage plus the harmonics introduced by the resonators. The more are the harmonics added, the higher is the amplifier drain efficiency (the resonator losses are assumed negligible), reaching an efficiency of 100% with an infinite number of resonators. The ideal maximum efficiency achievable by using only two series resonators (one at the third and one at fifth harmonic of the input signal) is however already 92%.

A.2.4 Switching amplifiers

The drain voltage squaring can be also achieved by overdriving the transistor with a sufficiently high input waveform (ideally a square waveform) in such a way the active device behaves like a switch. This generates an ideal conversion efficiency equal to 100%, since no overlap in between the drain current an the drain voltage waveforms can occur. To reach a drain efficiency of the same value no harmonic power has to be lost on the load, forcing to the use of a tuning network. While the class E amplifier has already been treated in this thesis, here the behavior of the other switching amplifier, the class D, is briefly reported.

Class D

The class D power amplifier (Figure A.8) consists of one pMOS and one nMOS connected as for the digital inverter configuration. A series tank filters out the signal harmonics and allow to have theoretical sinusoidal output waveform. For a square wave input waveform having 50% duty cycle and infinite slope, the drain voltage is a

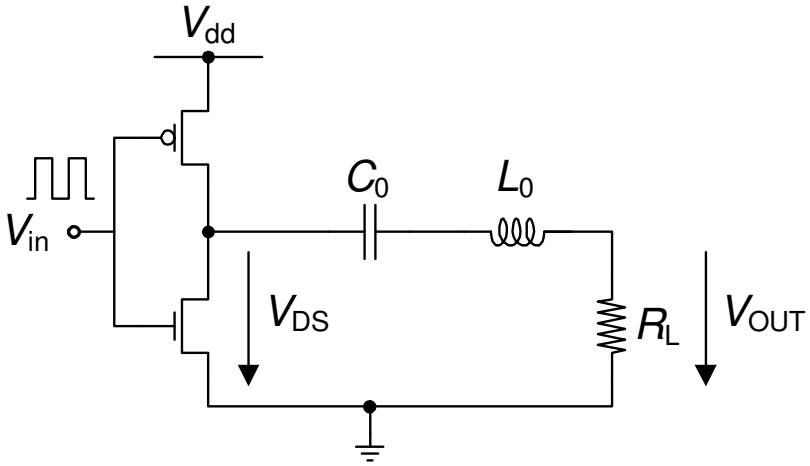


Figure A.8: Class D amplifier.

square wave between V_{DD} and zero, with DC value equal to $V_{DD}/2$. Its first harmonic coefficient is equal to $2V_{DD}/\pi$, hence the output current amplitude is

$$I_o = \frac{2/\pi V_{DD}}{R_L} \tag{A.23}$$

and the output power

$$P_o = \frac{2}{\pi^2}\frac{V_{DD}^2}{R_L} \tag{A.24}$$

Several drawbacks limit the efficiency of this amplifier in real implementations. For example, by dynamically switching the output voltage, the charges stored at the transistor drain are periodically discharged to ground, dissipating power. Moreover, finite rise and fall times of the amplifier waveforms decrease the amplifier efficiency. Finally, the lower mobility of the pMOS with respect to the nMOS requires a high total input gate capacitance to balance the inverter. This will necessitate a higher power consumption in the driver stage, with a negative effect on the amplifying chain overall efficiency. All these disadvantages make the use of the class D amplifier less attractive for RF applications.

Appendix B

Lumped element model for parallel bonds

The implemented model computes the inductance (L_b) and series resistance (R_b) of a bond, together with the coupling factor M and the coupling capacitors C_c with respect to a parallel bond with the same length. The parameters needed by the model are the bond length l_{bond}, the diameter d, the spacing between the two bonds g, material resistivity ρ and working frequency f.

To calculate the bond inductance, the Rosa estimation has been used:

$$L_b = 0.2 \cdot 10^{-9} \frac{\mathrm{H}}{\mathrm{mm}} l_{bond} \left(\ln \left(\frac{4 l_{bond}}{d} \right) - k \right), \tag{B.1}$$

where k is an empirical constant which can vary from 0.75 (DC) to 1 (at HF). The coupling in between the two wires can be computed by

$$\begin{aligned} M = 0.2 \cdot 10^{-9} \frac{\mathrm{H}}{\mathrm{mm}} l_{bond} \left[\ln \left[\frac{l_{bond}}{g} + \sqrt{1 + \left(\frac{l_{bond}}{g} \right)^2} \right] + \right. \\ \left. - \sqrt{1 + \left(\frac{l_{bond}}{g} \right)^2} + \frac{g}{l_{bond}} \right], \end{aligned} \tag{B.2}$$

while the coupling capacitance is

$$C_c = l_{bond} \frac{\pi \epsilon_0}{\ln \left(\frac{2g}{d} \right)}. \tag{B.3}$$

Finally, the wire resistance can be calculated taking into account the skin depth

$$s = \sqrt{\frac{2\rho}{2\pi f \mu_0}} \tag{B.4}$$

into the following formula:

$$R_b = l_{bond} \frac{\rho}{\pi (d - s) s}. \tag{B.5}$$

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2. D. Ruffieux, J. Chabloz, M. Contaldo, C. Muller, F. X. Pengg, P. Tortori, A. Vouilloz, P. Volet and C. Enz, "A narrowband multi-channel 2.4 GHz MEMS-based transceiver," in *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 228-239, Jan. 2009.

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