An 8W-2MHz buck converter with adaptive dead time tolerant to radiation and high magnetic field

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A high efficiency 8W-2MHz ASIC buck converter tolerant to radiation and high magnetic field is presented. A new adaptive control circuit for the dead time management is integrated to increase the efficiency during quasi-square wave (QSW) operation. The ASIC is designed in the IHP SGB25GOD 0.25µm technology and developed for the Large Handron Collider (LHC) experiments upgrade, where the main constrains are the presence of a severe radiation environment (up to hundreds of Mrad), a high magnetic field (up to 4 Tesla) and mass limitation because extra material is detrimental to the physics performance of the detector.

I. Introduction

Modern High Energy Physics experiments consist of huge detectors that nevertheless have to be built with minimum amounts of non-sensitive material as to maximize the coverage of sensors and to minimize the traversal of insensitive infrastructural materials. For instance, a detector such as the CMS experiment tracker consists of 10 cylindrical layers of thin (3-500 um) semiconductor sensors but also of several tons of copper and other metals to bring power to the electronics and consequently to cool it. The presence of this insensitive material is essential, but degrades through various phenomena, such as multiple scattering and nuclear interactions, the precision of measurement of the particles position actually performed by the sensors. The objective of this project is to provide a means to bring power to the front-end electronics with a minimum of copper and with high efficiency. As proposed in [1] and [2], an attractive power distribution scheme satisfying the new requirements is based on the use of buck DC-DC converters installed on-detector very close to the front-end readout electronics (the load). The converters would provide 1-3 A at a voltage of 3.3-1.8 V from a bus voltage of 10-12 V. A simplified scheme of this topology is shown in Figure 1.

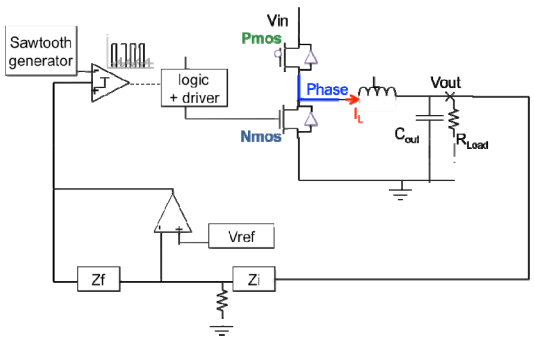

Figure 1. Block diagram of a buck converter

The radiation and magnetic field environment inside the detectors inhibits the use of a generic commercial converter. The static magnetic field in the installation reaches 4 T, a value exceeding saturation of all known ferromagnetic inductor cores. Magnetic tolerance can be attained using air-core inductors, but their value is limited below 500 nH because of space and material budget requirements dictated by the physics performance of the detectors [3]. This limitation implies the necessity of high frequency switching, f_s, above 1 MHz [4].

The radiation field can reach 250 Mrad in Total Ionizing Dose (TID), and dose of $2.5 \cdot 10^{15}$ n/cm^2 (1 MeV neutron equivalent, for displacement damage). Resilience to Single Event Effects (SEEs) is also mandatory for the reliable operation of the converter. A custom development specifically addressing tolerance to radiation and magnetic field, as well as low mass and high efficiency, is necessary. An Application Specific Integrated Circuit (ASIC) is the main building block for this custom device. ASIC radiation hardness can be achieved through the choice of a suitable commercial technology, combined with specific layout and circuit design techniques. The technology needs to offer low voltage devices for the control circuit and a high voltage extension for the design of the power transistors that need to stand the 10-12 V input voltage. Five commercial technologies have been evaluated for TID and displacement damage [5]. Two of them have shown good radiation tolerance, where the high voltage transistors could meet radiation specifications without any layout modification to the qualified design. The low-voltage transistors, instead, require modifications to the layout to meet the TID target. A first fully integrated rad-hard converter has been prototyped in one of the two technologies, in the 0.35µm node, and presented in [6]. A more advanced converter design has been made in the 0.25µm SGB25GOD technology from IHP (Innovations for High Performance microelectronics, Frankfurt Oder, Germany) that showed better radiation hardness and electrical performance [5]. The latter and more sophisticated design will be presented.

II. Converter Optimization

Efficiency, the output and input power ratio, is a fundamental estimator of the quality of a converter. The design of an ASIC for a very specific application allows the optimization of the converter to achieve the highest efficiency compatible with the global constraints. The optimization requires all sources of losses to be carefully evaluated. Losses can be divided in four different categories: conductive, switching, driving and in the control circuit. The first are due to the current flowing in the resistive power FET, in the inductor parasitic resistance and in the diodes during the dead time, the second to a non negligible Ids x Vds product during the switching time and the third to the charge and discharge of the power transistors' gate. All these losses have a strong technology dependence, hence we extracted the parameters and used them to evaluate the relative contribution of each source of losses in a multi-

dimensional space of parameters: inductor and power FET size, f_s, V_{in}, V_{out}, I_{out} and operational mode. The buck converter can operate in different modes whose characteristics depend on the inductor current during steady state. If it is continuous during the whole period the converter is operating in continuous mode (left side of Figure 2), while in discontinuous mode no current flows for some time. In the specific continuous case when a slightly negative current is allowed, the operational mode is called Quasi Square Wave (QSW) [7] [8](right side of Figure 2). This mode is conventionally used to achieve "soft" commutations with either almost zero I_{ds} current (zero current switching, ZCS) or almost zero V_{ds} voltage (zero voltage switching, ZVS).

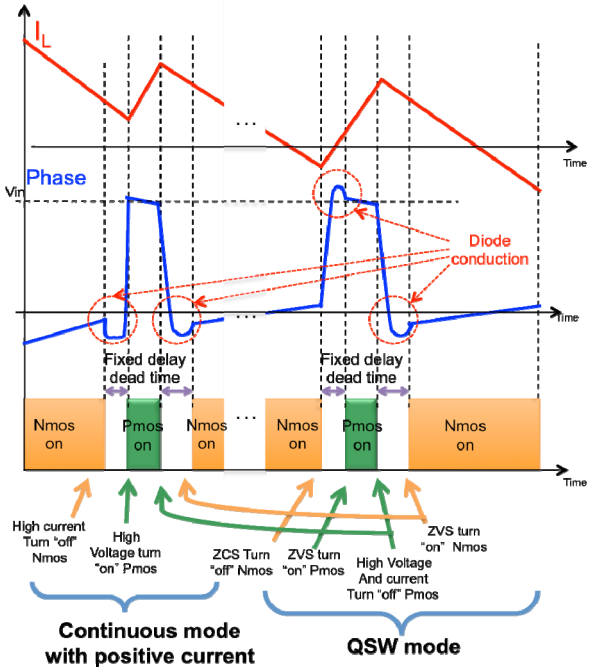

Figure 2. Continuous operational mode for a buck converter. When the current gets negative, the mode is called QSW

As shown in Figure 2 in a QSW, the small negative values of the inductor current I_L, the NMOS turns off with ZCS. During the following dead time the negative I_L charges the parasitic capacitance of the Phase node (mainly C_{gd} and C_{ds} of the power switches) until it reaches the value V_{in} + 0.7 V, thus the PMOS body diode starts conducting. The consequent turn-on of the PMOS is a ZVS because it happens at small V_{ds} (0.7 V). If the current I_L is always positive, and with a large value, these two commutations give instead origin to large losses: the NMOS turn-off happens at large I_L and the PMOS turn-on at large V_{ds} (the Phase node rises to V_{in} + 0.7 V during the dead time to allow I_L flowing in the NMOS body diode). For the remaining two commutations the situation is the same regardless the converter being in QSW or not: the PMOS turn-off is a hard switching due to the large I_L which, during the dead time, discharges the Phase capacitance and flows in the NMOS body diode allowing a ZVS NMOS turn-on (its V_{ds} is -0.7 V).

Summarizing, the QSW mode with small negative I_L allows having three soft commutations out of four. Its drawback is however the increased ripple of the inductor current, which originates more relevant conduction losses. Overall, given the target f_s above 1 MHz, the QSW mode gives the best estimated performance in our application. To reduce further the losses in this operational mode, we introduced a dedicated circuit block dynamically reducing the dead time to the minimum necessary to prevent cross-conduction. This logic block, called 'adaptive logic', is described in the next section and is effective in decreasing the losses in the body diodes.

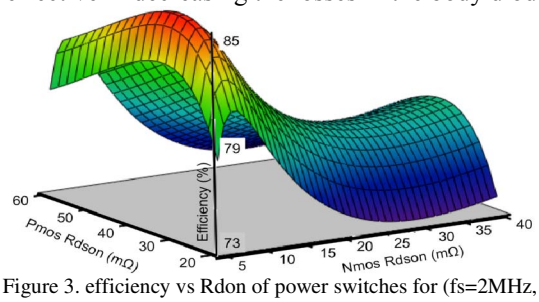

Figure 3. efficiency vs Rdon of power switches for (fs=2MHz, Vin=10V,Vout=2.5V, Iout=2A and L=200nH)

III. Circuit Design

The design of the ASIC has been mainly focused to two aspects: the design of the power FETs and associated drivers and the optimization of the control circuit with the adaptive logic.

A. *Power transistors*

As shown in Figure 3, with the developed model it is possible to choose the power FETs on-resistance to optimize the efficiency. For our requirement the best efficiency can be reached with a R_{on} of 10 and 30 m respectively for the N and PMOS that leads to a transistor width W of around 0.25 m for both and a gate capacitance around 2nF. Each power FET has been divided into eight blocks to minimize the parasitic gate resistance and each block has a driver circuit, shown in Figure 4.a. To drive the 1.6A needed to control the power transistor in less than 2 ns the last driver stage (an inverter, as shown in Figure 4) needs to be relatively big (W_{Pmos}= 0.7 mm and W_{Nmos}= 0.7 mm). The inverters are intentionally unbalanced to make the turn-off operation faster. With this size, a conventional inverter would present unacceptable cross-conduction during commutation. Therefore it is mandatory to implement a non-overlapping circuit as shown on Figure 4.b, where two different buffers drive the last inverter and their signals are generated with the required delay, as shown on Figure 4.b.

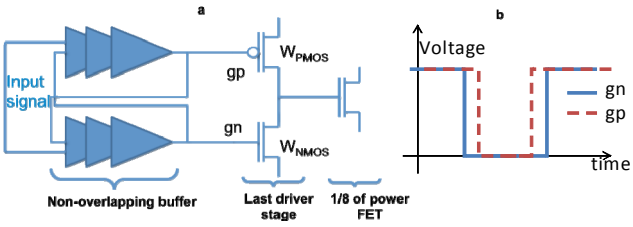

Figure 4. Non-overlapping driver (a) and inverter gate waveforms (b)

B. *Control circuit*

The analysis of the control section, leading to the choice of the architecture shown in Figure 5, has been developed in [9].

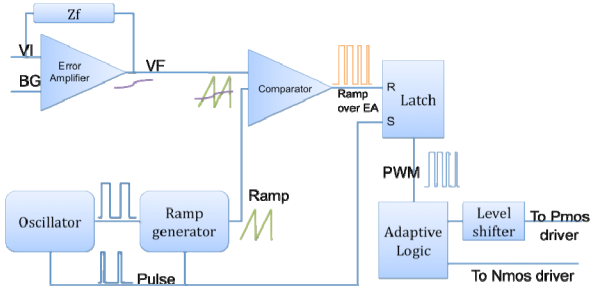

Figure 5. Control circuit building blocks

- The error amplifier (EA) has been designed with very high gain (100dB) to have high DC output voltage accuracy and a bandwidth of 20MHz for avoiding changes in the open loop transfer function (whose bandwidth f_c is $f_c < f_s$).

The error amplifier (shown in Figure 6) is a two stage OPA where the first stage is a folded cascoded OTA with symmetrical output stage. This configuration also allows having high PSRR (90dB in DC, 55dB at 2MHz)

- The oscillator generates two square waves with fixed frequency of 2MHz and duty cycle of 5% (Pulse) and 50% respectively. Both signals are used to generate the sawtooth signal. Its swing is intentionally limited between 0.7 V and 1.7 V to be smaller than the swing of VF (output of EA). "Pulse" is the reset signal for the ramp generator (it generates the falling edge of the ramp) and for the latch.

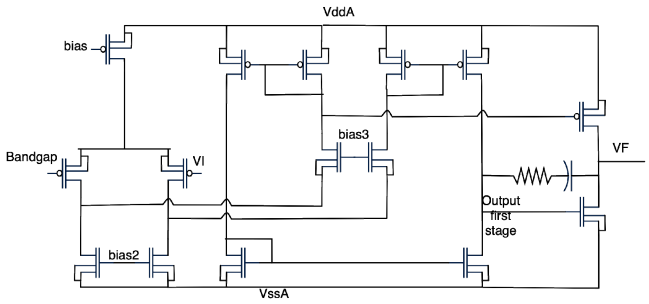

Figure 6. Error amplifier schematic

- The comparator generates the PWM modulation from the output of the EA and the sawtooth wave. The output signal can have 0 to 100% duty cycle. A SR latch has been added whose set signal is "Pulse" to avoid ringing on the output of the comparator. The latch is sensitive to Single Event Upset [11] and it has been triplicated to avoid change in the memory state.

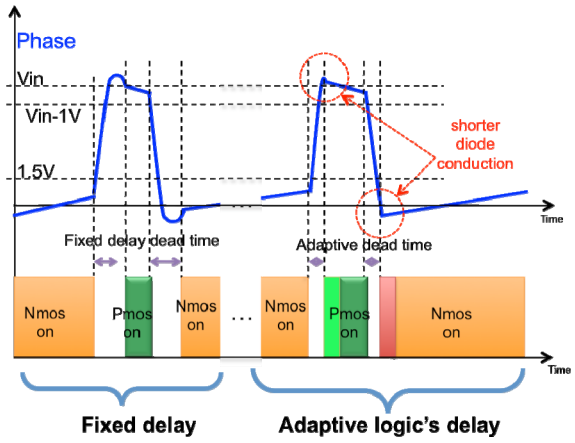

Figure 7. Adaptive and fixed dead time in QSW

C. *Adaptive Logic*

The adaptive logic block has been designed to optimize the dead time management during QSW operation. While conventional buck converter designs use a fixed dead time, our new adaptive circuit dynamically adapts the dead time duration to reduce it as much as possible for any combination of V_{in}, V_{out}, I_{out} and or inductance. In QSW mode after the turn-off of the NMOS power device, the negative inductor current charges the parasitic capacitance of the Phase node shown in Figure 1. A comparator (called high side, HS comp) senses if the Phase voltage exceeds the value (V_{in}–1) V and generates a turn-on signal for the power PMOS. Similarly, when the PMOS turns off, the inductor current discharges the Phase node capacitance. A comparator (called low side, LS comp) senses if the Phase voltage is lower than 1.5 V and produces a turn-on signal for the NMOS. Figure 7 shows the difference between the use of a fixed delay (on the left) and the adaptive logic (on the right). The PMOS and the NMOS FETs are turned on faster, leading to a shorter or almost zero diode conduction. In a multi-MHz converter, this can have a impact of 4-6% on the efficiency.

If the comparators do not sense the limit crossing, the power FETs are turned on after a fixed delay of 50ns. This can happen for instance to the high side comparator when I_L in continuous mode is always positive.

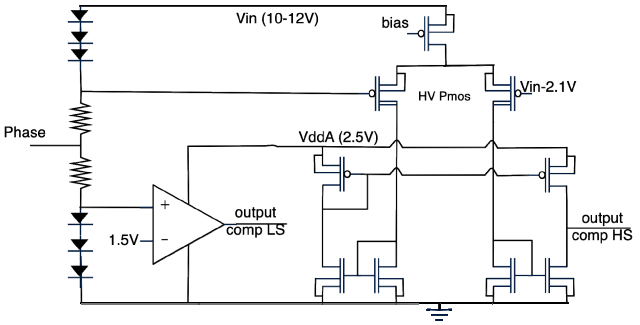

Figure 8. High side and low side comparators

The LS comp (Figure 8) is a conventional comparator, supplied at 2.5V with hysteresis. The HS comp (also in Figure 8) input signals are referred to Vin. High voltage (HV) PMOS transistors are used as differential pair and the differential signal is shifted in current to the 0↔2.5 V domain, typical of the whole control circuitry. The output of the HV and LV comparators go to the logic actually managing the delay time and providing the driving signals to the power NMOS and the level shifter that drives the power PMOS. The shifter is necessary to translate the signal from the 0↔2.5 V domain and refer it to V_{in} for driving the PMOS gate. The shifter (Figure 9) is a differential structure using HV NMOS as input elements and partially cross-coupled low-voltage PMOS transistors as load. This load refers the output voltage to V_{in} and actually latches the output value to avoid unwanted glitches in the PMOS driver signal.

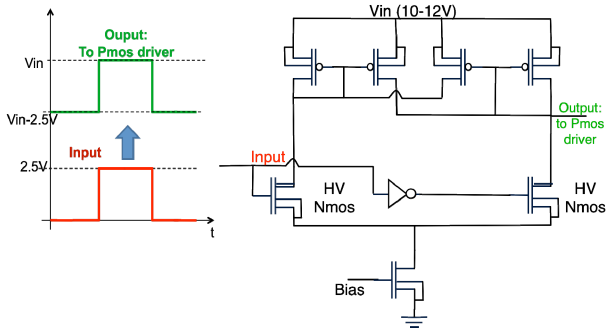

Figure 9. Level shifter schematic

D. *Circuit layout*

As reported in the introduction, all low-voltage NMOS transistors have been laid out with an enclosed shape where the drain electrode is fully surrounded by the gate (ELT, or Enclosed Layout Transistor) [10][11][12]. Additionally, all n+ diffusions and n-wells at different potential have been divided by a p+ guardring to avoid radiation-induced leakage currents across wells.

For the power transistors, given the large current flowing (up to 5 A) the layout was done to minimize the parasitic resistance of the metal lines along the on-chip current path. Multiple unit cells have been used allowing a more uniform distribution of the current, and two techniques to reduce coupling noise to/from the substrate have been adopted. Firstly the high voltage NMOS is in the native substrate, all low-voltage transistors have been isolated in separate n-wells. This is possible because the SGB25GOD technology offers true isolated NMOS transistors. Secondly large substrate

contacts and undoped substrate regions have been used to separate the control circuit from the power transistors.

The prototype ASIC, shown in Figure 10, measures 3 x 2.8 mm^2 and has been mounted for functional evaluation in QFN48 packages.

IV. Test Results

The ASIC has been successfully tested. As shown with the oscilloscope's waveforms in Figure 10 the converter is working in QSW because the inductor current goes negative. The delay between the two transistor gate signals (see Figure 10) is much smaller than the fixed 50 ns limit (22 ns for the first dead time and 24 ns for the second), demonstrating that the adaptive logic is acting properly. Looking at the Phase voltage node, it is possible to appreciate that the duration of the diode conduction is almost zero before the PMOS turn-on and 9 ns before the NMOS turn-on.

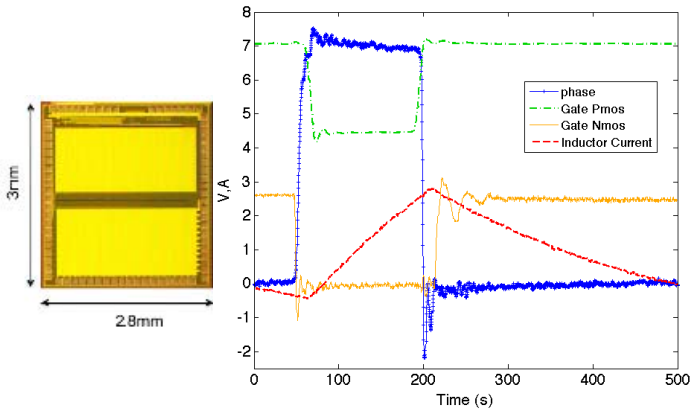

Figure 10. IHP 0.25µm ASIC picture and waveforms (with Vin=7V, Vout=2.5V, Iout=1.3A, f=2MHz and L=538nH)

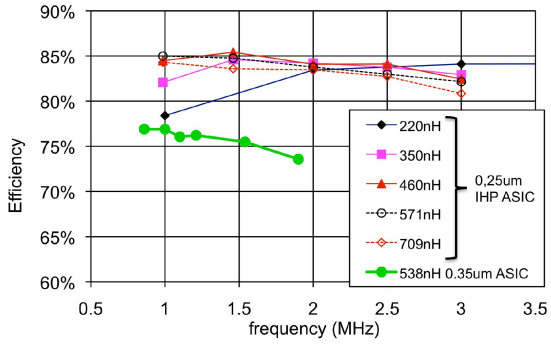

Figure 11. Efficiency vs frequency with different inductor values (with Vin=7V, Iout=2A and Vout=2.5V)

The efficiency has been measured for different frequency and inductor values as shown in Figure 11. In comparison with the measured efficiency of the previously designed 0.35µm ASIC [7] mounted in the same package, the new design has higher efficiency: the difference can be as high as 11%.

A further efficiency improvement is expected by replacing the current wire-bonding with bump bonding as foreseen for the production unit. We measured a total resistance of 68 m for the NMOS (only 10 m expected in silicon) and 109 m for the PMOS (only 30m expected in silicon). By adding these parasitic resistances to our model of losses, and using some specific measurements to properly extract the most relevant parameters for the estimation of the losses, we can predict the efficiency of the converter in any condition. This allows choosing the inductance and f_s leading to the highest efficiency for any combination of V_{in}, V_{out} and I_{out}. The comparison of the simulation with real measurements in Figure 12 indicates very close matching. The losses in the large ESR (30-60 mΩ in DC) of the air-core inductor represent a significant contribution – efficiency higher by 3-4% could be obtained using ferromagnetic inductors of the same value in the same conditions.

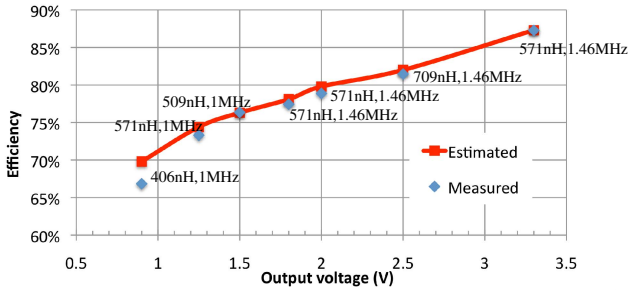

Figure 12. Optimal estimated and measured efficiency vs output voltage (with Vin=10V, Iout=1A). Inductance and frequency have been chosen for any point to achieve the highest efficiency.

V. Conclusions

A buck converter ASIC has been developed to specifically meet radiation and magnetic field tolerance to very challenging levels. Radiation tolerance was obtained by technology selection combined to dedicated layout and circuit design practices. Magnetic field tolerance forces the use of air-core inductors, in turn requiring high switching frequency for the converter. To get the highest efficiency in the target application (V_{in} = 10-12 V, V_{out} = 1.8-3.3 V, I_{out} = 1-3 A) the design has been optimized for working in the QSW mode, and a new control circuit based on adaptive dead time management has been successfully integrated. The prototype yielded a measured efficiency well matching a simulation model describing the different source of losses. Extrapolating efficiencies with the model for the same ASIC in optimized power packages and using a ferromagnetic inductance (much smaller ESR), values in excess of 90% are estimated for a conversion factor of 4 (10 V to 2.5 V) and currents of 1-2 A.

VI. References

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