

# Investigation of a contacting scheme for self-assembled cleaved edge overgrown InAs nanowires and quantum dot arrays

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A contacting scheme to measure the transport properties into self-assembled InAs Quantum Wires (QWRs) or Quantum Dots (QDs) is presented. The nanostructures are formed on the (110) cleaved edge of a AlAs/AlGaAs heterostructure substrate by means of the Cleaved Edge Overgrowth (CEO) technique and Molecular Beam Epitaxy (MBE). The InAs nanostructure grows directly on top of the AlAs layer, which hosts a two dimensional electron gas (2DEG). In a transistor-like schematic of the device, the 2DEG acts as a contact to the InAs nanostructure. A top gate is used to deplete the 2DEG, thereby defining the InAs nanostructure as a channel

between source and drain. Measurements confirm that the device can be operated as a field-effect transistor, but no evidence of a current flow through the InAs QWRs can be found. Numerical calculations of the electron density and the device band structure confirm that a depletion zone is present in the AlAs layer close to the cleaved edge and the InAs QWR seems electrically isolated from the AlAs 2DEG leads. Possible solutions could be an additional Schottky gate contact on the CEO side or selective doping inside the CEO barrier.

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**1 Introduction** The expanding of research in nanoscale systems is essentially driven by interest in the fundamental physical properties of solid state matter at the nanoscale and the hope to apply them to novel technological devices. With self-assembled (bottom-up approach) nanostructures it is possible to achieve even smaller sized structures in combination with top-down technologies and allow at the same time a high control of the size distribution. An example for such materials are defect free semiconductor QDs grown by MBE or CVD processes [1]. Especially III–V self-assembled QDs, e.g. InGaAs QDs, are subject to intense investigations due to their superior optical properties. These systems are interesting due to promising applications, like single photon sources, lasing, optical amplifiers or solar cells [2–4]. For this reason it is interesting to characterize the electronic properties of self-

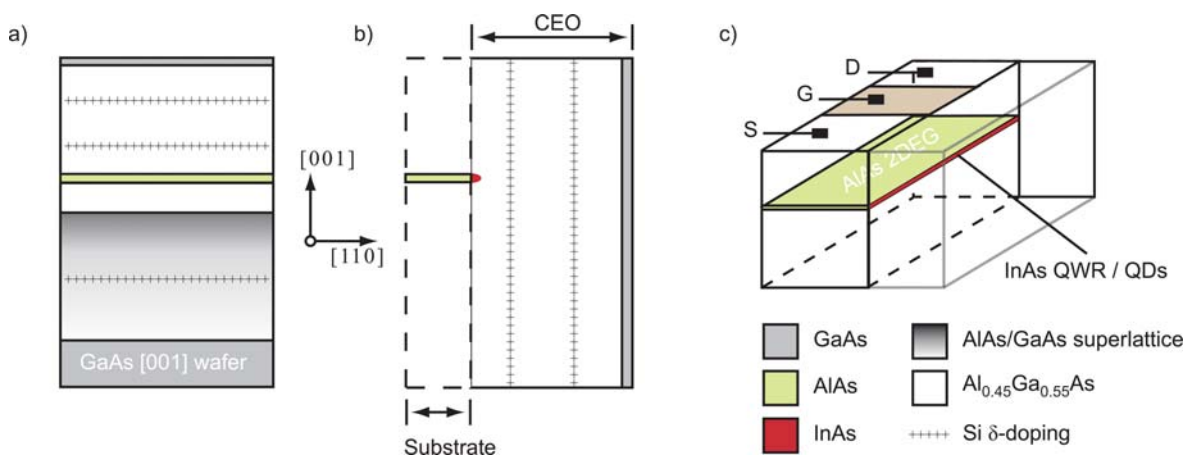
assembled nanostructures. Ensembles of QDs can be contacted by embedding the QDs film into a pin-diode structure. However to address single or a small ensemble of nanostructures still represents a challenging task. In several previous publications the promising approach of self-assembled InAs nanostructures obtained by cleaved edge overgrowth was presented [5, 6]. Again the optical properties are easily accessible [7], but for further investigations a direct injection of charge carriers into the nanostructures is interesting. Previous pioneering work has shown how CEO structures can be used for low-dimensional transport at the cleavage plane first in GaAs quantum wires [8] and more recently in AlAs quantum wires [9]. At this point we would like to shortly review the technique of self-assembled InAs nanostructure growth. The procedure relies on the fact that the three-dimensional InAs layer

growth on the  $\{110\}$  surfaces of GaAs is suppressed but can be restored by introducing an AlAs layer before the InAs deposition. In this case 3D-island growth is obtained [10]. This little trick allows the growth of InAs QDs on the  $(110)$  surface, using a prepatterned GaAs/AlAs heterostructure, where the InAs preferentially nucleates on the AlAs layer. Furthermore, the growth of InAs QDs can be tuned by the width of the AlAs layer and the nominal InAs layer thickness [6]. In addition to the growth of InAs QDs, a nucleation of quantum wires of InAs is obtained under special growth conditions before the QDs start to nucleate [6].

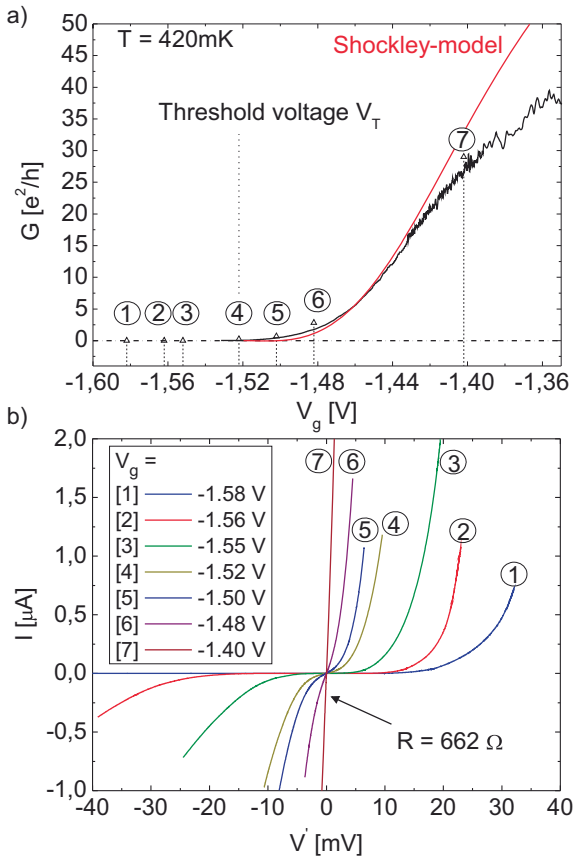
In order to prevent the nanostructures from oxidizing, a capping layer of GaAs is deposited. This procedure bears the disadvantage that the nanostructures are difficult to access by electrical means but preserves their high crystal quality and purity. In order to establish electrical contacts to the InAs nanostructure the adjacent AlAs layer is utilized as an ohmic lead. By selective doping of the original substrate with silicon impurities, electrons can be provided to the AlAs layer (Fig. 1a). As AlAs is an indirect semiconductor with the lowest conduction band minimum at the X-point, the GaAs spacer needs to be replaced by an  $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$  barrier to keep the electrons in the AlAs layer [11, 12]. Reference [6] points out that the AlAs layer thickness is usually below 50 nm, in order to obtain an aligned chain of QDs, and below 15 nm in order to obtain QWR. For this reason the electron gas in the AlAs layer exhibits quantized electronic subbands and hosts a two-dimensional electron gas. Please note that the two-dimensional property of the electron gas is not crucial for the device operation. However, throughout this publication we will be concerned with a Quantum Well (QW) thickness of 12 nm and for this reason the QW characteristics are important. The contacting of the AlAs 2DEG is done fairly easily on a macroscopic length scale by annealing indium on the wafer epitaxial (001) surface after the sample growth.

An important issue in the device is clearly the interface of the AlAs 2DEG and the InAs nanostructure. As the two nanostructures are epitaxially grown on top of one another, we expect them to be in electric contact (Fig. 1b). However, in addition to spatial degrees of freedom also the electrostatics in the device have to be considered. Indeed, in AlAs electrons are in the X-valley, while in InAs electrons are in the  $\Gamma$ -valley, meaning that electrons must also scatter in momentum space in order to transfer from one system to the other. Either disorder, alloy scattering, or quantum confinement could assist in this  $k$ -space scattering or mixing. In the next sections, transport measurements and numerical bandstructure calculations will show that the InAs nanostructure is actually electrically isolated from the AlAs-2DEG and a refinement of the device structure would be necessary to achieve full transistor function.

**2 Measurements** In Fig. 1c the contacting scheme is shown, which is organized in a Field-Effect Transistor (FET) structure. The additional metallic gate on top of the wafer surface is used to separate the 2DEG into source and drain contacts. Furthermore, the conductance in the channel of the FET can be controlled by varying the gate bias. In the ideal case, the field effect design allows to reduce contributions of 2DEG conductance to a very low level, while it is still possible to use the remaining 2DEG as ohmic contacts. In the limit of a depleted 2DEG region below the gate structure, the current path eventually lies in the InAs nanostructure. Source and drain-contacts (S, D) are used to apply a constant voltage across the sample, while the channel conductance is controlled via a gate (G). Usually, the source contact is kept grounded and the gate voltage  $V_g$  is applied with respect to the ground potential. As the contact resistance of AlAs-2DEGs is relatively high (10 k $\Omega$ ), it is preferable to use a four-point contact scheme. The four contacts are then used for two current and voltage contacts. The current contacts are used to send a current across the sample (current biased or voltage biased) and



**Figure 1** (online colour at: [www.pss-a.com](http://www.pss-a.com)) Device structure. a) Substrate layer sequence, b) cleaved edge overgrowth, c) device schematic. Source (S), drain (D) and gate (G) are indicated.



**Figure 2** (online colour at: [www.pss-a.com](http://www.pss-a.com)) a) Source–drain conductance as function of the top-gate voltage. b)  $I$ – $V$  characteristics of the device near the transistor threshold  $V_T = -1.53$  V at fixed top-gate bias.

the voltage drop ( $V'$ ) between two voltage contacts can be measured with a high impedance voltmeter.  $V'$  together with the current ( $I$ ) provide a direct measure of the sample conductance

$$G = \frac{I}{V'} \quad (1)$$

In Fig. 2a the four-point conductance near the device threshold and the current–voltage characteristics at fixed gate bias are shown. The measurements were performed in a  $^3\text{He}$  cryostat at a base temperature of 400 mK. The measurements show that the linear source–drain ( $V_{dc} = 0$ ) conductance  $G_{ac}$  can be controlled by changing the top-gate bias. At the threshold voltage  $V_T = -1.52$  V,  $G_{ac}$  approaches zero as the AIAs-2DEG channel is pinched off. The conductance trace is reproduced by a simple Shockley charge-control model under the assumption that the electron mobility follows a power-law  $\mu \propto N_s^\alpha$  [13]. Furthermore, the conductance trace does not exhibit a stepwise increase or plateaus at discrete conductance values typical for conductance quantization in one-dimensional systems [14]. To clarify this point we measured the  $I$ – $V$  characteristics near the device threshold (Fig. 2b). While the  $I$ – $V$  charac-

teristics indicate an ohmic dependence above  $V_T$  (curve 7), an activated behavior is observed near the device threshold. The activation energy  $\phi_B$  is obtained by fitting the data within the Schottky–Richardson model (data not shown)

$$\phi_B(V_g) = -0.56 \cdot V_g(V) \text{ meV} \quad (2)$$

The fact that there exists a linear relationship between  $\phi_B$  and the  $V_g$  indicates that most of the current flow occurs via the channel under the gate structure. Furthermore the absolute value of the activation energy lies in the range of the Fermi energy of the AIAs-2DEG leads ( $E_F = 0.58$  meV). The facts that  $\phi_B(V_T) = 0.85$  meV is close to  $E_F$  and the linear dependence of  $\phi_B$  in  $V_g$  fit very well into a simple barrier model, where the gate voltage  $V_g$  creates a rectangular energy barrier for electrons running from source to drain. As the electric field at the quantum well is proportional to the applied gate voltage, the barrier height is linear in  $V_g$ . At the threshold the barrier height  $\phi_B(V_T)$  is high enough to suppress any conductance at small source–drain voltages. As the channel, conductivity is proportional to the space charge in the channel the first quantum well subband has to be depopulated entirely, resulting in  $\phi_B(V_T) \approx E_F$ . As the experimental data can be explained within the simple charge control model mentioned above, we suggest that the activation of charge carriers is taking place over the AIAs-2DEG channel barrier induced by the finite bias at the top-gate. This result suggests that if a current path along the InAs nanostructure or anywhere else in the device exists, the conductance along this path is presumably much smaller than the conductance across the gate channel, even below the device threshold.

**3 Calculations** To clarify whether a conducting path between the 2DEG and the InAs nanostructure can exist and why typical conduction features are absent in the experimental data, we performed detailed calculations of the device bandstructure and the electron distribution. The simulations were carried out with the semiconductor simulation package *nextnano*<sup>3</sup> [15]. In order to analyse the electrostatics at the interface, the simulation of a homogeneous InAs QWR is sufficient. The extension to a more complex structure with several QDs in a row is readily done, but the essential qualitative results are not affected by the simplified treatment. Furthermore, the calculations will be restricted to the case of thermal equilibrium and all potential-differences between the three contacts (S, D, G) are set to zero, i.e. no current flowing between source and drain. In this case, the device is translationally invariant along the  $[1\bar{1}0]$ -axis and the simulation of a plane representing the device cross-section is sufficient. To calculate the bandstructure and the electron density, the Poisson equation and the Schrödinger equation are solved self-consistently by numerical methods using a parameter set to simulate different materials [16, 17]. A detailed description of the defined parameters can be found in Ref. [18]. Using the Hartree–Fock approximation, the quantum (mechanical)

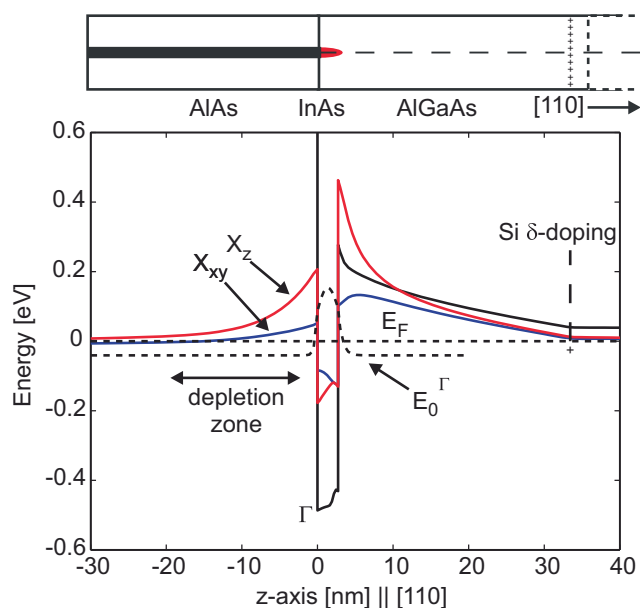
electron density is calculated from

$$n(x) = \sum_{i,s} |\Psi_i^s(x)|^2 f\left(\frac{E_F(x) - E_i^s}{k_B T}\right), \quad (3)$$

where  $\Psi_i^s(x)$  is the electron wavefunction of the eigenstate ( $E_i$ ),  $s$  denotes the band index,  $f(E)$  the Fermi–Dirac distribution.

In the following discussion, we study a particular example of an InAs QWR on a 12 nm wide AlAs layer. The height of the InAs QWRs in such samples was measured with AFM on uncapped samples and lies in the range 2–3 nm [6]. We therefore fix the InAs QWR height to 3 nm in the calculations [19]. To understand the result of the calculations, we first concentrate on the influence of strain in AlAs/GaAs/InAs heterostructures. In contrast to GaAs QWs, strain modifies the electronic bandstructure significantly in AlAs QWs [12]. Furthermore, strain is the important parameter for the growth of InAs nanostructures. For this reason full numerical minimization of the strain energy is included in the calculations, using a continuum strain model. The calculated displacement is then taken into proper account in the calculation of the electronic bandstructure by deformation potential theory. Again, the material parameters (e.g. deformation potentials) are taken from literature [17]. We plot the resulting bandstructure (Fig. 3) along the [110]-direction, essentially crossing all relevant material layers, i.e. regions with non-zero electron density. In the following we will neglect the presence of donors in the CEO barrier (Fig. 1 donors are present) and surface states. All energies in the plot are normalized to the  $E_F$ , while the  $z$ -axis has its origin at the cleavage plane. From the plot it is apparent that the  $X$ -valley splits into a doublet  $X_{xy}$  and a singlet  $X_z$  [11, 12] due to the pseudomorphically strained AlAs bulk layer. Close to the cleavage plane the strain condition changes due to the presence of the highly strained InAs and InAlAs, and the valley splitting increases. Furthermore, due to the high compressive strain in the InAs the band offset is modified, because the absolute band-gap  $E_g$  increases with hydrostatic pressure. This leads to a decrease in the binding energy for electrons in the InAs  $\Gamma$ -valley.

**3.1 Electron density distribution** The calculation yields a localized state in the InAs QWR  $\Gamma$ -valley, denoted by  $E_0^\Gamma$  in Fig. 3. As the energy of this eigenstate lies below  $E_F$ , the InAs nanostructure is occupied with electrons. However, to populate the InAs cluster the electrons have to be removed from the AlAs 2DEG, leading to a local depletion of the 2DEG close to the cleavage plane. The depletion causes an upward bending in energy of the electronic bands to a value above the Fermi level. The electron density in the depletion region is reduced by several orders of magnitude in this case but takes a finite value because the electronic wavefunction in the InAs QWR leaks through the finite potential well into the barrier. The conductivity

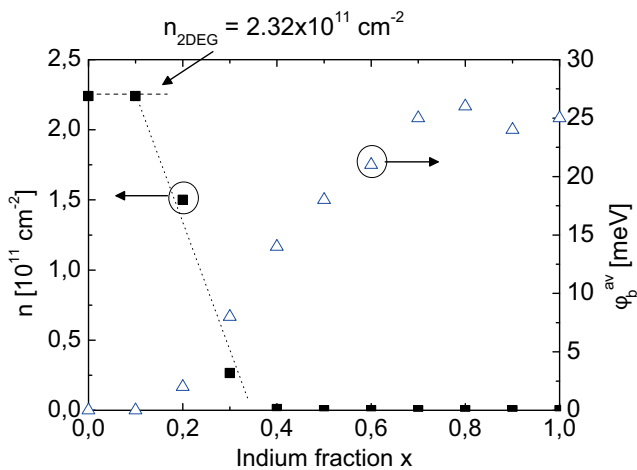


**Figure 3** (online colour at: [www.pss-a.com](http://www.pss-a.com)) (upper panel) Device structure with different material clusters. Note that the structure (Fig. 1) extends further along [110]. (lower panel) Calculated conduction bandstructure and eigenstates long the dashed line of the upper panel.

through this depletion zone will be fairly small, therefore isolating the AlAs 2DEG from the InAs QWR.

**3.2 Depletion region** At first glance it is surprising that such a depletion region can exist in our device, since the interface of AlAs 2DEGs and AlAs QWRs were fabricated by CEO, where a nearly identical device geometry was shown to be highly conductive [20]. To clarify this point we simply replace the pure InAs cluster with an  $\text{In}_x\text{Al}_{1-x}\text{As}$  alloy in the simulation. This step allows us to vary the confinement potential and therefore the binding energy in the InAs/ $\text{In}_x\text{Al}_{1-x}\text{As}$  nanostructure. To display the calculations in a convenient way, the electron density is integrated along the substrate growth direction (i.e. [001]) and depletion barrier height is averaged over the length of the depletion zone. The result (Fig. 4) of the calculations confirms that AlAs QW/AlAs QWR interfaces are highly conductive, while AlAs QW/ $\text{In}(\text{Al})\text{As}$  interfaces are insulating as discussed before. The calculations clearly confirm that the barrier, separating the AlAs 2DEG from the InAs nanostructure, increases as the indium content in the alloy increases. This trend can be explained from the larger confinement energy in the indium rich alloys, which accumulate more electrons from the 2DEG. The increase in barrier height goes hand in hand with a decrease of the electron density in the depletion zone. However, in the transition region of  $x = 0.2$ – $0.4$ , the finite barrier height and the fact that the Fermi energy lies below the conduction band edge do not exclude a finite electron density in the depletion region. This is due to the quantum mechanical nature of the electron density (Eq. (3)). The electronic wavefunctions



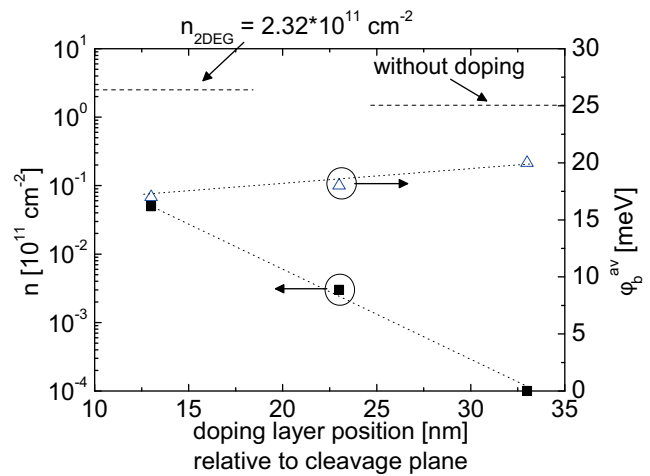


**Figure 4** (online colour at: [www.pss-a.com](http://www.pss-a.com)) Depletion barrier height between the AlAs 2DEG and the In(Al)As QWR is strongly dependent on the In content in the alloy, which accumulates more electrons from the 2DEG.

penetrate into the depletion barrier and generate a finite electron density.

**3.3 Device optimization** Several methods can be considered to remove the depletion zone. A first approach implies the fabrication of an additional side-gate on the CEO facet. In the past such devices were successfully used to study voltage-induced low-dimensional systems on cleaved edges [21]. However, the side-gate would have to be operated in forward direction, which might lead to increased leakage currents. Furthermore, a relatively large forward bias can create an accumulation layer in the AlAs 2DEG at the cleavage plane, which can be easily mistaken as conductance through the InAs nanostructure in transport experiments. Nevertheless, careful device design and optimization are likely to provide a solution for the problem discussed above.

A second approach introduces an additional Si- $\delta$ -doping layer into the CEO AlGaAs barrier (see Fig. 1b). This increases the electron density in the AlAs 2DEG and the InAs nanostructure at the cleaved edge. Several calculations were performed to visualize the influence of the additional Si-donors. Again, the doping layer is divided into two parts, a  $\delta$ -doping layer near the surface, to saturate the surface charges, and one close to the cleavage plane, to introduce electrons into the depletion zone. It is important to note that the minimal doping layer distance from the cleaved edge is limited by the silicon forward diffusion during the growth. Figure 5 shows the result of calculations, which were performed for different positions of the layer relative to the cleavage plane assuming of a pure InAs nanostructure ( $x = 1$ ). Clearly, the electron density in the depletion zone increases by several orders of magnitude when the doping layer is moved closer to the cleaved edge, while the donor density is held at saturation [11]. At the same time, the averaged depletion barrier height  $\phi_b^{av}$



**Figure 5** Introducing a  $\delta$ -doping layer on the CEO side of a pure ( $x = 1$ ) InAs QWR reduces the barrier height in the depletion zone and increases the minimal electron density in the depletion zone.

decreases slightly. From these results it becomes clear that additional doping cannot restore the fully conductive state as in the case of AlAs QWRs [20]. The critical point is not the electron density itself (or the ohmic resistance) but the fact that injected electrons must surmount a barrier, the depletion barrier height, in order to contribute to electrical conductance. This leads to a non-ohmic interface resistance between the AlAs 2DEG leads and the InAs nanostructure, which is likely to mask typical one-dimensional features like conductance quantization or Luttinger liquids.

**4 Conclusion** In summary, a contacting scheme for self-assembled InAs nanostructures was developed based on cleaved edge overgrown QWRs or QDs chain in conjunction with an adjacent 2DEG hosted in an AlAs layer. Electrical measurements at low temperature and quantum-mechanical calculations of the electron distribution reveal that the InAs nanostructure is electrically isolated from the AlAs 2DEG leads by a broad depletion zone. The latter is a result of a local redistribution of electrons in the device into the lower-lying states in the InAs nanostructure. Additional doping of the CEO barrier increases the electron density in the depletion region but does not remove the barrier completely. Further device concepts like a side gate on the CEO facet are discussed, which can allow a defined control of the electric field at the cleavage plane.

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