Solid-State Electronics 54 (2010) 935–941

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

# Asymmetrically strained all-silicon multi-gate *n*-Tunnel FETs

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ARTICLE INFO

*Article history:*
Available online 20 May 2010

The review of this paper was arranged by Prof. S. Cristoloveanu

*Keywords:*
Tunnel FET
Band-to-band tunneling
Local lateral uniaxial tensile strain
Asymmetric strain profile
Local strain engineering
Local band-gap modulation
Subthreshold swing
Scaling
Multi-gate
Si nanowires

ABSTRACT

This paper reports all-silicon asymmetrically strained Tunnel FET architectures that feature improved subthreshold swing and $I_{on}/I_{off}$ characteristics. We demonstrate that a lateral strain profile corresponding to at least 0.2 eV band-gap shrinkage at the BTB source junction could act as an optimized performance Tunnel FET enabling the cancellation of the drain threshold voltage. To implement a real device, we demonstrate using GAA Si NW with asymmetric strain profile using two local stressor technologies to have >4–5 GPa peak of lateral uniaxial tensile stress in the Si NW.



## 1. Introduction

Tunnel FET devices have been reported as interesting candidates for low standby power applications, and various device architectures were proposed [1–6]. Tunnel FETs are gated reverse-biased p–i–n junctions that are expected to have off-on transitions much more abrupt than conventional MOSFETs, whose 60 mV/decade subthreshold swing limit is set by the thermal injection of carriers from the source to the channel. Today, one of the major engineering challenges of Tunnel FETs is the boosting of their $I_{on}$ at low voltage operation, while preserving a very low $I_{off}$. In order to achieve such a high $I_{on}$, some of the previous reports suggested replacing the silicon source region with a lower band-gap material [1,4]. However, we believe that such an option could add significant complexity to the existing processing and potential non-compatibility with advanced CMOS platforms. Moreover, since Tunnel FETs could not fully replace high performance CMOS, a more realistic solution would be to fabricate Tunnel FETs on advanced silicon platforms, as a low standby power technology option with CMOS. Tunnel FETs can then fully take advantage of some of the features of advanced CMOS such as strain engineering, advanced gate stack (high-k dielectrics and metal gate), and multi-gate ultra-thin body (UTB) devices to boost their performance.

This is the main rationale for this work, in which we investigate by simulation how *all-silicon* Tunnel FET performance can be improved based on optimization of the lateral strain profile, by placing the tunneling source junction at the strain peak where the band-gap is smallest, and the drain junction where the strain is lowest and the band-gap is largest. The goal of this work is to investigate the lateral strain profile and the practical values of the strain peaks needed to significantly boost the device $I_{on}$. We find that the optimization of the lateral strain profile on thin SOI and silicon nanowire platforms can produce future low standby power Tunnel FETs with beneficial effects including a very low off-current, a significantly enhanced on-current, low average subthreshold swing $S_{avg}$, a drain threshold voltage that reduces exponentially with the linear increase of the strain level at the tunnel junction, and low $R_{on}$ at low drain voltage.

Parallel to the asymmetric strain profile, in this work we focus on the contributions of strained source and channel scaling as performance boosters. It is worth mentioning that further improvements e.g. high-k gate dielectric and oxide alignment to i-region can be employed as additive device optimization strategies, enabling future sub-1 V operation of Tunnel FETs [7].

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doi:10.1016/j.sse.2010.04.037

## 2. Asymmetrically strained Tunnel FET principle

### 2.1. Device architecture for simulation

Our Tunnel FETs are simulated with Atlas (Silvaco) version 5.13.16.C in 2D as double-gate reverse-biased p–i–n junctions with various strain profiles having the highest value at the source BTB junction, as shown in Fig. 1a. They are doped with $5 \times 10^{18}$, $10^{16}$, and $10^{20}$ atoms/cm$^3$ in the n-type drain, slightly n-type intrinsic region, and p$^+$-type source respectively, and the tunnel junction doping abruptness is 2 nm/decade. The simulated devices have a silicon thickness of 10 nm, a dielectric ($SiO_2$) thickness of 1.2 nm, and a gate length of 50 nm. The metal gates have a midgap work function. A nonlocal band-to-band tunneling model was used, along with band-gap narrowing and a quantum model. All the devices were in (100) and ⟨110⟩ crystal orientation and direction, respectively.

The key parameter of the investigated device is the asymmetrical tensile strain which has a very high level at the source side, and relaxes according to e.g. a Gaussian profile (the profiles that found experimentally after local oxidation of suspended Si NWs in [8,9]) to the drain side, as represented in Fig. 1a. The high level of tensile strain at the source side induces a local band-gap shrinkage. The lateral strain profile is incorporated in simulations by changing the band-gap along the intrinsic region of the device. The band diagram profile along the channel for a reference silicon Tunnel FET (band-gap = 1.1 eV) and lateral strain profile channel (with band-gap varying from 0.9 eV, corresponding to the highly strained part, up to 1.1 eV corresponding to the non-strained part) in on conditions is presented in Fig. 1b. A narrowing of the barrier of 13% is seen in the case with the lateral profile, which increases tunneling probability and hence $I_{on}$.

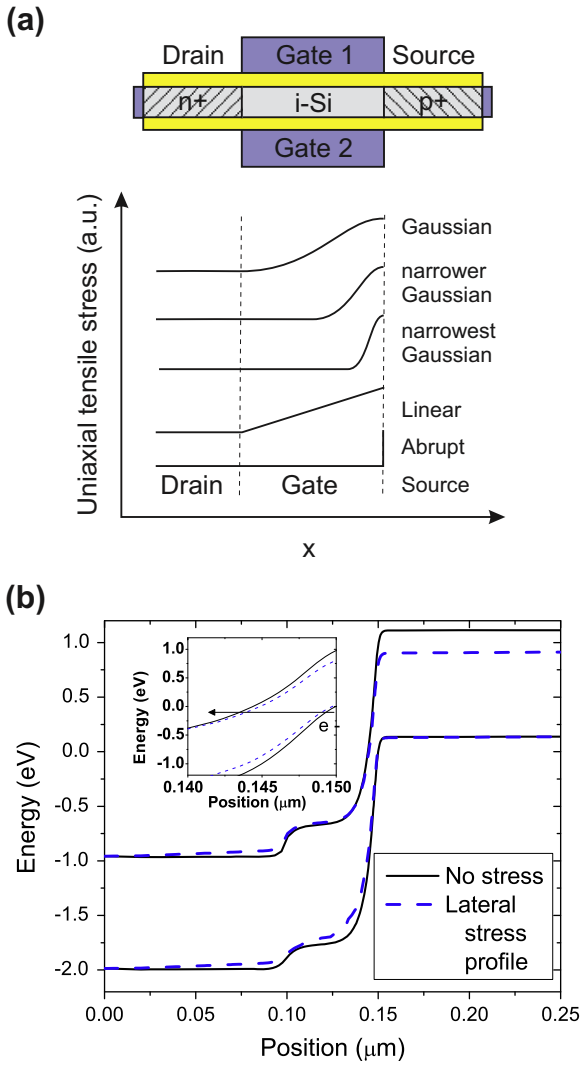


**Fig. 1.** (a) Cross section of simulated all-silicon double-gate Tunnel FET and lateral strain profiles (arbitrary units) applied on silicon films with a thickness of 10 nm, investigated in this work, (b) Band diagram profile along the channel for silicon Tunnel FET ("No stress" band-gap = 1.1 eV) and strained channel ("Lateral profile" varying from 0.9 eV to 1.1 eV) in ON conditions: $V_D = V_G = 1$ V. Inset: barrier narrowing is 13% in the case with a lateral profile.

The optimization of silicon Tunnel FETs by using a lateral strain profile results in high $I_{on}$ and preserves very low $I_{off}$, while avoiding the incorporation of low band-gap materials (SiGe or Ge), as suggested in [1–4] and avoiding a high $I_{off}$, which is observed in all SiGe or GeOI Tunnel FETs [14].

The improvement in Tunnel FETs with a lateral strain profile can be seen in Fig. 2, where we compare the $I_{DS}$–$V_{GS}$ characteristics with those of Tunnel FETs on *unstrained silicon*, and on *uniformly strained* silicon. The unstrained device has an $I_{off}$ (at $V_{DS} = 1$ V and $V_{GS} = 0$ V) several decades lower than the uniformly strained device, due to the large band-gap and therefore the wider tunneling barrier at the drain-side junction, but has comparatively low on-current. The uniformly strained device with 0.2 eV shrinkage of band-gap everywhere has an $I_{on}$ (at $V_{DS} = V_{GS} = 1$ V) ten times higher than the unstrained device, thanks to the smaller band-gap (0.9 eV here) at the source-side junction, but has high leakage. With our proposed asymmetrically strain-engineered Tunnel FET, we take the best of both: high $I_{on}$, a decade higher than that of the unstrained device, and low $I_{off}$, about three decades lower than the device with strain everywhere.

### 2.2. Band-gap narrowing and uniaxial tensile stress

As mentioned in Section 2.1, the band-gap corresponding non-strained Si is assumed to be 1.1 eV, similar to bulk Si. According to the earlier reported empirical formulas in [10,11], 0.2 eV band-gap shrinkage in Si can correspond to 3.3 or 5.5 GPa uniaxial tensile stress, respectively (see Fig. 4). Both expected stress values are below the yield strength of Si (7 GPa for bulk Si [12]) and therefore, more than 0.2 eV local shrinkage of band-gap can be achievable by local strain engineering.

It is also worth mentioning that our simulation work is done, in general, to represent the validity of the local band-gap shrinkage

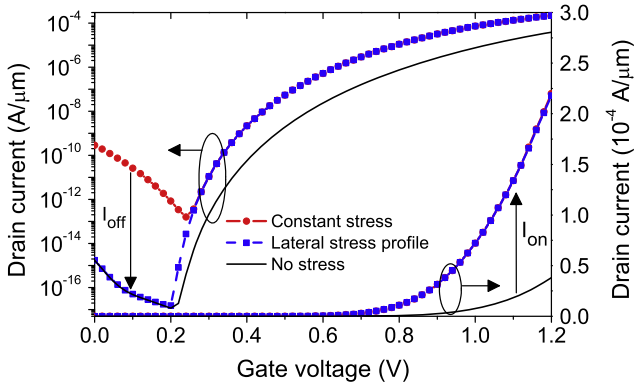


**Fig. 2.** Drain current versus gate voltage for all-silicon Tunnel FETs with $L = 50$ nm and strain profile as a parameter. $I_{off}$ is reduced for a lateral stress profile (band-gap shrinkage peak: 0.2 eV), with respect to constant stress (uniform 0.2 eV band-gap shrinkage everywhere), and on-current is improved compared to the device without stress. $V_{DS} = 1$ V.

concept as a booster and to be more accurate, the simulation can also take into account the variation of band-gap for the Si thin films in comparison to bulk Si [13].

## 3. Implementation of an asymmetrically strained multi-gate tunnel

### 3.1. Impact of lateral uniaxial stress profiles

Fig. 3 reports simulations of $I_D$–$V_G$ characteristics for the various lateral strain profiles shown in Fig. 1a; we conclude that the influence of the exact profile is not very critical for the $I_{on}/I_{off}$ improvement. However, an extension of the strain profile in the MOS channel followed by a total relaxation at the drain side to keep the $I_{off}$ low could possibly further improve the device transport characteristics.

### 3.2. Introduction to the available stressor technologies

Until now, several techniques e.g. strained substrate [15], STI induced strain [16], silicidation in the S/D [17], contact etch stop layer (CESL) [18], epitaxial thin films in the S/D [19,20] and stress memorization technique (SMT) [21] have been reported to induce stress in the channel of planar bulk and SOI devices.

Because of scalability issues regarding planar bulk and even SOI devices, multi-gate devices are being considered as the promising candidates for the 32 nm technology node and beyond. To enhance the performance of the multi-gate devices, innovative stressor technologies compatible with scaled multi-gate devices with the capability of scaling down parallel to the downscaling of the channel should be developed. For the attached multi-gate devices to the BOX layer (e.g. Fin-FET but not GAA), four stressor technologies have been reported until now: epitaxial films in the S/D [22,23], CESL [24], strained substrate [25] and metal gate strain [26].

For the suspended GAA devices, because of a three-dimensional architecture, inducing stress in the channel properly is even more challenging than the attached multi-gate devices and until now, only three techniques have been reported to include uniaxial tensile stress in a suspended channel: local oxidation together with tensile hard mask and spacer technology [8,9,27] with a peak of local tensile stress up to 2.6 GPa in the suspended Si NWs as a local stressor technology, metal gate strain [28] with tensile stress >4 GPa in suspended Si NWs as a local stressor technology and finally, suspending straight Si NWs from a strained substrate (SSDOI wafer) with uniform stress of ≈2.1 GPa along the suspended Si NW

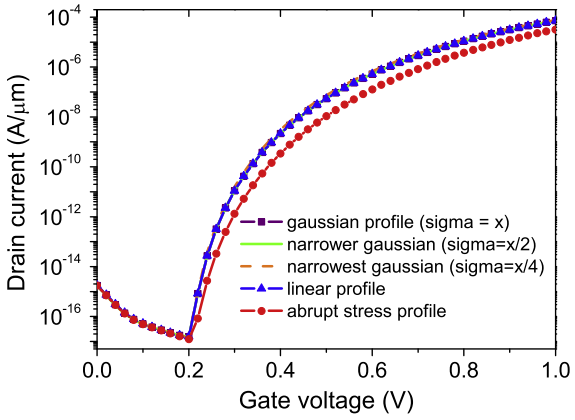


**Fig. 3.** Influence of the shape of the lateral strain profile on all-silicon Tunnel FET characteristics.

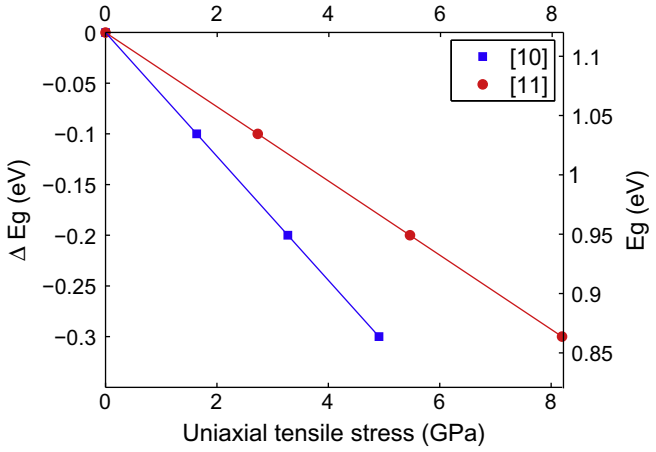


**Fig. 4.** Band-gap shrinkage of Si due to uniaxial tensile stress according to [10,11].

[29,30] as a global stressor technology. Table 1 represents the summary of these three stressor technologies.

To demonstrate a multi-gate device with a suitable stress profile for the strained Tunnel FET and due to having the best electrostatic control on the channel in a GAA architecture, in this work we focus on the GAA Si NW devices only. As also described earlier, the stressor should provide a full relaxation of stress in the drain area and therefore using a global stressor is not an optimized solution. Therefore, in this work we consider the available local stressor technologies to make a strained GAA architecture.

### 3.3. Local oxidation together with tensile hard mask as a local stressor technology

An accumulation of tensile stress after oxidation of naked suspended Si nano-beams followed by stripping the grown oxide is reported in [31]. The source of this stress was unknown and it was assumed to be associated with the injection of self-interstitial Si atoms to the oxidation front during oxidation; a model based on this proposal was also developed and presented in [31]. However, according to [32] the level of this strain was below 0.012% even the strain corresponding to 90% oxidation of 50 μm long Si beams and therefore, not a promising candidate as a local stressor technology.

In this section and as described earlier in [8,9], we present local oxidation together with tensile hard mask technology to provide a local stressor technology. Fig. 5 represents the built-in stress analysis during the process, verified by direct strain measurement on the Si NWs using a non-destructive technique with acceptable precision for nano-scale applications (micro-Raman) [33]. Because of using a non-strained substrate (bulk Si), the initial stress in the attached Si NWs to the bulk with a tensile nitride hard mask on top was almost zero. A tensile thin film tends to shrink [34] and therefore, after suspending the Si NWs from the substrate using isotropic Si etching, a temporary accumulation of tensile stress up to 4.4 GPa was found in the Si NWs because of relaxation of tensile stress in the hard mask across the suspended Si NW as well as on the S/D pads close to the anchors. Heating the wafer up to the oxidation temperature can cause relaxation of the major amount of the stress because of viscoelastic relaxation of stress in the thin films of the hard mask as well as geometrical reconfiguration of the Si NW during oxidation. Because of lattice expansion during oxidation at oxidation temperature and afterward, difference in thermal expansion coefficient of Si and $SiO_2$ during cooling down the wafer to room temperature, accumulation of growth and thermal tensile stresses in the Si NW is expected but the actual stress measurements in [8] represent saturation of tensile stress in the locally oxi-

**Table 1**
The available local and global stressor technologies to make a GAA uniaxially tensile strained Si NW architecture.

| | Architecture | Dimension (nm) | Stressor | Stress (GPa) |
|---|---|---|---|---|
| Singh, EDL 07 [28] | Bended circular GAA Si NWs | ≈5–7 nm diameter | Metal gate | >+4 |
| Hashemi, IEDM 08 [30] | Straight GAA Si NWs | Width * thickness: (49 * 9)–(8 * 7) | Strained substrate | ≈+2.1 |
| Moselund, IEDM 07 [27]; Najmzadeh, INFOS 09 [8] | Bended triangular GAA Si NWs | ≈100–500 nm wide and thick | Local oxidation together with tensile hard mask technology | +0.2 to +2.6 |

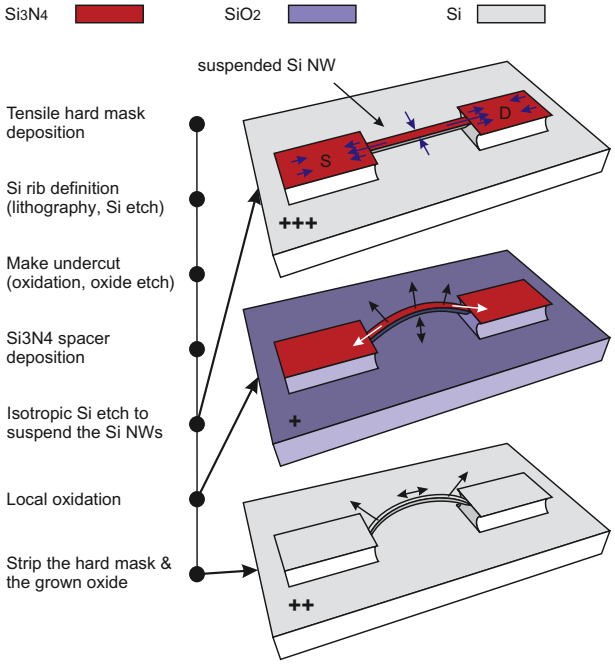


**Fig. 5.** Analysis of strain during the local oxidation process of a Si NW covered with a tensile nitride hard mask on bulk Si. The "+" signs on the wafer represent the level of tensile stress in the Si NW. The blue arrows represent relaxation of tensile stress in the tensile nitride hard mask after suspending the wire. The black arrows represent the elongation of Si NW because of forces or releasing the stored energy. The white arrows represent restriction on out-of-plane elongation because of tensile hard mask.

dized Si NW <1.0 GPa due to restrictions on in-plane elongation of the Si NW because of the doubly-clamped design and restrictions on out-of-plane buckling because of the tensile hard mask on top. The accumulated mechanical potential energy especially in the saturated area releases itself after the stripping step causing to in-plane elongation as well as out-of-plane buckling of the Si NW and at this stage, a peak of stress up to 2.6 GPa was found in the Si NWs [8].

Fig. 6 represents the actual stress profile along a 5 μm long Si NW after a poly-Si gate stack deposition step. According to the figure, the stress profile is almost uniform in the areas about 1.5–2.0 μm far from the S/D pads and the stress relaxes along the anchor parts until a complete relaxation on the pads satisfying the required strain profile for a strained Tunnel FET application.

It is worth mentioning that the process represented in [9] offers triangular Si NWs with one (100) face and two non-well defined slanted faces. The process can be adopted using a SOI platform to perform local oxidation on suspended rectangular Si NWs with a tensile hard mask on top to finally get rectangular strained Si NWs or Fins with defined e.g. (100) or (110) top and bottom faces for further optimization of the performance of the devices.

Also in this work, the almost long Si NWs fabricated from bulk Si were used to prove the concept of local oxidation as a local stressor technology (see Fig. 7). As mentioned in [9], this stressor technology can be scaled down to provide e.g. 1 μm long and 10 nm thick strained Si NWs using a SOI platform.

### *3.4. The architecture to practically implement a gate-all-around strained Tunnel FET with asymmetric uniaxial tensile strain profile*

To gain different stress profiles along the channel and even get higher stress in the channel, the available local stressor techniques can be used simultaneously. To avoid creation of voids and plastic relaxation, the final level of stress should be below the yield strength of Si (7 GPa for bulk Si [12]). According to the simulation results, the actual strain profile along the channel is not an issue and therefore, in the processes we target to place an abrupt S–G junction at the highly strained region of the Si NW together with a complete relaxation of stress in the drain area.

In general, to make a GAA suspended uniaxially tensile strained FET there are only two available local stressor technologies until now: local oxidation and metal gate strain. Fig. 8 represents a combination of these two local stressor technologies to obtain >4–5 GPa lateral uniaxial tensile stress in the Si NW. In the mentioned figure, the cross section of the channel can be triangular with two non-well defined faces, circular (using hydrogen annealing or self-limiting oxidation) or even a thin rectangular structure with defined faces to offer a Fin-FET or a rectangular GAA structure. To

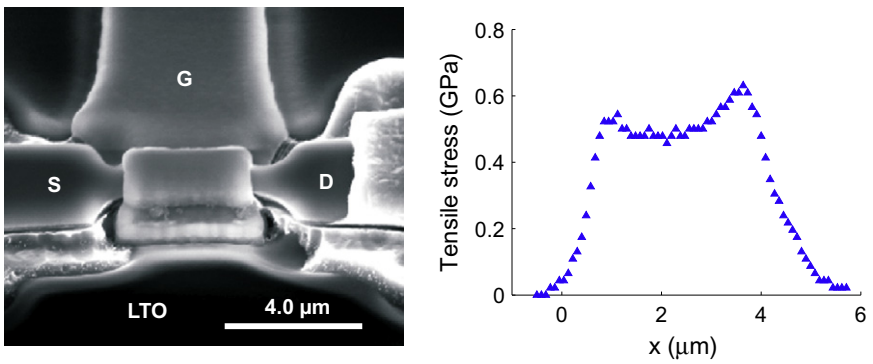


**Fig. 6.** SEM picture of a fully processed GAA Si NW FET (left). Actual local stress profile along the channel of the device, measured using micro-Raman spectroscopy (right).

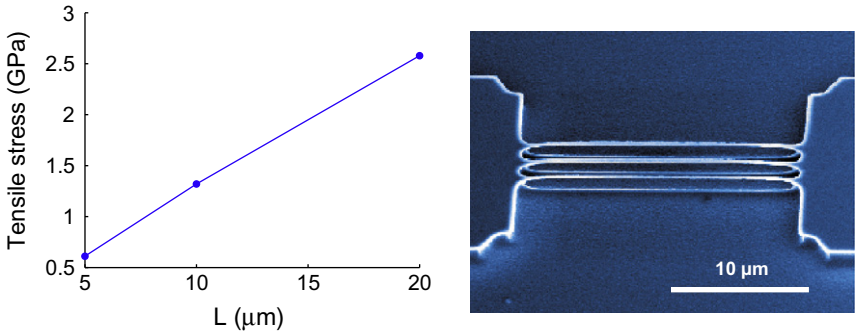


**Fig. 7.** The stress peak along three Si NWs with three different lengths after local oxidation and stripping steps (left). SEM picture of three parallel suspended strained Si NWs with a lateral uniaxial tensile stress peak of 2.6 GPa after the stripping step representing controllability and reproducibility of the local stressor technology (right).

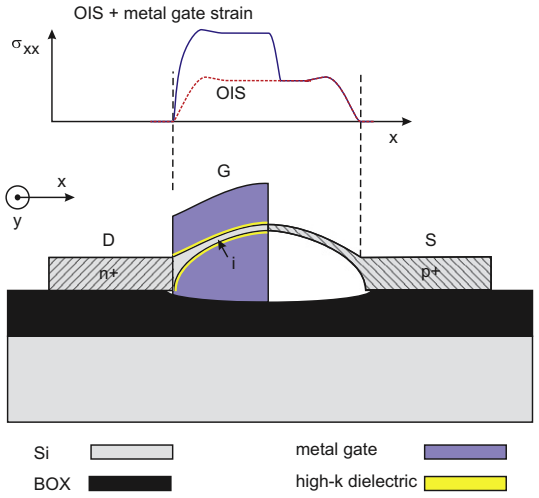


**Fig. 8.** Implementation of a strained Tunnel FET with a sub-hundred nm gate length at the stress region of a strained Si NW. The red curve represents the stress profile after local oxidation and stripping steps while the blue curve represents the stress profile after both local oxidation/stripping and metal gate deposition steps. To have the best control on the thickness of Si NW and therefore, the best control on OIS, a SOI platform was used.

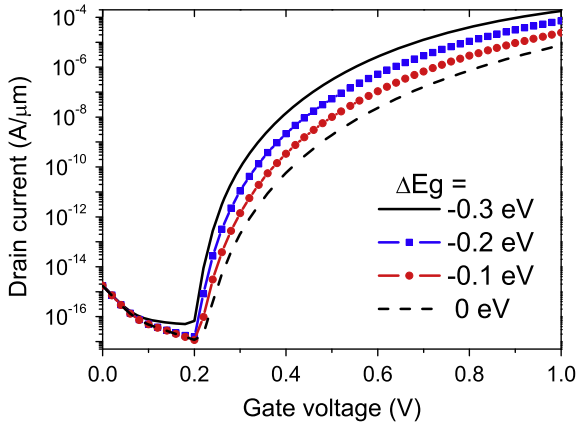


**Fig. 9.** Simulation of $I_D$–$V_G$ characteristics' improvement with decreasing band-gap at the source BTB junction ($L$ = 50 nm).

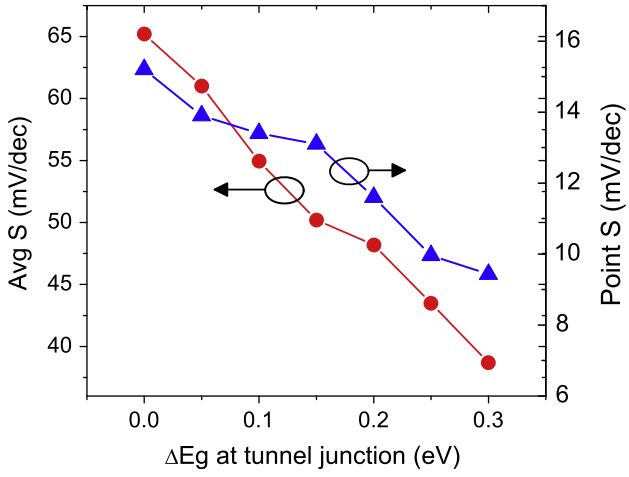


**Fig. 10.** Average and point swings versus band-gap reduction at source side in DG Tunnel FET with $L_G$ = 50 nm.

obtain a higher current density, dense array of Si NWs similar to [29] can be considered.

## 4. Simulation study of Tunnel FET performance enhancement by a lateral strain profile

### 4.1. Average subthreshold swing improvement

Fig. 9 shows the transfer characteristics for Tunnel FETs with different amounts of maximum tensile strain at the tunnel junction and a lateral Gaussian profile. A remarkable improvement is found in the average subthreshold swing ($S_{avg}$), taken over more than seven decades from the turn-on point up to a current of $10^{-7}$ A/μm, Fig. 10. $S_{avg}$ ranges from 65 mV/dec. for the optimized Tunnel FET without strain, down to 36 mV/dec. for the device whose band-gap shrinks to 0.8 eV at the tunnel junction.

### 4.2. Threshold voltage reduction

The output characteristics presented in Fig. 11 show further important improvements in asymmetrically strained Tunnel FET behavior. First, $I_{on}$ at $V_{DS} = V_{GS} = 1$ V is increased from 8 μA/μm in devices without strain to 72 μA/μm when a tensile strain of 4 GPa is applied on the source side. Second, Tunnel FETs, unlike conventional MOSFETs, have a drain threshold voltage as presented in [6]. The drain threshold voltage, $V_{TD}$, gives an unwanted high $R_{on}$ resistance at low $V_{DS}$ that is detrimental to the design and operation of Tunnel FETs as fast logic devices; this could also affect the obtainable $I_{on}$ level with a given supply voltage. If one decreases the band-gap at the source tunneling junction by increasing the level of strain there (or by any technique that reduces

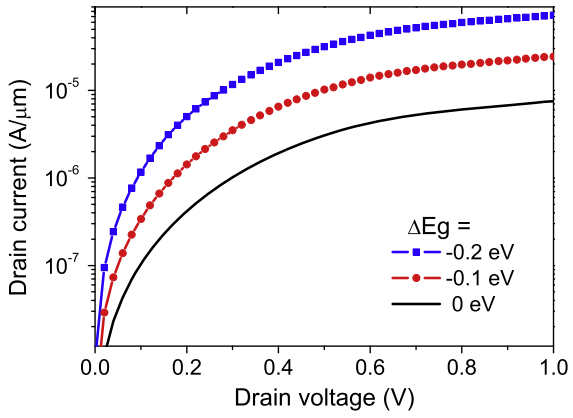


**Fig. 11.** Drain current versus drain voltage for Tunnel FETs with different max. band-gap shrinkage at the tunnel junction due to strain, for $V_{GS}$ = 1 V.

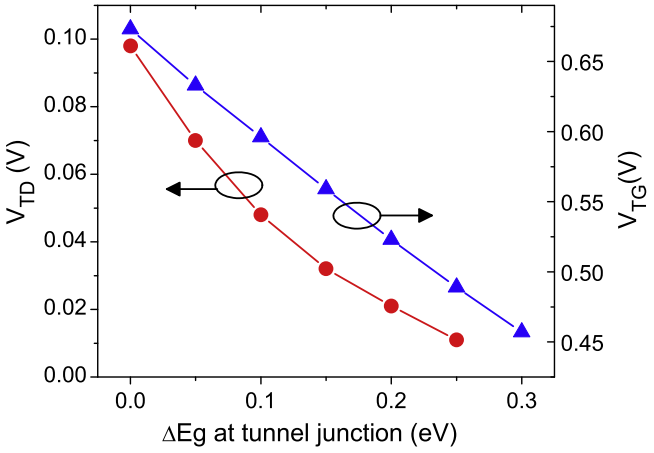


**Fig. 12.** Drain and gate threshold voltages', $V_{TD}$ and $V_{TG}$, dependence on ΔEg at the tunnel junction; while a quasi-linear decrease is observed for $V_{TG}$, the $V_{TD}$ decrease is much faster (quasi-exponentially). Both $V_{TD}$ and $V_{TG}$ are extracted at $I_D = 10^{-7}$ A/μm.

band-gap at that junction), the drain threshold voltage decreases quasi-exponentially (Fig. 12), and both $R_{on}$ (especially at low $V_{DS}$) and $I_{on}$ are significantly improved. Finally, we note that for our investigated device, the gate threshold voltage decreases almost linearly with increasing strain at the source side (from 0.67 V for no strain, to 0.49 V for ΔEg = 0.25 eV), without affecting $I_{off}$, kept low by the non-strained drain junction.

### 4.3. Gate length scaling and drain current enhancement

In Fig. 13 we present the relative improvement (%) of the drain current in all regions of operation, as induced by 4 GPa of stress as a technology booster applied on the source junction. The Tunnel FET intrinsic channel length is varied from 2 μm down to 50 nm. Typical $I_{on}$ improvements at maximum applied drain and gate voltage (=1 V) range from ≈400% (in long channels) to ≈800% (in short channels) for ΔEg = 0.2 eV. A significantly higher improvement is observed in channels where the intrinsic gate region is shorter than 100 nm; here the highest current increase (>1000%) is observed near the transistor turn-on point. In these short channel transistors, the strained tunnel junction influence extends over the subthreshold region of operation of the transistor, where the current of the reference transistor is very low.

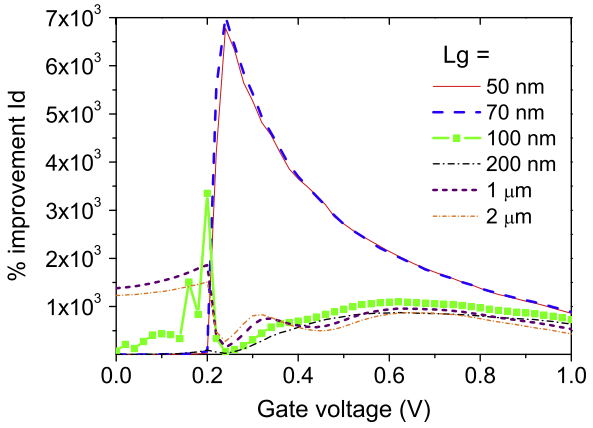


**Fig. 13.** Percent improvement in drain current between a Tunnel FET without stress (reference), and devices with a tensile stress (ΔEg = 0.2 eV) at the tunnel junction, for various intrinsic region lengths.

## 5. Conclusion

In this work we demonstrated that a lateral strain profile corresponding to at least 0.2 eV band-gap shrinkage at the tunnel junction of all-silicon Tunnel FETs acts as a key performance booster. Based on existing technology reports on strained silicon nanowires, we have proposed a possible implementation of a Tunnel FET using GAA Si NW with asymmetric strain profile using two local stressor technologies with a peak of >4–5 GPa lateral uniaxial tensile stress in the Si NW.

## Acknowledgments

This work is partially funded by the Nanosil European Network of Excellence (FP7). Thanks to Peter Dobrosz and Sarah Olsen, Newcastle University, for direct strain characterization on the fabricated samples using micro-Raman spectroscopy.

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