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# Memristive Devices Fabricated with Silicon Nanowire Schottky Barrier Transistors

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***Abstract*—This paper reports on the memory and memristive effects of *Schottky barrier field effect transistors (SBFET)* with *gate-all-around (GAA)* configuration and *Si nanowire (SiNW)* channel. Similar behavior has also been investigated for *SBFETs* with *poly-Si nanowire (poly-SiNW)* channel in back-gate configuration. The memristive devices presented here have the potential of a very high integration density, and they are suitable for hybrid CMOS co-fabrication with a CMOS-compatible process. We show that 2 different regimes are possible, making these devices suitable either for volatile ambipolar memory or *resistive random access memory (RRAM)* applications. In addition, frequency- and amplitude- dependence of the memristive behavior are reported.**

***Index Terms*—memristor, nanowire, Schottky barrier, ambipolar, transistor**

## I. Introduction

THE recent realization of Stanley Williams' memristor [1] gave new push on solid state research for memory applications. The huge availability of different physical phenomena with memristive behaviors has lead to a spread of observations in different domains of research, from flickering light bulbs to polymer based devices, neuronsynapses interaction or solid-state ionics. Nowadays it is generally admitted that memristive system can be used for modeling any kind of phenomena for which memory and signal processing coexist [2].

The basic memristor operation consists in the modulation of its conductance between two states, such as in a *resistive random access memory (RRAM)*. Several solid state phenomena could be implicated in the memristive behavior of the memristor-based RRAMs. Two-terminal solid-state memristive devices have been recently found in spintronic devices [3], metal/organic-molecule/metal [4], metal/insulator/metal configurations [5]. In these solid-state memristors coupled drift-diffusion equations for electrons and ions can be employed to simulate the memristive dynamics assuming mobile dopants and charge trapping sites [6]. These phenomena are mainly based on the application of an external bias across the device which results in a drift of charged dopant in the device channel [5]. However, memristors based on either organic materials [4], [7] or $TiO_2$ [1] cannot be easily integrated with silicon technology for VLSI applications. Therefore, new fabrication processes are required to investigate memristor as a novel element for realization of integrated circuits.

In this paper we report and propose a three-terminal memristive device based on the *gate-all-around (GAA) Schottky barrier field effect transistor (SBFET)* concept with *Si nanowire (SiNW)* channels on bulk-Si wafers. The fabrication is CMOS compatible, making this technology suitable for CMOS integration. The obtained electrical characteristics can be attributed to the coexistence of different physical phenomena, such as device ambipolarity (both holes and electrons are responsible for conduction), Schottky barrier modulation induced by interface trap charging and charge trapping at the gate oxide interface. We confirm some of these statements with previously reported *poly-crystalline Si nanowires (poly-SiNWs)*, which show a similar memristive behavior.

This paper is organized as follows. Section II introduces two device architectures for hybrid ambipolar memory and memristive operation. In section III the employed fabrication processes are surveyed. Section IV reports on the obtained electrical measurements of the different device configurations. Finally, in section V we draw the conclusions.

## II. Overview on fabricated devices

Two basic device architectures have been investigated. The first device (device A, see Fig.1) consists of a SiNW channel with GAA configuration and silicided source/drain. The fabrication flow of device A has been reported in a previous work [8] and is surveyed in Section III. The second device (device B, Fig. 1) has a poly-SiNW channel and uses the substrate as a gate to control the device behavior. Fabrication of device B has been previously reported [9]. Both devices have NiSi source/drain extensions so that the silicide to body Schottky junction is the same for both devices. The use of a NiSi/poly-Si or NiSi/Si with undoped or lightly doped channel gives rise to a mid-gap Schottky barrier responsible for ambipolar conductance (see Fig. 2). The ambipolar nature of the mid-gap SBFETs can be qualitatively understood by the equal probability of either electron or hole injection, which is related to the mid-gap Schottky barriers. Both devices confirm the existence of an ambipolar conduction with a hysteretic behavior due to either charge trapping or modulation of the Schottky barrier through current flow. The following section surveys the fabrication details for both devices.

## III. Device fabrication

This section summarizes the main fabrication steps for the devices considered in this work. More details about the process flow can be found in [8] and [9]. Both techniques yield nanowires with a sub-photolithographic thickness.

### A. Gate-All-Around Nanowire FETs

Bulk-Si wafers with low boron concentration ($N_A \sim 10^{15}$ atoms/$cm^3$) have been used as a substrate for the fabricated devices. Vertical stacks of Si nanowires are defined on the substrate by optical lithography (see Fig. 3.a) without any constraint on the resolution limit (1 $\mu$m). The photoresist is then used as a mask for a *deep reactive ion etching (DRIE)* (Fig. 3.b). The optimized DRIE

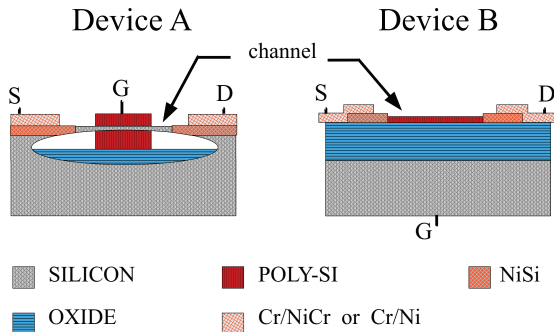


Figure 1. Device concepts. Device A: GAA SBFET with NiSi/Si contacts. A local-SOI technique is used to isolate the gate with the substrate. Device B: poly-Si NW SBFET with NiSi/poly-Si contacts.

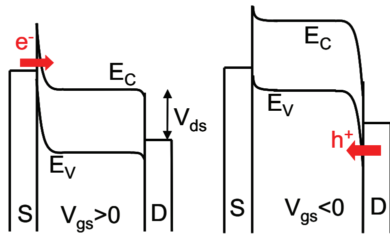


Figure 2. Band diagram explaining ambipolarity: high positive (negative) $V_{\rm gs}$ makes Schottky barrier thinner for electrons (holes).

technique, which alternates plasma etching with passivation steps, defines scalloped trenches attached to Si pillars with high reproducibility. The enhanced scalloping effect produces vertical modulation of the trench width. A sacrificial oxidation is then carried out with the double purpose of eliminating the Si where the trench is thin, and also to reduce the surface roughness induced by the etching (Fig. 3.c). A combination of *chemical mechanical polishing (CMP)* and buffered HF dip leaves vertically stacked nanowires suspended on a thick layer of insulating oxide (Fig. 3.d). The gate oxide is grown in a horizontal furnace with a dry atmosphere (Fig. 3.e). The gate poly-silicon is conformally deposited and doped with phosphorous by means of a diffusion process and then patterned with a combination of isotropic and anisotropic plasma etching steps (Fig. 3.f). The fabrication of SBFETs requires the use of metallic source and drain contacts, meaning source-to-body and drain-to-body Schottky junctions. We pattern a Cr/Ni bilayers (10 nm / 50 nm) on top of the Si pillars, partially covering the SiNW at the anchor points (see Fig. 4). This leads to the silicidation of the nanowire channel from the Cr/Ni bilayer toward the gated region of the nanowire.

### B. Poly-Silicon Nanowire FETs

The spacer technique is a promising approach to define sub-photolithographic dimensions by using standard photo-lithography and CMOS steps [9]. The process flow is illustrated in Fig. 5. We start by defining a $SiO_2$ sacrificial layer on a Si substrate. We then deposit a thin conformal layer of poly-Si (Fig. 5.a). Next, we etch this layer with a *reactive ion etching (RIE)* technique, in order to remove the lateral layer and keep the sidewalls as a spacer; and we densify the poly-Si spacer (Fig. 5.b). Then we define a second *low temperature oxide (LTO)* spacer next to the poly-Si in a similar way in order to

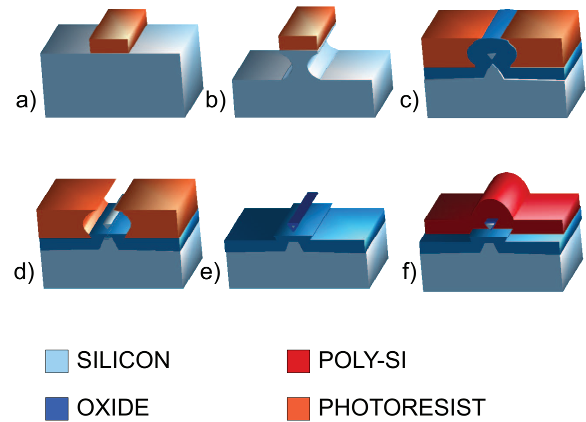


Figure 3. GAA SiNW SBFET process flow. a) A photoresist line determines the nanowire position. b) DRIE etching forms a scalloped trench. c) After wet oxidation, the Si trench reduces to a suspended nanowire. The caves are filled with photoresist and planarized with CMP. d) Buffered HF oxide etch releases the SiNWs. e) Gate oxidation. f) Poly-silicon is deposited and patterned to form the gate.

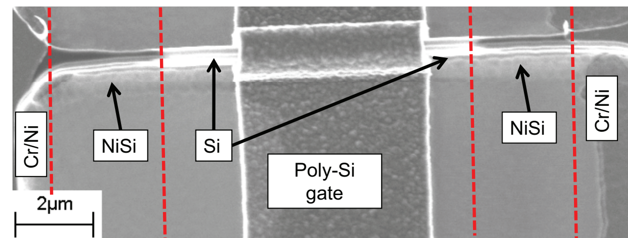


Figure 4. GAA SiNW SBFET with Cr/Ni source/drain after the lift-off process. The change in contrast on the NW channel is attribute to a difference between Si and silicided regions.

isolate the first poly-Si spacer, then we densify it (Fig. 5.c). The spacers are reminiscent of nanowires with thicknesses ranging between 20 and 60 nm. The contact regions of the undoped poly-Si nanowire are defined by the electron-beam evaporation of 10 nm Cr and 50 nm nichrome ($Ni_{0.8}Cr_{0.2}$) and lift-off (Fig. 5.d). The chromium enhances the adhesion and thermal stability of Ni to oxidation during the following 2-step annealing process. The substrate is used as a back-gate with a thick dry oxide as insulator (up to 400 nm thick). A SEM image of the obtained structure with an additional top gate defined on the poly-SiNW is shown in Fig. 6.

## IV. Results

### A. Two-Terminal Memristive Behavior

First, two terminal measurements are performed. The drain-source current $I_{\rm ds}$ is measured vs. the drain-source voltage $V_{\rm ds}$ at constant $V_{\rm gs} = 5\ V$. The device is equivalent to two back-to-back Schottky diodes. The two diodes operate in opposite regimes: for negative $V_{\rm ds}$ , the source-to-channel diode is reversely biased while the drain-to-channel diode is forward biased. For positive $V_{\rm ds}$ both diodes invert their respective bias conditions. In either case, $I_{\rm ds}$ is limited by the current flowing in the reverse-biased diode. The reverse current of a metal-insulator-semiconductor diode has been observed to be very sensitive to charge trapping at the metal/semiconductor interface [10]. The large current value in the range of mA is

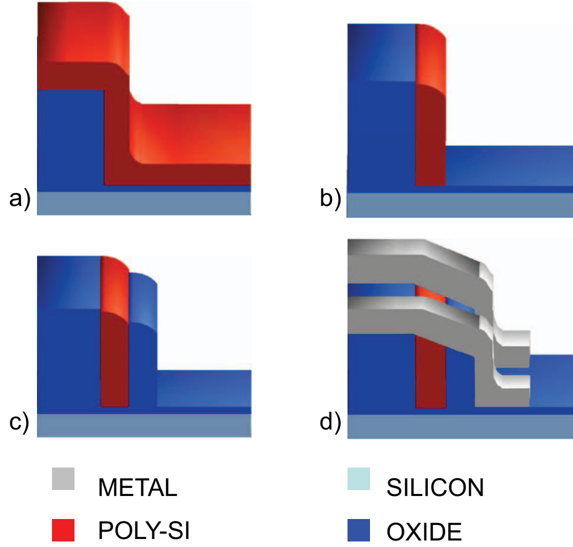


Figure 5. Main steps of the poly-SiNW with the spacer patterning technique. a) Conformal deposition of poly-Si. b) RIE etch. c) Definition of a $SiO_2$ spacer. d) Metalization of the structure

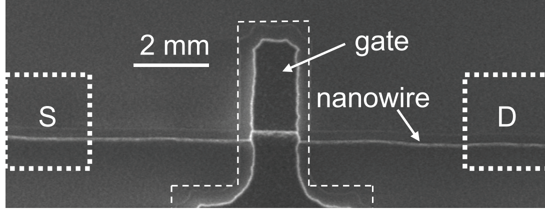


Figure 6. SEM image of a poly-SiNW with a top gate and $Cr/Ni_{0.8}Cr_{0.2}$ drain and source.

most likely due to the large parallel parasitic structure in the bulk.

The result depicted in Fig. 7 shows a hysteretic behavior that is reminiscent of a two-terminal monolithic memristive device [11]. The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward $V_{ds}$ sweep is not identical to the same curve for backwards $V_{ds}$ sweep. It can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [12]. In an ideal Schottky diode, the current is given by:

$$I = I_S \cdot e^{-\phi_B/kT}(e^{V/kT} - 1) \qquad (1)$$

with $I$ and $V$ the diode current and voltage respectively, $\phi_B$ the Schottky barrier, $k$ the Boltzmann constant and $T$ the absolute temperature. From the measured hysteretic behavior, it seems that the diode curve is modified as follows:

$$I = I_S \cdot e^{-\phi_B/kT}(e^{(V-V_0(V))/kT} - 1) \qquad (2)$$

with $V_0$ a built-in voltage at the Schottky contact that is positive for a positive $V$ sweep and negative for a negative $V$ sweep.

### B. Hysteretic Charge Trapping

We measure $I_{ds}$ for constant $V_{ds} = 1$ V while sweeping $V_{gs}$ back and forth between −5 V and +5 V (see Fig. 8). The devices are not annealed, and the source is connected to the substrate.

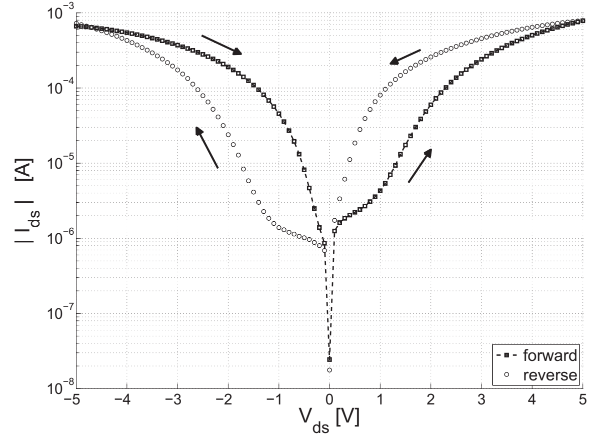


Figure 7. $I_{ds} - V_{ds}$ characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 SiNW in parallel. The forward sweep curve has a symmetrical correspondence with the reverse sweep curve, showing the respective Schottky barrier modulation. A current ratio of about 50 is found at either $V_{ds} = \pm 1V$ . This behavior is typical of two-terminal memristive devices for RRAM applications.

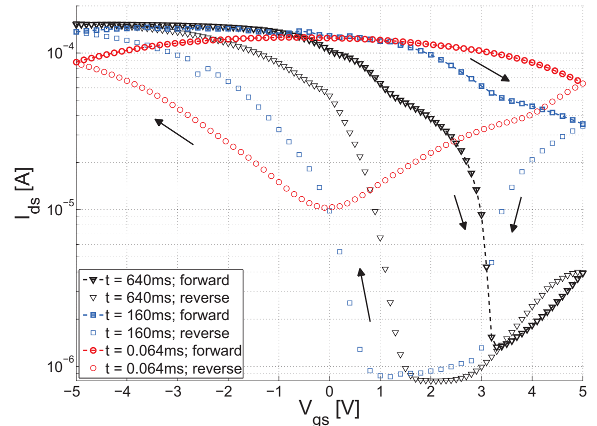


Figure 8. $I_{ds} - V_{gs}$ characteristics for a device with 10 SiNW channels and Cr/Ni contacts. $V_{ds}$ is kept at 1V. According to a certain integration time, the effect of trapping/detrapping of charges can be modulated, with effects on the hysteresis window and on the current levels. a) Integration time = 640us; b) Integration time = 160ms; c) Integration time = 640ms.

This measurement is repeated for different integration times; which is a parameter of the measurement set-up that can be set by the operator; and it represents the time over which the measurement is repeated and averaged.

The $I_{ds} - V_{gs}$ curves show an ambipolar behavior, meaning a large current conductance under either high and low gate bias. This is mainly due to the utilization of a mid-gap silicide (NiSi), *i.e.*, a silicide whose work function falls within the silicon bandgap, and to the utilization of a lightly doped silicon. On the other hand, the $I_{ds} - V_{gs}$ curves have a hysteretic behavior that suggests the hypothesis of charge trapping at the semiconductor/oxide interface of the MOS capacitor, as well as the existence of interface states at the metal/semiconductor junction

Both ambipolarity and hysteresis depend on the integration

time. When $V_{gs}$ reaches $+5\ V$ in forward mode, the electrons experience a maximum probability of trapping in the gate oxide, which is enhanced when the integration time is longer. Due to the electron trapping at the gate oxide, the channel operates in accumulation mode, with a lower conductance state for positive $V_{gs}$, than in the inversion mode for negative $V_{gs}$. Sweeping $V_{gs}$ back to negative values, reduces the amount of electrons trapped and the device operates in inversion mode, which restores the higher conductance state.

The threshold at which this high conductance state is reached depends on the integration time. The hysteresis window is larger when the integration time is shorter, because the charges have less time to be trapped and detrapped. In the case of a very short integration time the charges cannot be completely trapped and the lower conductance state is not reached (see blue curve in Fig. 8).

### C. Poly-Crystalline SiNWs

Similar results to those measured in this work on crystalline silicon nanowires have been reported in the past on poly-SiNWs [9] and they confirm through simulations and measurements the major role played by trapped charges in the observed behavior. The device structure is depicted in Fig. 1.

Fig. 9 represents the characterization of single poly-SiNWs (width $W_{NW} \sim 67$ nm) with $Cr/Ni_{0.8}Cr_{0.2}$ drain and source contacts and the substrate used as a 20-$\mu$m long back gate with a thick $SiO_2$ gate oxide (0.4 $\mu$m). The $I_{ds}$-$V_{gs}$ curve shows an ambipolar behavior, with a more dominant hole conduction under high negative gate voltage. The $I_{ds}$-$V_{gs}$ curve in Fig. 9 shows a hysteresis which became larger by enlarging the $V_{gs}$ sweep range from [-10V,10V] to [-40V,40V].

Device-level Silvaco simulation [9] have qualitatively confirmed that charge trapping and detrapping explain the hysteresis in Fig. 9. From (1) to (2), trapped holes at the $SiO_2$/poly-Si interface create positive fixed charges, and are detrapped with increasing $V_{gs}$. From (2) to (3), an electron channel is created. With the increasing electron density, more electrons are trapped at the $SiO_2$/poly-Si interface, leading to a negative interface charge density. From (3) to (4), electrons are detrapped with the vanishing electron channel. Detrapping is a slower process than trapping, explaining the hysteresis (2)-(3)-(4). From (4) to (1), a hole channel is created and increases the trapping probability for holes. This is a faster process than detrapping holes; explaining again the hysteresis (4)-(1)-(2). This behavior that was measured and simulated with poly-SiNWs can also explain the behavior of the SiNWs reported in Section IV.B .

## V. Conclusions

In this work we reported two different nanowire-based transistors for which memristive behavior and memory functionality was observed. Depending on which one of the terminals is used as the input for voltage signal, either ambipolar memory or memristive behavior can be obtained. In addition to the classical two-terminal memristive behavior we showed that either signal frequency or amplitude are important for ambipolar memory operation. Future work will focus on extensive electrical characterizations of the hysteresis dependence. We believe that the added functionality of these three-terminal memristive devices will add more flexibility for design optimization.

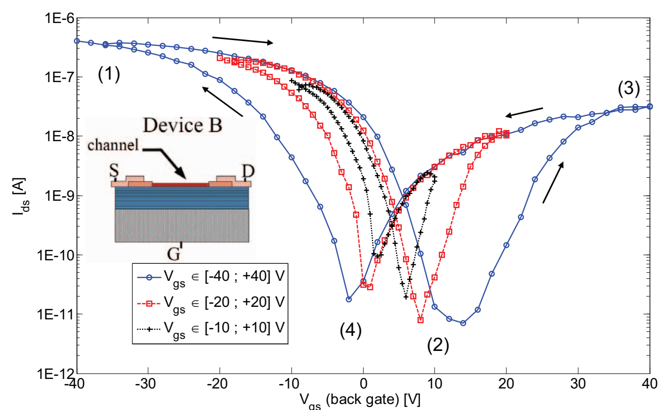


Figure 9. $I_{ds} - V_{gs}$ characteristic for a PolySiNW device with poly-Si channel and Cr/Ni contacts showing hysteresis dependence with amplitude sweeping.

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