Nucleation mechanism of gallium-assisted molecular beam epitaxy growth of gallium arsenide nanowires

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Molecular beam epitaxy Ga-assisted synthesis of GaAs nanowires is demonstrated. The nucleation and growth are seen to be related to the presence of a SiO_2 layer previously deposited on the GaAs wafer. The interaction of the reactive gallium with the SiO_2 pinholes induces the formation of nanocraters, found to be the key for the nucleation of the nanowires. With SiO_2 thicknesses up to 30 nm, nanocraters reach the underlying substrate, resulting into a preferential growth orientation of the nanowires. Possibly related to the formation of nanocraters, we observe an incubation period of 258 s before the nanowires growth is initiated. © 2008 American Institute of Physics. [DOI: 10.1063/1.2837191]

Semiconductor nanowires are believed to play a decisive role in the electronic and optoelectronic devices of the 21st century. Up to now, the synthesis of nanowires is mainly based on the vapor-liquid-solid and vapor-solid-solid mechanisms.[1,2] Common in both mechanisms is that a metal nanoparticle gathers and decomposes catalytically the precursor molecules. Supersaturation of the metal droplet follows and leads to the precipitation of a solid phase underneath the droplet in the form of a nanowire. Typically, gold is used as a catalyst. The use of such an extrinsic catalytic metal is in general not desired and some effort has been directed into finding alternatives.[3,4] Recently, catalyst-free growth has been achieved both with metal-organic chemical vapor deposition and molecular beam epitaxy (MBE).[5,6] This type of growth has always been linked to the existence of a plain or patterned SiO_2 surface, whose role has still to be clarified. To our knowledge, a detailed study on the nucleation stage of the nanowires and an analysis of the role of the SiO_2 are still missing.

Nanowires were grown in a Gen-II MBE system. 2 in. GaAs wafers were sputtered with silicon dioxide; the thickness was varied between 20 and 100 nm. In order to ensure a contamination-free surface, the substrates were dipped for 2 s in a 12% HF aqueous solution, nitrogen blow dried, and were immediately after transferred in the load lock of the growth chamber. In order to desorb any remnant adsorbed molecules at the surface, the wafers were heated to 650 °C for 30 min prior to growth. The synthesis was carried out at a temperature of 630 °C, an arsenic As_4 partial pressure of 8×10^{-7} mbar, a Ga rate of 0.25 Å/s and under rotation of 4 rpm.

We first discuss nanowires which were grown simultaneously on two different halves of GaAs substrates with the (001) and (111)B orientations. After cleaning of the surface and HF dip, the two halves were still coated with a 6 nm

SiO_2 thin film. Cross-sectional scanning electron microscopy (SEM) measurements of the grown nanowires are shown in Fig. 1. The micrographs clearly reveal that the nanowires mainly grow perpendicular to the substrate in the case of the (111)B GaAs, and with an angle of $\sim 35°$ in the case of the (001) GaAs. This result clearly proves the existence of a relation between the nanowire orientation and the crystalline structure of the substrate underneath the thin SiO_2 layer. This result certainly leads to the question about how the substrate orientation influences the nanowire orientation through the passivation SiO_2 layer and about what is the thickness limit for it.

We fabricated a series of samples with varying SiO_2 thickness. GaAs nanowires were grown simultaneously on four fourths of the (001) GaAs wafers covered with 6, 30, 60, and 90 nm thick SiO_2 (thickness after HF dip). SEM micrographs of the surface of two extreme cases are shown in Fig. 2. Nanowires grown with a 6 nm thick oxide are shown in Fig. 2(a), while nanowires obtained with a 90 nm oxide are depicted in Fig. 2(b). Nanowires are observed on all the substrates, in similar length and a slightly decreasing density for thicker oxide films. The main difference between the four samples is the existence or not of a preferential orientation of
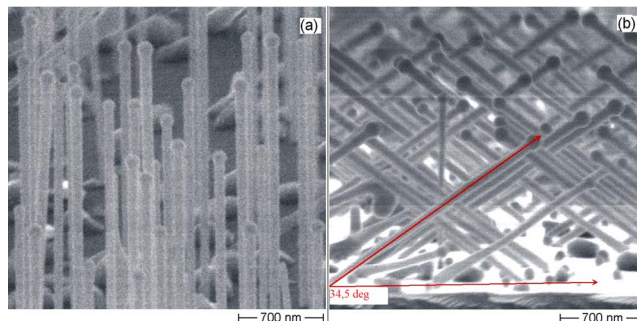

FIG. 1. (Color online) Nanowires obtained on SiO_2 coated GaAs wafers with two different surface orientations: (a) (111)B and (b) (001).
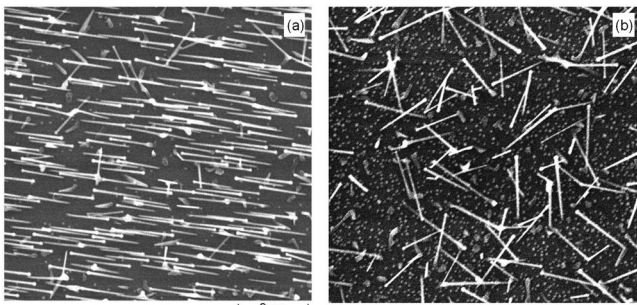
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FIG. 2. Scanning electron micrographs of GaAs nanowires grown on (001) GaAs substrate coated with a (a) 6 nm and (b) 90 nm thick SiO$_2$ layer.

the nanowires. In the case of the 6–30 nm thick oxide, the nanowires mainly align on the same angle, with their growth axis coinciding with (111)B directions of the underlying substrate. As it appears in Fig. 2(b), nanowires grow in random orientations when a thicker SiO$_2$ layer is used. The transition between aligned and not aligned nanowires occurs at an oxide thickness of 30 nm. From this results, we conclude that the existence of an oxide is necessary for the nanowire growth. Moreover, when the oxide is up to 30 nm thick, a correlation between the crystalline orientation of the substrate and the nanowires occurs.

We performed cross-sectional TEM measurements at the interface between the GaAs substrate, the SiO$_2$ layer and the GaAs nanowires. Figures 3(a) and 3(b) correspond to the analysis of the sample grown with a 6 nm oxide and Fig. 3(c) to the sample grown with a 90 nm oxide. A representative high resolution TEM (HRTEM) micrograph of the 6 nm sample is given in Fig. 3(a). In this case, the GaAs nanowire is clearly in physical contact with the substrate through a 10 nm hole in the oxide. Several twin dislocations are present in the nucleation area. In order to determine the correlation between the substrate structure and the nanowire base, the crystalline orientation of the different regions of the HRTEM micrograph was calculated. In Fig. 3(b), the power spectra [fast Fourier transform (FFT)] corresponding to the nanowire, nanowire-substrate interface, and substrate are shown. Each region and their corresponding analysis are framed with a number. We find that the GaAs nanowires
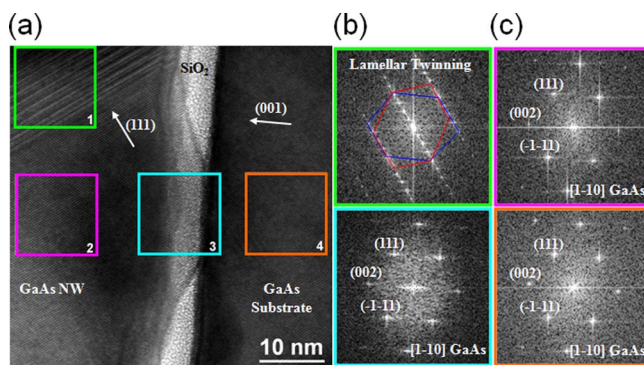

FIG. 3. (Color online) Cross-sectional transmission electron microscopy analysis of the nucleation stage of GaAs nanowires. (a) High resolution TEM micrograph interface with the substrate, in the case that the GaAs wafer is coated with a 6 nm SiO$_2$ layer. (b) Power spectra analysis of the different areas squared in (a), from which it is possible to deduce a perfect epitaxial relation between the substrate and the nanowire. (c) Bright Field TEM micrograph of a nanowire grown on a thick SiO$_2$ layer. The dashed line indicates the presence of a nanocrater in the region where the nanowire nucleates.
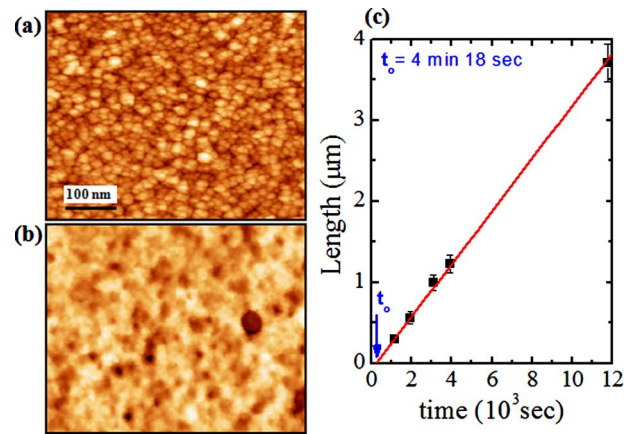

FIG. 4. (Color online) Morphology of surface of the SiO$_2$ (a) after sputtering and (b) before being introduced in the MBE system, measured with atomic force microscopy. The darker regions indicate the presence of some pinholes which are present at the surface after dipping the sample in 12% HF. These pinholes appear to be related to the nucleation of the GaAs nanowires. (c) Length of the nanowires as a function of the deposition time. From the graph, it is possible to deduce an incubation time of 4 min and 18 s.

grow along the (111)B direction. We note that multiple periodical twining is also observed at the initial stage of growth, frame number 1, which has already been reported before.[7–9] The FFTs of the nanowire and substrate indicate the same crystallographic orientation. The structure of the GaAs appearing at the nanocrater follows also the same orientation. The existence of this crater must be linked to the nucleation and explains the crystallographic relation between the substrate and the nanowires. The wire seems to nucleate in the limited space of the nanocrater, which is smaller than the total diameter. The diameter has probably increased during the growth process. Cross-sectional TEM measurements were also realized in the case of nanowires grown on a 90 nm thick oxide [Fig. 3(c)]. There is no epitaxial relation with the substrate. Nanoscale craters are also observed at the surface of the oxide and are directly linked to the nucleation of a nanowire. The depth of the crater is about 30 nm and does not reach the substrate. From the complete cross-sectional TEM analysis of Fig. 3, it is possible to draw the following two conclusions. (i) The nucleation of GaAs nanowires occurs inside nanoscale craters in the oxide. (ii) When the oxide is thin enough (≤30 nm) the nanocraters reach the underlying GaAs surface, allowing the epitaxial growth of the GaAs nanowires, which results in their alignment.

Atomic force microscopy measurements of the surface at the different stages of substrate preparation were carried out. The oxide surface after sputtering deposition is relatively smooth, with a rms roughness of 1.6 nm [Fig. 4(a)]. The film surface presents some granularity, usual in sputtered layers. The surface topology after the HF dip is presented in Fig. 4(b). The surface roughness has decreased down to 1.1 nm. However, as indicated in a circle in Fig. 3(c), the HF seems to have preferentially etched some intergranular regions, leading to the formation of pin holes. The pin holes are smaller and sparser than the nanocraters observed at the nucleation stage by cross-sectional TEM. The opening of the pin holes could originate from the interaction of the oxide with the Ga and As adatoms. Previous scanning tunneling microscopy studies corroborate that Ga adatoms tend to accumulate in existing defects on SiO$_2$ surfaces, leading to the

formation of bigger nanocavities.[10] The reaction of Ga with SiO_2 forming a eutectic may also play a role: $Ga(l) + SiO_2(s) \rightarrow Ga:Si(l) + O_2(g)$.

We also monitored the growth of the nanowires with the goal of capturing the nucleation. In Fig. 4(c), the length of the nanowires as a function of time is plotted. There is a delay of 258 s in the growth start. Incubation times have indeed been measured before in other type of nanowires.[11,12] In our case, the incubation time is more likely related to the formation of holes in the oxide that host the nucleation of the nanowires. We should also add here that growth directly on a GaAs surface under the same conditions did not result into the formation of nanowires.

In summary, we have demonstrated the growth of GaAs nanowires on GaAs wafers coated with SiO_2. We have shown that gallium adatoms interact with SiO_2 forming sparse nanocraters on preexisting subnanometer pinholes. For SiO_2 thicknesses below 30 nm, the nanocraters reach the underlying GaAs surface, resulting in an epitaxial relation of this with the GaAs nanowires. Finally, we have shown that the formation of nanocraters is characterized by an incubation period before the nanowire growth is initiated. This time has been estimated to be 258 s.

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