

Micro-Channel Plate Detectors Based on Hydrogenated Amorphous Silicon

Nicolas Wyrsh¹, François Powolny², Matthieu Despeisse², Sylvain Dunand¹, Pierre Jarron², Christophe Ballif¹

¹Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of Microengineering (IMT), Photovoltaics and thin film electronics laboratory, Breguet 2, 2000 Neuchâtel, Switzerland,

²CERN, CERN Meyrin, 1211 Genève 23, Switzerland.

ABSTRACT

A new type of micro-channel plate detector based on hydrogenated amorphous silicon is proposed which overcomes the fabrication and performance issues of glass or bulk silicon ones. This new type of detectors consists in 80-100 μm thick layers of amorphous silicon which are micro-machined by deep reactive ion etching to form the channels. This paper focuses on the structure and fabrication process and presents first results obtained with test devices on electron detection which demonstrate amplification effects. Fabrication and performance issues are also discussed.

INTRODUCTION

As an alternative to particle detection using diodes, micro-channel plates (MCP) detectors are used for fast-time resolution. Such detectors consist in thick plates having very narrow micro-channel drilled throughout the plate. A high electrical field is applied between the two faces of the plate to create avalanche mechanisms in the micro-channels upon the hit of the channel wall with a primary electron. These avalanches lead to an amplification of the signal and are commonly used as image intensifying devices [1]. Such detector can be considered as an array of microscopic electron multiplier tubes. MCPs are conventionally fabricated from lead glass plates and treated to enhance secondary electron emission and to render the wall of the channels semiconducting (for charge replenishment). To overcome some of the performance limitations and manufacturing issues associated to glass MCPs, MCPs based on micro-machined Si wafers have been recently introduced [2,3]. However, the low bulk resistivity of c-Si requires an additional and critical deposition of a layer stack on the channel walls to achieve optimum MCP performances.

To overcome some critical limitations of current MCPs, we proposed a very innovative type using a-Si:H thick layers [4]. In this context, a-Si:H offers three important advantages for MCPs: A high bulk resistivity that can be tuned, the fact that a-Si:H can be micro-machined as c-Si material and the possibility to deposit the material (and the devices) on various type of substrates including CMOS readout chips [5]. The latter point implies that a-Si:H based MCP (AMCP) detectors could also be vertically integrated, greatly simplifying the cumbersome construction of usual MCPs, broadening the range of application including particle detection and imaging. The fact that AMCPs compared to glass MCPs do not require isolation/resistive layer stack greatly simplify the fabrication and should permit, thanks to an ideal bulk resistivity of a-Si:H, a fast charge recovery of the depleted micro-channels (after an avalanche event).

The typical structure of an AMCP and its functioning principle is given in Fig. 1. A primary electrons (coming directly on the device or generated by a photo-cathode or ionization converter) is multiplied by successive hits on the walls of the micro-channels and collected at the back of the MCP by a pixel electrode. Note here that we have in general many micro-channels on

top of each individual pixel electrode. The latter can be part of an underlying readout chip or connected to adjacent electronic circuits. Such AMCP consists in a very thick (typically between 80 and 100 μm) a-Si:H deposited on the pixel electrode back plane (or readout chip) with at top common electrode. Micro-channels of a few microns in diameter are drilled by deep reactive ion etching (DRIE).

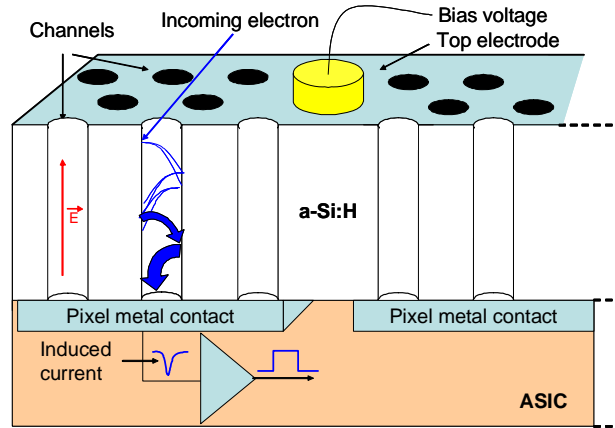


Figure 1. a-Si:H based MCP (AMCP) structure.

In this paper, we will describe and discuss the processes and issues related the fabrication of such AMCPs. First results on electron detection obtained using an electron beam induced current apparatus will be presented, demonstrating avalanche mechanisms in the micro-channels. Present performances, limitations and possible improvements will be discussed.

EXPERIMENT

AMCP structure and layout

First AMCP prototypes were fabricated on oxidized Si wafer covered with an Al back pixel electrodes. These devices comprise channels with a diameter of 3-5 μm drilled by DRIE into 80-100 μm thick a-Si:H layers. For testing purposes, 15x15 mm^2 reticles have been defined with 24 pixels with sizes of 0.5x0.5, 1x1 and 2x2 mm^2 (see Fig. 2). Various reticles were

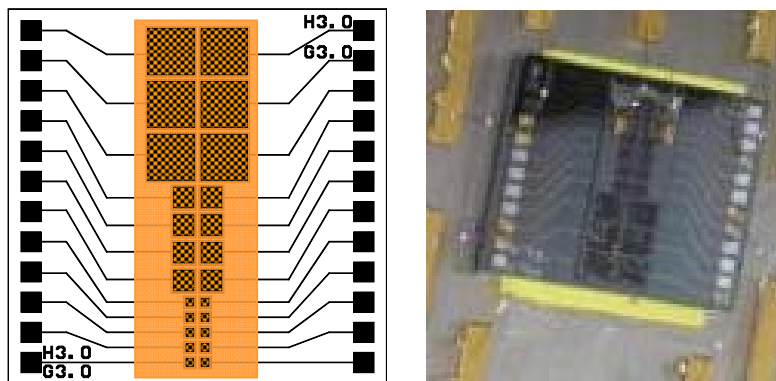


Figure 2. AMCP test reticle design (left) with the back electrodes and bonding pads in black; the colored area is covered by the thick a-Si:H layer while the patterned squares correspond to the area where the micro-channels are drilled. Picture of such a reticle (right).

designed with micro-channels (over each pixel) with a (nominal) diameter of 1.5 to 5 μm separated by a gap of (nominally) 2.5 to 3.5 μm .

AMCP fabrication

Deposition of these thick a-Si:H layers requires a careful optimization in order to achieve high deposition rate with reasonable material quality while maintaining a low internal mechanical stress. All a-Si:H layers were deposited by VHF PECVD (very high frequency plasma enhanced chemical vapor deposition) at a plasma frequency of 70 MHz on oxidized 4" Si wafers with an oxide layer thickness of 1-2 μm covered with the Al back contact plane. Even though almost stress free layers a-Si:H layer can be deposited by VHF PECVD at 170°C on c-Si [5], such temperature resulted in too high stress and delamination during the deposition of the a-Si:H layer. Successful growth of 80 to 100 μm with reasonable compressive stress (without delamination and allowing consecutive micro-machining process steps) was achieved at a deposition temperature of 235°C. With a deposition rate of approx. 2 nm/s, the 14 hours deposition time required for 100. As a front common electrode, a 100 nm thick a-Si:H n-type layer was also deposited by VHF PECVD.

Prior to the micro-fabrication of the channels, the a-Si:H was patterned over the pixel regions in order to release stress on the wafer and to get access to the bonding pads. This step was carried out using a hard mask and dry etching in O_2/SF_6 plasma. Drilling of the channels was performed by DRIE using a Bosh Process (DRIE machine from Surface Technology Systems). Micro-channels with aspect ratios over 25 could be obtained after optimization of the process. Part of this optimization process was done on c-Si wafer as the etching behavior of a-Si:H is very similar to the one of c-Si. Top and side views (Scanning Electron Microscope - SEM pictures) of holes drilled in thick a-Si:H layers are show in Fig. 3. SEM pictures of the details of a complete AMCP are given in Fig. 4.

AMCP characterization

Test devices were characterized using either a 10 kV electron gun or by electron beam

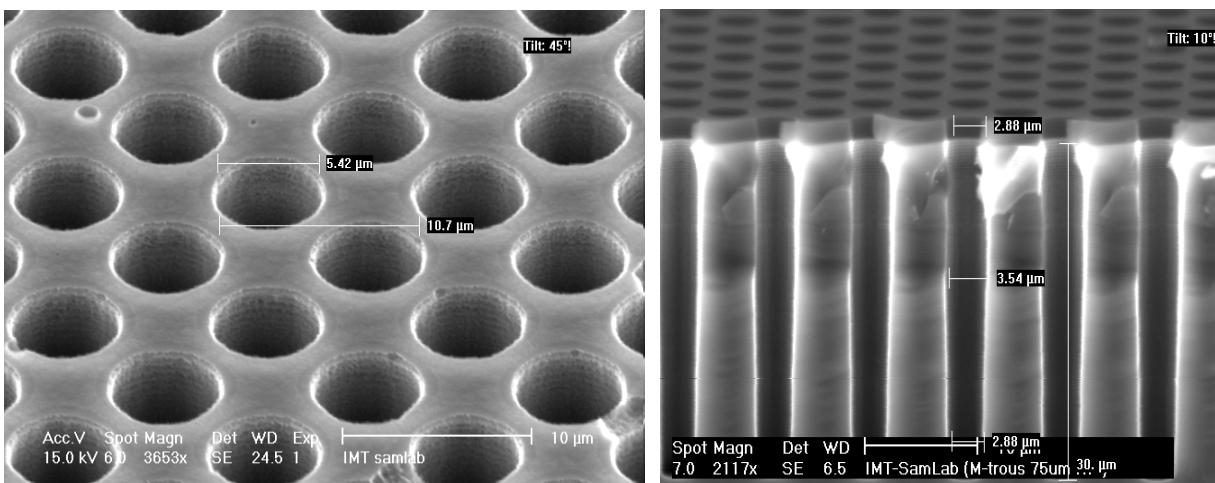


Figure 3. SEM pictures of the surface and cross section of thick a-Si:H layers with holes drilled by DRIE.

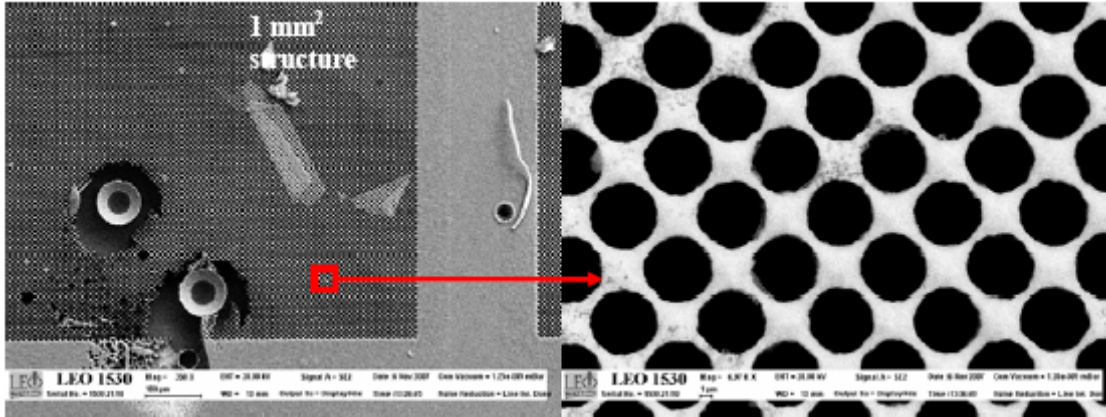


Figure 4. SEM pictures showing the corner of one AMCP pixel as well as a zoom (right) over that pixel. One may also observe large defects (left picture) created during the DRIE process.

induced current (EBIC) mapping. The latter was performed at the European Synchrotron Radiation Facility (ESRF) in Grenoble, on a Scanning Electron Microscope (SEM) from Carl ZEISS (named "Leo 1530 Gemini"). A schematic view of the electrical set-up is given in Fig. 5. A Keithley 2410 was used for the application of the bias voltage and for the measurement of the current. Samples have been measured as a function of the bias voltage and e-beam intensity. For EBIC imaging the AMCP pixel were connected to a custom fast current/voltage converter and amplifier for leakage compensation and signal conditioning. Samples were characterized as a function of the bias voltage, beam incidence angle and beam energy (between 4 and 30 keV).

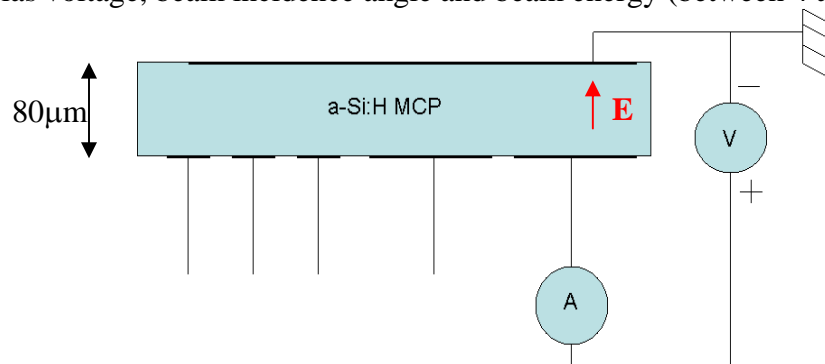


Figure 5. Electrical set-up for AMCP signal/leakage measurements.

RESULTS AND DISCUSSION

Several reticles were mounted on test circuits for electrical characterization (cf. Fig. 2) and exposed to an electron beam of 10 keV of variable intensity. Preliminary results obtained on one of the samples are shown. Figure 6 shows the current measured on a $1 \times 1 \text{ mm}^2$ pixel as a function of bias voltage and beam intensity. As one can observe, above 400 V bias voltage, the current induced by the electron beam increase proportionally with the bias voltage (amplification effect). A clear dependency on the beam intensity is also observed. Rather large discrepancies were observed between structures and the difficulties to evaluate a gain values called for more detailed analysis of the detector response. The presence of a threshold voltage for the amplification effect is not yet understood. It is probably an artifact introduced by the poor uniformity of the response of the present device as discussed below.

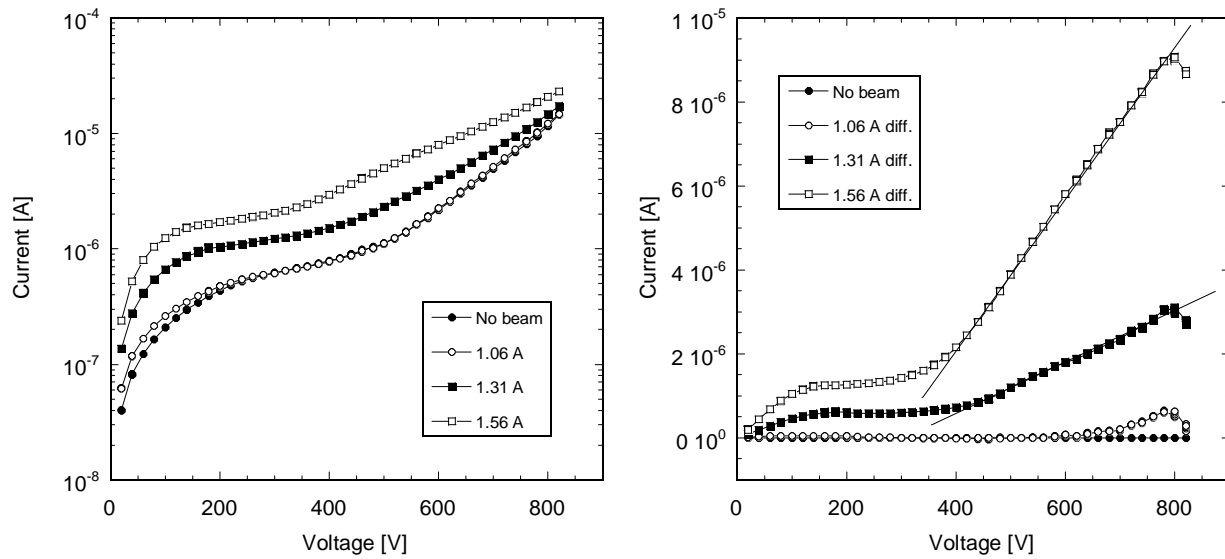


Figure 6. Electrical current measured on a $1 \times 1 \text{ mm}^2$ pixel as a function of bias voltage and beam intensity (indicated here as a function of the e-gun filament current): (left) Raw current value, (right) current after subtraction of the leakage current (current without beam).

EBIC images were taken under various electron beam energy to evaluate the local response of the detector. The DC signal was here compensated to reveal the “active” area of the AMCP area where signal amplification takes place. Three EBIC images of a $0.5 \times 0.5 \text{ mm}^2$ pixel are shown in Fig. 7. One can first observe (left) that the response is not homogeneous over the pixel area. Only the channels at the periphery are responding while the central area of the pixel is inactive. Detailed analysis revealed that an important erosion of the surface of the n-doped top layer, over the entire area of the pixel back electrode, took place during the DRIE process. We believe that this erosion process is also related to the formation of the large defects (seen in Fig. 2) and takes place at the end of the DRIE process when the channels start to open down to the back electrodes. The effect of this erosion is to strongly increase the surface resistivity which leads in a drop of the electrical field for channels far from the pixel edge. One can also observe

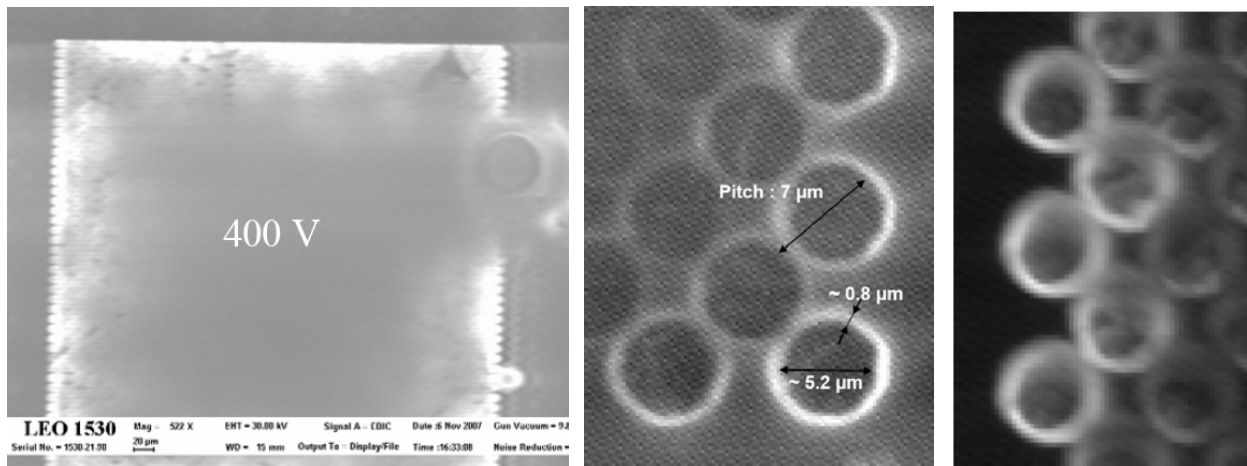


Figure 7. EBIC pictures of a $0.5 \times 0.5 \text{ mm}^2$ pixel biased with 400 V: (left) overall pixel image, (centre) zoom on the corner, (right) zoom on the periphery with a sample tilting of 5° .

that the presence of the large defects seen in Fig. 2 do not affect the overall functioning of the AMCP, those defects being electrically isolated from their surrounding.

A zoom over a few channels (Fig. 7 centre) shows that, as expected, only electrons hitting walls of the channels are detected. Electrons going through the channel in the center do not create any avalanche. In order to increase the sensitivity and gain of a MCP, channels have to be at a certain angle with respect to the angle of incidence of the primary electron as used for example in the chevron design of standard MCPs [1]. When tilting our AMCP by 5 degrees one can observe (Fig. 7 right) that a much larger surface area starts to be active as almost all electrons entering the channels are now expected to impinge on the walls.

CONCLUSIONS

First prototypes of AMCP were successfully fabricated on 4" Si wafers. Amplification effects have been demonstrated even though the gain value has not yet been extracted. For the time being the fabricated devices suffer from fabrication issues responsible for a strong inhomogeneity of the response over the pixel areas. An erosion of the surface and the creation of local defects are observed which will require an optimization of the DRIE process as well as an adaptation of the device structure. Replacement of the n-doped a-Si:H top contact layer by a metallic contact (not implemented so far to avoid any contamination of the DRIE system with metallic impurities) could also be applied.

Beside the improvement of the fabrication process, detailed investigation are needed to first understand and, secondly, to improve the avalanches process in the micro-channels. This should help define the limitations and potential of this new technology. Nevertheless, the high bulk resistivity of a-Si:H as used in AMCP should eliminate the issue of charge replenishment in conventional glass MCP. The fact that AMCP performance can be easily imaged by EBIC is here a first evidence of this advantage. Compared to c-Si MCP, this high bulk resistivity considerably simplifies the device structure and eases the fabrication.

These first encouraging results support the expectations for AMCP. The devices can be fabricated using known and mastered technology over 4" wafers and the processing steps are compatible with CMOS technology. Vertical integration of MCP over readout chip should be possible allowing higher performance and reliability.

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