Power Consumption of Logic Circuits in Ambipolar Carbon Nanotube Technology

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Abstract

Ambipolar devices have been reported in many technologies, including *carbon nanotube field effect transistors (CNTFETs)*. The ambipolarity can be in-field controlled with a second gate, enabling the design of *generalized logic gates* with a high expressive power, *i.e.*, the ability to implement more functions with fewer physical resources. Reported circuit design techniques using generalized logic gates show an improvement in terms of area and delay with respect to conventional CMOS circuits. In this paper, we characterize and study the power dissipation of generalized logic gates based on ambipolar CNTFETs. Our results show that the logic gates in the generalized CNTFET library dissipate 28% less power on average than a library of conventional CMOS gates. Further, we also perform logic synthesis and technology mapping, demonstrating that synthesized circuits mapped with the library of ambipolar logic gates dissipate 57% less power than CMOS circuits. By combining the benefits coming from the expressive power of generalized logic and from the CNTFET technology, we demonstrate that we can reduce the *energy-delay-product* by a factor of 20× using the ambipolar CNTFET technology.

1. Introduction

Traditional CMOS libraries provide the universal NAND, NOR, and compound AOI/OAI gates but fail to efficiently implement circuits that contain one or more binate operations such as the XOR. This makes them inefficient for circuits such as n-bit adders and parity functions that are efficiently implemented using XOR gates [1]. Recently, new *ambipolar* devices have been reported, which conduct under both positive and negative gate voltages. It has been demonstrated that their ambipolarity can be in-field controlled [2], making such devices suitable candidates for building libraries of complex logic gates that efficiently embed XOR functions. The *expressive power* of such libraries, *i.e.*, their ability to implement more logic functions with fewer physical resources, was shown to be higher than the expressive power of CMOS libraries based on conventional unipolar MOSFETs [3].

Ambipolar behavior has been reported in *carbon nanotube field effect transistors (CNTFETs)* [2]. The electrostatic field applied at the back gate of the CNT-to-metal contacts is responsible for controlling the device polarity. The ultimate goal of design using such devices is to leverage their controllable ambipolarity at the gate level, which yields a very compact realization of the XOR function, and its integration into more complex logic gates for a negligible cost [4]. In prior work, it has been demonstrated that embedding the XOR function into complex gates results in a higher *expressive power*, *i.e.*, the potential to implement more complex functions using fewer physical resources. Dynamic reconfigurable logic gates with ambipolar CNTFETs were demonstrated in [5, 6]. A library of static and pseudo-logic gates with ambipolar CNTFETs based on transmission gates and pass-transistors was introduced in [3], showing a considerable area and delay saving in multi-level logic synthesis. However, no estimation of the cost of the proposed designs in terms of power dissipation was presented, despite the fact that the extensive utilization of XOR gates and transmission gates is expected to increase the power consumption.

This paper addresses the issue of power consumption of ambipolar logic gates, and focuses on the static CNTFET transmission-gate library presented in [3]. The work presents for the first time, a characterization of a full library of ambipolar logic gates for power dissipation. It uses an efficient method based on off-current pattern classification in order to characterize the leakage of logic gates, taking into account its dependence on the input vector. We demonstrate that leakage in ambipolar gates slightly increases the static power, which is negligible compared to dynamic power. On average, the ambipolar CNTFET library reduces total power by 28% in comparison to the CMOS library. Further, we also present results for synthesis and technology mapping of logic circuits with the characterized ambipolar CNTFET library. Our results indicate a reduction in the number of mapped gates by 23%, an average delay improvement by a factor of 7×, a power saving of 57%, and a reduction of the *energy-delay-product (EDP)* by 20× in comparison to a library of conventional CMOS gates.

This paper is organized as follows. The next section provides a background for ambipolar devices and ambipolar circuit design. Section 3 introduces the model used to estimate the power dissipation of the ambipolar library and an off-current pattern classification technique to estimate static power. Section 4 presents results for power dissipation using the ambipolar library. Section 5 is a conclusion.

2. Background

This section surveys previous works related to physics and technology of ambipolar devices based on CNTFETs, and summarizes previous approaches to leverage the controllable ambipolarity at the circuit level.

2.1 Ambipolar technology

It has been recently reported [2] that CNTFETs with intrinsic CNT channels operate either as n- or as p-type transistors if a Schottky contact is formed at the drain and source with a mid-gap metal, *i.e.*, a metal having its work function in the CNT bandgap. Given an intrinsic channel, both electrons and holes carry current simultaneously. Depending on the voltage applied at the bulk, which operates as a second gate, the band diagrams at the drain-to-gate and source-to-gate contacts are bent such that the Schottky barrier becomes much thinner for one of the charge carriers than the other. In this case, the device has a unique polarity and the majority charge carrier is determined by the applied second gate voltage. This property

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motivates the use of the back gate as a second gate, which controls the n- or p-type polarity of the transistor. Such devices have two gates; one of them operates as a *polarity gate* (n- or p-type), while the other gate operates as a conventional gate (on- and off-state).

A technique to manufacture controllable ambipolar CNTFETs with a top and a back gate has been reported [2]. The symbol of the in-field programmable CNTFET is shown in Fig. 1(a) and the configuration of n- and p-type devices is illustrated in Fig. 1(b) and 1(c) respectively: if the polarity gate is set to 0, the device exhibits n-type behavior; otherwise it exhibits p-type behavior.

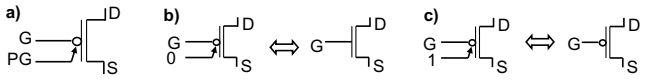

Figure 1: Ambipolar CNTFET: device symbol (a), configuration as n-type (b) and p-type (c).

2.2 Logic design with ambipolar CNTFETs

The ambipolarity of CNTFETs was investigated in [4], where a single CNTFET with a resistive pull-up to V_{DD} was used in order to implement a dynamic XOR logic gate. In [5], the novel programmability of CNTFETs was leveraged in a compact in-field reconfigurable logic gate that maps eight different logic functions of two inputs using only seven CNTFETs. In [6], the design of a *generalized NOR (GNOR)* gate in dynamic logic was proposed as the core building block to realize in-field PLAs. It has a compact design and high expressive power by combining both NOR and XOR operations in the output function.

A new approach to design static logic gates with ambipolar CNTFETs was presented in [3]. It is based on the utilization of two different building devices within the logic gates. The first building block is a single transistor with a fixed polarity that can be either n or p. The second building block is a transmission gate formed by two ambipolar CNTFETs biased with opposite polarities. In a transmission gate, both ambipolar devices biased with opposite signals have distinct polarities and are in parallel, thus ensuring in all cases that one of the two parallel devices properly conducts the signal (Fig. 2). A transmission gate with signals A and B applied respectively on the polarity gate and the conventional gate of one transistor and their complements applied on the other transistor implements the XOR function by passing current if and only if $A \oplus B = 1$.

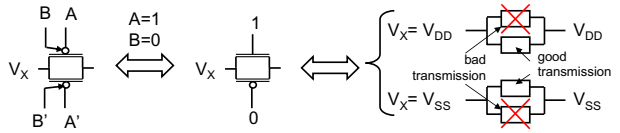

Figure 2: CNTFET transmission gate: any passing configuration ($A \oplus B = 1$) prevents signal degradation.

By combining single transistors and transmission gates, it is possible to extend basic logic gates such as the NAND gate $\overline{A \cdot B}$ to their generalized counterparts. For example, the *generalized NAND (GNAND)* gate has the form $\overline{(A \oplus C) \cdot (B \oplus D)}$. In a similar manner, NOR, AOI and OAI gates can be extended to *generalized NOR, AOI* and *OAI (GNOR, GAOI* and *GOAI)* gates respectively. Figure 3 illustrates the circuit implementation of some gates that can be obtained using no more than two transmission gates or transistors in series/parallel in the *pull-up (PU)* and *pull-down (PD)* networks.

3. Simulating power dissipation

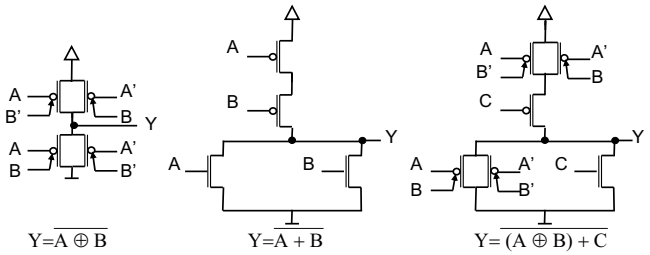

Figure 3: Example of static ambipolar CNTFET gates

The frequent utilization of embedded XOR functions in the library presented in [3] may increase the dynamic power dissipation because of the high activity factor of these functions. The activity factor is defined as the number of times a gate switches from 0 to 1 and from 1 to 0 on average, when all its input combinations are applied. For 2-input NOR and NAND gates, three input combinations yield an output polarity different from the fourth input polarity for an activity factor of 25%. On the other hand, for 2-input XOR gates, the activity factor is 50%. Moreover, even when the embedded XOR gates are not switching, their static power is expected to be high, given the fact that they are formed by transmission gates whose leakage is twice as high as the static leakage of a single transistor with the same size.

3.1 Model of power dissipation

In order to study the power dissipation of static logic gates in ambipolar CNTFET technology, we consider the different components of power dissipation reported in static logic gates in CMOS technology [7]. The total power dissipation of a logic gate is modeled as follows:

$$P_T = P_D + P_{SC} + P_S + P_G \quad (1)$$

where P_D is the dynamic power, P_{SC} the short-circuit power, P_S the static power and P_G the power dissipation due to gate leakage. Dynamic power is dissipated whenever the gate switches from 0 to 1 and from 1 to 0 in order to charge or discharge the load capacitance. In this work, we do not consider the dynamic power dissipated by the interconnect. Short-circuit power is dissipated during the switching phase when devices in both PU and PD networks are temporarily and simultaneously conducting current from V_{DD} to V_{SS}. Static power is dissipated when the gate is idle due to the sub-threshold leakage. The power dissipation due to gate leakage is caused by the tunneling current through the gate oxide. The different components of the total power can be estimated as follows [7, 8]:

$$P_D = \alpha \cdot C \cdot f \cdot V_{DD}^2 \quad (2)$$

$$P_{SC} \approx 0.15 \cdot P_D \quad (3)$$

$$P_S = I_{off} \cdot V_{DD} \quad (4)$$

$$P_G = I_g \cdot V_{DD} \quad (5)$$

where α is the activity factor, C the load capacitance, f the operating frequency, V_{DD} the power supply, I_{off} the sum of all sub-threshold currents, and I_g is the sum of all gate leakage currents. The conjecture $P_{SC} \approx 0.15 \cdot P_D$ has been verified for CMOS technology [7] and is also assumed to be valid for CNTFETs.

Generally, f and V_{DD} are fixed for a given process and design, C is given by the process and geometry, and α is statistically estimated for a given circuit and application. This gives analytical expressions for P_D and P_{CS}. However, the static leakage currents I_{off} and I_g do not have any analytical expression for CNTFET technology, and they strongly depend on the input vector. We therefore

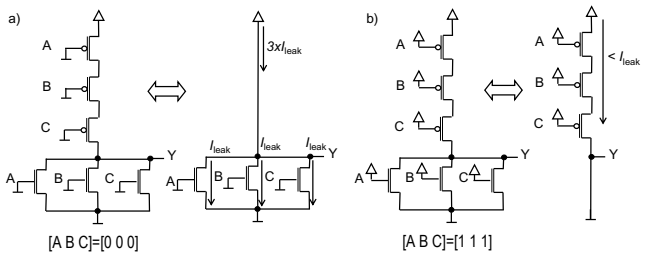

Figure 4: Example of leakage: (a) High leakage through parallel transistors. (b) Lower leakage through series transistors.

deploy a method that uses the SPICE model of CNTFETs in an efficient way by classifying the patterns generated by the input vectors, in order to estimate P_S and P_G.

3.2 Pattern-based power model

In order to estimate the static power, we need to consider all input vectors that strongly impact the static power. For example, given a 3-input NOR gate, depending on the input vector, we may have an increase of static power by a factor of more than $3\times$ if we compare leaking parallel transistors (input [0 0 0]) to those that are in series (input [1 1 1]) as depicted in Fig. 4.

The number of input vectors increases exponentially with the number of inputs. We can avoid running a large number of simulations to quantify I_{off} for every input pattern by using the I_{off} pattern classification method [8]. This method is based on identifying the pattern of on- and off-transistors for every given input vector. Then, the on-transistors are considered to have a negligible resistance and just replaced by a short circuit in the pattern. Also off-transistors that are shorted by parallel on-transistors are removed from the pattern. For instance, a 3-input NOR gate with the input vectors [1 1 0] and [1 0 1] generates the same I_{off} pattern. Once an I_{off} pattern is mapped onto every input vector, only the set of different I_{off} patterns has to be quantified. We found out that for all gates in the library there are in total 26 different I_{off} patterns, if we assume that the current leaking through n-type and p-type off-transistors with the same size is equal.

Further, since the gate leakage is also a static current that occurs under the same circumstances as I_{off}. Consequently, it also depends on the input vector and it can be assessed by using the same pattern-based method.

3.3 Simulation flow

The library characterization for power dissipation was carried out in two steps (Fig. 5). First, we performed the mapping between the off-current patterns and the input vectors for every logic gate in the library by determining the topology of the logic gate given the input vector, to obtain a netlist of off-transistors. This *gate topology analyzer* also calculates the activity factor of every logic gate. Then, we performed circuit level simulations in order to determine the exact value of I_{off} and I_g characterizing every off-current pattern. Thus, for every logic gate, we obtained a vector of I_{off} and I_g values for every input vector, which were averaged and used to estimate the static power dissipation. This flow is depicted in Fig. 5.

In [5], it was suggested and proven that a behavioral model for ambipolar CNTFETs can be built on a SPICE model for MOSFET-like CNTFETs by using a parallel pair of n- and p-type devices. We used the HSPICE Stanford model for MOSFET-like CNTFETs [9] in order to emulate the ambipolar devices, by applying the approach suggested in [5].

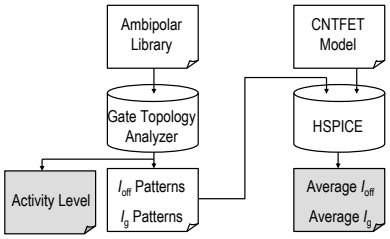

Figure 5: Simulation flow

4. Power consumption of logic circuits

We used the static ambipolar CNTFET transmission-gate library designed in [3]. The load capacitance depends on the intrinsic drain capacitance and on the gate fanout, assumed to be equal to 3. We assumed identical values for unit gate, drain and source capacitances, as well as a 32 nm gate width and 3 CNTs per channel. Based on these assumptions, the unit capacitances can be derived from [10]. In order to compare the power dissipation of CNTFET logic gates with those in CMOS technology, we also characterized the logic gates taken from the considered library, and which are available in CMOS technology. Leakage currents I_{off} and I_g for a unit transistor as well as unit capacitances were estimated using the MASTAR simulator provided by the *international technology roadmap for semiconductors* [11]. In these simulations, we assumed the built-in model for 32 nm bulk technology with metal gate and strained channel. For both CNTFET and CMOS logic gates, we set the power supply and operating frequency to 0.9 V and 1 GHz respectively. Short circuit power was assumed to be 15% of P_D [7].

Based on these assumptions, we characterized the whole library of 46 logic gates designed in [3]. Power dissipated as gate leakage was found to be about 10% of P_S for CMOS gates and less than 1% of P_S for CNTFET because of the high-κ dielectric used as gate insulator in CNTFETs [9]. One of the key contributions to dynamic power comes from the activity factor. The CNTFET library shows on average the same activity factor as the CMOS library, despite the frequent presence of XOR functions. Although the XOR function has a higher activity factor when it is used as a stand-alone gate, we observed that embedding the XOR function in complex generalized gates does not increase the overall activity factor. The CNTFET gates dissipate 27% less dynamic power on average than CMOS gates, which is mainly due to the lower CNTFET input capacitance, given the equal activity factors. Further, under these technological assumptions, the input capacitance of a CNTFET inverter is 36 aF, while it is 52 aF for CMOS inverters (31% difference). Static power of CNTFET gates is about one order of magnitude less than CMOS gates, because of the use of a thick insulator separating drain/source from the substrate of CNTFETs. Across the library, the CNTFET gates dissipate 28% less power than CMOS gates.

In order to estimate the power consumption of complex logic circuits in the following set of simulations, we synthesized logic circuits and mapped them with the considered library (generalized gates), with a reduced CNTFET library including only MOSFET-like CNTFETs, and with a CMOS library. We used the tool ABC developed at Berkeley [12] for logic synthesis and technology mapping of several benchmark circuits. The circuits were first synthesized using the `resyn2rs` script, followed by technology mapping using genlib libraries that were compiled for each logic family based on the area/delay values from [3]. This generates the number of gates and the total delay of the synthesized circuits. Based on the obtained netlists, the power consumption and EDP were estimated using 640K random patterns. The results for 12 benchmark circuits

Table 1: Logic synthesis and technology mapping: gate count, delay (ps), P_D (μW), P_S (μW), P_T (μW) and energy-delay-product (10^{-24} J $\cdot$ s), simulated at $f = 1$GHz and $V_{DD} = 0.9$V

Benchmark		CNTFET Technology (generalized gates)						CNTFET Technology (conventional gates)						CMOS Technology					
Circuit	Function	No.	Delay	P_D	P_S	P_T	EDP	No.	Delay	P_D	P_S	P_T	EDP	No.	Delay	P_D	P_S	P_T	EDP
C2670	ALU and control	541	52	10.95	0.10	12.70	0.66	631	62	14.52	0.14	16.83	1.04	632	320	20.34	1.84	25.42	8.13
C1908	Error correcting	261	50	4.23	0.05	4.91	0.25	569	90	11.34	0.13	13.17	1.19	544	452	15.81	1.63	19.98	9.04
C3540	ALU and control	871	80	17.35	0.18	20.13	1.61	1126	109	24.06	0.26	27.93	3.04	1084	551	32.24	3.29	40.70	22.41
dalu	Dedicated ALU	892	68	13.29	0.19	15.48	1.06	1142	79	17.24	0.26	20.08	1.59	1046	401	22.38	3.20	29.26	11.73
C7552	ALU and control	1229	59	24.68	0.24	28.62	1.69	1722	77	40.74	0.38	47.23	3.65	1615	401	55.45	4.85	69.10	27.71
C6288	Multiplier	1645	161	31.53	0.31	36.57	5.88	3405	245	79.40	0.78	92.09	22.57	3653	1268	114.20	11.09	143.53	181.96
C5315	ALU and selector	1163	58	23.69	0.24	27.47	1.59	1368	88	31.96	0.31	37.06	3.28	1496	448	48.53	4.41	60.66	27.20
des	Data encryption	3429	40	59.02	0.72	68.59	2.75	3483	59	64.71	0.78	75.19	4.41	3668	301	98.34	11.26	125.48	37.82
i10	Logic	1680	82	23.37	0.34	27.21	2.24	1979	95	31.29	0.43	36.41	3.47	2073	486	45.90	6.00	59.39	28.88
t481	Logic	860	54	6.92	0.19	8.15	0.44	709	58	5.08	0.15	6.00	0.35	743	290	7.73	2.24	11.36	3.30
i8	Logic	961	37	19.72	0.21	22.89	0.86	987	37	19.98	0.22	23.19	0.87	974	191	29.06	2.93	36.65	7.00
C1355	Error correcting	212	27	3.34	0.04	3.88	0.10	428	62	10.73	0.10	12.43	0.78	607	320	18.16	1.83	22.89	7.33
Average		1145	64	19.84	0.23	23.05	1.59	1462	89	29.25	0.33	33.97	3.85	1511	452	42.35	4.55	53.70	31.04
Improvement vs. CMOS		24.2%	7.1×	53.4%	94.5%	57.1%	19.5×	3.2%	5.1×	30.9%	92.7%	36.7%	8.1×	-	-	-	-	-	-

are summarized in Table 1.

On average, technology mapping with the CNTFET library using generalized gates results in more than 20% saving in terms of number of logic gates compared to the CNTFET library using conventional gates. Both CNTFET technology with conventional gates and CMOS technology need the same physical resources, because they implement the same set of gates. The compact design with the generalized CNTFET library is on average 25% faster than the conventional CNTFET library, and 7× faster than CMOS designs, because the intrinsic CNTFET delay is 5× lower than the MOSFET delay [10]. Circuits that embed XOR operations (multiplier, and error correcting circuits) require the fewest gates and can be mapped with the lowest delay when the generalized CNTFET library is used.

On average, static power is about two orders of magnitude less than dynamic power for both types of CNTFET families and one order of magnitude less for the CMOS family. This is mainly due to the better isolation of CNTFETs in the off-state. The generalized CNTFET library is, on average, 28% more power efficient than the conventional CNTFET library. The highest power savings were observed for the multiplier C6288 and the error correcting circuits. The same trend can be seen when circuits mapped with the generalized CNTFET gates are compared with those mapped with CMOS gates, showing an average power saving of 57%.

The generalized CNTFET library outperforms the conventional CNTFET library in terms of EDP by 43% on average. The lowest EDP is found with the circuits embedding XOR operations frequently (C1908, C6288 and C1355), because their delay and power consumption are lower with the generalized CNTFET implementation. The EDP of CMOS-based circuits is much larger than circuits mapped with either CNTFET family. Whereas the EDP of conventional CNTFET gates is expected to be 13× lower than CMOS gates [10], the simulated EDP of circuits mapped with generalized CNTFET gates is on average 20× lower than CMOS circuits, resulting from the cumulative benefits of the proposed design technique and the technology boosters of CNT technology.

Finally, we highlight that our approach is a first-order technique that allows us to assess the benefits of ambipolar CNTFET technology. More accurate results will require the utilization of a better device model. In the underlying CNTFET model, only band-to-band tunneling was included, but leakage through the Schottky contacts [9] was ignored. Moreover, the short-circuit power was assumed to be 15% of the static power based upon published results for CMOS technology, and this may be different for CNT technology. It is important to note that we did not consider the full layout in order to estimate the capacitances and the dynamic power, but just the input and output capacitances, which limits the accuracy of the estimation.

5. Conclusions

In-field programmable ambipolar logic gates generalize conventional gates by efficiently integrating the XOR function. We presented a method to estimate the power dissipation of such generalized logic gates depending on the input vectors using the pattern classification method. Generalized logic gates based on ambipolar CNTFETs dissipate 28% less power on average than CMOS gates. Generalized logic gates have a higher expressive power than conventional ones and they map synthesized logic circuits more efficiently. Synthesis results for several circuits including ALUs, multipliers, and error correcting circuits show that on average, a power saving of 57% can be achieved with the ambipolar CNTFET library over a conventional CMOS library. The cumulative benefits of the design approach and the CNT technology result in an EDP reduction by a factor of 20×.

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