

Translating Dataflow Programs to Efficient Hardware: an *MPEG-4 Simple Profile Decoder* Case Study

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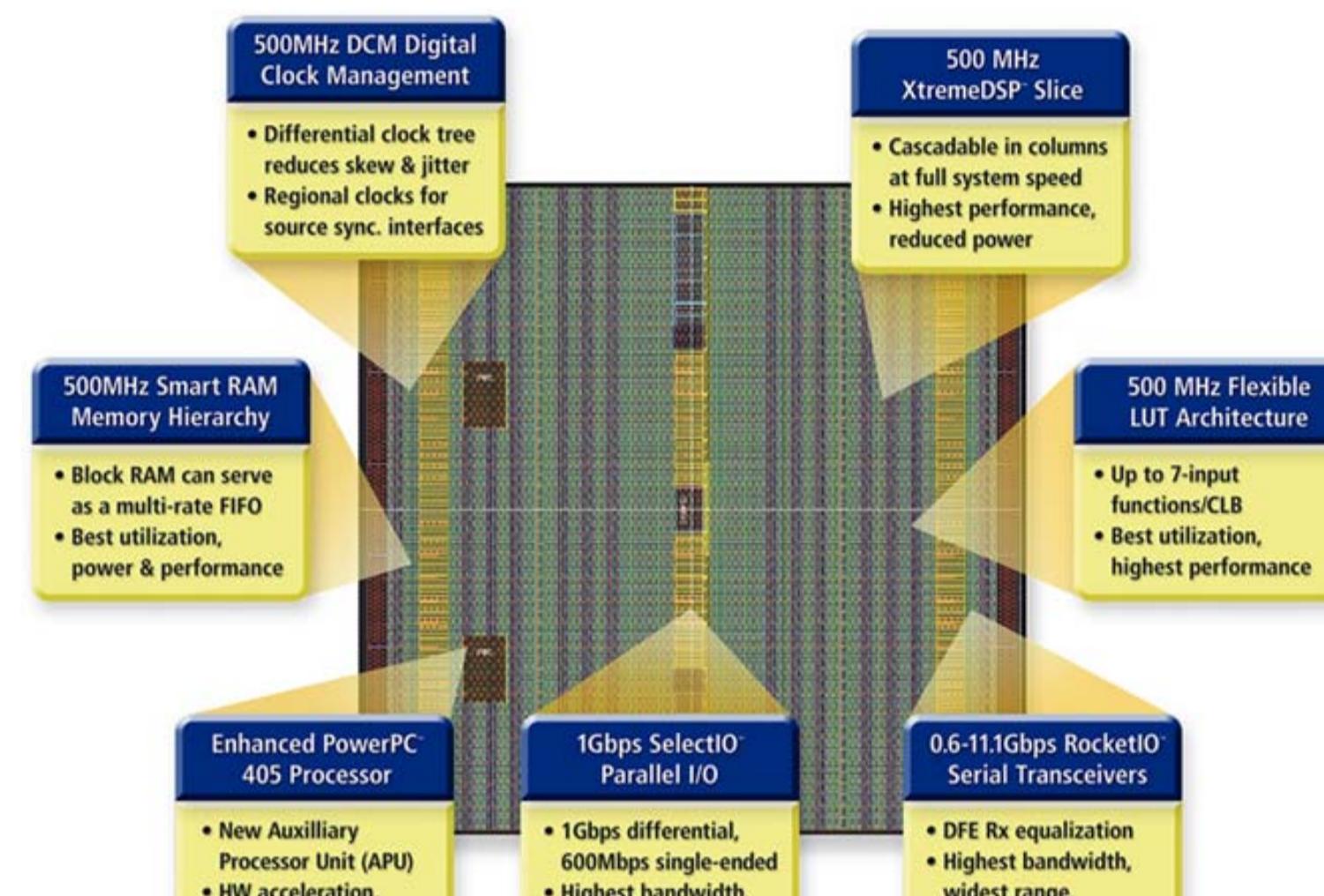
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Dataflow programming

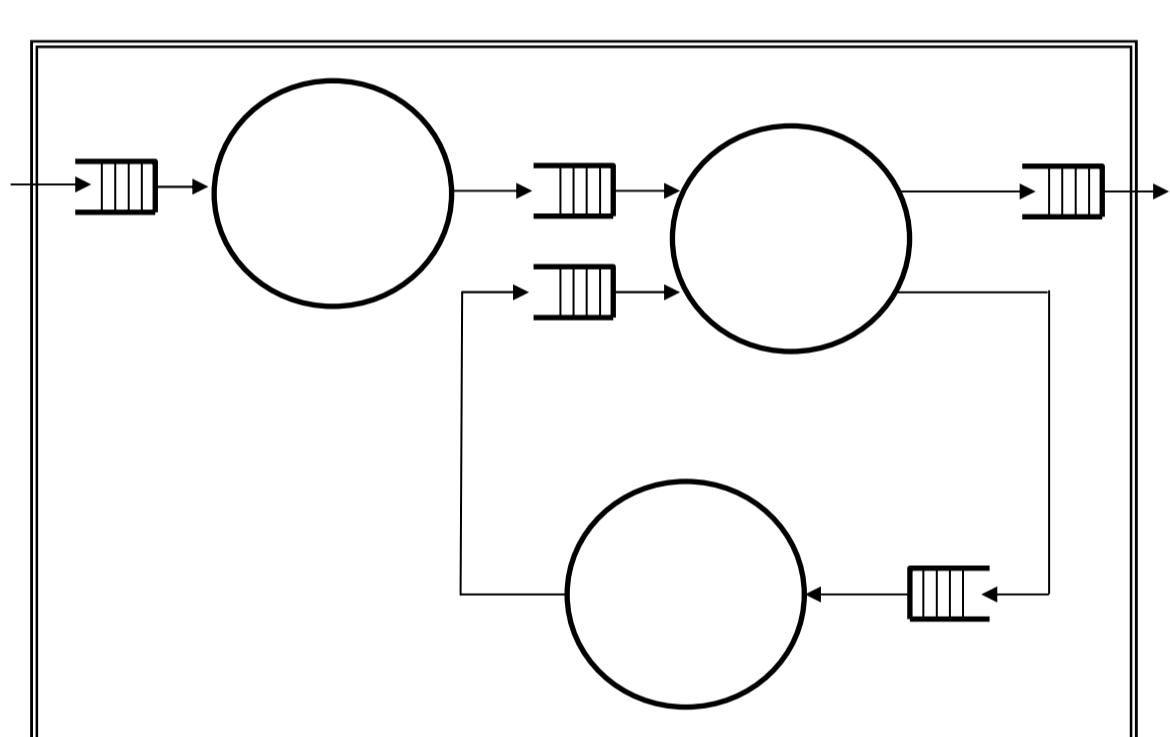
Highly parallel computing platform



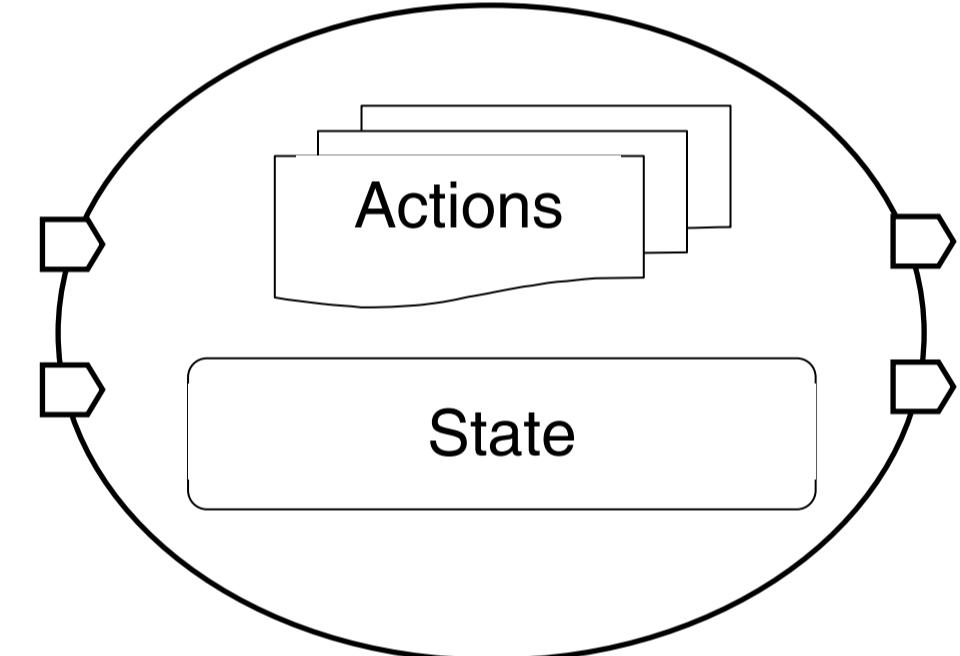
Example: Xilinx Virtex-4 (XC4VFX140)

- 142k logic cells
- 552 RAMs
 x 18Kbits each
- 192 DSP ALUs
- 2 PowerPC 405
- 4 Ethernet MACs

Programming model: dataflow with actors

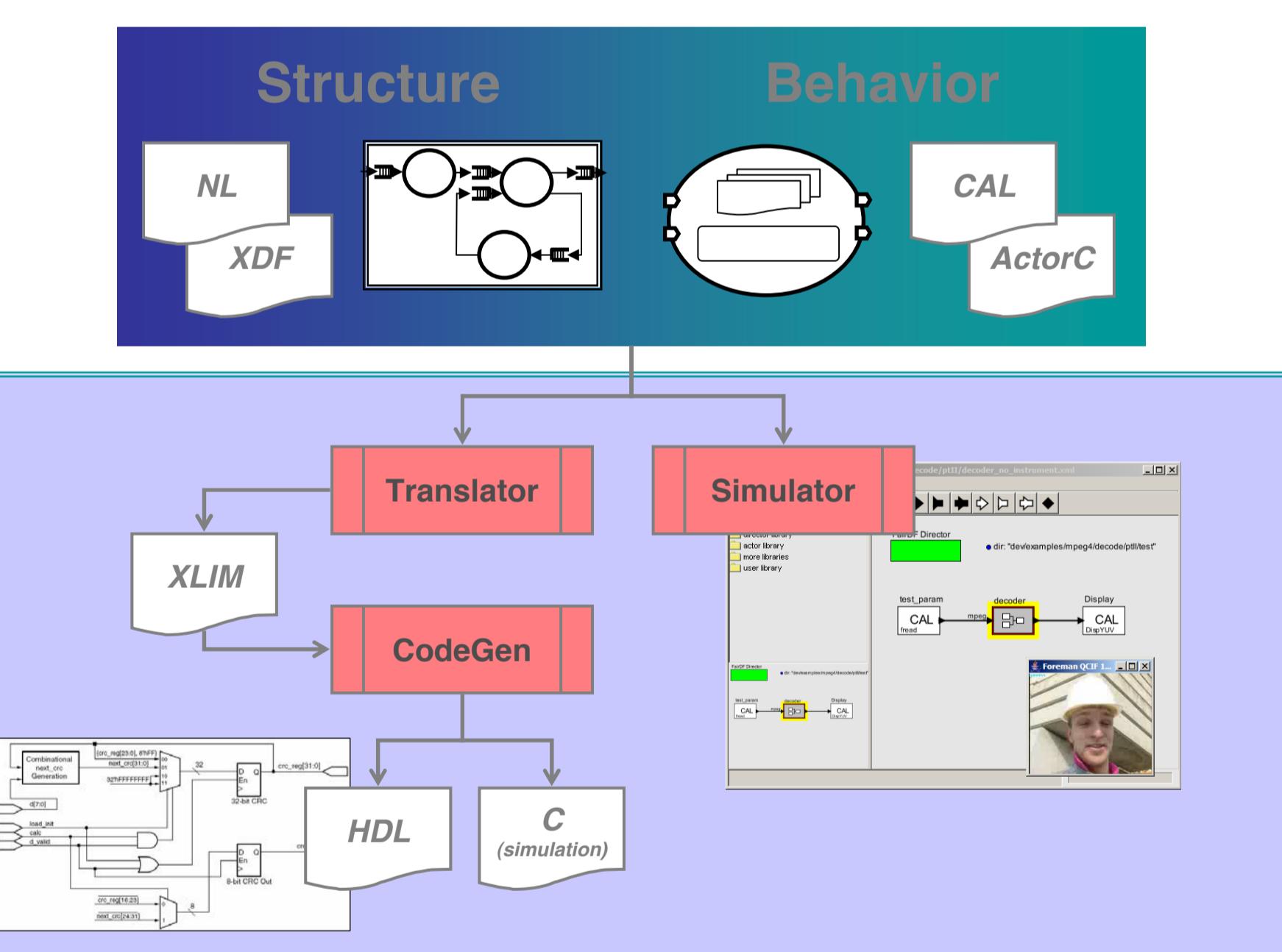


- FIFO connections
- encapsulated state
- atomic state transitions



Dataflow Tools

opendf.sourceforge.net



- various input languages e.g. CAL
- untimed simulation
- HDL code generation

Translation Process

```
actor SendDC (int T_INTER) int TYPE, int IN => int DC :  

int count := 0;  

action TYPE: [t], IN, [v] => DC: [v]  

do  

    count := count + 1;  

end  

action TYPE: [t], IN, [v] =>  

guard count = 0, t = 1  

do  

    count := count + 1;  

end  

action IN: [v] =>  

guard count > 0  

do  

    if count < 63 then  

        count := count + 1;  

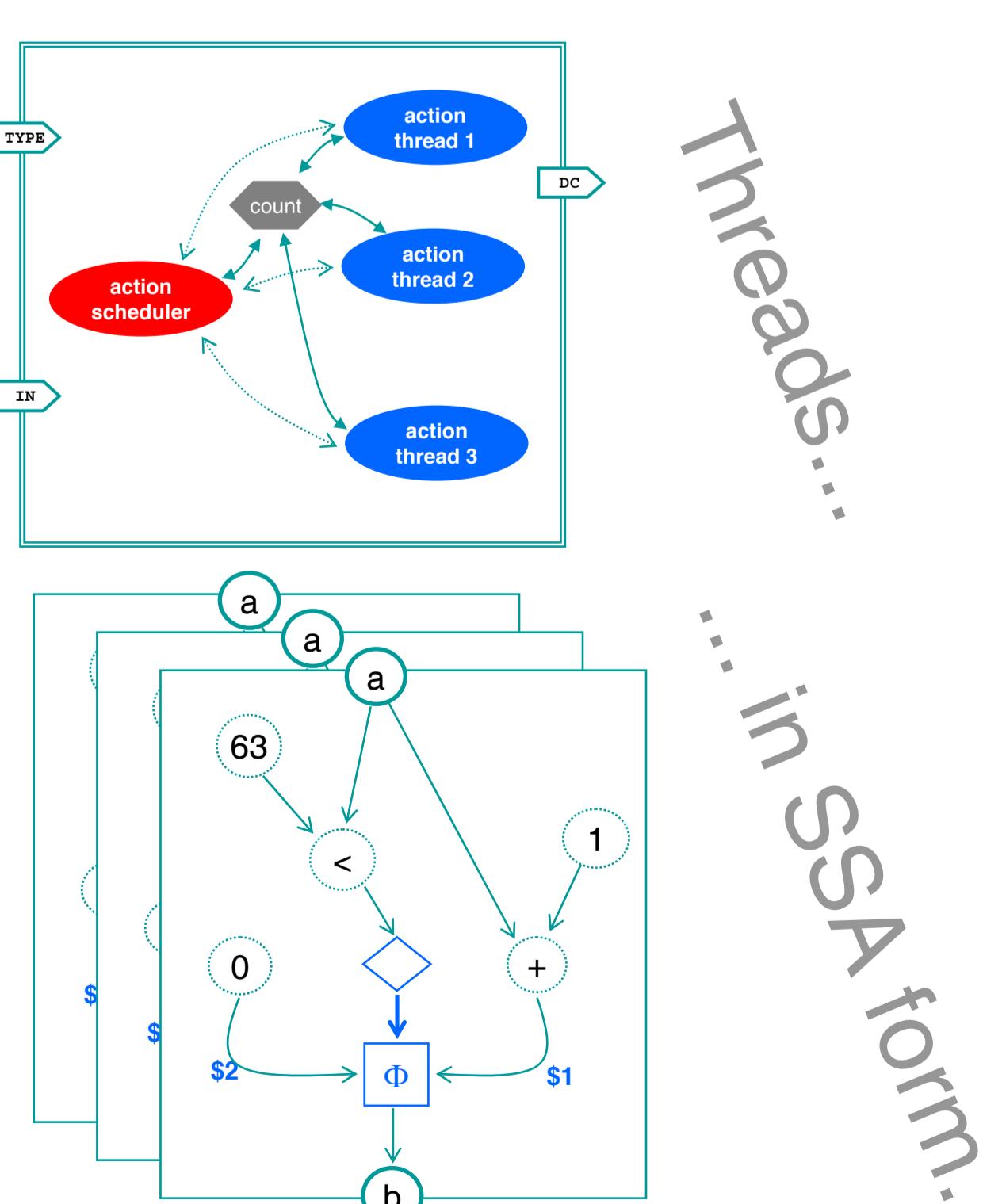
    else  

        count := 0;  

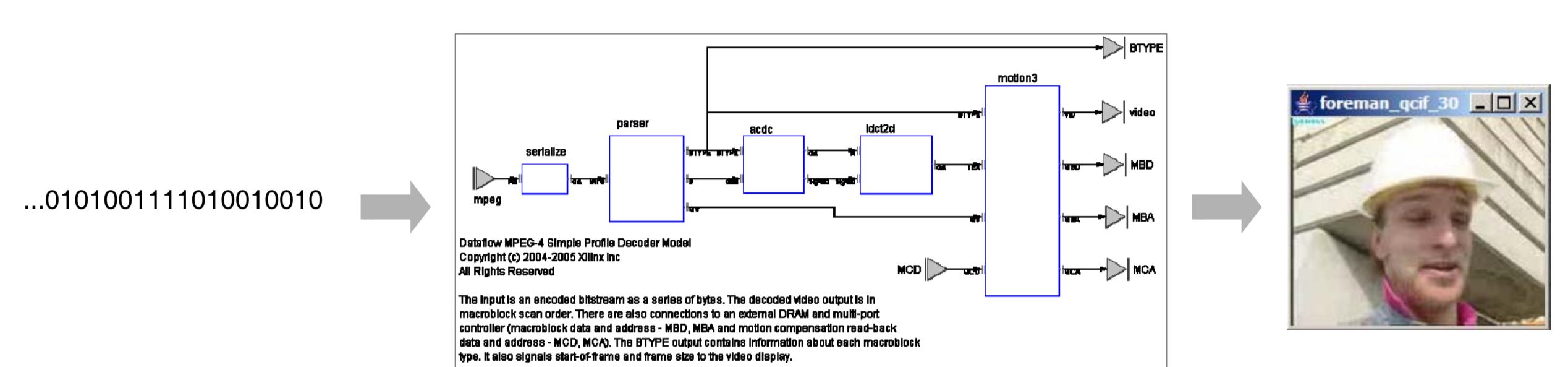
    end  

end
```

1. Actor code split into threads:
 1 thread per action
 +1 thread for the scheduler
2. Each thread represented in SSA form.
3. Produce circuit from SSA form.
4. Optimize data paths (bit-accurate constant prop).
5. Schedule operations when possible.
6. Insert registers where required.



Application: MPEG-4 Simple Profile Decoder



Actors, big and small

CAL actor language

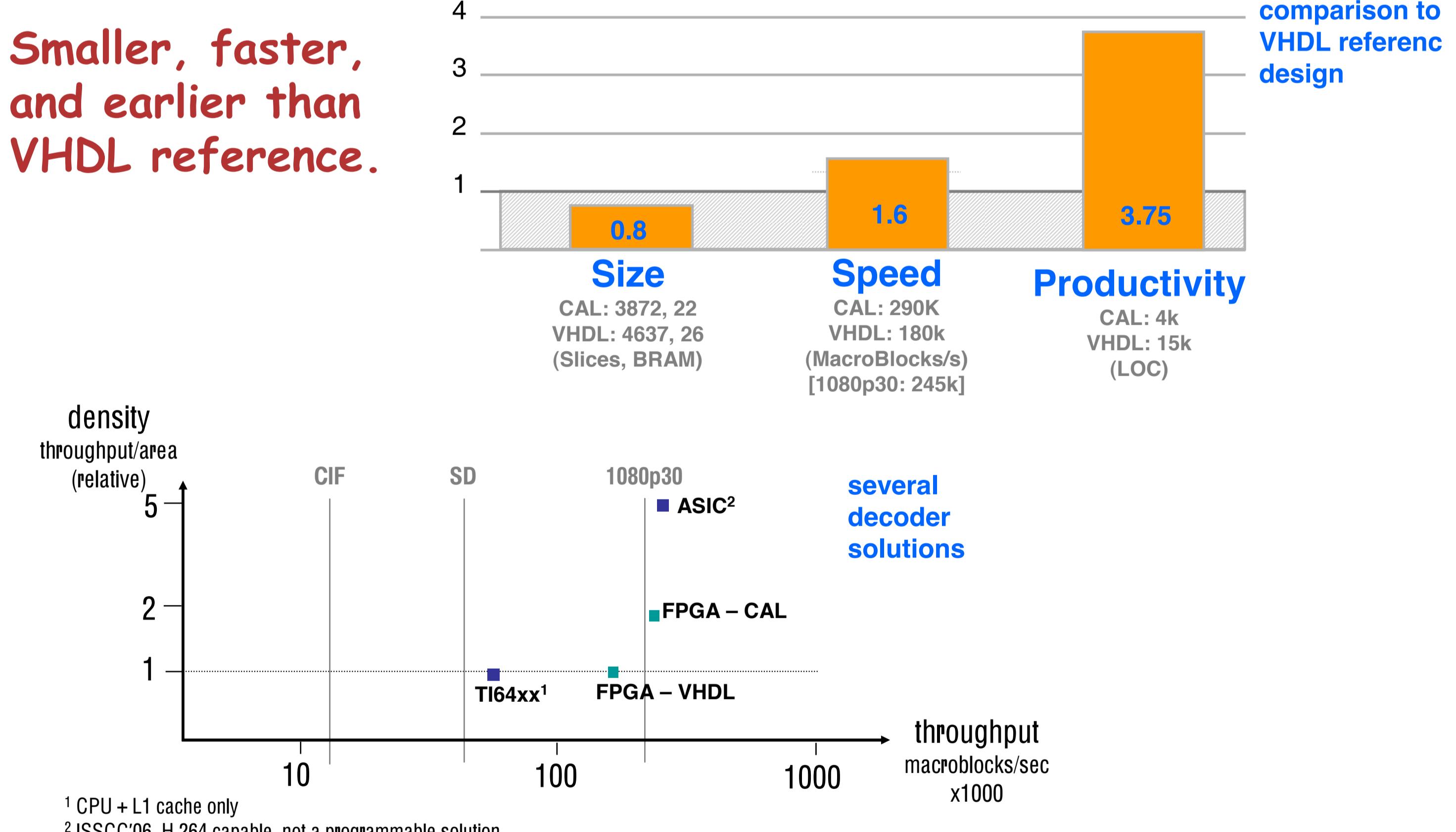
ParseHeaders
 1320 lines
 (without header comments)

Range of actors

- small compute kernels
- large control-dominated actors

Compare
 23 lines
 (without header comments)

Hardware Synthesis - Quality of Result



Conclusion

- Parallel platforms require parallel programming models.
- Dataflow is a general and portable way to describe highly parallel computational systems.
- MPEG-4: an at-size, real world application, with a broad spectrum of computational elements.
- All actors built in the CAL actor language, and composed using the NL network language.
- Our tools generate implementations that actually beat the VHDL reference in terms of QoR.
- Any abstraction cost was dwarfed by the ability to quickly iterate over multiple versions of the design.