Repeater Insertion for Two-Terminal Nets in Three-Dimensional Integrated Circuits

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Abstract. A new approach for inserting repeaters in 3-D interconnects is proposed. The allocation of repeaters along an interplane interconnect is iteratively determined. The proposed approach is compared with two other techniques based on conventional methods used for 2-D interconnects. Simulation results show that the proposed approach decreases the total wire delay up to 42% as compared to conventional approaches. The complexity of the proposed algorithm is linear to the number of planes that the wire spans.

Key words: 3-D ICs, repeater insertion, on-chip interconnect, timing optimization

1 Introduction

In 3-D ICs, the wire length is significantly reduced due to the short vertical interconnects. Although 3-D ICs are expected to greatly reduce the wire length as compared to planar circuits, methods to further improve the interconnect delay are required. This situation is due to the length of the global interconnects that limit the overall performance of a 3-D circuit.

Many repeater insertion algorithms have been proposed for 2-D interconnects. The optimal number and size of the repeaters to achieve the minimum interconnect delay for a distributed *RC* interconnect are described in [1], [2]. A uniform repeater design methodology for efficiently driving *RC* tree structures is presented in [3]. Alpert and Devgan present theoretical results, which determine the required number of repeaters for a wire with uniform impedance characteristics [4].

Applying these repeater insertion techniques for 2-D interconnects to 3-D nets traversing multiple planes does not result in the minimum interconnect delay. In a 3-D system, each physical plane can be fabricated with a different process or technology node resulting in diverse interconnect impedance characteristics. In addition, the various manufacturing technologies for the vertical interconnects (*e.g.*, through silicon via (TSV)) affect the delay of the interplane interconnects [5]. All of these factors complicate the repeater insertion task for 3-D interconnects. Recently, a simultaneous buffer and TSV planning algorithm for 3-D circuits has been presented in [6] where the size and number of the repeaters are considered known. The impedance characteristics of each plane are

considered uniform. In practice, however, the size and number of repeaters on different planes need to be determined considering the disparate interconnect impedance characteristics. Additionally, the repeaters inserted in one plane affect the total delay of the interconnect and the size, number, and location of the repeaters inserted in adjacent planes.

The objective of this paper, therefore, is to determine the size, number, and location of the repeaters cohesively inserted in all of the segments. A methodology for determining these solutions for a 3-D wire that spans several physical planes is introduced, where the traits of the 3-D interconnects are properly considered. The proposed approach considers the effect of repeaters on the delay of the wire segments on adjacent planes and iteratively decreases the delay of a 3-D wire.

The remainder of the paper is organized as follows. The delay model for a 3-D interconnect with repeaters used in this paper is introduced in Section 2. The proposed method for inserting repeaters in 3-D interconnects is presented in Section 3. Simulation results are shown in Section 4. The conclusions are summarized in the last section.

2 Delay Model for a 3-D Wire

The delay model of a wire segment within one physical plane of a 3-D circuit and the method to determine the number, size, and location of the repeaters for this segment is discussed in this section. The delay model for a 3-D wire comprising several of these segments is also presented.

A 3-D wire with repeaters is illustrated in Figure 1. x_i $(1 \leq i \leq n)$ is the distance between the first repeater and the TSV for $i > 1$ or the driver of the wire for $i = 1$. y_i is the distance between the last repeater and the TSV for $i < n$ or the receiver of the wire for $i = n$. k_i is the number of repeaters inserted in plane i. h_i represents the size of the repeaters, which is the multiple of the minimum size of the repeater that can be used in plane i.

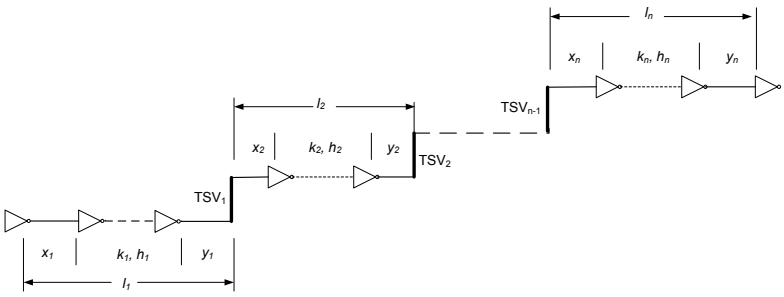


Fig. 1: A 3-D wire with repeaters.

The total delay of a 3-D interconnect can be divided into $2n-1$ components including the delay of the horizontal segments on the n planes where repeaters can be inserted and the delay of the TSVs. The delay of the TSVs can be considered constant. The delay of a horizontal segment i can be modeled by an RC distributed line with repeaters, as illustrated in Figure 2.

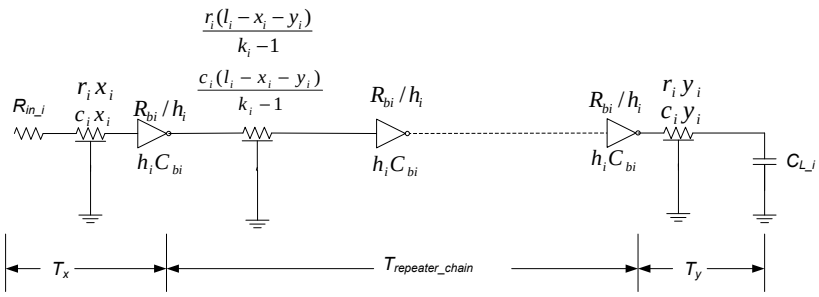


Fig. 2: The electrical model of one interconnect segment of a 3-D wire.

In Figure 2, R_{in_i} is the input resistance of the segment. C_{L_i} is the load capacitance. For the segment on the first plane, $R_{in\_i} = R_{source}$ and for the segment on the last plane, $C_{L\_i} = C_{sink}$. R_{bi} and C_{bi} are the resistance and capacitance, respectively, of the minimum size repeater on plane i. If R_{in_i} and C_{L_i} are known and there are k_i repeaters with size h_i, where $k_i \geq 2$, the total delay of a wire segment on plane i based on Elmore delay model [7] can be written as

$$\begin{aligned} T_{seg} =& T_{x_i} + T_{repeater\_chain} + T_{y_i} \\ =& R_{bi}C_{bi}(k_i - 1) + \frac{(l_i - x_i - y_i)^2 r_i c_i}{2(k_i - 1)} + \frac{R_{bi}(C_{L\_i} + (l_i - x_i)c_i)}{h_i} + \\ & C_{bi}(R_{in\_i} + (l_i - y_i)r_i)h_i + R_{in\_i}c_i x_i + \frac{x_i^2 r_i c_i}{2} + \frac{y_i^2 r_i c_i}{2} + y_i r_i C_{L\_i}. \quad (1) \end{aligned}$$

The variables in (1) are h_i, k_i, x_i, and y_i. The physical constraints for these variables, respectively, are

$$h_i \geq 1;\ k_i \geq 2;\ 0 \leq x_i \leq l_i;\ 0 \leq y_i \leq l_i;\ 0 \leq x_i + y_i \leq l_i. \quad (2)$$

To minimize (1) is a rather formidable task. Alternatively, (1) can be written as a two-variable function. For given x_i and y_i, T_{seg} is convex with respect to k_i and h_i, which means that for each pair of (x_i, y_i), there is a pair of (k_i, h_i) that produces the minimum delay.

Let $\frac{\partial T_{seg}}{\partial h_i} = 0$ and $\frac{\partial T_{seg}}{\partial k_i} = 0$, (k_i, h_i) can be written as a function of (x_i, y_i),

$$k_i = (l_i - x_i - y_i)\sqrt{\frac{r_i c_i}{2R_i C_i}} + 1, \quad h_i = \sqrt{\frac{R_{bi}(C_{L\_i} + (l_i - x_i)c_i)}{C_{bi}(R_{in\_i} + (l_i - y_i)r_i)}}\ . \quad (3)$$

Replacing (k_i, h_i) by (3), the delay $T_{seg}(x_i, y_i)$ is

$$T_{seg}(x_i, y_i) = (l_i - x_i - y_i)\sqrt{2R_{bi}C_{bi}r_ic_i} + R_{in\_i}c_ix_i + \frac{x_i^2 r_i c_i}{2} + \frac{y_i^2 r_i c_i}{2} + y_i r_i C_{L\_i} + 2\sqrt{R_{bi}C_{bi}(C_{L_i} + (l_i - x_i)c_i)(R_{in_i} + (l_i - y_i)r_i)}. \quad (4)$$

Since x_i and y_i are constrained according to (2), the minimum of (4) and a feasible solution (x_i, y_i) can be determined with numerical methods [8]. If there is only one repeater inserted along the segment, $k_i = 1$ and $y_i = l - x_i$. The total delay is $T_{seg} = T_{x_i} + T_{l-x_i}$. The expressions for the delay of the segment where $k_i \geq 2$ or $k_i = 1$ are consistent.

For a horizontal segment within a 3-D circuit consisting of n planes, the expressions for the input resistance and the output capacitance of each segment are modified to include the impedance of the TSVs and the interconnect sections x_{i+1} and y_{i-1}, respectively,

$$R_{in\_i} = \begin{cases} R_{source}, & \text{if } i = 1 \\ \frac{R_{b(i-1)}}{h_{i-1}} + r_{i-1}y_{i-1} + R_{tsv}, & \text{if } i \neq 1 \end{cases},$$
$$C_{L\_i} = \begin{cases} C_{sink}, & \text{if } i = n \\ C_{b(i+1)}h_{i+1} + c_{i+1}x_{i+1} + C_{tsv}, & \text{if } i \neq n \end{cases}. \quad (5)$$

Due to (5), the repeaters inserted in segments $i - 1$ and $i + 1$ can considerably affect the repeaters inserted in segment i. For a 3-D interconnect shown in Figure 1, expressions (5) and (3) are used to determine (k_i, h_i) for segments 1 to n. T_{total} can be expressed as a function of $\{(h_i, x_i, y_i) | 1 \leq i \leq n\}$,

$$T_{total} = \sum_{i=1}^{n} \Bigg((l_i - x_i - y_i)\sqrt{2R_{bi}C_{bi}r_ic_i} + \frac{R_{bi}((l_i - x_i)c_i + C_{L\_i})}{h_i} + (R'_{in\_i} + (l_i - y_i)r_i)C_{bi}h_i + R'_{in\_i}c_ix_i + \frac{x_i^2 r_i c_i}{2} + \frac{y_i^2 r_i c_i}{2} + y_i r_i C_{L\_i} \Bigg),$$
$$\text{where } R'_{in\_i} = \begin{cases} R_{source} & \text{if } i = 1 \\ R_{tsv} & \text{if } i \neq 1 \end{cases}. \quad (6)$$

By replacing R_{in_i} and C_{L_i} in (3) with (5), h_i is coupled to the solution for the two adjacent segments. This dependency complicates the optimization process. To formally minimize (6) requires computationally expensive optimization techniques since (6) is a non-polynomial function. Instead, (4) is utilized in the proposed approach to minimize the delay of each segment iteratively and results in a near-optimum solution for inserting repeaters in a multiplane net. This approach completes the repeater insertion in $O(n)$ time, where n is the number of planes. Note that the effect of the repeaters inserted in adjacent segments on the delay of the investigated segment is considered in (4) through (5).

3 Repeater Insertion Algorithm

In this section, an algorithm for inserting repeaters in 3-D interconnects is presented. The proposed algorithm determines a near-optimal solution S based on (4). The pseudo-code of this algorithm (Iterated Optimization) is illustrated in Algorithm 1. The proposed algorithm consists of two phases described in the following subsections.

Algorithm 1 Iterated Optimization

Input: 3-D wire W.
Output: T, $\{(h_i, k_i, x_i, y_i)|1 \leq i \leq n\}$.

1: $R_{in\_1} \leftarrow R_{source}$; $C_{L\_n} \leftarrow C_{sink}$; $T = 0$
{first phase}
2: **for all** segment i in W **do**
3: $R_{in\_i} \leftarrow R_{b\_(i-1)} + r_{tsv\_(i-1)}$
4: **end for**
5: **for** $i = n$ to 1 **do**
6: $[T, (h_i, k_i, x_i, y_i)] \leftarrow T + segt\_opt(R_{in\_i}, C_{L\_i})$;
7: $Update(R_{in\_i+1}, C_{L\_i-1})$;
8: **end for**
{second phase}
9: **while** $\Delta T > target\_ratio$ **do**
10: $T \leftarrow 0$
11: **for** $i = n$ to 1 **do**
12: $[T, (h_i, k_i, x_i, y_i)] \leftarrow T + seg\_opt(R_{in\_i}, C_{L\_i})$;
13: $Update(R_{in\_i+1}, C_{L\_i-1})$;
14: **end for**
15: **end while**

3.1 Determine an initial solution

In the first phase, an initial solution is obtained. The minimum delay of each segment i is successively determined, for $i = n$ to 1, assuming that a minimum size repeater (*i.e.*, $h_{i-1} = 1$) is inserted in the preceding segment $i - 1$, exactly before the TSV (*i.e.*, $y_{i-1} = 0$), as illustrated in Figure 3.

The algorithm starts from plane n. The corresponding h_n, k_n, x_n and y_n are determined based on (3) - (4) by the procedure $seg\_opt(R_{in\_i}, C_{L\_i})$ in Algorithm 1. In the procedure $Update(R_{in\_i+1}, C_{L\_i-1})$, the load for segment $n-1$ is determined by the resulting h_n and x_n. By assuming that $R_{in\_n-1} = R_{tsv} + R_{b(n-2)}$, a solution for segment $n - 1$ can be determined. Steps 7 to 10 in Algorithm 1 are applied to all of the wire segments. In this way, the initial delay T^0_{total} of the entire wire is determined, where the superscript indicates the number of iterations. With the initial solution S^0, the set $\{(R_{in\_i}, C_{L\_i})|1 \leq i \leq n\}$ for all segments is updated (see expression (5)).

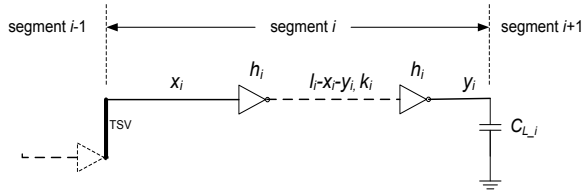


Fig. 3: A minimum size repeater next to the TSV in segment $i-1$ is assumed.

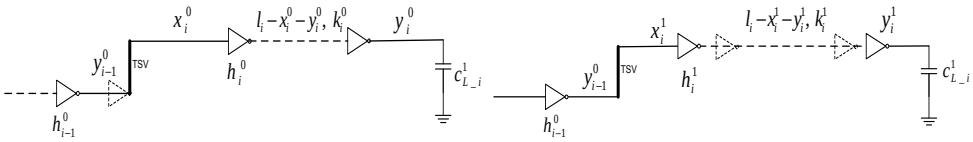
3.2 Refinement of the solution

In the second phase, the interconnect delay is iteratively improved. The second phase starts with the updated set $\{(R_{in\_i}, C_{L\_i}) | 1 \leq i \leq n\}$ obtained in the first phase. Similar to the first phase, from $i = n$ to 1, (3) and (4) are used to determine a new (h_i, k_i, x_i, y_i), as described in lines 12 - 16 in Algorithm 1. Compared with the first phase, the R_{in_i} used for each segment is updated. Since the R_{in_i} and C_{L_i} used in (3) - (4) include the effect of the new (h_i, k_i, x_i, y_i) on the delay of segments $i-1$ and $i+1$, the delay determined in this iteration is smaller or at least no greater than the previously determined delay.

Proposition 1 *Given the initial delay T^0_{total}, the solution S^0 obtained in the first phase and the delay T^1_{total} obtained by the solution S^1 determined in the first iteration of the second phase, $T^1_{total} \leq T^0_{total}$.*

Proof. Proposition 1 is proved by induction.

1. Assuming that segment i $(1 \leq i \leq n-1)$ is processed, the new solution for this segment is $s^1_i = (h^1_i, k^1_i, x^1_i, y^1_i)$ and the previous solution is $s^0_i = (h^0_i, k^0_i, x^0_i, y^0_i)$, where the superscripts indicate the number of iteration. The new solutions s^1_{i+1} to s^1_n for segment $i+1$ to n have been determined, since the wire is traversed from the sink towards the driver. The solutions for segment 1 to $i-1$, however, are those of the previous iteration s^0_1 to s^0_{i-1}, as illustrated in Figure 4(a).



(a) An initial solution for segment i. (b) Refinement of the solution.

Fig. 4: Iterative process to insert repeaters in segment.

The allocation of the repeaters in segment i based on the solution s^0_i is illustrated in Figure 4(a), while the repeaters in segments $i+1$ to n are adjusted according to s^1_{i+1} to s^1_n during iteration 1. The total delay of the 3-D wire in Figure 4(a) is T^1_{i+1}, where the subscript indicates that segments $i+1$ to n have been processed in iteration 1. For segment i, s^0_i is determined based on the assumption of placing a repeater in segment $i-1$ depicted by

the dashed line in Figure 4(a). s_i^0, therefore, does not provide the minimum delay from the last repeater (depicted by the solid line) in segment $i-1$ to the first repeater in segment $i+1$ in iteration 1. This behavior is due to the updated input resistance and the load capacitance of segment i according to s_{i-1}^0 and s_{i+1}^1, respectively. The allocation of the repeaters in segment i after this segment has been processed in the first iteration is depicted in Figure 4(b). The total delay of the 3-D wire in Figure 4(b) is now T_i^1. For $R_{in\_i}^0$ and $C_{L\_i}^1$, s_i^1 is determined through (3) and (4). s_i^1 results in a smaller delay from the last repeater in segment $i-1$ to the first repeater in segment $i+1$ as compared to s_i^0, since s_i^1 is determined by using the updated R_{in_i} and C_{L_i}. Consequently, the total delay of the 3-D wire in Figure 4(b) is not greater than the total delay of the 3-D wire in Figure 4(a), *i.e.*, $T_i^1 \leq T_{i+1}^1$.

2. For segment n, $C_{L\_n}^1 = C_{sink}$. Similar to the aforementioned proof, $T_n^1 \leq T_{total}^0$. Consequently, from 1 and 2, $T_{total}^1 = T_1^1 \leq T_n^1 \leq T_{total}^0$.

After the first iteration, a new solution S^1 and delay T_{total}^1 are obtained, as well as a new set $\{(R_{in\_i}^1, C_{L\_i}^1) | 1 \leq i \leq n\}$. Since h_{i-1}^1 and y_{i-1}^1 can be different from h_{i-1}^0 and y_{i-1}^0, $R_{in\_i}^1$ also differs from $R_{in\_i}^0$. The solution s_i^1 for segment i, however, is determined based on $R_{in\_i}^0$. Consequently, in the next iteration, the total wire delay is further decreased by re-determining the solution for segment i based on $R_{in\_i}^1$. Based on S^1 and $\{(R_{in\_i}^1, C_{L\_i}^1) | 1 \leq i \leq n\}$, the second iteration commences. Similar to Proposition 1, $T_{total}^2 \leq T_{total}^1$. The resulting delay of the 3-D wire at each iteration will be no greater than the result of the previous iteration. As illustrated in line 11 of Algorithm 1, when $\Delta T = \frac{T_{total}^i - T_{total}^{i+1}}{T_{total}^i}$ is smaller than *target_ratio*, the algorithm terminates. The *target_ratio* is considered to be user-specified. Considering that the time used to minimize (4) is constant $O(1)$, the complexity of the proposed algorithm is $O(n)$.

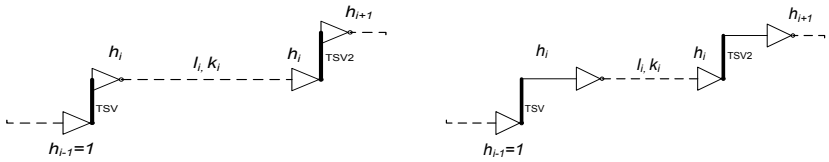
4 Simulation Results

In this section, the simulation results are presented. The Iterated Optimization is applied to several 3-D interconnects. The ASU predictive technology model (PTM) [9] is used to extract the parameters of the interconnect and the repeaters. To investigate the effectiveness of the proposed algorithm, two other approaches for inserting repeaters in 3-D interconnects have been adapted from the methods used for 2-D interconnects.

The first approach assumes that the repeaters are equally spaced in each segment [1], [3]. There is a repeater inserted before and after each TSV, respectively, as illustrated in Figure 5(a). With this assumption, each segment is treated as a 2-D interconnect. The delay of the segments is decoupled and repeaters are individually inserted in each segment based on [1]. In this approach, $\{x_i = 0, y_i = 0 | 1 \leq i \leq n\}$. The optimum number k_i and size h_i of the repeaters can be determined by (3).

Alternatively in the second approach, the last repeater in each plane is inserted right before the TSV that connects this segment, as illustrated in Figure

5(b). In Figure 5(b), the solution $\{(h_i, k_i, x_i)|1 \leq i \leq n\}$ is determined through (3) and (4) from plane 1 to plane n, respectively.



(a) Approach 1 (b) Approach 2

Fig. 5: Approaches from the repeater insertion method used in 2-D.

All of the approaches are applied to 3-D wires of different length that span three physical planes. The parameters used in the simulations are listed in Table 1. The location of the repeaters inserted by employing the Iterated Optimization algorithm and the wire delay after applying the three approaches are listed in Table 2. The number and size of the repeaters inserted in the three approaches are reported in Table 3.

Table 1: Simulation Parameters.

Plane	Tech. [nm]	r [Ω/mm]	c [fF/mm]	R_b [Ω]	C_b [fF]	R_{source} [Ω]	C_{sink} [fF]	R_{tsv_1} [Ω]	C_{tsv_1} [fF]	R_{tsv_2} [Ω]	C_{tsv_2} [fF]
1	130	36.7	260	800	30						
2	65	50	300	1000	40	800	20	2	10	2.3	13.2
3	90	40	290	900	35						

Table 2: 3-D Wire Delay after Applying the Three Approaches.
The wire spans three planes. l_1, l_2, l_3 are the length of the segment on plane 1, 2, and 3, respectively; $Itnum$ is the number of iterations and the $target\_ratio$ is 1%; Area $= \sum_{i=1}^{3} h_i k_i$. %Impr1 $= \frac{T_1 - T_{min}}{T_1}$, %Impr2 $= \frac{T_2 - T_{min}}{T_2}$.

l_1 [mm]	l_2 [mm]	l_3 [mm]	Iterated Optimization								Approach 1		Approach 2	
			x_1 [mm]	y_1 [mm]	x_2 [mm]	y_2 [mm]	x_3 [mm]	y_3 [mm]	$Itnum$	T_{min} [ps]	T_1 [ps]	% Impr1	T_2 [ps]	% Impr2
0.50	0.60	0.65	0.00	0.50	-	-	-	-	3	223.66	384.36	41.81%	302.96	26.18%
0.89	1.07	1.16	0.00	0.89	-	-	-	-	3	329.95	473.46	30.31%	390.37	15.48%
1.28	1.53	1.66	0.00	1.28	0.00	1.53	-	-	3	436.71	562.27	22.33%	476.25	8.30%
1.67	2.00	2.17	0.00	0.00	-	-	0.00	2.17	3	531.09	655.17	18.94%	565.01	6.00%
2.06	2.47	2.67	0.00	2.06	0.00	2.47	0.00	2.67	4	634.47	753.73	15.82%	658.46	3.64%
2.44	2.93	3.18	0.00	0.25	0.65	2.28	0.00	3.18	4	719.44	858.65	16.21%	752.30	4.37%
2.83	3.40	3.68	0.00	0.29	0.96	2.44	0.00	3.68	3	811.81	962.50	15.66%	846.94	4.15%
3.22	3.87	4.19	0.00	0.29	1.29	2.58	0.00	4.19	3	908.66	1053.57	13.75%	946.57	4.01%
3.61	4.33	4.69	0.00	1.09	0.26	2.06	0.00	4.69	3	1014.94	1144.95	11.35%	1044.34	2.82%
4.00	4.80	5.20	0.00	1.25	0.29	2.38	0.00	3.31	3	1108.13	1240.48	10.67%	1147.53	3.43%
Average decrease in delay											19.69%		7.84%	

Table 3: The Number and Size of Repeaters Assigned by Different Approaches. k_i, h_i are the number and size, respectively, of the repeaters inserted on plane i. Area $= \sum_{i=1}^{3} h_i k_i$.

Iterated Optimization						Approach 1						Approach 2					
h_1	h_2	h_3	k_1	k_2	k_3	h_1	h_2	h_3	k_1	k_2	k_3	h_1	h_2	h_3	k_1	k_2	k_3
4.21	-	-	1	0	0	3.52	5.99	5.11	2	2	2	3.23	4.25	1.00	2	1	1
5.54	-	-	1	0	0	4.19	7.67	7.04	2	2	2	4.24	5.97	1.09	2	1	1
5.08	10.79	-	1	1	0	4.67	8.74	8.31	2	2	2	5.03	7.21	1.11	2	1	1
6.48	-	8.50	2	0	1	5.05	9.47	9.19	2	2	2	5.68	8.13	1.10	2	1	1
5.75	11.15	9.55	1	1	1	5.36	10.00	9.82	2	2	2	6.26	8.82	1.07	2	1	1
6.35	12.29	10.69	2	1	1	5.64	10.39	10.30	2	2	2	6.76	11.76	1.10	2	2	1
6.75	12.28	11.21	2	1	1	5.89	10.69	10.68	2	2	3	7.22	12.18	1.05	2	2	1
7.13	12.37	11.87	2	1	1	6.11	10.92	10.98	2	3	3	7.64	12.53	1.01	2	2	1
6.73	12.23	13.14	2	2	1	6.31	11.11	11.22	3	3	3	8.02	12.83	1.00	3	2	1
6.94	12.27	11.63	2	2	2	6.50	11.27	11.42	3	3	3	8.38	13.07	1.00	3	2	1
Average area				29.47		**Average area**				57.75		**Average area**				31.10	

Compared with approach 1 and approach 2, the Iterated Optimization decreases the interconnect delay by 10% to 42% and 3% to 26%, respectively. To utilize the methods used in 2-D interconnects in approaches 1 and 2, at least two (one) repeaters are inserted in each segment in approach 1 (2) to decouple the delay of the investigated segment from the adjacent segments. In the Iterated Optimization, the location of the first and the last repeater can be iteratively adjusted. In addition, no repeater is inserted for specific short segments as listed in Table 3. Consequently, the Iterated Optimization produces the smallest interconnect delay. Note that when the total number of inverters inserted along the wire is the same for all of the approaches, the Iterated Optimization produces the smallest delay.

For each segment of a 3-D wire, the effect of the adjacent segments on the delay of the segment is considered during the repeater insertion process. Redundant or oversized repeaters are therefore not inserted. As reported in Table 3, fewer repeaters are inserted into 3-D interconnects where the Iterated Optimization is applied as compared to the other two approaches. Consequently, the proposed approach decreases the power consumed and the area occupied by repeaters. In addition, for the investigated interconnects, the iterations of the proposed approach are approximately four, which shows that the algorithm converges fast.

5 Conclusions

A method to insert repeaters for 3-D interconnects is described. The size and number of repeaters is iteratively adapted to decrease the delay of a 3-D wire. This novel technique is compared to two approaches adapted from repeater insertion techniques for 2-D interconnects. Simulation results demonstrate that the proposed approach for inserting repeaters in 3-D circuits decreases the total delay up to 42% and reduces the number and area of the inserted repeaters within

a few iterations. By properly inserting repeaters into 3-D wires, the interconnect performance of 3-D circuits is significantly improved.

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